COMPSCI 313 Assignment 3

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1. Cache Measurement

Name of processor: Intel Core i5-3317U

L2 Cache size: 256K

Array Size	**Throughput**
128KB	15844.30 MBytes/sec
256KB	13967.98 MBytes/sec
512KB	12129.98 MBytes/sec
4MB	5097.49 MBytes/sec

2. Matrix Product

1. Time taken is: 10.54 sec.
   The problematic access pattern of this implementation is that matrix B access is via columns. In relation to the cache this is going to cause a lot of misses because the successive values of B lack spatial proximity in memory. Transposing the matrix B so rows of the transposed B can now go into the cache is one way to work around this issue.

2. Time taken is: 1.26 sec

3. Time taken is: 0.85 sec.
   The approach taken is to use k = 8 for blocks of 8x8 in a tiling approach to matrix multiplication. Smaller blocks can fit into the cache and increase their reuse before they are moved out the cache again. Essentially this improves the temporal locality of matrix B (or more accurately submatrices of B) by the inner loops which perform matrix multiplications on the submatrices (the smaller blocks).K was chosen to be 8 because of its relationship to the cache size line (and that 1000 is divisible by 8). In this case the cache size line is 64 bytes, our arrays are of type double which is 8 bytes. A cache size line will fit 8 doubles, hence using 8x8 blocks is optimum.