APPLICATION NOTE for TCM8230MD

Ver. 1.1

CONTENTS

UPDATE INFORMATION

Ver 1.0 December 2nd, 2003
Ver 1.1 January 27, 2004

1 Controllable Functions

The setting registers are shown in Table1.
Gray character parameters are for test .(Don't change these parameters.)
Black character parameters are for user.

Table 1. Setting register table

ADDRESS			fast							last
DEC	BIN	HEX	BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	00000000	00								
1	00000001	01	**TESTMODE**							
2	00000010	02	**FPS** 0:30fps 1:15fps	**ACF** 0:50Hz 1:60Hz					**DCLKP** 0 : normal 1: reverse	**ACFDET** 0 : AUTO 1: MANUAL
3	00000011	03	**DOUTSW** 0:ON 1:0FF	**DATAHZ** 0:OUT 1:Hi-Z	**PICSIZ**[3:0] 0h:VGA 1h:QVGA(f) 2h:QVGA(z) 3h:QQVGA(f) 4h:QQVGA(z) 5h:CIF(f) 6h:QCIF(f) 7h:QCIF(z) 8h:subQCIF(f) 9h:subQCIF(z)				**PICFMT** 0:YUV422 1:RGB565	**TESTMODE**
4	00000100	04	**V_INV** 0:normal 1:invert	**H_INV** 0:normal 1:invert	**ESRLSW[1:0]** 0h : Short 1h : Long 2h & 3h : Extra long		**V_LENGTH**[3:0]			
5	00000101	05	**ALCSW** 0:AUTO 1:MANUAL	**ESRLIM**[1:0]		**ESRSPD**[12:8]				
6	00000110	06	**ESRSPD**[7:0]							
7	00000111	07	**AG**[7:0]							
8	00001000	08			**ALCMODE**[1:0] 0h: Center Weight 1h: Average 2h: Center only 3h: Backlight		**ALCH**[3:0]			
9	00001001	09	**ALCL**[7:0]							
10	00001010	0A	**AWBSW** 0:AUTO 1:MANUAL							
11	00001011	0B	**MRG**[7:0]							
12	00001100	0C	**MBG**[7:0]							
13	00001101	0D	**GAMSW** 0:ON 1:OFF							
14	00001110	0E	**HDTG**[7:0]							
15	00001111	0F	**VDTG**[7:0]							
16	00010000	10	**HDTCORE**[3:0]				**VDTCORE**[3:0]			
17	00010001	11	**CONT**[7:0]							
18	00010010	12	**BRIGHT**[7:0]							
19	00010011	13		**VHUE**[6:0]						
20	00010100	14		**UHUE**[6:0]						
21	00010101	15			**VGAIN**[5:0]					
22	00010110	16			**UGAIN**[5:0]					
23	00010111	17					**UVCORE**[3:0]			
24	00011000	18		**SATU**[6:0]						
25	00011001	19	**MHMODE** 0: 1:	**MHLPFSEL** 0: 1:	**YMODE**[1:0]			**MIXHG**[2:0]		
26	00011010	1A			**LENS**[5:0]					
27	00011011	1B	**AGLIM**[2:0]			**LENSRPOL** 0:Gain up 1:Gain down	**LENSRGAIN**[3:0]			
28	00011100	1C	**ES100S**[7:0]							
29	00011101	1D	**ES120S**[7:0]							
30	00011110	1E	**D_MASK**[1:0]		**CODESW** 0:OFF 1:OUT	**CODESEL** 0 : original 1 : ITU656	**HSYNCSEL** 0 : normal 1 : h_blanking	**TESPIC** 0:Not out 1:Out	**PICSEL**[1:0] 0h:Colorbar 1h:Ramp1 2h :Ramp2 3h: Not supported	
31	00011111	1F	**SLEEPSW** 0:ACTIVE 1:SLEEP	**SRST** 0:OFF 1:reset						

ADDRESS			fast							last
DEC	BIN	HEX	BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
32	00100000	20	**HNUM**[7:0]							
33	00100001	21	**TESTMODE**							
34	00100010	22	**TESTMODE**							
35	00100011	23	**TESTMODE**							
36	00100100	24	**TESTMODE**							
37	00100101	25	**TESTMODE**							
38	00100110	26	**TESTMODE**							
39	00100111	27	**HOUTPH**[7:0]							
40	00101000	28	**HOUTPH**[8]	**VOUTPH**[6:0]						
41	00101001	29	**FSSTBSW** 0 : NOT OUT 1 : OUT	**FSSTBPOL** 0 : normal 1 : invert			**FSSTBPH[3:0]**			
42	00101010	2A					**FSSTBW[3:0]**			
43	00101011	2B					**TESTMODE**			
44	00101100	2C	**TESTMODE**							
45	00101101	2D	**TESTMODE**							
46	00101110	2E	**TESTMODE**							
47	00101111	2F	**TESTMODE**							
48	00110000	30		**TESTMODE**			**TESTMODE**			
49	00110001	31	**TESTMODE**							
50	00110010	32		**ESROUT**[14:8] ✱						
51	00110011	33	**ESROUT**[7:0] ✱							
52	00110100	34	**AGOUT**[7:0] ✱							
53	00110101	35			**DGOUT**[5:0] ✱					
54	00110110	36	**ALCDATA**[7:0] ✱							
55	00110111	37	**AWBRYDA**[7:0] ✱							
56	00111000	38	**AWBBYDA**[7:0] ✱							
57	00111001	39	**AGSLOW1**[1:0]		**FLLSMODE**[1:0]		**FLLSLIM**[3:0]			
58	00111010	3A	**DETSEL**[3:0]				**ACDETNC**[3:0]			
59	00111011	3B	**AGSLOW2**[1:0]		**DG**[5:0]					
60	00111100	3C	**REJHLEV**[7:0]							
61	00111101	3D	**ALCLOCK** 0: 1:	**FPSLNKSW** 0: 1:	**ALCSPD[1:0]**		**ALCSTEP[1:0]**		**REJH**[1:0]	
62	00111110	3E	**SHESRSW** 0:Disable 1:Enable	**ESLIMSEL** 0: 1:	**SHESRSPD**[1:0]		**ELSTEP**[1:0]		**ELSTART**[1:0]	
63	00111111	3F	**AGMIN**[7:0]							

ADDRESS			fast							last
DEC	BIN	HEX	BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
64	01000000	40	**TESTMODE**							**TESTMODE**
65	01000001	41	**JAMP** 0: 1:	**JAMG**[6:0]						
66	01000010	42			**PREGRG**[5:0]					
67	01000011	43			**PREGBG**[5:0]					
68	01000100	44			**PRERG**[5:0]					
69	01000101	45			**PREBG**[5:0]					
70	01000110	46								
71	01000111	47		**MSKBR**[6:0]						
72	01001000	48		**MSKGR**[6:0]						
73	01001001	49		**MSKRB**[6:0]						
74	01001010	4A		**MSKGB**[6:0]						
75	01001011	4B		**MSKRG**[6:0]						
76	01001100	4C		**MSKBG**[6:0]						
77	01001101	4D	**HDTCSW** 0: 1:	**VDTCSW** 0: 1:	**DTCYLV**[5:0]					
78	01001110	4E	**HDTPSW** 0: 1:	**VDTPSW** 0: 1:	**DTCGAIN**[5:0]					
79	01001111	4F	**TESTMODE**			**DTLLIMSW** 0: 1:	**DTLYLIM** [3:0]			
80	01010000	50	**YLCUTLMSK** 0: 1:		**YLCUTL**[5:0]					
81	01010001	51	**YLCUTHMSK** 0: 1:		**YLCUTH**[5:0]					
82	01010010	52		**UVSKNC**[6:0]						
83	01010011	53		**UVLJ**[6:0]						
84	01010100	54	**WBGMIN**[7:0]							
85	01010101	55	**WBGMAX**[7:0]							
86	01010110	56	**AWBCSPOLE** 0: 1:	**WBDIVCLP** 0: 1:	**WBNOLJ**[1:0]		**WBNOLJSC** 0: 1:	**WB2IM1** 0: 1:	**WBSPDUP**[1:0]	
87	01010111	57						**WBDIVSC**[2:0]		
88	01011000	58			**ALLAREA** 0: 1:	**WBLOCK** 0: 1:	**WB2SP** [3:0]			
89	01011001	59			**KIZUSW** 0:OFF 1:ON	**PBRDSW**			**ABCSW**[1:0]	
90	01011010	5A	**PBDLV**[7:0]							
91	01011011	5B	**PBC1LV**[7:0]							
92	01011100	5C	**PBC2LV**[7:0]							
93	01011101	5D	**PBC3LV**[7:0]							
94	01011110	5E	**PBC4LV**[7:0]							
95	01011111	5F	**PBC5LV**[7:0]							

2 Explanation of each address

Note : <V> means the command affects in vertical synchronize timing.
<N> means the command affects right away.
< R only > Read only register
< R / W > Read / Write register

1/0 : Default value is 1
0/1 : Default value is 0
* : Read Only
0 : Fixed 0 (Can't change)
1 : Fixed 1 (Can't change)
< Test Mode > : Absolutely don't change these parameters in any situation.
: Can't be changed

* Each default setting is tentative.

ADDRESS 00h **DEF:70h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0	0	0	0	0	0

There's no parameter in this address..

ADDRESS 01h < R only > **DEF:x0h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
*	*	*	*	0	0	0	0

BIT7-4 : Internal test mode

ADDRESS 02h < R / W > **DEF:40h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	1/0					0/1	0/1

BIT7 : FPS <V> is the frame rate setting
0h : 30fps 1h : 15fps
This fps is based on normal input of external clock. In detail please refer to table ***** .

BIT6 : ACF <V> is the AC frequency setting. This address is for flickerless operation.
0h : AC50Hz , 1h : AC60Hz

BIT1 : DCLKP <V> is the polarity switch of DCLK.
0h : normal polarity 1h : inverted polarity

BIT0 : ACFDET <V> is the automatic flicker detection switch
0h : ON 1h : OFF

ADDRESS 03h < R / W > **DEF:80h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7 : DOUTSW <N> is digital output switch (for Dout, HD, VD and Dclk)
0h : Output enable 1h : Output disable (Fixed to low level)

BIT6 : DATAHZ <N> is the selection of the output (for Dout, HD, VD, Dclk and FSSTB)

0h : Output is enabled. 1h : Output pins are High-Impedance

BIT5-2 : PICSIZ <V> is the image format selection. See the table 3.

Table 3

Data (Dec)	Mode
0	VGA full
1	QVGA full
2	QVGA zooming
3	QQVGA full
4	QQVGA zooming
5	CIF full
6	QCIF full
7	QCIF zooming
8	subQCIF full
9	subQCIF zooming

BIT1 : PICFMT <N> is the output format switch
0h : YUV422 1h : RGB565

BIT0 : CM <Test mode> <N> is the sensor selection switch
0h : Color sensor 1h : B/W sensor

ADDRESS 04h < R/W > DEF:0Fh

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	1/0	1/0	1/0	1/0

BIT7 : V_INV <V> is the vertical flip selection
0h : Normal 1h : Vertical flip

BIT6 : H_INV <V> is the horizontal flip selection
0h : Normal 1h : Horizontal flip

BIT5-4 : ESRLSW <V> is selection of output frame rate to adjust the maximum exposure time .
0h : Normal mode (every one frame output , 15 fps or 30 fps)
1h : Long exposure mode (intermittent output every 4 frames, = 3.75 fps)
2h & 3h : Extra long exposure mode (intermittent output : up to V_LENGTH setting (1frame-15V frames))

BIT3-0 : V_LENGTH <V> is the interval setting in the intermittent output operation. This command is only for the extra long exposure mode. (ESRLSW = 2 or 3)
0h & 1h : one frame interval
2h : 2 frame intervals
| |
Fh : 15 frame intervals (The image data is output once every 15 frames. Namely 1 fps)

ADDRESS 05h < R / W > DEF:02h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	1/0	0/1

BIT7 : ALCSW <V> is the ALC (Automatic Luminance Control) ON / OFF switch
0h : ALC ON (for automatic control)
1h : ALC OFF (for manual control)

BIT6-5 : ESRLIM <V> is the maximum exposure time setting.
0h : up to 1/30 sec (in FPS=0h) / up to 1/15 sec (in FPS=1h)
1h : up to 1/15 sec (in FPS=0h) / up to 1/7.5 sec (in FPS=1h)
2h : up to 1/7.5 sec (in FPS=0h) / up to 1/3.75 sec (in FPS=1h)
3h : up to 1/3.75 sec (in FPS=0h) / up to 1/3.75 sec (in FPS=1h)

BIT4-0 : ESRSPD[12:8] <V> is the manual setting of electronic shutter speed (upper 5 bit) for manual luminance control (in ALCSW = 1h).
In combination with these bits and ADDRESS 06h, totally 13 bits are used as ESRSPD[12:0]
0001h : 1H(minimum)
| | 1H step
1EC3-1FFFh : 7875H(maximum)

ADDRESS 06h < R / W > **DEF:0Dh**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	1/0	1/0	0/1	1/0

BIT7-0 : ESRSPD[7:0] <V> is the manual setting of electronic shutter speed (lower 8 bit)
Refer to ESRSPD[12:8] description.

ADDRESS 07h < R / W > **DEF:C0h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	1/0	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-0 : AG <V>is the manual setting of sensor analog gain in ALCSW = 1h.

0Ch : +24dB
| |
18h : +18dB
| |
30h : +12dB
| |
60h : +6dB
| |
C0h : +0dB

ADDRESS 08h < R / W > **DEF:38h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	1/0	1/0	1/0	0/1	0/1	0/1

BIT5-4 : ALCMODE <V> is the light metering mode selection for ALC.
0h : Center-weighted & full area averaging
1h : Full area averaging
2h : Center area only
3h : Backlight

BIT3-0 : ALCH <V> ALCH is the convergence range of luminance level in ALC .
0h : 0 level in range
|
Fh : 16 level in 255 level

ADDRESS 09h < R / W > **DEF:40h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	1/0	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-0 : ALCL <V> is the lower limit for luminance level converging in ALC
10h : black level
|
88h: 100% white level as a reference
|
FFh : peak white level

The upper limit for converging luminance level in ALC is ALCL+ALCH.

ADDRESS 0Ah < R / W > DEF:00h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0	0	0	0	0	0	0

BIT7 : AWBSW <V> is the auto white balance control (AWB) ON / OFF switch
0h : AWB on
1h : AWB off

ADDRESS 0Bh < R / W > DEF:40h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	1/0	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-0 : MRG <V> is the setting of R gain in manual white balance (in AWBSW = 1).
00h : x0
| |
40h : x1
| |
FFh : x3.984375

ADDRESS 0Ch < R / W > DEF:40h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	1/0	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-0 : MBG <V> Setting of B gain for manual white balance (in AWBSW = 1).
00h : x0
| |
40h : x1
| |
FFh : x3.984375

ADDRESS 0Dh < R / W > DEF:00h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0	0	0	0	0	0	0

BIT7 : GAMSW <N> is the gamma correction ON/OFF switch <Gamma=0.55>
0h : gamma ON 1h : gamma OFF

ADDRESS 0Eh < R / W > DEF:2Fh

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	1/0	0/1	1/0	1/0	1/0	1/0

BIT7-0 : HDTG <N> is the horizontal edge enhancement gain (emphasis of the contour (edge) of the shape).
00h : x0
| |
20h : x1
| |
FFh : x7.96875

ADDRESS 0Fh < R / W > DEF:04h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	1/0	0/1	0/1

BIT7-0 : VDTG <N> is the vertical edge enhancement gain

00h : x0
| |
20h : x1
| |
FFh : x7.96875

ADDRESS 10h < R / W > DEF:22h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	1/0	0/1	0/1	0/1	1/0	0/1

BIT7-4 : HDTCORE <N> is the coring of horizontal edge enhancement
0h : Coring OFF
1h : Coring up to 1LSB
| |
Fh : Coring up to 15LSB

BIT3-0 : VDTCORE <N> is the coring of vertical detail enhancement
0h : Coring OFF
1h : Coring up to 1LSB
| |
Fh : Coring up to 15LSB

ADDRESS 11h < R / W > DEF:9Ah

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	0/1	0/1	1/0	1/0	0/1	1/0	0/1

BIT7-0 : CONT <N> is the contrast setting
00h : x0
| |
80h : x1
| |
FFh : x1.9921875

ADDRESS 12h < R / W > DEF:0Ch

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	1/0	1/0	0/1	0/1

BIT7-0 : BRIGHT <N> is brightness setting (black level setting) (This data to be set by 2's)
00h : Black level 0
| |
7Fh : Black level 127
FFh : Black level -1
| |
80h : Black level -128

ADDRESS 13h < R / W > DEF:0Ah

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0/1	0/1	0/1	1/0	0/1	1/0	0/1

BIT6-0 : VHUE <N> is the hue adjustment (V value is added to U)
BIT6 is the polarity . When BIT6=0, the sign P =+ and when BIT6=1, the sign P = -- ,
BIT5- 0 is the gain factor.
00h : x0
| |
3Fh : x1.96875

The formula is U' = U + P x VHUE

ADDRESS 14h < R / W > **DEF:08h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0/1	0/1	0/1	1/0	0/1	0/1	0/1

BIT6-0 : UHUE <N> is the hue adjustment (U value is added to V).
BIT6 is the polarity . When BIT6=0, the sign P =+ and when BIT6=1, the sign P = -- ,
BIT5-0 : is the gain factor.

00h : x0
| |
3Fh : x1.96875

The formula is V' = V + P x UHUE

ADDRESS 15h < R / W > **DEF:38h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	1/0	1/0	1/0	0/1	0/1	0/1

BIT5-0 : VGAIN <N> is the gain setting of V component.
00h : x0
| |
20h : x1
| |
3Fh : x1.96875

ADDRESS 16h < R / W > **DEF:38h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	1/0	1/0	1/0	0/1	0/1	0/1

BIT5-0 : UGAIN <N> is the gain setting of U component.
00h : x0
| |
20h : x1
| |
3Fh : x1.96875

ADDRESS 17h < R / W > **DEF:01h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0	0	0/1	0/1	0/1	1/0

BIT3-0 : UVCORE <N> is coring level of UV in case of low color level.
0h : Coring OFF
1h : Suppression under +/-1LSB
| |
Fh : Suppression under +/-15LSB

ADDRESS 18h < R / W > **DEF:27h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0/1	1/0	0/1	0/1	1/0	1/0	1/0

BIT6-0 : SATU <N> is the color saturation control (UV gain control).
00h : x0 (B/W)
| |

20h : x1
| |
3Fh : x1.96875

ADDRESS 19h < R / W > DEF:04h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0	1/0	1/0	1/0

BIT7 : MHMODE <N> is selection of the generating method of Y (Y means luminance signal)
0h : Y=(YL-YHL)*MIXHG + YH
1h : Y=(YH-YHL)*MIXHG + YL

BIT6 : MHLPFSEL <N> is the selection of boosting center frequency for YHL in Mixed highs
0h : Normal (up to 1/2 nyquist frequency)
1h : Lower frequency (up to 1/4 nyquist frequency)

BIT5-4 : YMODE <N> is the selection of Y signal generation method
0h : Mixed Highs 1h : YH only 2h : YL only 3h : YHL only

BIT2-0 : MIXHG <N> is the setting of the Mixed Highs ratio
In the case of MHMODE=0 (Normal)
Y=(YL-YHL) * M+YH M= MIXHG[2:0]
0h : 0% 1h : 25%2h : 50%3h : 75%4h-7h : 100%

In the case of MHMODE=1 (Boost Middle-High frequency)
Y=(YH-YHL) * m+YL m= MIXHG[2:0] (x0 to x3.5)

0h : 0% 1h : 50% 2h : 100% 3h : 150% 4h: 200% 5h: 250% 6h: 300% 7h : 350%

ADDRESS 1Ah < R / W > DEF:20h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	1/0	0/1	0/1	0/1	0/1	0/1

BIT5-0 : LENS <N> is the compensation level of lens shading
00h : Compensation OFF
| |
35h : x2 (at diagonal corner of VGA image)
| |
3Fh : x2.3 (at diagonal corner of VGA image)

ADDRESS 1Bh < R / W > DEF:46h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	1/0	0/1	0/1	0/1	1/0	1/0	0/1

BIT7-5 : AGLIM <V> is the upper limit setting of sensor gain-up for ALC operation
0h : up to 0dB 1h : up to +6dB 2h : up to +12dB
3h : up to +18dB 4h : up to +24dB 5h : up to +30dB
6h : up to +36dB 7h : up to +42dB

BIT4 : LENSRPOL <N> is the polarity of LENSRGAIN
0h : R Gain up 1h : R Gain down

BIT3-0 : LENSRGAIN <N> Gain setting of R shading compensation.
When LENS, LENSRPOL and LENSRGAIN are set to certain values,
each color level is changed according to following equation.
R' = "LENS" x "LENSRGAIN" x R
G' ="LENS" x G

B' ="LENS" x B

This command is used to compensate the color shading more precisely because the R level is likely to change differently in the corner of picture.

ADDRESS 1Ch < R / W > DEF:9Eh

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	0/1	0/1	1/0	1/0	1/0	1/0	0/1

BIT7-0 : ES100S <V> Setting the number of horizontal lines corresponding to 1/100 sec.
This command is for flickerless ALC.

ADDRESS 1Dh < R / W > DEF:83h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	0/1	0/1	0/1	0/1	0/1	1/0	1/0

BIT7-0 : ES120S <V> Setting the number of horizontal lines corresponding to 1/120 sec.
This command is for flickerless ALC.

ADDRESS 1Eh < R / W > DEF:68h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	1/0	1/0	0/1	1/0	0/1	0/1	0/1

BIT7-6 : D_MASK <V> set masking periods. This function affects only sensor mode switching.
0h : Don't mask
1h : 1V (one- frame interval) mask
| |
3h : 3V(three- frame interval) mask

BIT5 : CODESW <V> is addition of synchronization code for output data.
0h : Output data without synchronization code , 1h : Output data with synchronization code

BIT4 : CODESEL <V> is selection of synchronization code.
0h : FS,FE,LS,LE (FS: Frame Start FE: Frame End LS: Line Start LE: Line End)
1h : Based on ITU656

BIT3 : HSYNCSEL <V> is the selection of H sync format
0h : Normal HD signal
1h : H blanking type (High level during image data outputting)

BIT2 : TESPIC <V> is the switch of test pattern output
0h : OFF(Normal picture output) 1h : ON (Test pattern output)

BIT1-0 : PICSEL <V> is the selection of test pattern
0h : Color bar 1h : Ramp wave after gamma 2h : Ramp wave before gamma 3h : Normal picture

ADDRESS 1Fh < R / W > DEF:00h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0	0	0	0	0	0

BIT7 : SLEEPSW <N> is the operation mode switch
0h : active (operating) mode 1h : sleep mode
In entering sleep mode, the register values are restored.

BIT6 : SRST <N> is software reset
0h : Active 1h : Reset
When set "1", all register values are initialized to the default values in the internal ROM.

This register value is reset to “0” by automatically after the soft reset is finished.

ADDRESS 20h < R / W > DEF:00h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-0 : HNUM <V> can adjust clock numbers of horizontal period from 780 to 1290..
00h : 780 clock
| | 2 clock step
1Fh: 1290 clock
CAUTION: In case of use this parameter (in case set this parameter except 00h), address 3E bit7 SHESRSW must be set to 0h (Disable). This is mandatory setting.

ADDRESS 21h < R / W > DEF:01h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	0/1	1/0

BIT7-0 : HPPH[7:0] <Test mode> <V> is the phase offset of HP (internal horizontal sync pulse) timing (lower 8bit) in the sensor portion. The phase is shifted with 1 pixel clock step.

ADDRESS 22h < R / W > DEF:26h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	1/0	0/1	0/1	1/0	1/0	0/1

BIT7 : HPPH[8] <Test mode> <V> is the phase offset of HP (internal horizontal sync pulse) timing (MSB) in the sensor portion

BIT6-0 : VRRPH <V> is the phase offset of VRR (internal vertical sync pulse) timing in the sensor portion. The phase is shifted with single H(horizontal) period step.

ADDRESS 23h < R / W > DEF:40h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	1/0	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-0 : HDSPPH[7:0] <Test mode> <V> is the phase offset of HDDSP (internal horizontal sync pulse) timing (lower 8bit) in the camera DSP. The phase is shifted with 1 pixel clock step.

ADDRESS 24h < R / W > DEF:27h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	1/0	0/1	0/1	1/0	1/0	1/0

BIT7 : HDSPPH[8] <Test mode> <V> is the phase offset of HDDSP (internal horizontal sync pulse) timing (MSB) in the camera DSP.
BIT6-0 : VDSPPH <V> is the phase offset of VDDSP (internal vertical sync pulse) timing in the camera DSP. The phase is shifted with single H(horizontal) period step.

ADDRESS 25h < R / W > DEF:5Fh

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	1/0	0/1	1/0	1/0	1/0	1/0	1/0

BIT7-0 : HAPRPH[7:0] <Test mode> <V> is the phase offset of HAPR (internal horizontal sync pulse) timing (lower 8bit) in the camera DSP. The phase is shifted with 1 pixel clock step.

ADDRESS 26h < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0	0	0	0	0	0	0

BIT7 : HAPRPH[8] <Test mode> <V> is the phase offset of HAPR (internal horizontal sync pulse) timing (MSB) in the camera DSP.

ADDRESS 27h < R / W > **DEF:16h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	1/0	0/1	1/0	1/0	0/1

BIT7-0 : HOUTPH[7:0] <V> is the phase offset of HD (@ output terminal) timing (lower 8bit)
The phase is shifted with 1 pixel clock step.

ADDRESS 28h < R / W > **DEF:23h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	1/0	1/0	1/0	1/0	0/1

BIT7 : HOUTPH[8] <V> is the phase offset of HD (@ output terminal) timing (MSB)

BIT6-0 : VOUTPH <V> is the phase offset of VD (@ output terminal) timing
The phase is shifted with single H(horizontal) period step.

ADDRESS 29h < R / W > **DEF:08h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0	0	1/0	0/1	0/1	0/1

BIT7 : FSSTBSW <V> is output selection of flash strobe pulse.
0h : Output disable ("L" by Positive)1h : Output enable

BIT6 : FSSTBPOL <V> is the setting of flash strobe pulse polarity
0h : Positive 1h : Negative

BIT3-0 : FSSTBPH <V> is the phase offset of FSSTB (@ output terminal) timing
The phase is shifted with single H(horizontal) period step.

ADDRESS 2Ah < R / W > **DEF:08h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0	0	1/0	0/1	0/1	0/1

BIT3-0 : FSSTBW <V> is able to change pulse width of FSSTB (@ output terminal) .
The width is changed by one H(horizontal) period.

ADDRESS 2Bh < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0	0	0/1	0/1	0/1	0/1

BIT3-0 : SCMD <Test mode> <N> TEST mode of sensor block

ADDRESS 2Ch < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-0 : SCMD <Test mode> <N> TEST mode of sensor block

ADDRESS 2Dh < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-4 : SCMD <Test mode> <N> TEST mode of sensor block
BIT3 : SCMD <Test mode> <N> Compensation function in Spot light.
0h : Compensation function OFF 1h : Compensation function ON

BIT2-0 : SCMD <Test mode> <N> TEST mode of sensor block

ADDRESS 2Eh < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7 : TCSB1L <Test mode> <N>
BIT6-4 : TCPEROSW <Test mode> <N>
BIT3 : TCSBIN <Test mode> <N>
BIT2 : TCRAM <Test mode> <N>
BIT1-0 : TCROM <Test mode> <N>

ADDRESS 2Fh < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7 : TCRAMS <Test mode> <N>
BIT6 : TSPCHK <Test mode> <N>
BIT5 : TCPERAGC <Test mode> <V>
BIT4 : TALCRST <V> is non-effect switch of ALC counter reset when FPS or ESRLSW have changed.
0h : reset 1h : non-reset

BIT3 : TWBS <Test mode> <V>
BIT2 : TWBG <Test mode> <V>
BIT1-0 : TACDET <Test mode> <V>

ADDRESS 30h < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)

ADDRESS 31h < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7 : TALCDISP <Test mode> <N>
BIT6-4 : TALCOSW[2:0] <Test mode> <V>
BIT3-2 : PBDISP <Test mode> <N>
BIT1-0 : TDISP <Test mode> <N>

ADDRESS 32h < R only > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	*	*	*	*	*	*	*

BIT6-0 : ESROUT is the current internal electrical shutter speed of ALC operation

ADDRESS 33h < R only > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
*	*	*	*	*	*	*	*

BIT7-0 : ESROUT is the current internal electrical shutter speed of ALC operation

ADDRESS 34h < R only > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
*	*	*	*	*	*	*	*

BIT7-0 : AGOUT is the current internal analog gain up data for ALC operation

ADDRESS 35h < R only > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	*	*	*	*	*	*

BIT7-0 : DGOUT is the current internal digital gain up data for ALC operation

ADDRESS 36h < R only > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
*	*	*	*	*	*	*	*

BIT7-0 : ALCDATA is the current accumulated luminance data.

ADDRESS 37h < R only > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
*	*	*	*	*	*	*	*

BIT7-0 : AWBRYDA is the current accumulated R-Y data.

ADDRESS 38h < R only > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
*	*	*	*	*	*	*	*

BIT7-0 : AWBBYDA is the current accumulated B-Y data.

ADDRESS 39h < R / W > **DEF:8Ch**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	0/1	0/1	0/1	1/0	1/0	0/1	0/1

BIT7-6 : AGSLOW1 <V> is the function to improve ALC operation in dark light condition. From this gain level sensor shifts ALCSPD 1 step down.
0h : OFF 1h : +21.5dB 2h : +15.5dB 3h : +9.5dB

BIT5-4 : FLLSMODE <V> is additional function for flickerless operation .
0h : Normal mode (normal ALC operation without special treatment)
1h : Procedure1 : This mode never go faster exposure time than 10 msec (in case of 50 Hz flickerless mode) or 8.3 msec (in case of 60 Hz flickerless mode).
2h : Procedure 2 : Until luminance exceeds the value of FLLSLIM stay on the fastest flickerless electrical shutter speed.
3h : In addition to procedure 2, a hysteresis characteristics is implemented.

BIT3-0 : FLLSLIM <V> is the brightness limiter of FLLSMODE 2h or 3h.

FLLSLIM is the value of luminance level divided by 16.
For example, when the average converging luminance level is 150 in ALC operation, if the brightness

limit is assumed 192, “Ch” is loaded in FLLSLIM register under the calculation of 192 /16 = 12.

ADDRESS 3Ah < R / W > DEF:CFh

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	1/0	0/1	0/1	1/0	1/0	1/0	1/0

BIT7-4 : DETSEL <V> is the setting of flicker detection time (The unit is V (frame interval))
0h : 15V (slowest)
| |
Bh : 4V
| |
Ch : 3V (fastest)
The camera DSP detects appearance of drifting flicker during the detection time stipulated by DETSEL. When the drifting flicker is detected, the 60Hz or 50 Hz setting is automatically changed to the other.

BIT3-0 : ACDETNC <V> is the flicker detection sensitivity in flicker detection mode
0h : highest sensitivity (luminance level difference is more than 1/16LSB)
| |
Fh : lowest sensitivity (luminance level difference is more than 1LSB)

ADDRESS 3Bh < R / W > DEF:80h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-6 : AGSLOW2 <V> is the function to improve ALC operation in dark light condition. From this gain level sensor shifts ALCSPD 2 step down.
0h : OFF 1h : +18dB 2h : +12dB 3h : +6dB

BIT5-0 : DG <N> is Manual setting of digital gain.
This command is effective in ALCSW=”1”.
00h : x1
| |
3Fh : x1.984375

ADDRESS 3Ch < R / W > DEF:00h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-0 : REJHLEV <V> is threshold level of bright block rejection. If those blocks are brighter than this level, they are rejected up to the numbers of REJH. This mode affects only in ALC back light mode (in case of ALCMODE =’ 3h’).
00h : Minimum level (In this case the maximum blocks determined by REJH are automatically rejected.)
| |
FFh : Maximum level (In this case no blocks are excluded.)

ADDRESS 3Dh < R / W > DEF:17h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	1/0	0/1	1/0	1/0	1/0

BIT7 : ALCLOCK <V> is freezing function of ALC operation. Shutter speed and gain setting are kept in freezing.
0h : ALC operation 1h : Operation freeze

BIT6 : FPSLNKSW <V> is link switch of maximum exposure time to FPS
0h : Link to FPS 1h : Not link to FPS

BIT5-4 : ALCSPD <V> is the setting of ALC response speed. The actual speed is depend on frame rate.

0h : Slow 1h : Normal 2h : Fast

BIT3-2 : ALCSTEP <Test mode> <V> is the setting of ALC control step
0h : Logarithmic step for the range of >32 H electrical shutter control with flickerless operation.
Linear step for other range.
1h : Linear step in all range
2h-3h : Linear step for the range of >32 H electrical shutter control with flickerless operation.
Logarithmic step for other range.

BIT1-0 : REJH <V> is selection of reject block numbers in back light mode.
0h : 0 block 1h : 1 block 2h : 2 blocks 3h : 4 blocks (out of 16 blocks)

ADDRESS 3Eh < R / W > DEF:85h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	0/1	0/1	0/1	0/1	1/0	0/1	1/0

BIT7 : SHESRSW <V> is the Enable/Disable switch of super high speed ESR. It realize less than 1H operation in ALC.
0h : Disable 1h : Enable

BIT6 : ESLIMSEL <V> is link switch of maximum exposure time to ESRLSW
0h : Link to ESRLSW 1h : Not link to ESRLSW

BIT5-4 : SHESRSPD <V> is the manual setting of super high speed ESR
0h : OFF (more than 1H) 1h : 1/2H 2h : 1/4H 3h : 1/8H

BIT3-2 : ELSTEP <V> is the response speed in extra long ESR mode
0h : x1 (slow) 1h : x2 2h : x4 3h : x8 (fast)

BIT1-0 : ELSTART <V> is the setting of an initial ESR value in extra long ESR mode
0h : 1/4 of maximum ESR 1h : 1/2 of maximum ESR
2h : 3/4 of maximum ESR 3h : maximum ESR

ADDRESS 3Fh < R / W > DEF:C0h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	1/0	0/1	0/1	0/1	0/1	0/1	0/1

BIT7-0 : AGMIN[7:0] <Test mode> <V> is the setting of reference voltage for AD converter level (higher 8bit).

ADDRESS 40h < R / W > DEF:00h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0	0	0	0/1

BIT7 : LI1POL <Test mode> <N>
BIT6 : CS1POL <Test mode> <N>
BIT5 : LI3POL <Test mode> <N>
BIT4 : CS3POL <Test mode> <N>
BIT0 : DINCKSW <Test mode> <N>

ADDRESS 41h < R / W > DEF:00h

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT7 : JAMP <Test mode> <N> is the polarity switch for color jam correction
0h : to add R to G on GR line 1h : to subtract R to G on GR line

BIT6-0 : JAMG <Test mode> <N> Value of color jam correction
00h : 0%
| |
7Fh : 24.8% of original R

ADDRESS 42h < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0/1	0/1	0/1	0/1	0/1	0/1

BIT5-0 : PREGRG <N> is the preset of RGB gain setting (G on GR line)
00h : x1
| |
3Fh : x2.96875

ADDRESS 43h < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0/1	0/1	0/1	0/1	0/1	0/1

BIT5-0 : PREGBG <N> is the preset of RGB gain setting (G on BG line)
00h : x1
| |
3Fh : x2.96875

ADDRESS 44h < R / W > **DEF:15h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0/1	1/0	0/1	1/0	0/1	1/0

BIT5-0 : PRERG <N> is the preset RGB gain setting (R)
00h : x1
| |
3Fh : x2.96875

ADDRESS 45h < R / W > **DEF:1Fh**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0/1	1/0	1/0	1/0	1/0	1/0

BIT5-0 : PREBG <N> is the preset RGB gain setting (B)
00h : x1
| |
3Fh : x2.96875

ADDRESS 46h **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0	0	0	0	0	0

There are no parameter in this address.

ADDRESS 47h < R / W > **DEF:44h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	1/0	0/1	0/1	0/1	1/0	0/1	0/1

BIT6-0 : MSKBR <N> is the masking level setting (R value to B) in the color correction matrix
BIT6:
0h : Addition 1h : Subtraction
BIT5-0:

00h : 0%
| |
3Fh : 49.21876%

ADDRESS 48h < R / W > **DEF:44h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	1/0	0/1	0/1	0/1	1/0	0/1	0/1

BIT6-0 : MSKGR <N> is the masking level setting (R value to G) in the color correction matrix
BIT6:
0h : Addition 1h : Subtraction
BIT5-0:
00h : 0%
| |
3Fh : 49.21876%

ADDRESS 49h < R / W > **DEF:20h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0/1	1/0	0/1	0/1	0/1	0/1	0/1

BIT6-0 : MSKRB <N> is the masking level setting (B value to R) in the color correction matrix
BIT6:
0h : Addition 1h : Subtraction
BIT5-0:
00h : 0%
| |
3Fh : 49.21876%

ADDRESS 4Ah < R / W > **DEF:45h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	1/0	0/1	0/1	0/1	1/0	0/1	1/0

BIT6-0 : MSKGB <N> is the masking level setting (B value to G) in the color correction matrix
BIT6:
0h : Addition 1h : Subtraction
BIT5-0:
00h : 0%
| |
3Fh : 49.21876%

ADDRESS 4Bh < R / W > **DEF:66h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	1/0	1/0	0/1	0/1	1/0	1/0	0/1

BIT6-0 : MSKRG <N> is the masking level setting (G value to R) in the color correction matrix
BIT6:
0h : Addition 1h : Subtraction
BIT5-0:
00h : 0%
| |
3Fh : 49.21876%

ADDRESS 4Ch < R / W > **DEF:30h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0/1	1/0	1/0	0/1	0/1	0/1	0/1

BIT6-0 : MSKBG <N> is the masking level setting (G value to B) in the color correction matrix
BIT6:
0h : Addition 1h : Subtraction
BIT5-0:
00h : 0%
| |
3Fh : 49.21876%

ADDRESS 4Dh < R / W > **DEF:E0h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
1/0	1/0	1/0	0/1	0/1	0/1	0/1	0/1

BIT7 : HDTCSW <N> is the Enable/Disable switch for enlarging coring level of horizontal detail in dark light condition.
0h : Disable 1h : Enable

BIT6 : VDTCSW <N> is the large coring of vertical detail in dark light condition.
0h : Disable 1h : Enable

BIT5-0 : DTCYLV is the luminance level setting for enlargement of coring in dark light condition.
Enlargement of coring is enabled in the case of Luminance level < DTCYLV.

ADDRESS 4Eh < R / W > **DEF:20h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	1/0	0/1	0/1	0/1	0/1	0/1

BIT7 : HDTPSW <N> is the switch for extra enhancement of horizontal detail
0h : Normal 1h : 4 times enhancement

BIT6 : VDTPSW <N> is the switch for extra enhancement of vertical detail
0h : Normal 1h : 4 times enhancement

BIT5-0 : DTCGAIN <N> is the gain setting for enlargement of coring in dark light condition.
00h : (DTCYLV-YH)x0
| |
3Fh : (DTCYLV-YH)x1.96875

ADDRESS 4Fh < R / W > **DEF:09h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0	0/1	1/0	0/1	0/1	1/0

BIT7 : LI12POL <Test mode> <N>
BIT6 : CS12POL <Test mode> <N>
BIT4 : DTLLIMSW <N> is vertical detail suppression in bright light condition..
0h : OFF 1h : Suppression is active

BIT3-0 : DTLYLIM <N> is suppression level of vertical detail in bright light condition.
00h : maximum suppression
| |
3Fh : minimum suppression

ADDRESS 50h < R / W > **DEF:07h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0	0/1	0/1	0/1	1/0	1/0	1/0

BIT7 : YLCUTLMSK <N> is ON / OFF of Y lower limit for white pixel detection in AWB.
0h : Y lower limit ON 1h : Y lower limit OFF

BIT5-0 : YLCUTL <N> Y lower limit level for white pixel detection in AWB.
0h : If Y level of the pixel is more than 0LSB, the pixel is considered as white pixel
| |
1h : If Y level of the pixel is more than 4LSB, the pixel is considered as white pixel
| |
3Fh : If Y level of the pixel is more than 255LSB, the pixel is considered as white pixel

ADDRESS 51h < R / W > **DEF:2Fh**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0	1/0	0/1	1/0	1/0	1/0	1/0

BIT7 : YLCUTHMSK <N> is ON / OFF of Y upper limit setting for detection of white pixels in AWB
0h : Y upper limit ON 1h : Y upper limit OFF

BIT5-0 : YLCUTH <N> is the Y upper limit level for detection of white pixel in AWB
0h : If Y level of the pixel is less than 3LSB, the pixel is considered as white pixel
| |
1h : If Y level of the pixel is less than 7LSB, the pixel is considered as white pixel
| |
3Fh : If Y level of the pixel is less than 255LSB, the pixel is considered as white pixel

ADDRESS 52h < R / W > **DEF:02h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0/1	0/1	0/1	0/1	0/1	1/0	0/1

BIT6-0 : UVSKNC <V> is the setting for AWB. If B-R value have changed beyond this setting range, AWB will be activated.
1h : Suppression is minimum
| |
7Fh : Suppression is maximum

ADDRESS 53h < R / W > **DEF:00h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

BIT6-0 : UVLJ <V> is gain setting to set the range AWB converge slowly.
When integrated value of B or R gain is not over UVLJ during 5V, convergence speed for AWB will be slow.

ADDRESS 54h < R / W > **DEF:2Bh**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	1/0	0/1	1/0	0/1	1/0	1/0

BIT7-0 : WBGMIN <V> is the minimum setting of R gain and B gain
00h : x0
| |
20h : x0.25
| |
FFh : x4

ADDRESS 55h < R / W > **DEF:60h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	1/0	1/0	0/1	0/1	0/1	0/1	0/1

BIT7-0 : WBGMAX <V> is maximum setting of R gain and B gain
00h : x0
| |
80h : x2
| |
FFh : x4

ADDRESS 56h < R / W > **DEF:40h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	1/0	0/1	0/1	0/1	0/1	0/1	0/1

BIT7 : AWBCSPOL <Test mode> <N> is phase adjustment for AWB calculation
0h : Normal 1h : Inverted

BIT6 : WBDIVCLP <Test mode> <V> is selection of clipping way in divide calculation
0h : Normal 1h : 2 times sensitivity

BIT5-4 : WBNOLJ <Test mode> <V> is switch for UVLJ non-effect detection level
0h : OFF 1h : 4/16 2h : 8/16 3h : 12/16

BIT3 : WBNOLJSC <Test mode> <V> is source selection of UVLJ non-effect detection
0h : Result of division 1h : Multiplied value

BIT2 : WB2IM1 <Test mode> <V> is AWB mode it acts like 1 axis AWB.
0h : 2 axis AWB 1h : Acts like 1 axis AWB

BIT1-0 : WBSPDUP <V> is base source of speed up AWB convergence.
0h : Off
1h : by multiplied value
2h : by divided value
3h : by multiplied pixel number

ADDRESS 57h < R / W > **DEF:06h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	0	0	0	1/0	1/0	0/1

BIT2-0 : WBDIVSC <Test mode> <V> is the division way selection of AWB.
0h : Divided by the integral value.
| |
7h : Divided by the pixel number

ADDRESS 58h < R / W > **DEF:22h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	1/0	0/1	0/1	0/1	1/0	0/1

BIT5 : ALLAREA <N> is the ON/OFF switch of white area detection
0h : White area detection is ON 1h : White area detection is OFF
When white area detection is ON, the gain adjustment of RGB is adjusted by the value of pixels that are regarded as white according to the setting of YLCUTLMSK,YLCUTL,YLCUTHMSK and YLCUTH.
BIT4 : WBLOCK <V> is for freeze AWB operation.
0h : Normal mode 1h : White balance AWB operation freeze
BIT3-0 : WB2SP <V> is the converging speed of AWB
0h : Slow

| |
Fh : Fast

ADDRESS 59h < R / W > **DEF:23h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0	0	1/0	0/1	0	0	1/0	1/0

BIT5 : KIZUSW <N> is the ON/OFF switch for automatic blemish detection and correction.
0h : Blemish detection OFF 1h : Blemish detection ON

BIT4 : PBRDSW<N> is the blemish correction mode switch (the way of correction)
0h : Interpolation with the surrounding 8 pixels with the same color
1h : Interpolation with the surrounding 4 pixels with the same color

BIT1-0 : ABCSW <N> is the blemish detection mode switch (the way of detection)

1h When the level difference between the pixel checking and the surrounding pixels of the same color is larger than PBDLV described in ADDRESS 37h, the pixel is regarded as a blemish pixel.
2h : When the level of the pixel checking is the maximum or minimum compared with the surrounding 8 pixels with the same color. the pixel is regarded as a blemish pixel.
0h : OR of the above 1h and 2h
3h : AND of the above 1h and 2h

ADDRESS 5Ah < R / W > **DEF:08h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	1/0	0/1	0/1	0/1

BIT7-0 : PBDLV <N> is the threshold level setting for blemish detection
00h : Maximal capability of detection
| |
FFh : Minimal capability of detection

ADDRESS 5Bh < R / W > **DEF:04h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	0/1	1/0	0/1	0/1

BIT7-0 : PBC1LV <N> is the exclusion level setting to avoid misdetection of the stars as blemish
00h : Maximum exclusion
| |
FFh : Minimum exclusion

ADDRESS 5Ch < R / W > **DEF:08h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	1/0	0/1	0/1	0/1

BIT7-0 : PBC2LV <N> is the exclusion level setting to avoid misdetection of the vertical or horizontal stripe.

00h : Minimum exclusion
| |
FFh : Maximum exclusion

ADDRESS 5Dh < R / W > **DEF:08h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	1/0	0/1	0/1	0/1

BIT7-0 : PBC3LV <N> is the exclusion level setting to avoid misdetection of tilt line.

(the tilt line with 45 degree)
00h : Minimum exclusion
| |
FFh : Maximum exclusion

ADDRESS 5Eh < R / W > **DEF:08h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	1/0	0/1	0/1	0/1

BIT7-0 : PBC4LV <N> is the exclusion level setting to avoid misdetection of the acute angle.
00h : Minimum exclusion
|
FFh : Maximum exclusion

ADDRESS 5Fh < R / W > **DEF:08h**

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
0/1	0/1	0/1	0/1	1/0	0/1	0/1	0/1

BIT7-0 : PBC5LV <N> is the exclusion level setting to avoid misdetection of the type two of tilt line.
(the tilt line (flip of PBC3LV))

00h : Minimum exclusion
| |
FFh : Maximum exclusion

3 Selection of input clock (External clock)

3.1 Clock format

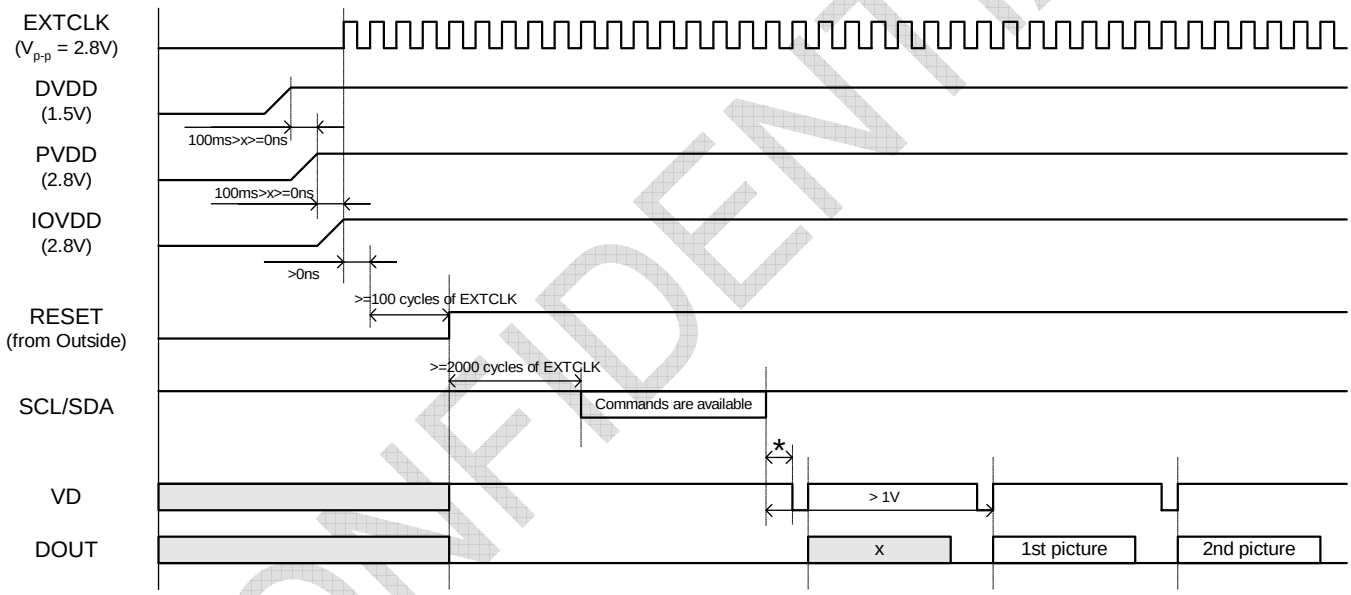
Please use clock format that are defined in Technical data.

3.2 Clock frequency

No PLL circuit is provided. Data rate is proportional to external clock input. In case of 24.57MHz as external clock, 30fps is available.

4 Power on sequence

4.1 Power on



* ((VOUTPH + 3) - VRRPH) + 4
In default case: VOUTPH=35dec, VRRPH=38dec, ((35 + 3) - 38) + 4 = 4H

D_MASK=1

TCM8230MD cannot output pictures after power on immediately. You should be sent some I^2C commands after power on as below.

Address=03h, Data=00h (Default Data=80h)

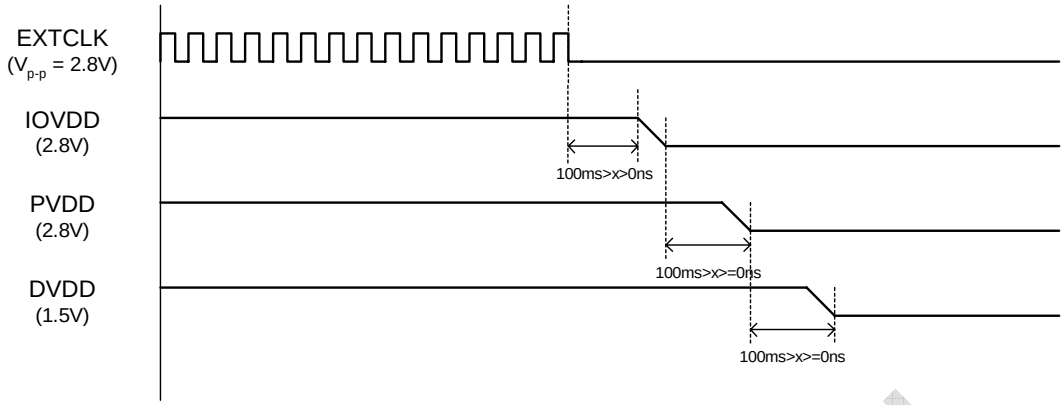
4.2 Initialization

Be sure to set following command in initialization. These address need to be fixed to those settings. This is mandatory.

Address = Data
0x22 = 0x28

Other settings except for above are need to decide according to the system condition. Please define initialize setting suitable for your opportunity. And set only different settings compared with default.

5 Power off sequence



6 Sleep mode

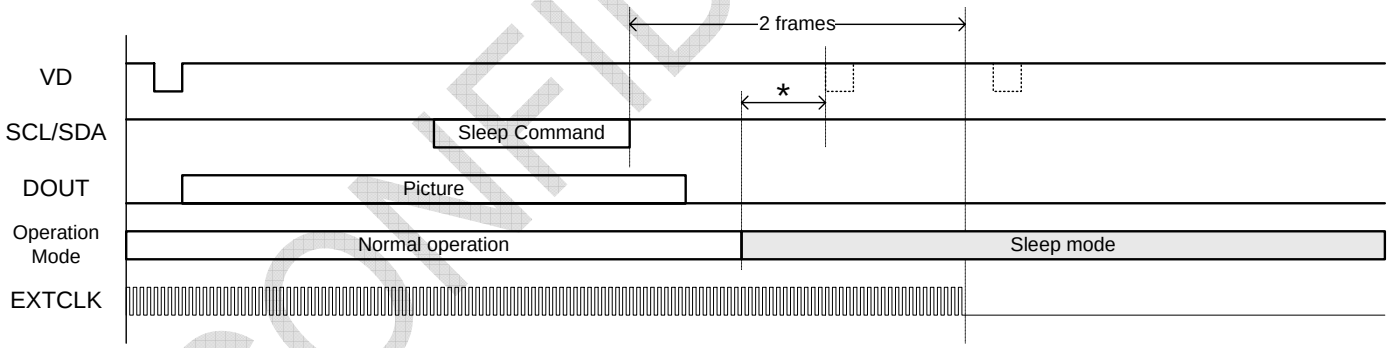
6.1 Sleep sequence

(1) Sleep mode command ON : 0x1F=0x80

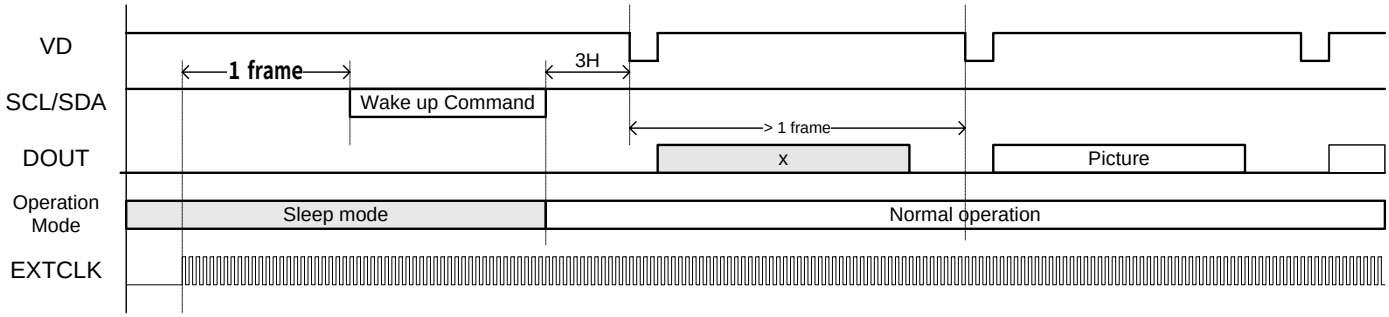
Note: All VDD is need to keep supplying in Sleep mode, and Extclk should be off.
But it doesn't matter External clock ON and OFF.

6.2 Wake-up sequence

(1) Sleep mode command OFF: 0x1F=0x00



* ((VOUTPH + 3) - VRRPH) + 4
In default case: VOUTPH=35dec, VRRPH=38dec, ((35 + 3) - 38) + 4 = 4H



D_MASK=1

6.3 Sleep mode pin status

DOUT0-7 HD,VD: Keep final status before sleep.

6.4 Sleep mode register status

Keep final status before sleep.
Note : All parameters cannot be read and written in sleep mode except for SLEEPSW.

7 I/F for parameter setting

This module use IICBUS fast mode for parameter setting.

7.1 Slave address

0x78 : Write data to this module by controller operation.
0x79 : Read data from this module by controller operation.
Note : Please refer to technical data in detail.

8 Explanation of each function

8.1 Output format

8.1.1 Registers for this function

0x02 FPS, DCLKP
0x03 DOUTSW , DATAHZ , PICSIZ , PICFMT
0x04 V_INV , H_INV , ESRLSW , V_LENGTH
0x1E D_MASK , CODESW , CODESEL , HSYNCSEL , TESPIC , PICSEL
0x20 HNUM
0x27 HOUTPH
0x28 HOUTPH , VOUTPH
0x29 FSSTBSW
0x2F TALCRST

8.1.2 Frame rate

Frame rate can be decide by the FPS , ESRLSW , V_LENGTH , HNUM
If external clock input is standard for this module.

Note :
~~~~~~
* HNUM need to be used with SHESRSW [0x3E bit7]=0h. | This is mandatory.
~~~~~~
If you want to use SHESRSW [0x3E bit7]=1h , HNUM must be set to 00h.

Other frame rate can be adjusted little bit by HNUM.
Frame rate = PCK / (780 + HNUM x 2) x 525

8.1.3 Output data status (DCLK, DOUT, HD, VD, FSSTB)

By using following registers, output data status can be changed.

Registers			Output pins	
DATAHZ	DOUTSW	FSSTBSW	DOUT,DCLK,HD,VD	FSSTB
0	0	-	Normal output	-
	1	-	Low fixed	-
1	Don't care	Don't care	Hiz	Hiz
-	-	0	-	Low fixed
-	-	1	-	FSSTB output

By using DCLKP, DCLK polarity can be changed.
0: Data can be captured by rising edge of DCLK.
1: Data can be captured by falling edge of DCLK.

8.1.4 Output Image

<SIZE>
Output image size can be changed by PICSIZ

<ASPECT>
Output image aspect can be changed by H_INV and V_INV.
H_INV is for horizontal flip and V_INV is for vertical flip.

<FORMAT>
RGB and YUV can be select by PICFMT

<MASKING>
Out put picture can be masked by D_MASK.
When you set D_MASK , output pictures are fixed to black in following case.
1. After Power on
2. After FPS and PICSIZE have been changed.

<TEST PICTURE>
Following test picture can be available by TESPIC and PICSEL.
1. Color bar
2. Ramp

8.1.5 Vertical and Horizontal synchronization

Synchronization code and pulse are available.

<In case of synchronization code>
By setting CODESW it can be selected if codes are embedded in DOUT or not.
2 mode can be selected by CODESEL

<In case of synchronization pulse>
Those pulses are output from VD and HD pin.
By setting HSYNCSEL, horizontal pulse can be selected from HD or H blanking.

8.2 Luminance control

8.2.1 Registers for this function

0x0D GAMSW
0x11 CONT
0x12 BRIGHT
0x19 MHMODE , MHLPFSEL , YMODE , MIXHG
0x32 ESROUT
0x33 ESROUT
0x34 AGOUT
0x35 DGOUT
0x36 ALCDATA

8.2.2 Basic luminance adjustment

< Gamma>
Gamma can be set ON/OFF by GAMSW.

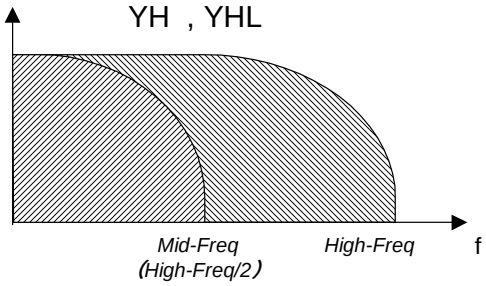
< Brightness>
Black level can be adjust by BRIGHT. Each brightness can be sift by this register.

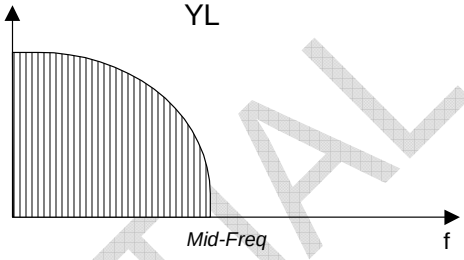
< Contrast>
Contrast can be change by CONT.

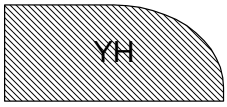
8.2.3 Y calculation setting

Y is made from composition of YH,YHL and YL

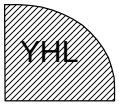
YH -------- Luminance signal with high frequency component
YL -------- Basic Luminance signal with middle frequency component
YHL ------ Luminance signal with middle frequency component (half of high frequency) of YH. .



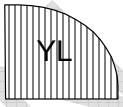




YH means Y data includes high frequency component.



YHL means only low frequency component deprived from YH

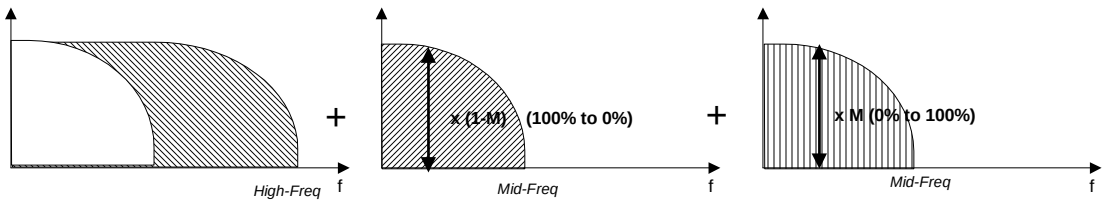


YL means Y data includes only low frequency component

< YMODE >
Combination of Y components can be select by YMODE.
0 : Mixed Highs
1 : YH only
2 : YL only
3 : YHL only

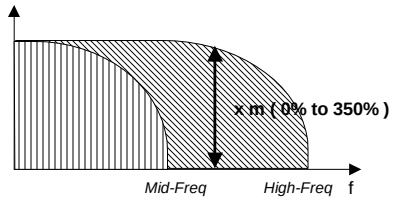
< MIXED HIGHS >
Mixed Highs means the way of composition YH YL and YHL.
The way of mixing can be select by MHMODE.
Percentage of mixing can be set by MIXHG.

MHMODE
0 : Y = (YL-YHL)*MIXHG + YH
This setting uses YH In high frequency area and mix of YHL*[1-MIXHG)%, YL *[MIXHG]% in middle-low frequency area.



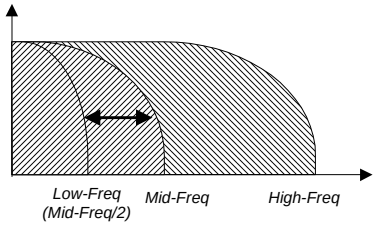
1 : Y
= (YH-YHL)*MIXHG + YL
This setting uses YL In middle-low frequency area and high frequency area of YH*[MIXHG)%

in high frequency area.



< Setting of YHL >
YHL frequency area can be changed by MHLPFSEL.

MHLPFSEL
0 : YHL = Low-middle frequency area, YH-YHL = High frequency area
1 : YHL = Low frequency area, YH-YHL = Middle-high frequency area



8.2.4 Readout internal status

Internal status can be read for external brightness control

ESROUT ---------- Electrical shutter status
AGOUT ---------- Sensor gain up status
DGOUT ---------- DSP digital gain up status
ALCDATA---------- Reference data of brightness

8.3 Auto luminance control

8.3.1 Registers for this function

0x02 FPS , ACF , ACFDET
0x04 ESRLSW , V_LENGTH
0x05 ALCSW , ESRLIM
0x08 ALCMODE , ALCH
0x09 ALCL
0x1B AGLIM
0x1C ES100S
0x1D ES120S
0x39 AGSLOW1 , FLLSMODE , FLLSLIM
0x3A DETSEL , ACDTNC
0x3B AGSLOW2
0x3C REJHLEV
0x3D ALCLOCK , FPSLNKSW , ALCSPD , REJH
0x3E SHESRSW , ESLIMSEL , SHESRSPD , ELSTEP , ELSTART

8.3.2 ALC (automatic luminance control)

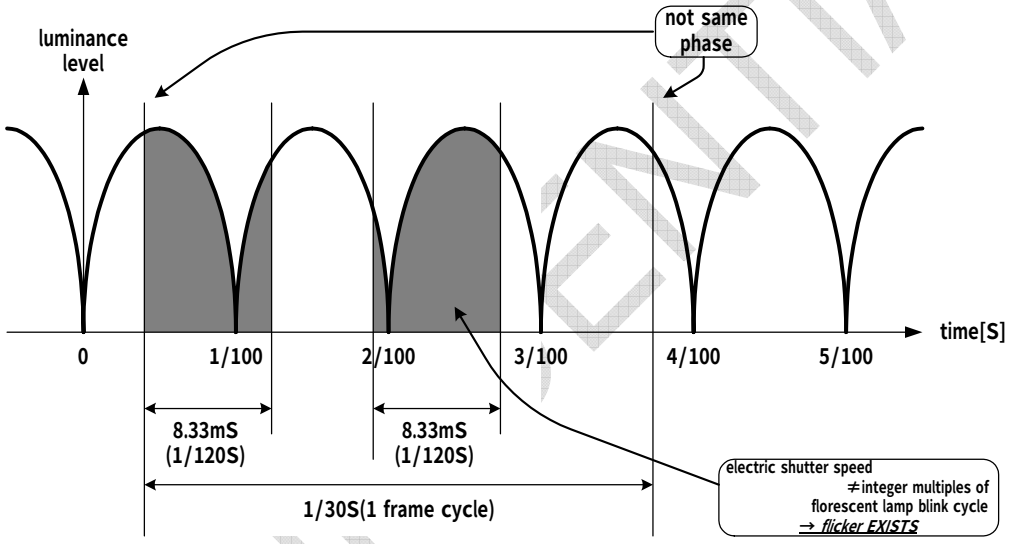
<Selection of ALC or manual exposure>
Auto exposure or manual exposure can be selected by ALCSW.

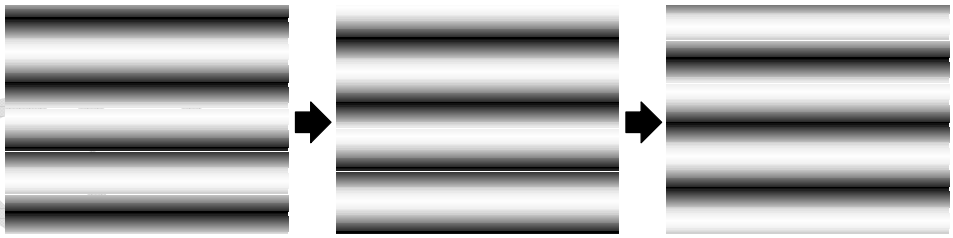
<ALC OPERATION>

ALC mode can be change by ESRLSW.
Normal mode (0h) and Long exposure mode (1h) is Flickerless ALC.
Extra long exposure mode is not Flickerless ALC.

<Basic Flickerless settings>
ES100S is need to be set for AC=50Hz flicker.
ES120S is need to be set for AC=60Hz flicker.
Both of them need to set as follows.
PCK/{(780+2*HNUM)*2*(AC frequency)}
*Note : In regarding as the PCK , please refer to 9.1.2.
Ex. In the condition of PCK=12,285MHz, HNUM=0, AC=50Hz and 60Hz
12.285M/{(780+2*0)*2*(50)}=158[dec]=9E[hex]
12.285M/{(780+2*0)*2*(60)}=131[dec]=83[hex]

<Auto detection of 50Hz / 60Hz flicker>
Auto detection can be available by ACFDET.
Initial mode of auto detection can be set by ACF
If flicker is drift as follow figure , this function switch mode to the other.





The case of "drifting flicker"

Drift condition can be checked as follows.
2*(AC frequency)/frame rate

If this result is almost an integer, flicker detection is not work.
If this result is not an integer (it's better if it close to *.5), flicker detection will work.

Ex1. In the condition AC=50Hz, 60Hz frame rate =15
2*50/15=6.7 2*60/15=8
So in AC=50Hz condition it will work but in the AC=60Hz condition it won't.
So in this condition ACF (Start mode setting) need to be set as 60Hz mode.

Ex2. In the condition AC=50Hz, 60Hz frame rate =20
2*50/20=5 2*60/20=6
So in both of AC=50Hz and AC=60Hz condition it won't work.
So flickerlss auto detection cannot be used in this framerate.

Speed of detection can be set by DETSEL
Sensitivity of detection can be set by ACDETNC.
Note: If you want to change these parameter from default, you have to check carefully if it cause miss-detection or not. Basically DETSEL Is better to use by default.

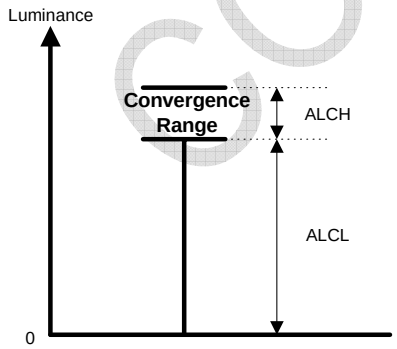
<Manual 50Hz / 60Hz frickerless mode>
If you set ACFDET as manual, 50Hz or 60Hz mode can be select in ACF.

<Maximum exposure time setting in ALC>
In case of ESRLSW=Normal(0h) or Long(1h)
It can be set by the combination of ESRLIM , FPSLINKSW and ESLIMSEL
Note : Please set this by faster time than one frame speed. If you set this slower than one frame speed flickerless operation will cause some trouble. In case of no PLL operation, Extclk of 24.57MHz realize 30fps operation.

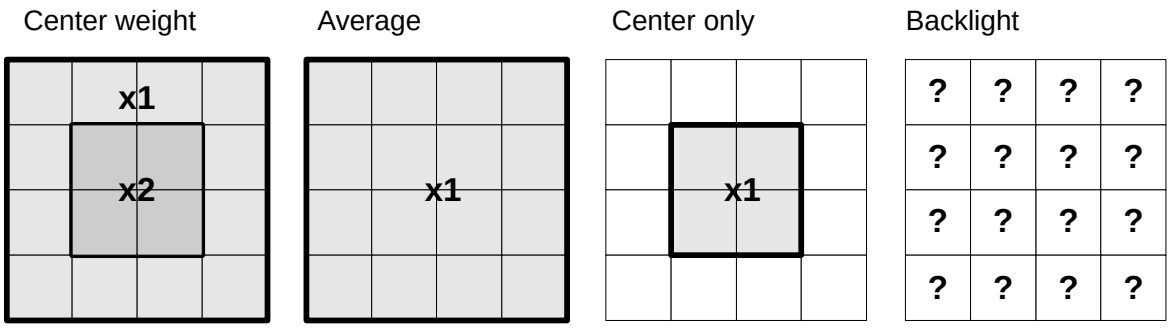
FPS	Max exposure time	Registers				
		FPS	ESRLSW	ESRLIM	FPSLINKSW	ESLIMSEL
30 fps	1/30 s	0	0	0	0	0
15 fps	1/30 s	1	0	0	1	0
	1/15 s				0	
7.5 fps	1/30 s	0	1	0	0	1
	1/15 s			1		
	1/7.5 s			2		
3.75 fps	1/30 s	1	1	0	1	1
	1/15 s				0	
	1/7.5 s			1		
	1/3.75s			0		0

<Maximum gain-up setting in ALC>
Maximum gain can be set by AGLIM.

<ALC convergence range >
ALC convergence range can be set by ALCL and ALCH.



<ALC reference average calculation >
ALC reference average can be select by ALCMODE.
For each mode luminance average is calculated from following area.



In Back light mode luminance average will be calculated by following settings

Rejection block numbers in calculation can be set by REJH.

Thresh level of rejection can be set by REJHLEV.

The blocks which brightness level is over REJHLEV are removed from calculation up to the numbers of REJH.

<Super High speed shutter>
Super High speed shutter can be used by SHESRSW.
If you use super high, electrical shutter will go 1/4 H at the fastest. (Basic mode 1H is the fastest.)

<Convergence speed>
Speed can be selected by ALCSPD.
In Extra long exposure mode, ELSTEP can be used for speed control.
And for gain-up AGSLOW1 and AGSLOW2 can be used.

8.4 Manual exposure control

8.4.1 Registers for this function

0x05	ALCSW , ESRSPD
0x06	ESRSPD
0x07	AG
0x3B	DG
0x3E	SHESRSPD

8.4.2 Manual exposure setting

If you set ALCSW as manual , manual exposure can be used.
Exposure time can be set by ESRSPD. And Gain up can be set by AG and DG.
If you set SHESRSPD 1/2H,1/4H and 1/8H can be used.

8.5 Edge enhancement

8.5.1 Registers for this function

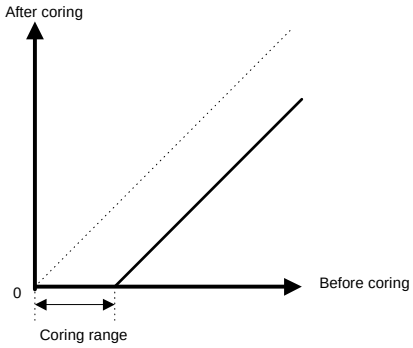
0x0E	HDTG
0x0F	VDTG
0x10	HDTCORE , VDTCORE
0x4D	HDTCSW , VDTCSW , DTCYLV
0x4E	HDTPSW , VDTPSW , DTCGAIN
0x4F	DTLLIMSW , DTLYLIM

8.5.2 Edge enhancement setting

<Basic edge enhancement>
HDTG and VDTG is the basic edge enhancement setting.
If you use HDTPSW and VDTPSW those enhancement boost x4.

Edge enhancement coring>

HDTGCORE and VDTGCORE is the coring of edge enhancement.
If you set this parameter, following coring range turn to 0 level. By this parameter low noise can be neglected.



In dark portion coring can be enhanced by the setting of HDTCSW , VDTCSW , DTCYLV and DTCGAIN.
HDTCSW and VDTCSW is ON/OFF of coring enhancement.
DTCYLV is thresh level of dark pixel.
DTCGAIN is enhancement level.

In bright light pixel edge enhancement suppression can be suppressed by DTLLIMSW and DTLYLIM.
DTLLIMSW is ON/OFF switch of suppression in bright light pixel.
DTLYLIM is suppression level setting.

8.6 Color control

8.6.1 Registers for this function

0x13	VHUE
0x14	UHUE
0x15	VGAIN
0x16	UGAIN
0x17	UVCORE
0x18	SATU
0x37	AWBRYDA
0x38	AWBBYDA

8.6.2 Color correction

Hue can be adjust by VHUE,UHUE,VGAIN and UGAIN
Saturation can be set by SATU.
Color coring can be set by UVCORE. Please refer to figure of HDTGCORE.

8.6.3 Readout internal status

Internal status can be read for external white balance control

AWBRYDA ---------- R-Y reference data for white balance (2's)
AWBBYDA ---------- B-Y reference data for white balance (2's)

8.7 Auto white balance control

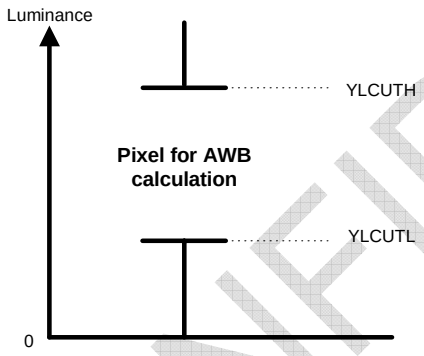
8.7.1 Registers for this function

0x0A	AWBSW
0x42	PREGRG
0x43	PREGBG
0x44	PRERG

0x45 PREBG
0x47 MSKBR
0x48 MSKRG
0x49 MSKRB
0x4A MSKGB
0x4B MSKRG
0x4C MSKBG
0x50 YLCUTLMSK , YLCUTL
0x51 YLCUTHMSK , YLCUTH
0x52 UVSKNC
0x53 UVLJ
0x54 WBGMIN
0x55 WBGMAX
0x56 WBSPDUP
0x58 ALLAREA , WBLOCK , WB2SP

8.7.2 Basic parameters
AWB or manual white balance can be select by AWBSW.
White balance starting position can be set by PRE***.
White balance convergence range can be set by WBGMIN and WBGMAX
Cross color correction can be set by MSK***.

8.7.3 Gate setting
Luminance gate can be set by ALLAREA, YLCUTL, YLCUTLMSK, YLCUTH and YLCUTHMSK.
If the pixel is not in the range which determined by above setting, it is not calculated in AWB.



In the condition of ALLAREA=0 , gate is available.
And if you set YLCUTLMSK or YLCUTHMSK, one side of the gate is disabled.

8.7.4 Hysterisis setting
Hysterisis can be set by UVSKNC.

8.7.5 Speed setting
Basic speed can be set by WB2SP.
Additionally speed control can be change by WBSPDUP.
Slow down range can be set by UVLJ.

8.7.6 Other setting

WB freeze can be set by WBLOCK.

8.8 Manual white balance control

8.8.1 Registers for this function

0x0A AWBSW
0x0B MRG
0x0C MBG

8.8.2 Settings
Manual white balance can be select by AWBSW.
White balance gain can be set by MRG and MBG.

8.9 Other function

8.9.1 Registers for this function
0x1F SLEEPSW , SRST
0x2D SCMD3

8.9.2 Sleep mode
Sleep mode can be used by SLEEPSW.
8.9.2 Reset
Software reset can be used by SRST.

8.10 Lens shading compensation

8.10.1 Registers for this function
0x1A LENS
0x1B LENSRPOL , LENSRGAIN

8.10.2 Basic lens shading compensation
Basic lens shading compensation can be used by LENS.

8.10.3 Corner colored shading compensation
Corner colored shading compensation can be used by LENSPOL and LENSRGAIN.
By this function red color in the corner area can be added or reduced. .

8.11 Dot noise compensation

8.11.1 Registers for this function
0x59 KIZUSW , PBRDSW , ABCSW
0x5A PBDLV
0x5B PBC1LV
0x5C PBC2LV
0x5D PBC3LV
0x5E PBC4LV
0x5F PBC5LV

8.11.2 Basic function
Dot noise compensation can be enabled by KIZUSW.
The way of dot noise detection can be selected by ABCSW.
Thresh level of detection can be set by PBDLV.
The way of dot noise correction can be selected by PBRDSW.

8.11.3 Cancellation of detection
Dot noise detection can be cancelled by PBC****.

8.12 Flash timing function

8.12.1 Registers for this function

0x29 FSSTBSW , FSSTBPOL , FSSTBPH
0x2A FSSTBW

8.12.2 Setting for FSSTB

FSSTB pulse can be output by FSSTBSW.
Polarity can be changed by FSSTBPOL.
Phase can be changed by FSSTBPH.
Width can be changed by FSSTBW.

This pulse can be used for recognition of the flash timing.

8.13 Test mode **<** Absolutely don't change these parameters in any situation. >

8.13.1 Registers for this function

0x01 VNUM
0x03 CM
0x21 HPPH
0x22 HPPH , VRRPH
0x23 HDSPPH
0x24 HDSPPH , VDSPPH
0x25 HAPRPH
0x26 HAPRPH
0x2B SCMD19-16
0x2C SCMD15-8
0x2D SCMD7-4 , SCMD2-0
0x2E TCSB1L , TCPEROSW , TCSBIN , TCRAM , TROM
0x2F TCRAMS , TSPCHK , TCPERAGC , TWBS , TWBG , TACDET
0x30 PCMODE , TGAMROM , TCSB
0x31 TALCDISP , TALCOSW , PBDISP , TDISP
0x3F AGMIN
0x40 LI1POL , CS1POL , LI3POL , CS3POL , DINCKSW
0x41 JAMP , JAMG
0x4F LI12POL , CS12POL
0x56 AWBCSPOL , WBDIVCLP , WBNOLJ , WBNOLJSC , WB2IM1
0x57 WBDIVSC

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PCK : Pixel clock (clock for sensor portion). This is half speed of output clock.