Universal Frequency Synthesizer

Product Description

MS5351/MS5351M is a universal frequency synthesizer chip that can be connected via I2C

Configuration, can generate any clock output from 2.5kHz to 200MHz.

Body, crystal oscillator, phase-locked loop, output buffer.

Main Features

ÿ 3-channel output, from 2.5kHz to 200MHz clock ÿ Output frequency

error 0ppm ÿ High resolution, low

output jitter ÿ Can work with 25MHz or

27MHz quartz crystal ÿ Output clock phase adjustable ÿ Output

delay adjustable ÿ Output clock rise/

fall time controllable

ÿ Frequency switching without glitch

ÿ Independent power supply pins

    Internal core circuit power supply VDD: 3.0V

   Output stage power supply VDDO: 1.8V or 2.5V or 3.3V

ÿ Internal high power supply rejection ratio

ÿ Compatible with HCSL and PCIE Gen 1

eMSOP10

MSOP10

application

ÿ HDTV, set-top box ÿ Printer,

scanner, projector ÿ Handheld device ÿ

Network/

communication ÿ

Server ÿ Quartz

crystal/crystal oscillator/phase-locked loop replacement

Product Specifications

product	Package	Silk screen name
MS5351	eMSOP10	MS5351
MS5351M	MSOP10	MS5351M
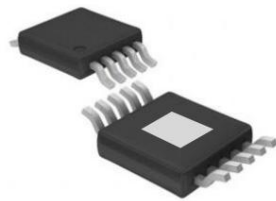
Pin diagram
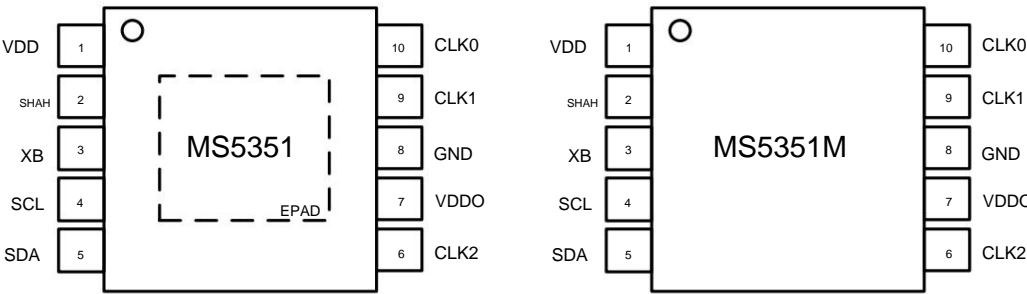
Pin Description

Pin number Pin name	Pin attribute		Pin Description
1	VDD	.	Internal core circuit power supply
2	SHAH	I External quartz crystal input	
3	XB	I External quartz crystal input	
4	SCL	.	I2C clock input, needs to be connected to at least 1kÿ pull-up resistor
5	SDA	I/O	I2C data input/output, need to connect at least 1kÿ pull-up resistor
6	CLK2	O Output clock	
7	VDDO	- Output stage power supply	
8	GND	- Reference ground	
9	CLK1	O Output clock	
10	CLK0	O Output clock	
.	EPAD	- Heat sink, grounding recommended	

Internal Block Diagram
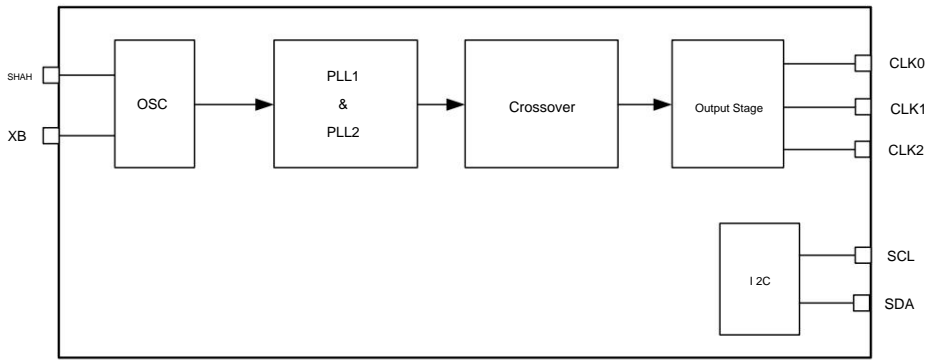
Limit parameters

When using the chip, any application method that exceeds the limit parameters will cause permanent damage to the device.

The state may affect the reliability of the device. The limit parameters are only obtained by a series of extreme tests and do not mean that the chip can work normally under

Under this limit condition.

parameter	Symbol	Test Conditions	Parameter range	unit
DC supply voltage	VDD		-0.5 ÿ 3.6	V
Output stage supply voltage	VDDO		-0.5 ÿ 3.8	V
Input voltage	VIN_SCL	SCL,SDA pin	-0.5 ÿ 3.8	V
	VIN_XA/XB	XA,XB pins	-0.5 ÿ 1.3	V
Junction temperature	TJ		-55 ÿ 150	°C
Soldering temperature (lead-free)	TPEAK		260	°C
Duration of soldering at TPEAK temperature (lead-free) tP			10	s
Storage temperature	TSTG		-65 ÿ 150	°C

Recommended operating conditions

parameter	symbol	Minimum	typical	Maximum Unit	
Operating temperature	FACING	-20	25	85	°C
Core circuit voltage	VDD	2.7	3.0	3.3	V
Output stage voltage	VDDO	1.71	1.8	1.89	V
		2.25	2.5	2.75	V
		3.0	3.3	3.6	V

Electrical parameters

Unless otherwise specified, VDD=VDDO=3.0V±10%, TA=-20°Cÿ85°C.

parameter	symbol	Test conditions	Min Typ Max Unit			
DC Characteristics						
VDD Current	IDD	3-channel output		31		mA
Single channel output stage current	DDOx	CL=5pF, less than 100MHz\n\nMaximum driving capability		5		mA
Input Current	ISCL	SCL,SDA			10	ÿA
Output Impedance	LIKE THIS	3.3V VDDO, high drive		50		Oh
AC Characteristics						
Power-on time	tRDY	From VDDmin to valid output clock,\n\nfCLKn>1MHz		2	10	ms
When PLL is bypassed\n\nPower-on time	tBYP	From VDDmin to valid output clock,\n\nfCLKn>1MHz		0.5	1	ms
Output frequency switching time tFREQ		fCLKn>1MHz			20	ÿs
Output Phase Deviation	PSTEP			333		ps/step
Spread spectrum range	SSDEV	Down spread, 0.1% per step	-0.1		-2.5	%
		Center spread spectrum, 0.1% per step	±0.1		±2.5	%
Spread spectrum modulation rate	SSMOD		30	31.5	33	kHz
Crystal Oscillator Specifications						
Quartz crystal frequency	fXTAL		25		27	MHz
Load Capacitance	CXL		6		12	pF
Equivalent series resistance	RESR				150	Oh
Maximum drive level	dL		100			ÿW
Input voltage	VIN_XA/AB XA and XB pins		-0.3		1.1	V
Output Clock Specifications						
Output frequency	fCLK		0.0025		200	MHz
Load Capacitance	CL				15	pF
Duty Cycle	DC	fCLK<160MHz	45	50	55	%
		fCLK<160MHz	40	50	60	%
Rise time	tR	20%ÿ80%, CL=5pF maximum drive		0.5	1.2	ns
Fall time	tF	20%ÿ80%, CL=5pF maximum drive		0.5	1.2	ns

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parameter	symbol	Test conditions	Min Typ Max Unit			
Output high level voltage	VOH	CL=5pF	VDDO-0.6			V
Output low level voltage	VOL	CL=5pF			0.6	V
Period Jitter	JPER	3 channels simultaneous output		60	180	ps,pk
Adjacent clock jitter	JCC	3 channels simultaneous output		60	180	ps,pk

I2C Specifications (SCL , **SDA)**

parameter	Symbol Test Conditions		Standard mode 100kbps Fast mode 400kbps				unit
			Min Max	Min Max			
Input low level voltage VILI2C			-0.5	0.3×VDDI2C	-0.5	0.3×VDDI2C V	
Input high level voltage VIHI2C			0.7×VDDI2C	3.6	0.7×VDDI2C	3.6	V
Schmitt hysteresis voltage VHYS					0.1		V
Output low level voltage VOLI2C	VOLI2C=2.5/3.3Vÿ Open drain, 3mA current sink		0	0.4	0	0.4	V
Input Current	III2C		-10	10	-10	10	ÿA
Pin capacitance	CI2C VIN=-0.1ÿVDDI2C			4		4	pF
I2C bus pause time tTO pause enable			25	35	25	35	ms

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Typical application diagram

Title

MS53

Size A4
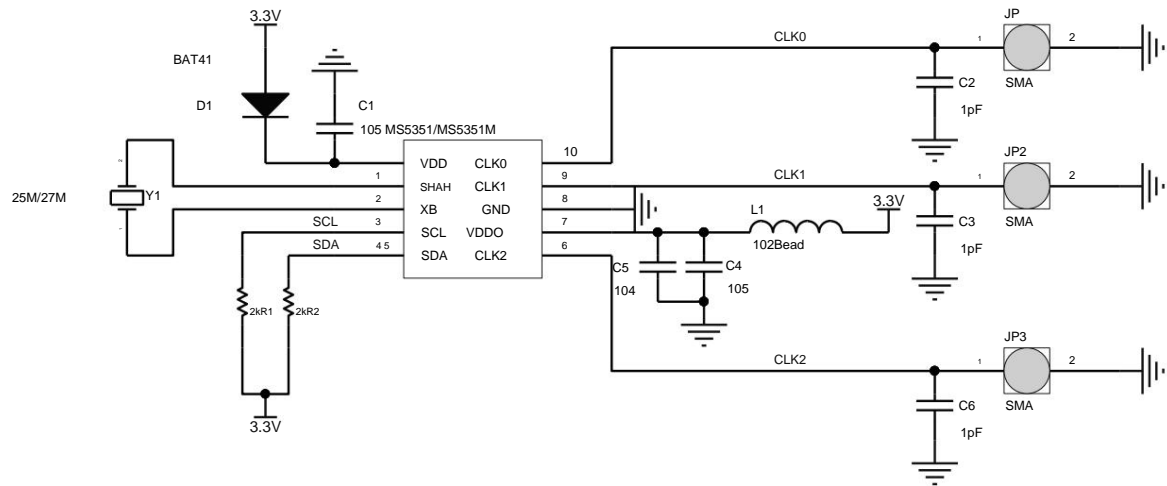
Number

Date: 2023/9/20 D:

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Package outline drawing

eMSOP10

BOTTOM VIEW

EXPOSDE THERMAL PAD ZONE

SECTION B-B

BASE METAL

WITH PLATING
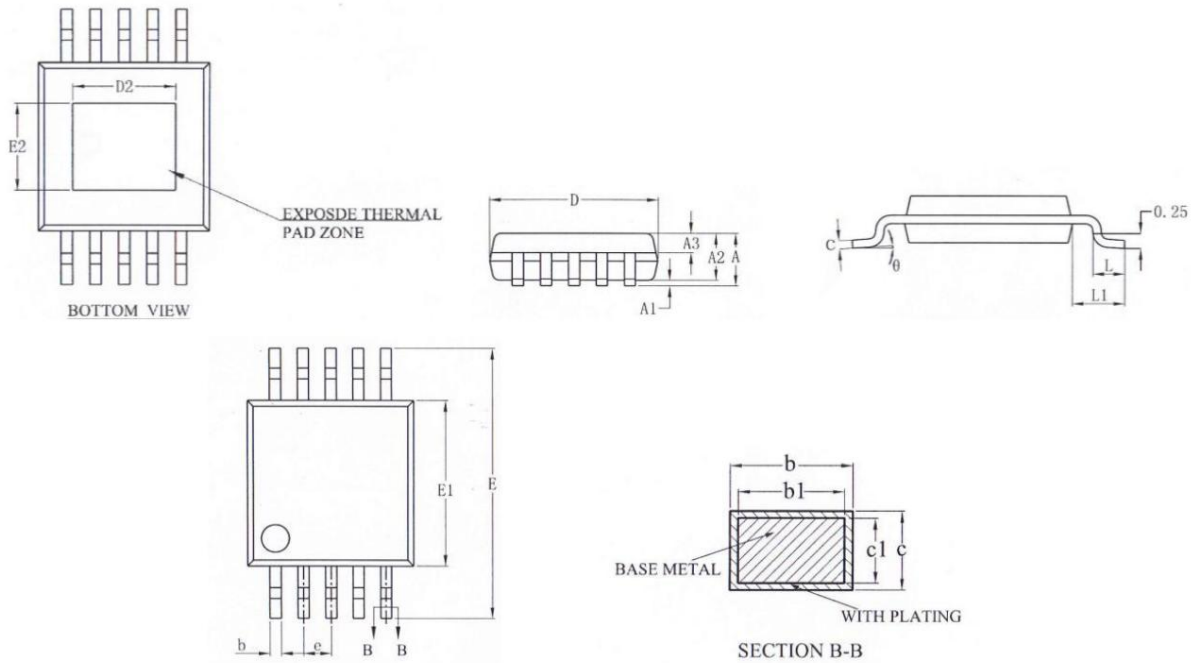
symbol	Dimensions (mm)		
	Minimum	typical	maximum
A	.	.	1.10
A1	0.05	.	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18	.	0.26
b1	0.17	0.20	0.23
c	0.15	.	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
D2	1.80 REF		
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
E2	1.55 REF		
e	0.50 BSC		
L	0.40	.	0.70
L1	0.95 REF		
i	0	.	8°
L/F (mil)	71×71		

Version number: V1.4   2023.11.24

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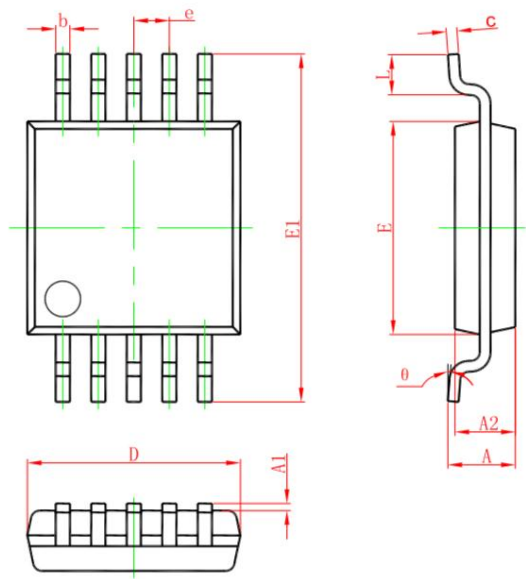
symbol	Dimensions (mm)		Dimensions (inches)	
	Minimum	maximum	Minimum	maximum
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
and	0.50 BSC		0.020 BSC	
AND	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
i	0^{the}	6^{the}	0^{the}	6^{the}

Seal and packaging specifications

1. Introduction to the content of the seal

| MS5351 XXXXXX ◯ | MS5351M XXXXXX ◯ |

Product model: MS5351, MS5351M

Production batch number: XXXXXX

2. Seal Standard Requirements

Laser printed, centered throughout and in Arial font.

3. Packaging Specifications

model	Packaging type: only/reel		Roll/Box	Piece/box	Box/Carton	Piece/box
MS5351	eMSOP10	3000	1	3000	8	24000
MS5351M	MSOP10	3000	1	3000	8	24000

statement

ÿ Ruimeng reserves the right to change the instructions without prior notice! Customers should obtain the latest version of the information and verify the relevant information before placing an order.

Is it complete?

ÿ When using Ruimeng products for system design and whole machine manufacturing, the buyer is responsible for complying with safety standards and taking corresponding safety measures.

To avoid personal injury or property loss caused by potential failure risks!

ÿThere is no end to product improvement, our company will wholeheartedly provide customers with better products!

MOS circuit operation precautions

Static electricity can be generated in many places. Taking the following precautions can effectively prevent MOS circuits from being

Damage caused by electrostatic discharge:

1. Operators must be grounded using an anti-static wrist strap.

2. The equipment casing must be grounded.

3. Tools used during the assembly process must be grounded.

4. Conductive packaging or antistatic materials must be used for packaging or transportation.

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