I2C Programmable Arbitrary Frequency **CMOS** Clock Generator

Product Description

The MS5351M is an I2C configurable, 3-channel output clock generator chip that can completely replace crystals, crystal oscillators, phase-locked loops, and output buffers used in cost-sensitive applications. Thanks to the use of fractional-frequency phase-locked loops + high-precision fractional divider structures, the MS5351M can generate any clock output from 2.5kHz to 200MHz.

Main features

ÿ 3-channel output from 2.5kHz to 200MHz non-integer related clocks ÿ

I2C user-defined configuration output

clock ÿ Accurate frequency

synthesis ÿ Low

output jitter ÿ Can work with low-cost, fixed-frequency quartz crystals: 25MHz or

27MHz ÿ Output clock supports static phase

offset ÿ Programmable control of output clock rise/

fall time ÿ Glitch-free

frequency switching ÿ Independent power supply pins

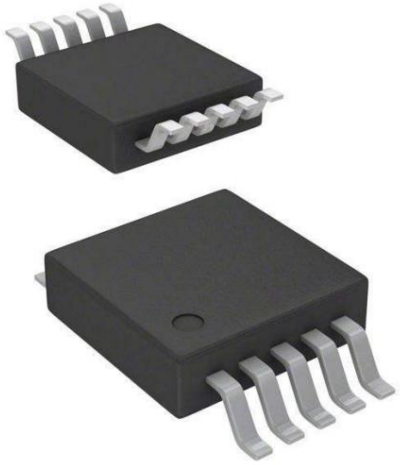
Internal core circuit power supply VDD: 2.5V or 3.3V Output

stage power supply VDDO: 1.8V or 2.5V or 3.3V

ÿ Internal high power supply rejection ratio can save external filter

capacitors ÿ Adjustable

output delay ÿ Compatible with HCSL and PCIE Gen 1



MSOP10 package

Applications

Applications ÿ HDTV, DVD/Blu-ray, set-top boxes ÿ Audio/

video equipment, game consoles ÿ

Printers, scanners, projectors ÿ Handheld

devices ÿ Home

gateway equipment ÿ

Network/

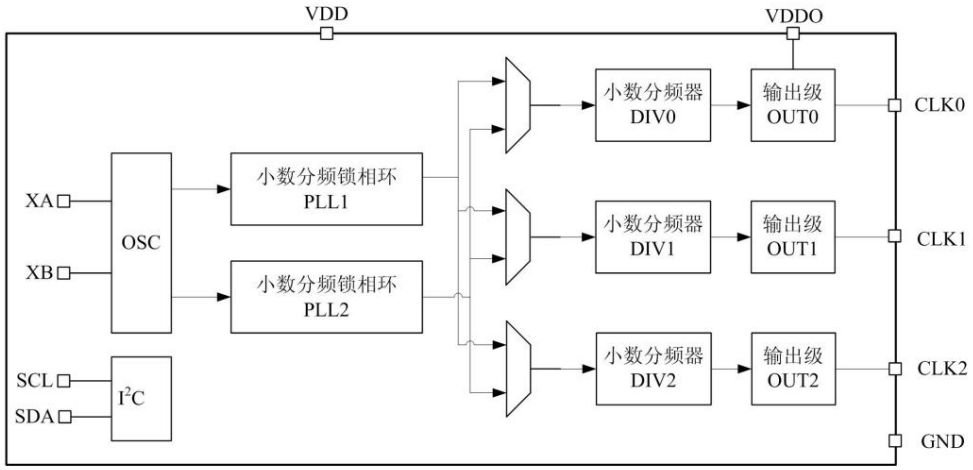
communication ÿ Servers,

storage ÿ Quartz crystal/crystal oscillator/phase-locked loop replacement

Product Specifications

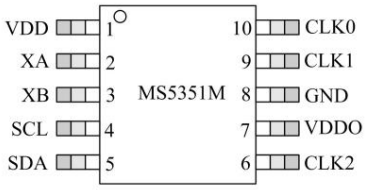
product	Package	Silk screen name
MS5351M	MSOP10	MS5351M

Internal Block Diagram



Pin Arrangement

MS5351M adopts MSOP10 package, and the pin arrangement is as follows:



Pin Description

Pin Number	Pin Name	Pin Properties	Pin Description
1	VDD	Power	Internal core circuit power supply
2	SHAH	enter	External quartz crystal input
3	XB	enter	External quartz crystal input
4	SCL	enter	I2C clock input, must be connected to at least 1kÿ pull-up resistor
5	SDA	Input/output I2C data input/output, must connect at least 1kÿ pull-up resistor	
6	CLK2	Output	Output Clock
7	VDDO	power supply	Output stage power supply
8	GND	land	Reference location
9	CLK1	Output	Output Clock
10	CLK0	Output	Output Clock

Limit parameters

Absolute Maximum Ratings

Note: In actual application, it is not allowed to exceed the rated value range*1

Parameters	symbol	condition	Rating unit	
DC supply voltage	VDD		-0.5 to 3.8	V
Output stage supply voltage	VDDO		-0.5 to 3.8	V
Input voltage	VIN_SCL	SCL,SDA pins -0.5 to 3.8		V
	VIN_XA/XB	XA, XB pins - 0.5 to 1.3		V
Junction	TJ		-55 to 150 °C	
temperature Soldering iron temperature	TPEAK		260	ÿ
(lead-free)*2 Duration of soldering iron temperature at TPEAK (lead-free)*2	TP		10	Second

*1 Exceeding the absolute maximum rating may cause permanent damage to the chip

*2 The chip complies with JEDEC J-STD-020 specification

Recommended operating conditions

	symbol	Minimum	standard	maximum	unit
Parameters	FACING	-40	25	105	ÿ
Operating Temperature Core Circuit Voltage VDD		3.0	3.3	3.6	V
		2.25	2.5	2.75	V
Output stage voltage VDDO		1.71	1.8	1.89	V
		2.25	2.5	2.75	V
		3.0	3.3	3.6	V

Electrical parameters

(Unless otherwise specified, VDD=VDDO=3.3V±10%, VA=-40ÿ~105ÿ)

parameter	symbol	Test conditions	Min Typ Max Unit			
DC Characteristics						
VDD Current	IDD	3 channel output,		33		mA
Single Channel Output Stage Current	IDDOx	CL=5pF, less than 100MHz Maximum driving capability		5		mA
Input current	ISCL	SCL,SDA			10	uA
output impedance	LIKE THIS	3.3V VDDO, high drive		50		Oh
AC Characteristics						
Power-on time	TRDY from VDDmin to valid output	Clock, fCLKn>1MHz		2	10	ms
Powering up with PLL bypassed time	TBYP from VDDmin to valid output	Clock, fCLKn>1MHz		0.5	1	ms
Output frequency switching time	TFREQ	fCLKn>1MHz			20	us
Output phase shift PSTEP				333		ps/step
Spread spectrum range	SSDEV down spread spectrum, 0.1% per step		-0.1		-2.5	%
		Center spread spectrum, 0.1% per step	±0.1		±2.5	%
Spread spectrum modulation rate SSMOD			30	31.5	33	kHz
Crystal Oscillator Specifications						
Quartz crystal frequency fXTAL			25		27	MHz
Load Capacitance	CXL		6		12	pF
Equivalent series resistance rESR					150	Oh
Maximum drive level dL			100			your
Input voltage VIN_XA/AB output clock specifications		XA and XB pins	-0.3		1.1	V
Output frequency*1	FCLK		0.0025		200	MHz
load capacitance	CL				15	pF
duty cycle	DC	FCLK<160MHz	45	50	55	%
		FCLK<160MHz	40	50	60	%
Rise time	tr	20%~80%, CL=5pF maximum drive move		0.5	1.2	ns
Fall time	tf	20%~80%, CL=5pF maximum drive move		0.5	1.2	ns
Output high level VOH Output low level		CL=5pF	VDD-0.6			
VOL		CL=5pF 3			0.6	
Period jitter JPER *2,3 Adjacent clock		channels output simultaneously		60	180	ps,pk
jitter JCC *2,3		3 channels output simultaneously		60	180	ps,pk

I2C Specifications (SCL, SDA)

Parameter symbol test condition			Standard mode 100kbps Min.		Fast Mode 400kbps Unit		
			Max.		Minimum	Maximum V	
Low level input Voltage	VILI2C		-0.5	0.3*VDDI2C	-0.5	0.3*VDDI2C	V
High level input Voltage	VIHI2C		0.7*VDDI2C	3.6	0.7*VDDI2C	3.6	V
Schmidt Hysteresis Voltage	VHYS		·	·	0.1	·	V
Low level output Voltage*4	LOVE2C	VOLI2C=2.5/3.3V, open drain, 3mA Current Sink	0	0.4	0	0.4	V
Input current III2C pin			-10	10	-10	10	uA
capacitance CI2C		VIN = -0.1 to VDDI2C	·	4	·	4	pF
I2C Bus Suspend time	TTO pause enable		25	35	25	35	ms

*1. Clocks greater than 112.5MHz are only allowed to output 2 at the same time

*2. Clock jitter test 10000 cycles, and measured at maximum output drive capability

*3. Jitter is highly dependent on frequency configuration

*4. I2C only supports 2.25V to 3.6V power supply

register

1.1 Register Summary Table

Register D7		D6	D5	D4	D3	D2	D1	D0
0	SYS_INIT	LOL_2	LOL_1	Reserved				
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	Reserved					OUT2_AND	OUT1_AND	OUT0_AND
4-8	Reserved							
9	0	0	0	0	0	0	0	0
10-14	Reserved							
15	0	0	0	0	0	0	0	0
16	DIV0_PDN	DIV0_INT	DIV0_SRC	OUT0_INV		OUT0_SRC[1:0]		OUT0_IDRV[1:0]
17	DIV1_PDN	DIV1_INT	DIV1_SRC	OUT1_INV		OUT1_SRC[1:0]		OUT1_IDRV[1:0]
18	DIV2_PDN	DIV2_INT	DIV2_SRC	OUT2_INV		OUT2_SRC[1:0]		OUT2_IDRV[1:0]
19-23	Reserved							
24			OUT2_DIS_STATE		OUT1_DIS_STATE		OUT0_DIS_STATE	
25	Reserved							
26	PLL1_P3[15:8]							
27	PLL1_P3[7:0]							
28	Unused				Reserved		PLL1_P1[17:16]	
29	PLL1_P1[15:8]							
30	PLL1_P1[7:0]							
31	PLL1_P3[19:16]				PLL1_P2[19:16]			
32	PLL1_P2[15:8]							
33	PLL1_P2[7:0]							
34	PLL2_P3[15:8]							
35	PLL2_P3[7:0]							
36	Unused				Reserved		PLL2_P1[17:16]	
37	PLL2_P1[15:8]							
38	PLL2_P1[7:0]							
39	PLL2_P3[19:16]				PLL2_P2[19:16]			
40	PLL2_P2[15:8]							
41	PLL2_P2[7:0]							
42	DIV0_P3[15:8]							
43	DIV0_P3[7:0]							
44	Reserved	OUT0_DIV[2:0]			DIV0_DIVBY4[1:0]		DIV0_P1[17:16]	
45	DIV0_P1[15:8]							
46	DIV0_P1[7:0]							
47	DIV0_P3[19:16]				DIV0_P2[19:16]			
48	DIV0_P2[15:8]							

49	DIV0_P2[7:0]			
50	DIV1_P3[15:8]			
51	DIV1_P3[7:0]			
52	Reserved	OUT1_DIV[2:0]	DIV1_DIVBY4[1:0]	DIV1_P1[17:16]
53	DIV1_P1[15:8]			
54	DIV1_P1[7:0]			
55	DIV1_P3[19:16]		DIV1_P2[19:16]	
56	DIV1_P2[15:8]			
57	DIV1_P2[7:0]			
58	DIV2_P3[15:8]			
59	DIV2_P3[7:0]			
60	Reserved	OUT2_DIV[2:0]	DIV2_DIVBY4[1:0]	DIV2_P1[17:16]
61	DIV2_P1[15:8]			
62	DIV2_P1[7:0]			
63	DIV2_P3[19:16]		DIV2_P2[19:16]	
64	DIV2_P2[15:8]			
65	DIV2_P2[7:0]			
66-92	Reserved			
149	SSC_EN	SSDN_P2[14:8]		
150	SSDN_P2[7:0]			
151	SSC_MODE	SSDN_P3[14:8]		
152	SSDN_P3[7:0]			
153	SSDN_P1[7:0]			
154	SSUDP[11:8]		SSDN_P1[11:8]	
155	SSUDP [7:0]			
156	SSUP_P2[14:8]			
157	SSUP_P2[7:0]			
158	SSUP_P3[14:8]			
159	SSUP_P3 [7:0]			
160	SSUP_P1 [7:0]			
161	SS_NOUT[3:0]		SSUP_P1[11:8]	
162	Reserved			
163	Reserved			
164	Reserved			
165	Reserved	OUT0_PHOFF[6:0]		
166	Reserved	OUT1_PHOFF[6:0]		
167	Reserved	OUT2_PHOFF[6:0]		
168	Reserved			
169	Reserved			
170	Reserved			

171-176	Reserved				
177	PLL2_RST Reserved		PLL1_RST		Reserved
178-182	Reserved				
183	XTAL_CL		Reserved		
184-186	Reserved				
187	Reserved XO_	FAN-OUT_EN	Reserved MS_	FAN-OUT_EN	Reserved
188-255	Reserved				

1.2 Register Detailed Description

Register 0. Chip status

Bit D7		D6	D5	D4	D3	D2	D1	D0
Name SYS_INIT Type		LOL_2	LOL_1					
	Read-only							

Bit	Name	Function
7	The device cannot work before SYS_INIT initialization is completed. It is not recommended to read and write registers through I2C before initialization is completed.	0: System initialization completed 1: The device is in system initialization mode
6	LOL_2 When the reference clock of the PLL exceeds its allowed input range, a loss of lock will occur.	0: PLL2 locked 1: PLL2 lost lock
5	LOL_1 When the reference clock of the PLL exceeds its allowed input range, a loss of lock will occur.	0: PLL1 locked 1: PLL1 lost lock
4:0	Reserved	

Register 3. Output stage enable control

Bit D7	Name	D6	D5	D4	D3	D2	D1	D0
Type						OUT2_EN	OUT1_EN	OUT0_EN
	Read/Write							

Bit	Name	Function
7:3	Reserved	reserve
2:0	OUTn_EN (n=0,1,2)	n=0,1,2 0: OUTn (n=0,1,2) output enable 1: OUTn (n=0,1,2) output disabled

Register 16. OUT0 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV0_PDN	DIV0_INT	DIV0_SRC	OUT0_INV	Type	Read/Write	OUT0_SRC[1:0]	OUT0_IDRV[1:0]

Bit	name	Function
7	DIV0_PDN	Controls the opening or closing of DIV0 0: DIV0 output is on 1: DIV0 output is off
6	DIV0_INT	This bit can control the DIV0 division mode 0: DIV0 works in decimal mode 1: DIV0 works in integer mode
5	DIV0_SRC	Select DIV0 input 0: Select PLL1 as the input of DIV0 1: Select PLL2 as the input of DIV0
4	OUT0_INV	Controls whether the output clock CLK0 is inverted 0: CLK0 is not inverted 1: CLK0 is inverted
3:2	OUT0_SRC[1:0] These two bits	determine the input of OUT0 00: Select crystal oscillator as the input of OUT0 01: Reserved 10: Reserve 11: Select DIV0 as the input of OUT0
1:0	OUT0_IDRV[1:0]	OUT0 output drive capability 00:3mA 01:6mA 10:9mA 11:12mA

Register 17. OUT1 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
NameDIV1_	PDN DIV1_INT Type		DIV1_SRC OUT1_	INV Read/write	OUT1_SRC[1:0]		OUT1_IDRV[1:0]	

Bit Name		Function
7	DIV1_PDN	Controls the opening or closing of the DIV1 output terminal 0: DIV1 output is on 1: DIV1 output is off
6	DIV1_INT	This bit can control the DIV1 frequency division mode 0: DIV1 works in decimal mode 1: DIV1 works in integer mode
5	DIV1_SRC	Select DIV1 input 0: Select PLL1 as the input of DIV1 1: Select PLL2 as the input of DIV1
4	OUT1_INV	Controls whether the output clock CLK1 is inverted 0: CLK1 is not inverted 1: CLK1 is inverted

3:2	OUT1_SRC[1:0] These two bits determine the input of OUT1	00: Select crystal oscillator as the input of OUT1 01: Reserved 10: Select DIV0 as the input of OUT1 11: Select DIV1 as the input of OUT1
1:0	OUT1_IDRV[1:0]	OUT1 output drive capability 00:3mA 01:6mA 10:9mA 11:12mA

Register 18. OUT2 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV2_PDN	DIV2_INT		DIV2_SRC	OUT2_INV	Type	Read/	OUT2_SRC[1:0] OUT2_IDRV[1:0]
Write					Read/write			

Bit Name		Function
7	DIV2_PDN	Control DIV2 open or closed 0: DIV2 open 1: DIV2 is closed
6	DIV2_INT	This bit can control the DIV2 division mode 0: DIV2 works in decimal mode 1: DIV2 works in integer mode
5	DIV2_SRC	Select DIV2 input 0: Select PLL1 as the input of DIV2 1: Select PLL2 as the input of DIV2
4	OUT2_INV	Controls whether the output clock CLK2 is inverted 0: CLK2 is not inverted 1: CLK2 is inverted
3:2	OUT2_SRC[1:0] These two bits determine the input of OUT2	00: Select crystal oscillator as the input of OUT2 01: Reserved 10: Select DIV0 as the input of OUT2 11: Select DIV2 as the input of OUT2
1:0	OUT2_IDRV[1:0]	OUT2 output drive capability 00:3mA 01:6mA 10:9mA 11:12mA

Register 24. OUT2~OUT0 status when no output

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		OUT2_DIS_STATE		OUT1_DIS_STATE		OUT0_DIS_STATE	
type	Read/Write							

Bit	name	Function
7:6	Reserved	reserve
5:0	OUTn_DIS_STATE (n=0,1,2)	n=0,1,2 Two bits determine the state of OUTn (n=0,1,2) when it is not output 00: OUTn (n=0,1,2) is 0 when no output is given 01: OUTn (n=0,1,2) is 1 when no output is given 10: OUTn (n=0,1,2) is high impedance when not outputting 11: OUTn (n=0,1,2) output is allowed

Register 26. PLL1 Parameters

Bit D7 Name	D6	D5	D4	D3	D2	D1	D0
PLL1_P3[15:8]							
type	Read/Write						

Bit	name	Function
7:0	PLL1_P3[15:8]	PLL1 parameter P3, which is the denominator of the internal fractional division of PLL1, has 20 bits in total.

Register 27. PLL1 Parameters

Bit D7 Name Type	D6	D5	D4	D3	D2	D1	D0
PLL1_P3[7:0]							
Read/Write							

Bit	name	Function
7:0	PLL1_P3[7:0]	PLL1 parameter P3, which is the denominator of the internal fractional division of PLL1, has 20 bits in total.

Register 28. PLL1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Unused				Reserved		PLL1_P1[17:16]	
type	Read/Write							

Bit	name	Function
7:4	Unused	Useless
3:2	Reserved	reserve
1:0	PLL1_P1[17:16]	PLL1 parameter P1, which is the integer frequency division part of the internal frequency divider of PLL1, a total of 18 bits.

Register 29. PLL1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL1_P1[15:8]							
type	Read/Write							

Bit	name	Function
7:0	PLL1_P1[15:8]	PLL1 parameter P1, which is the integer frequency division part of the internal frequency divider of PLL1, a total of 18 bits.

Register 30. PLL1 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL1_P1[7:0]							
type	Read/Write							

Bit	name	Function
7:0	PLL1_P1[7:0]	PLL1 parameter P1, which is the integer frequency division part of the internal frequency divider of PLL1, a total of 18 bits.

Register 31. PLL1 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL1_P3[19:16]				PLL1_P2[19:16]			
type	Read/Write							

Bit	name	Function
7:4	PLL1_P3[19:16]	PLL1 parameter P3, which is the denominator of the internal fractional division of PLL1, has 20 bits in total.
3:0	PLL1_P2[19:16]	PLL1 parameter P2, which is the numerator of the internal fractional division of PLL1, has a total of 20 bits.

Register 32. PLL1 parameters

Bit D7 Name Type	D6	D5	D4	D3	D2	D1	D0
PLL1_P2[15:8]							
Read/Write							

Bit	name	Function
7:0	PLL1_P2[15:8]	PLL1 parameter P2, which is the numerator of the internal fractional division of PLL1, has a total of 20 bits.

Register 33. PLL1 parameters

Bit D7 Name Type	D6	D5	D4	D3	D2	D1	D0
PLL1_P2[7:0]							
Read/Write							

Bit	name	Function
7:0	PLL1_P2[7:0]	PLL1 parameter P2, which is the numerator of PLL1 internal fractional division, has 20 bits in total.

Register 34. PLL2 Parameters

Bit D7 Name	D6	D5	D4	D3	D2	D1	D0
PLL2_P3[15:8]							
type	Read/Write						

Bit	name	Function
7:0	PLL2_P3[15:8]	PLL2 parameter P3, which is the denominator of the internal fractional division of PLL2, has 20 bits in total.

Register 35. PLL2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL2_P3[7:0]							
type	Read/Write							

Bit	name	Function
7:0	PLL2_P3[7:0]	PLL2 parameter P3, which is the denominator of the internal fractional division of PLL2, has 20 bits in total.

Register 36. PLL2 Parameters

Bit D7 Name	D6	D5	D4	D3	D2	D1	D0
Unused				Reserved		PLL2_P1[17:16]	
type	Read/Write						

Bit	name	Function
7:4	Unused	Useless
3:2	Reserved	reserve
1:0	PLL2_P1[17:16]	PLL2 parameter P3, which is the integer frequency division part of the internal frequency divider of PLL2, has 18 bits in total.

Register 37. PLL2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL2_P1[15:8]							
type	Read/Write							

Bit	name	Function
7:0	PLL2_P1[15:8]	PLL2 parameter P1, which is the integer frequency division part of the internal frequency divider of PLL2, a total of 18 bits.

Register 38. PLL2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL2_P1[7:0]							
type	Read/Write							

Bit	name	Function
7:0	PLL2_P1[7:0]	PLL2 parameter P1, which is the integer frequency division part of the internal frequency divider of PLL2, a total of 18 bits.

Register 39. PLL2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL2_P3[19:16]				PLL2_P2[19:16]			
type	Read/Write							

Bit	name	Function
7:4	PLL2_P3[19:16]	PLL2 parameter P3, which is the denominator of the internal fractional division of PLL2, has 20 bits in total.
3:0	PLL2_P2[19:16]	PLL2 parameter P2, which is the numerator of the internal fractional division of PLL2, has 20 bits in total.

Register 40. PLL2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL2_P2[15:8]							
Type	Read/Write							

Bit	name	Function
7:0	PLL2_P2[15:8]	PLL2 parameter P2, which is the numerator of the internal fractional division of PLL2, has 20 bits in total.

Register 41. PLL2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL2_P2[7:0]							
Type	Read/Write							

Bit	name	Function
7:0	PLL2_P2[7:0]	PLL2 parameter P2, which is the numerator of the internal fractional division of PLL2, has 20 bits in total.

Register 42. DIV0 Parameters

Bit D7 Name Type	D6	D5	D4	D3	D2	D1	D0
DIV0_P3[7:0]							
Read/Write							

Bit	name	Function
7:0	DIV0_P3[15:8]	DIV0 parameter P3, which is the denominator of DIV0 fractional division, has 20 digits in total.

Register 43. DIV0 Parameters

Bit D7 Name	D6	D5	D4	D3	D2	D1	D0
DIV0_P3[7:0]							
type	Read/Write						

Bit	name	Function
7:0	DIV0_P3[7:0]	DIV0 parameter P3, which is the denominator of DIV0 fractional division, has 20 digits in total.

Register 44. DIV0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		OUT0_DIV[2:0]			DIV0_DIVBY4[1:0]		DIV0_P1[17:16]	
type	Read/Write							

Bit	name	Function
7	Reserved	reserve
6:4	OUT0_DIV[2:0] Output stage division ratio	000: 1 frequency division, 100: 16 frequency division 001: 2-way, 101: 32-way 010: 4-way, 110: 64-way 011: 8-way, 111: 128-way
3:2	DIV0_DIVBY4[1:0]	DIV0 4-division enable 11: 4-frequency division is valid; 00: other frequency divisions
1:0	DIV0_P1[17:16]	DIV0 parameter P1, which is the integer division part of the divider DIV0, a total of 18 bits.

Register 45. DIV0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV0_P1[15:8]							
Type	Read/Write							

Bit	name	Function
7:0	DIV0_P115:8]	DIV0 parameter P1, which is the integer division part of the divider DIV0, a total of 18 bits.

Register 46. DIV0 Parameters

Bit D7 Name Type	D6	D5	D4	D3	D2	D1	D0
DIV0_P1[7:0]							
Read/Write							

Bit	name	Function
7:0	DIV0_P1[7:0]	DIV0 parameter P1, which is the integer division part of the divider DIV0, a total of 18 bits.

Register 47. DIV0 Parameters

Bit D7 Name	D6	D5	D4	D3	D2	D1	D0
DIV0_P3[19:16]				DIV0_P2[19:16]			
type	Read/Write						

Bit	name	Function
7:4	DIV0_P3[19:16]	DIV0 parameter P3, which is the denominator of DIV0 fractional division, has 20 digits in total.
3:0	DIV0_P2[19:16]	DIV0 parameter P2, which is the numerator of DIV0 fractional division, has 20 bits in total.

Register 48. DIV0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV0_P2[15:8]							
Type	Read/Write							

Bit	name	Function
7:0	DIV0_P2[15:8]	DIV0 parameter P2, which is the numerator of DIV0 fractional division, has 20 bits in total.

Register 49. DIV0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV0_P2[7:0]							
Type	Read/Write							

bit	name	Function
7:0	DIV0_P2[7:0]	DIV0 parameter P2, which is the numerator of DIV0 fractional division, has 20 bits in total.

Register 50. DIV1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV1_P3[15:8]							
type	Read/Write							

Bit	name	Function
7:0	DIV1_P3[15:8]	DIV1 parameter P3, which is the denominator of DIV1 fractional division, has 20 digits in total.

Register 51. DIV1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV1_P3[7:0]							
type	Read/Write							

Bit	name	Function
7:0	DIV1_P3[7:0]	DIV1 parameter P3, which is the denominator of DIV1 fractional division, has 20 digits in total.

Register 52. DIV1 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
NameReserved		OUT1_DIV[2:0]			DIV1_DIVBY4[1:0]		DIV1_P1[17:16]	
type	Read/Write							

Bit	name	Function
7:4	OUT1_DIV[2:0] Output stage division ratio	000: 1 frequency division, 100: 16 frequency division 001: 2-way, 101: 32-way 010: 4-way, 110: 64-way 011: 8-way, 111: 128-way
3:2	DIV1_DIVBY4[1:0]	DIV1 4-division enable 11: 4 frequency division is effective 00: Other frequency divisions
1:0	DIV1_P1[17:16]	DIV1 parameter P1, which is the integer division part of the divider DIV1, a total of 18 bits.

Register 53. DIV1 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV1_P1[15:8]							
type	Read/Write							

Bit	name	Function
7:0	DIV1_P1[15:8]	DIV1 parameter P1, which is the integer division part of the divider DIV1, a total of 18 bits.

Register 54. DIV1 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV1_P1[7:0]							
type	Read/Write							

Bit	name	Function
7:0	DIV1_P1[7:0]	DIV1 parameter P1, which is the integer division part of the divider DIV1, a total of 18 bits.

Register 55. DIV1 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV1_P3[19:16]				DIV1_P2[19:16]			
type	Read/Write							

Bit	name	Function
7:4	DIV1_P3[19:16]	DIV1 parameter P3, which is the denominator of DIV1 fractional division, has 20 digits in total.
3:0	DIV1_P2[19:16]	DIV1 parameter P2, which is the numerator of DIV1 fractional division, has 20 digits in total.

Register 56. DIV1 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV1_P2[15:8]							
type	Read/Write							

Bit	name	Function
7:0	DIV1_P2[15:8]	DIV1 parameter P2, which is the numerator of DIV1 fractional division, has 20 digits in total.

Register 57. DIV1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV1_P2[7:0]							
type	Read/Write							

Bit	name	Function
7:0	DIV1_P2[7:0]	DIV1 parameter P2, which is the numerator of DIV1 fractional division, has 20 digits in total.

Register 58. DIV2 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV2_P3[15:8]							
type	Read/Write							

Bit	name	Function
7:0	DIV2_P3[15:8]	DIV2 parameter P3, which is the denominator of DIV2 fractional division, has 20 digits in total.

Register 59. DIV2 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV2_P3[7:0]							
type	Read/Write							

Bit	name	Function
7:0	DIV2_P3[7:0]	DIV2 parameter P3, which is the denominator of DIV2 fractional division, has 20 digits in total.

Register 60. DIV2 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
NameReserved		OUT2_DIV[2:0]			DIV2_DIVBY4[1:0]		DIV2_P1[17:16]	
type	Read/Write							

Bit	name	Function
7:4	OUT2_DIV[2:0] Output stage division ratio	000: 1-way, 100: 16-way 001: 2-way, 101: 32-way 010: 4-way, 110: 64-way 011: 8-way, 111: 128-way
3:2	DIV2_DIVBY4[1:0]	DIV2 4-division enable 11: 4 frequency division is effective 00: Other frequency divisions
1:0	DIV2_P1[17:16]	DIV2 parameter P1, which is the integer division part of the divider DIV2, a total of 18 bits.

Register 61. DIV2 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV2_P1[15:8]							
type	Read/Write							

Bit	name	Function
7:0	DIV2_P1[15:8]	DIV2 parameter P1, which is the integer division part of the divider DIV2, a total of 18 bits.

Register 62. DIV2 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV2_P1[7:0]							
Type	Read/Write							

Bit	name	Function
7:0	DIV2_P1[7:0]	DIV2 parameter P1, which is the integer division part of the divider DIV2, a total of 18 bits.

Register 63. DIV2 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV2_P3[19:16]				DIV2_P2[19:16]			
type	Read/Write							

Bit	name	Function
7:4	DIV2_P3[19:16]	DIV2 parameter P3, which is the denominator of DIV2 fractional division, has 20 digits in total.
3:0	DIV2_P2[19:16]	DIV2 parameter P2, which is the numerator of DIV2 fractional division, has 20 digits in total.

Register 64. DIV2 parameters

Bit D7 Name		D6	D5	D4	D3	D2	D1	D0
	DIV2_P2[15:8]							
type	Read/Write							

Bit	name	Function
7:0	DIV2_P2[15:8]	DIV2 parameter P2, which is the numerator of DIV2 fractional division, has 20 digits in total.

Register 65. DIV2 parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIV2_P2[7:0]							
type	Read/Write							

Bit	name	Function
7:0	DIV2_P2[7:0]	DIV2 parameter P2, which is the numerator of DIV2 fractional division, has 20 digits in total.

Register 149. Spread Spectrum Parameters

Bit D7 Name SSC_EN		D6	D5	D4	D3	D2	D1	D0
		SSDN_P2[14:8]						
Type	Read/Write							

bit	name	Function
7	SSC_EN	1: Turn on spread spectrum 0: Disable spread spectrum
6:0	SSDN_P2[14:8]	PLL1 down spread spectrum parameters P2.

Register 150. Spread spectrum parameters

Bit D7 Name		D6	D5	D4	D3	D2	D1	D0
	SSDN_P2[7:0]							
type	Read/Write							

Bit	name	Function
7:0	SSDN_P2[7:0]	PLL1 down spread spectrum parameters P2.

Register 151. Spread spectrum parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
NameSSC_	MODE	SSDN_P3[14:8]						
type	Read/Write							

Bit	name	Function
7	SSC_MODE	0: Downward spread spectrum 1: Center spread spectrum
6:0	SSDN_P3[14:8]	PLL1 down spread spectrum parameter P3.

Register 152. Spread spectrum parameters

Bit D7 Name Type	D6	D5	D4	D3	D2	D1	D0
SSDN_P3[7:0]							
Read/Write							

Bit	name	Function
7:0	SSDN_P3[7:0]	PLL1 down spread spectrum parameter P3.

Register 153. Spread spectrum parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSDN_P1[7:0]							
Type	Read/Write							

Bit	name	Function
7:0	SSDN_P1[7:0]	PLL1 down spread spectrum parameters P1.

Register 154. Spread spectrum parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUDP[11:8]				SSDN_P1[11:8]			
Type	Read/Write							

Bit	name	Function
7:4	SSUDP[11:8]	PLL1 up/down spread spectrum parameters
3:0	SSDN_P1[11:8]	PLL1 down spread spectrum parameters P1.

Register 155. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUDP [7:0]							
Type	Read/Write							

Bit	name	Function
7:0	SSUDP[7:0]	PLL1 up/down spread spectrum parameters

Register 156. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUP_P2[14:8]							
type	Read/Write							

Bit	name	Function
7	Unused	Useless
6:0	SSUP_P2[14:8]	PLL1 upward spread spectrum parameter P2.

Register 157. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUP_P2[7:0]							
Type	Read/Write							

Bit	name	Function
7:0	SSUP_P2[7:0]	PLL1 upward spread spectrum parameter P2.

Register 158. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		SSUP_P3[14:8]						
Type	Read/Write							

Bit	name	Function
7	Unused	Useless
6:0	SSUP_P3[14:8]	PLL1 upward spread spectrum parameter P3.

Register 159. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUP_P3 [7:0]							
Type	Read/Write							

Bit	name	Function
7:0	SSUP_P3[7:0]	PLL1 upward spread spectrum parameter P3.

Register 160. Spread spectrum parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUP_P1 [7:0]							
Type	Read/Write							

Bit	name	Function
7:0	SSUP_P1[7:0]	PLL1 upward spread spectrum parameters P1.

Register 161. Spread spectrum parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SS_NOUT[3:0]				SSUP_P1[11:8]			
Type	Read/Write							

Bit	name	Function
7:4	SS_NOUT[3:0]	These four bits must be set to 0000
6:0	SSUP_P1[11:8]	PLL1 upward spread spectrum parameters P1.

Register 165. OUT0 Initial Phase Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		CLK0_PHOFF[6:0]						
Type	Read/Write							

Bit	name	Function
7	Reserved	This bit must be set to 0
6:0	CLK0_PHOFF[6:0] Output clock	CLK0 initial phase offset. CLK0_PHOFF[6:0] increases by 1, that is, 1LSB. This is equivalent to adding a delay of one quarter of the VCO cycle to the initial phase of the output clock.

Register 166. OUT1 Initial Phase Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		CLK1_PHOFF[6:0]						
Type	Read/Write							

Bit	name	Function
7	Reserved	This bit must be set to 0
6:0	CLK1_PHOFF[6:0] Output clock	CLK1 initial phase offset. CLK1_PHOFF[6:0] increases by 1, that is, 1LSB. This is equivalent to adding a delay of one quarter of the VCO cycle to the initial phase of the output clock.

Register 167. OUT2 Initial Phase Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		CLK2_PHOFF[6:0]						
Type	Read/Write							

Bit	name	Function
7	Reserved	This bit must be set to 0
6:0	CLK2_PHOFF[6:0] Output clock	CLK2 initial phase offset. CLK2_PHOFF[6:0] increases by 1, that is, 1LSB. This is equivalent to adding a delay of one quarter of the VCO cycle to the initial phase of the output clock.

Register 177. PLL Reset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name PLL2_RST Reserved PLL1_RST Type Read/Write				Reserved				
		Read/Write	Read/Write Read/Write Read/Write Read/Write Read/Write Read/Write					

Bit	name	Function
7	PLL2_RST	Writing 1 to this bit will reset PLL2. This is a self-clearing bit.
6	Reserved	reserve
5	PLL1_RST	Writing 1 to this bit will reset PLL1. This is a self-clearing bit.
4:0	Reserved	reserve

Register 183. Internal crystal load capacitance

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	XTAL_CL		Reserved					
type	Read/Write							

Bit	name	Function
7:6	XTAL_CL	These two bits determine the value of the crystal's internal load capacitance. 00: Reserved value (not used) 01ÿCL=6pF 10ÿCL=8pF 11: CL = 10pF (commonly used)
5:0	Reserved	These 6 bits must be written as 010010b

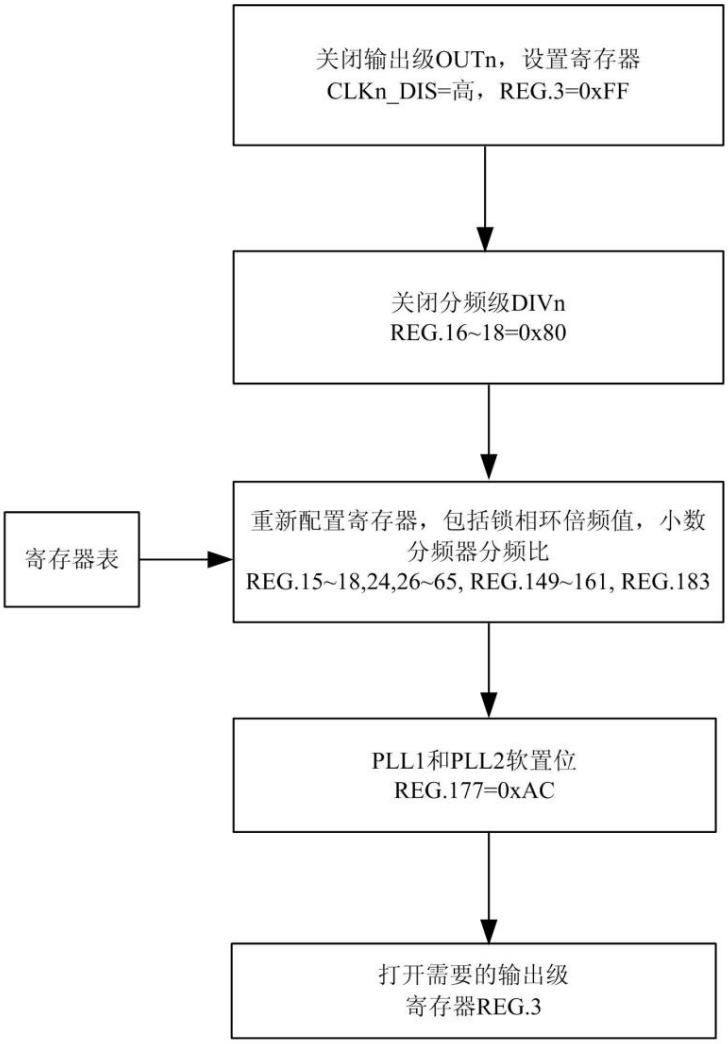
Register 187. Output Channel Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	XO_FANOUT_IN	Reserved	MS_FANOUT_IN	Reserved			
type	Read/Write							

Bit	name	Function
7	Reserved	reserve
6	XO_FANOUT_EN	XO outputs directly from the output stage, enable 1 is valid
5	Reserved	reserve
4	MS_FANOUT_EN	OUT1 and OUT2 can select OUT0 as input, enable 1 is valid
3:0	Reserved	reserve

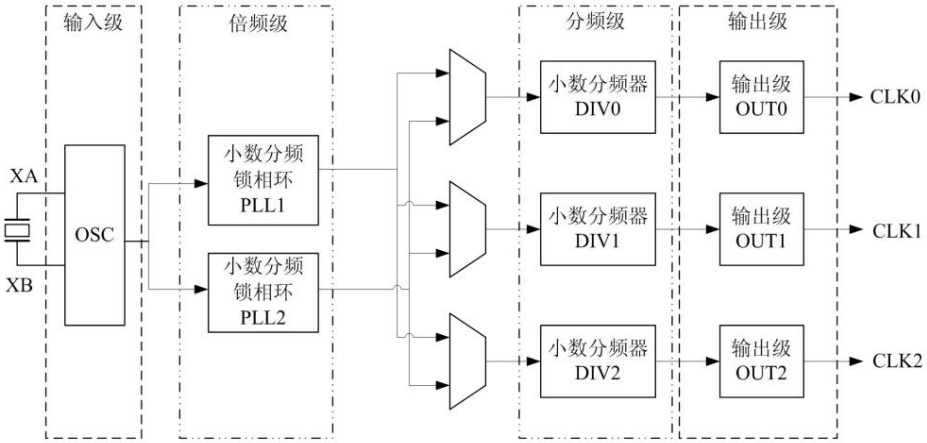
MS5351M is a flexible and configurable clock generator. To make the chip output the correct clock, it is recommended to use the following configuration process

Related registers.



Functional

DescriptionMS5351M is an I2C configurable clock generator chip that can completely replace crystals, crystal oscillators, phase-locked loops, and output buffers. The chip functional block diagram is as follows:



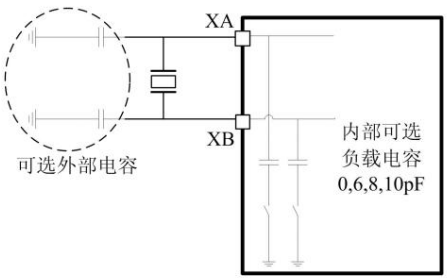
MS5351M is mainly composed of the following modules: crystal oscillator, fractional frequency phase-locked loop PLL1 and PLL2, fractional frequency divider DIV0, DIV1 and DIV2, output stage OUT0, OUT1 and OUT2 and I2C controller. The crystal oscillator as the input stage can receive the external 25MHz to 27MHz quartz crystal signal and amplify it to the logic level to provide the reference clock for the fractional frequency phase-locked loop. The fractional frequency phase-locked loop multiplies the reference clock to a high frequency, and then the required clock is generated by the high-precision fractional divider. In addition to providing configurable output drive capability, the output stage also provides additional integer division (the integer division ratio can also be configured), which can reduce the final output frequency to 2.5kHz. In addition, the chip uses a cross switch from the input to the output of the fractional divider, so that the output of any port can select PLL1 or PLL2 as the clock source. 2.1 Input stage

The input stage of the

MS5351M uses a

fixed frequency (25MHz-27MHz) AT-section quartz crystal as the clock of the crystal oscillator.

Source. Its output provides reference for two phase-locked loops to generate asynchronous clocks. When a quartz crystal is connected to the XA/XB terminal of the MS5351M, the chip provides a configurable load capacitor, which eliminates the need for external load capacitors. The internal total XTAL load capacitor can be selected as 0, 6, 8, or 10pF. Of course, you can also choose to use an external load capacitor of no more than 6pF. In this case, the capacitance of each end of XA and XB should not be greater than 12pF.



2.2 Frequency Synthesizer

The frequency synthesizer of MS5351M adopts the architecture of fractional frequency phase-locked loop + fractional frequency divider to generate the final output clock. The phase-locked loop multiplies the low-frequency reference clock to a high frequency, and then the high-precision fractional frequency divider generates the required clock. Only two different clocks greater than 112.5MHz are allowed to be output simultaneously, but the same clock greater than 112.5MHz can be output on 3 channels at the same time, and it is also possible to output two identical clocks greater than 112MHz while outputting another different clock greater than 112.5MHz.

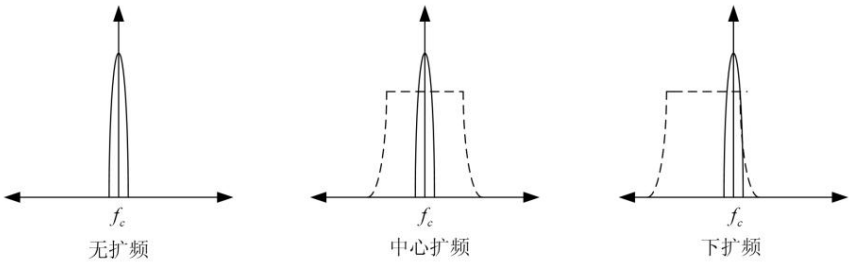
2.3 Output Stage

MS5351M provides an additional 2N (N is an integer from 0 to 7) division after the fractional divider, which makes MS5351M

The output clock can be as low as 2.5kHz. All three output stages can generate CMOS level outputs and share a single VDDO power supply, which can accept VDDO voltages of 1.8V, 2.5V, and 3.3V.

2.4 Spread

Spectrum When the spread spectrum function is enabled, only PLL1 can be selected as the reference clock source for the fractional divider. Spread spectrum technology is very effective in reducing electromagnetic interference. It uses a modulated signal to modulate the output clock, which reduces the signal strength originally concentrated at a certain frequency point and distributes it evenly within a certain spectrum range. MS5351M provides two modes, down-spread spectrum and center-spread spectrum, and multiple spread spectrum levels to balance system performance and anti-electromagnetic interference capabilities.



2.5 I2C Interface

Many functions of MS5351M are completed through I2C read and write registers. Read status

indication register ÿ PLL1 or

PLL2 lost lock, LOL_1 or LOL_2, REG0[6:5] Write register

ÿ Configure the fractional PLL multiplier value and the fractional divider ratio ÿ Configure

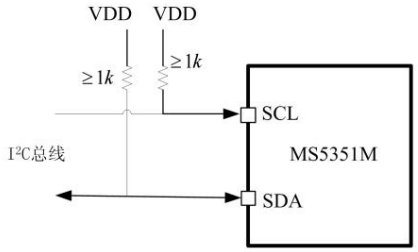
the spread spectrum mode and spread spectrum

range ÿ Configure the output clock to select PLL1 or PLL2 ÿ Set

output options: such as enabling or disabling any output, inverting or not inverting the output, output stage division ratio, output phase offset, and output

shutdown status

The I2C bus consists of a bidirectional serial data line SDA and a serial clock line SCL, as shown in the figure below. The SDA and SCL pins must be connected to pull-up resistors that comply with the I2C specification.



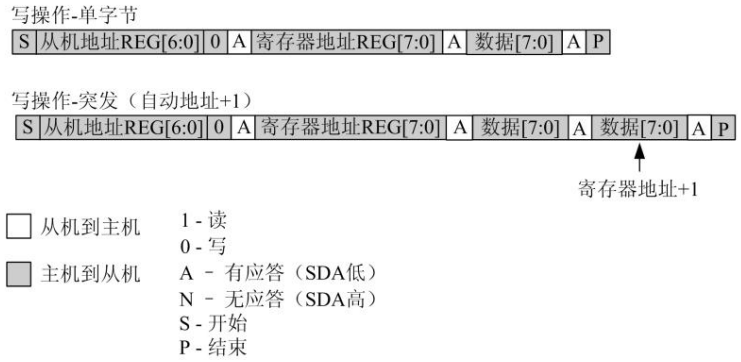
The I2C interface works in slave mode and has a 7-bit fixed address, as shown below. It can work in standard mode (100kbps) or fast mode (400kbps) and supports burst data transmission.

	6	5	4	3	2	1	0
从机地址	1	1	0	0	0	0	0

Data is transmitted from the highest bit of the 8 bits first. A write command consists of 7 slave address bits, 1 write operation bit, 8 register address bits and

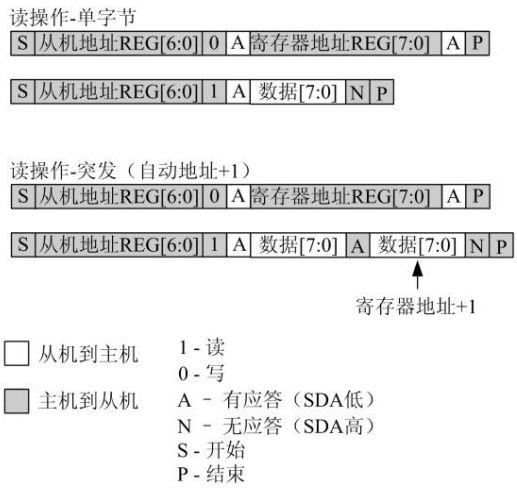
A burst write operation is also shown in the figure below, where each additional data word is automatically written to the register address + 1.

method is written.



The read operation is performed in two stages, first writing the register address, and then reading the data of the corresponding address register.

Indicated in the figure below.



The DC and AC specifications of the I2C interface are shown in the table. The timing specifications comply with the I2C bus standard.

2.6 Design Considerations

The MS5351M requires fewer external components and the following recommendations can optimize performance.

2.6.1 Decoupling capacitors

The MS5351M has built-in power supply decoupling circuits. Low dropout (LDO) circuits are widely used internally to reduce the use of external bypass devices.

Externally, only 0.1-1uF decoupling capacitors are needed on each power pin, which should be as close to VDD and VDDO as possible.

2.6.2 Power-on sequence

The internal core circuit and output stage are powered by VDD and VDDO respectively, and the power-on time of VDDO is required to be no later than that of VDD.

2.6.3 External Quartz Crystal

Place the external quartz crystal as close to XA/XB as possible to shorten the PCB trace length. Also note that these two pins should be kept away from other

High-speed signal routing.

2.6.4 External quartz crystal load capacitance

Internal load capacitors can be used on the XA and XB pins. When the internal load capacitors are insufficient, external load capacitors can be used.

External load capacitors should be placed as close to XA/XB as possible.

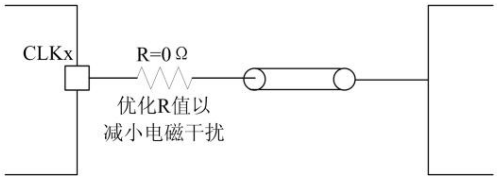
2.6.5 Unused Pins

Unused output pins CLKn (n=0,1,2) should be left floating

2.6.6 Wiring

The MS5351M provides a variety of current drive capabilities. When using the default maximum drive capability, it is recommended to use the following wiring to optimize the current.

Magnetic interference performance.



Frequency Planning

MS5351M contains two fractional-frequency phase-locked loops PLL1 and PLL2. Each phase-locked loop consists of an internal divider PLL1_DIV and

PLL2_DIV multiplies the low-frequency reference clock to a VCO frequency of 600MHz~900MHz. Each VCO can be

The fractional divider DIVn (n=0,1,2) divides the frequency to generate a clock of 320kHz~200MHz.

The output clock frequency is reduced to 2.5kHz in one step. The relationship between the output clock and the VCO clock is as follows:

$$CLKn = \frac{VCon}{DIVn\_DivideRatio\ OUTn}$$

In the above formula, *DIVn_DivideRation* represents the fractional division ratio of the external divider of the phase-locked loop, and OUTn represents the integer division ratio of the output stage.

Frequency ratio, n=0,1,2.

3.1 PLL Selection

If the spread spectrum function is turned off, then both PLL1 and PLL2 can be used as the output clock source. If the spread spectrum function is turned on, then it can only be used for

PLL1ÿ

3.2 Selecting the appropriate VCO frequency and division ratio

1) Taking the reference clock of 25MHz as an example, the division ratio of the internal divider PLL_DIV of the phase-locked loop can only be set to 24+1/1048575 to

36+0/1048575. This setting ensures that the VCO works in the normal frequency range.

2) The effective division ratio of the external fractional divider DIVn (n=0,1,2) can only be integers 4, 6, 8 or 8+1/1048575 to

Values between 1800+0/1048575.

3) For applications with high requirements on output clock jitter, it is recommended to set the loop external divider DIVn (n=0,1,2) to an integer. If possible,

Both the internal and external division ratios of the loop can be set to integers.

4) If possible, set the fractional divider DIVn (n=0,1,2) outside the loop to as many integer division ratios as possible.

3.3 Frequency multiplication level - Phase-locked loop internal frequency multiplication (division) formula

The output frequency of this stage is:

$$VCOn = XO \times PLLn\_DivideRation$$

The frequency division value is:

$$PLLn\_DivideRation = 4 + \frac{PLLn\_P1[17:0] + \frac{PLLn\_P2[19:0]}{PLLn\_P3[19:0]}}{128}$$

In the above formula, n = 1, 2. *XO* represents the output frequency of the crystal oscillator.

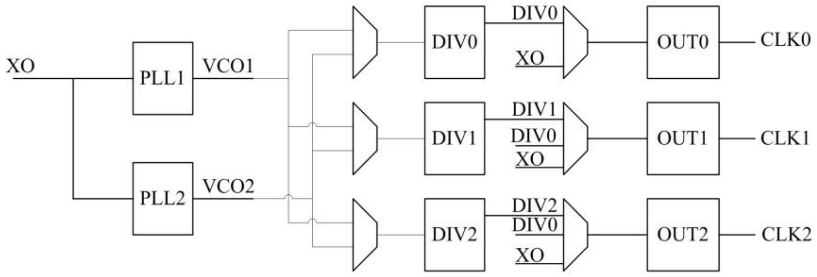
If *PLLn_DivideRatio* is an even number, registers PLL1_INT and PLL2_INT can be set separately.

In most cases, when the division ratio *PLLn_DivideRatio* is an even number, set registers PLL1_INT and PLL2_INT

The jitter performance can be significantly improved. When the spread spectrum is turned on, the register PLL1_INT must be set to 0.

3.4 Configuring Output

The figure below shows the path of the clock output and the selected clock source. The outputs of the fractional dividers DIV0~DIV2 correspond to DIV0~DIV2 respectively.



3.5 Frequency division level - Phase-locked loop external fractional frequency division formula

DIVn(n=0,1,2) can select PLL1 or PLL2 by setting register DIVn_SRC(n=0,1,2) to 0 or 1 respectively.

There are two scenarios:

1) When the output frequency is less than or equal to 150MHz, the output frequency of this level is:

$$DIVn = \frac{VCOx}{DIVn\ DivideRation}$$

The frequency division ratio is:

$$DIVn\ DivideRatio = 4 + \frac{DIVn\_P1[17:0] + \frac{DIVn\_P2[19:0]}{DIVn\_P3[19:0]}}{128}$$

VCOx (x = 1, 2). In the above formula, *DIVn_DivideRatio* can only be integers 4, 6, 8 or 8 + 1/1048575 to 1800 + 0/1048575

The value between *DIVn_DivideRatio* in n = 0, 1, 2. If the frequency division ratio of this stage is an even number, you can set the register

DIVn(n=0,1,2)_INT corresponding bit is equal to 1. In most cases, when the frequency division ratio *DIVn_DivideRatio* is an even number, set the register

Setting the corresponding bit of the device DIVn_INT(n=0,1,2) to 1 can significantly improve the jitter performance.

2) When the output frequency is greater than 150MHz, the frequency division ratio of this stage must be set to 4, and the register must be set as follows:

DIVn(n=0,1,2)_P1=0,

DIVn(n=0,1,2)_P2=0,

DIVn(n=0,1,2)_P3=1,

DIVn(n=0,1,2)_INT=1,

DIVn(n=0,1,2)_DIVBY4[1:0]=11b

The final output clock is: $foutn = \frac{VCon}{4}$

3.6 Output Level Settings

After the fractional division ratio outside the phase-locked loop is set, the output stage can be set according to the desired clock.

3.6.1 Selecting a clock source for the output stage

The register for selecting the output stage clock source is CLKn_SRC (n=0,1,2).

CLK0 can select either the crystal oscillator output XO or the DIV0 output as the clock source for this level. CLK1 can select XO,

DIV1 and DIV0. CLK2 can select XO, DIV2 and DIV0.

3.6.2 Output stage integer division ratio setting

When the required frequency is less than 320kHz, the output frequency division register OUTn_DIV (n=0,1,2) can be set to generate 2 N (N is from 0

The final output frequency can be as low as 2.5kHz.

3.6.3 Output inversion register CLKn_INV (n=0,1,2)

In some applications, it is necessary to generate a clock with an opposite phase to another clock. In this case, you can set the register CLKn_INV=1

3.6.4 Status register for output stage shutdown

When an output is turned off, you need to set the state of the output, which can be configured as low, high, or high impedance output.

Register CLKn_DIS_STATE (n=0,1,2).

3.6.5 Unused output ports

Any unused output port can be turned off to reduce power consumption. Set register CLKn_PDN = 1 to turn it off.

3.7 Configuring Spread Spectrum Register Parameters

The spread spectrum enable register SSC_EN controls the opening and closing of the spread spectrum function. SSC_EN=1 turns on the spread spectrum function.

Each output that selects PLL1 as the clock source can enable the spread spectrum function. The MS5351M provides downward spread spectrum and center spread spectrum for selection.

The downward spread spectrum range is -0.1%~-2.5%, and the center spread spectrum range is -1.5%~+1.5%. The spread spectrum modulation rate is limited to about 31.5kHz.

The following parameters must be understood before setting up spread spectrum:

ÿXO —— Reference clock of phase-locked loop PLL1

ÿPLL1_DivideRatio —— Division ratio of phase-locked loop PLL1

ÿsscAMP —— Spreading amplitude (for example, if the down-spreading and center-spreading amplitudes are 1%, then sscAMP=0.01)

Note: Register PLL1_INT must be set to fractional frequency mode.

Use the following formula to configure the required spread spectrum range

3.7.1 Downward Spread Spectrum

Need to write 4 register parameters: SSUDP[11:0], SSDN_P1[11:0], SSDN_P2[14:0], SSDN_P3[14:0]

UP/DN parameters

$$SSUDP[11:0] = Floor\left[\frac{XO}{4 \times 31500}\right]$$

Intermediate variables (no registers to write):

$$SSDN = 64 \times PLL\_DivideRation \times \frac{sscAMP}{1 - sscAMP \times SSUDP}$$

Downward spread spectrum parameters:

$$SSDN\_P1[11:0] = Floor[SSDN]$$

$$SSDN\_P2[14:0] = 32767 \times [SSDN - SSDN\_P1]$$

$$SSDN\_P3[14:0] = 32767 - 0x7FFF$$

Upward spread spectrum parameters:

$$SSUP\_P1[11:0] = 10$$

$$SSUP\_P2[14:0] = 20$$

$$SSUP\_P3[14:0] = 31$$

3.7.2 Center Spread Spectrum

Need to write 7 parameters: SSUDP[11:0],

SSDN_P1[11:0],SSDN_P2[14:0],SSDN_P3[14:0],

SSUP_P1[11:0],SSUP_P2[14:0],SSUP_P3[14:0].

UP/DN parameters:

$$SSUDP[11:0] = Floor\left(\frac{XO}{4 \times 31500}\right)$$

Intermediate variables (no registers to write):

$$SSUP = 128 \times PLL\ DivideRation \times \frac{sscAMP}{1 - sscAMP \times SSUDP}$$

$$SSDN = 128 \times PLL\ DivideRation \times \frac{sscAMP}{1 + sscAMP \times SSUDP}$$

Up-spread spectrum parameters:

$$SSUP\_P1[11:0] = Floor[SSUP]$$

$$SSUP\_P2[14:0] = 32767 \times [SSUP - SSUP\_P1]$$

$$SSUP\_P3[14:0] = 32767 - 0x7FFF$$

Downward spread spectrum parameters:

$$SSDN\_P1[11:0] = Floor[SSDN]$$

$$SSDN\_P2[14:0] = 32767 \times [SSDN - SSDN\_P1]$$

$$SSDN\_P3[14:0] = 32767 - 0x7FFF$$

3.8 Configuring the initial phase of the output clock

The initial phase of each output clock can be set by register CLKn_PHOFF[6:0] (n=0,1,2). The phase offset parameter is an unsigned bit.

Each change of CLKn_PHOFF[6:0] by 1, i.e. 1LSB, corresponds to a change of 1/4 VCO period in the output clock delay.

formula and determine the register value according to the required initial phase offset.

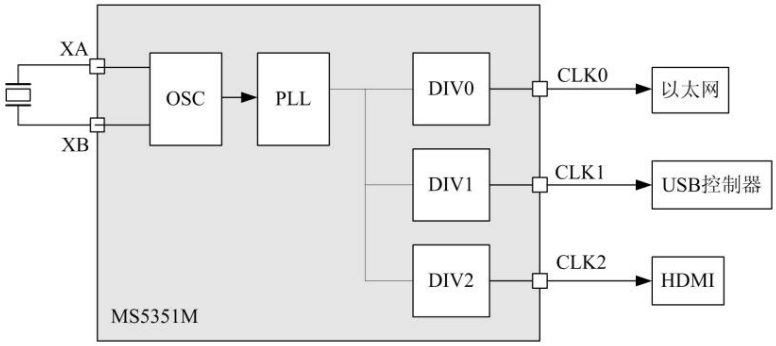
$$CLKn\_PHOFF[6:0] = Round(Offset \times 4 \times VCO)$$

Typical application diagram

4.1 Replacement of quartz crystals, crystal oscillators and phase-locked loops

MS5351M is a universal clock generator chip, which is widely used.

Generate 3 independent clocks, as shown below:

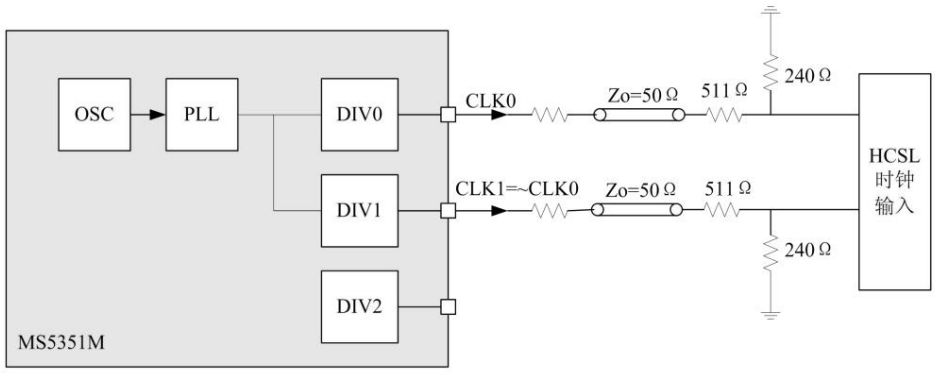


The XA terminal can also accept the CMOS clock, in which case XB should be left floating.

4.2 HCSL-Compliant Output

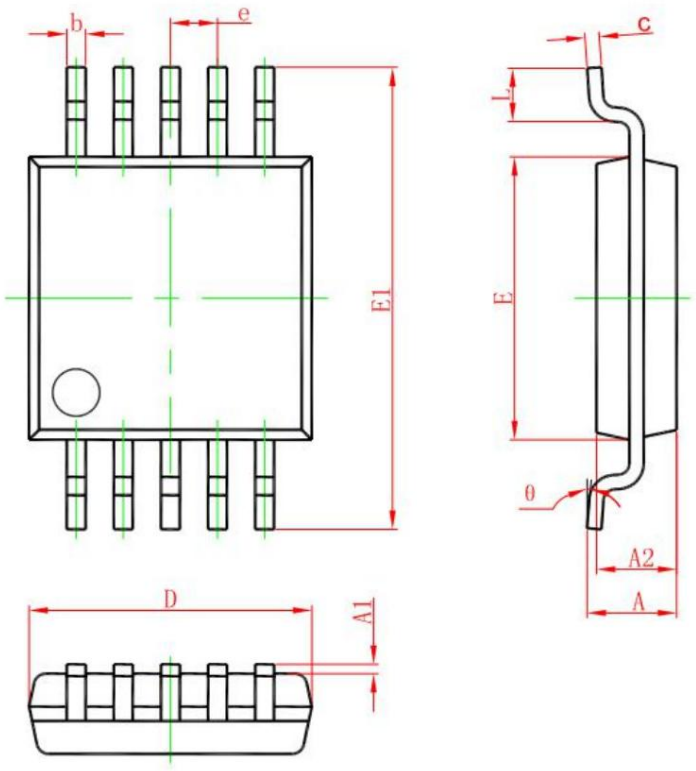
When the output stage supply voltage VDDO is 2.5V, the MS5351M can be configured to be compatible with the HCSL swing. The following figure is an HCSL application scenario.

In this case, since HCSL only receives differential signals, one of the outputs must be inverted, and the register CLKn_INV (n=0,1,2) can be set.



Package outline drawing

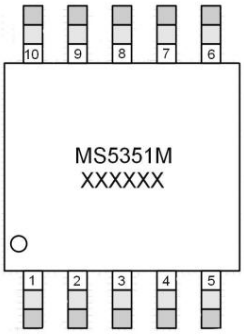
MSOP10



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Seal and packaging specifications

1. Introduction to the content of the seal



MS5351M: Product Model

XXXXXX: production batch number

2. Seal Standard Requirements

Laser printing is used, the whole is centered and the font is Arial. 3. Packaging instructions:

Model Packaging Type Piece/Reel		Roll/Box	Piece/box	Box/Carton	Piece/box
MS5351M MSOP10	3000	1	3000	8	24000

MOS circuit operation precautions:

Static electricity can be generated in many places. Taking the following preventive measures can effectively prevent MOS circuits from being affected by static electricity.

Damage caused by discharge:

1. Operators must be grounded using an anti-static wrist strap.

2. The equipment casing must be grounded.

3. Tools used during the assembly process must be grounded.

4. Conductive packaging or antistatic materials must be used for packaging or transportation.

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