Non-complex signal processing in a low-IF receiver for GSM

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Abstract: The low-IF receiver architecture has already proved its effectiveness in mobile radio applications such as GSM. By using an IF of half the channel spacing to facilitate the removal of DC offsets, it achieves the sensitivity of a conventional superhet whilst offering the full integration potential of a direct-conversion receiver. Previous attempts to improve its multi-mode capability have focussed on digitising as much as possible of the IF signal chain with the help of a complex ADC. The channel filtering then moves into the digital domain where reprogramming is comparatively easy for operation in other modes. However, the combination of an increased dynamic range requirement and the need for a complex ADC can make the circuit design problem unduly difficult. In the receiver architecture to be described, the need for a complex ADC is avoided by processing only the real part of the low-IF signal. This substantially simplifies the ADC design whilst retaining all the advantages of a digitised, low-IF receiver. Simplification of the ADC design is the main objective but there is also scope for a 17% reduction in power consumption.

1 Introduction

Handsets for GSM (Global System for Mobile Communications) are now in common use throughout the world. Some of the most recent of these use a low-IF receiver architecture [1, 2] as the preferred solution, thereby combining the excellent performance capabilities of a superhet with the attractive integration capability of the zero-IF concept [3]. As described in [1], the low-IF architecture or near-zero-IF architecture as it is sometimes known, overcomes the difficulties with DC offsets encountered in the zero-IF architecture by moving the wanted signal away from DC onto an IF of half the channel spacing. For GSM the IF is therefore 100 kHz. This is just high enough to allow AC coupling to be introduced to remove the DC offsets without damaging the spectrum of the wanted signal, but still low enough to have a minimal impact on the power consumption of the integrated channel filters.

More recent developments of the low-IF receiver architecture [4] have concentrated on the digitisation of the signal chain with a view to improving multi-mode capability. In an initial realisation, this involved positioning the analogue-to-digital converter (ADC) immediately after the mixers of the front end, eliminating the need for automatic gain control (AGC) and moving the channel filtering into the digital domain. Despite the obvious merit of this advance, one unattractive aspect has proved to be the need for a complex ADC resulting directly from the use of the low IF. The extra circuitry involved in making the ADC complex leads to severe difficulties if its bandwidth and clock speed need to be modified for operation with other radio standards besides GSM. Hence, in the receiver to be described, further changes have been made to the architecture with the main objective of avoiding the need for a complex ADC. The result is a highly adaptable, highly digitised, low-IF receiver requiring only a single, 'real' ADC.

After describing the digitisation problem in a little more detail, the paper will examine the basic performance requirements of GSM and derive some of the most important receiver dimensions. It will then present the revised low-IF receiver architecture in which the need for a complex ADC is avoided. The technique involves dropping the Q component of the IF output of the front end and then only processing the I component in the ADC. Details will be given of the three components most closely associated with the non-complex signal processing namely the poly-phase image-rejection filter, the digital make-complex filter and the ADC itself which is based on a fifth-order sigma–delta ($\Sigma\Delta$) modulator. The paper will present results derived from system simulations in validation of the modified architecture before drawing some final conclusions.

2 Digitising a conventional low-IF architecture

The diagram given in Fig. 1 illustrates a highly digitised, low-IF receiver architecture that has already been evaluated for use with GSM [4]. At the front end it comprises the usual combination of RF filter, low-noise amplifier and quadrature down-converter for capturing the incoming RF signals and placing the wanted channel on an IF of 100 kHz. To remove the troublesome DC offsets generated in the mixers, the I and Q components of the IF signal pass through a pair of AC couplings which act as first-order high-pass filters with a cut-off frequency of approximately 10 kHz. The cut-off frequency is not critical, but this value is high enough to allow the removal of dynamic as well as static DC offsets without damaging the wanted signal. As shown in the Figure, the IF signals are amplified by two fixed-gain elements and then fed directly into the complex ADC. The ADC is complex to align the spectrum of its quantisation noise with that of the wanted signal. It is

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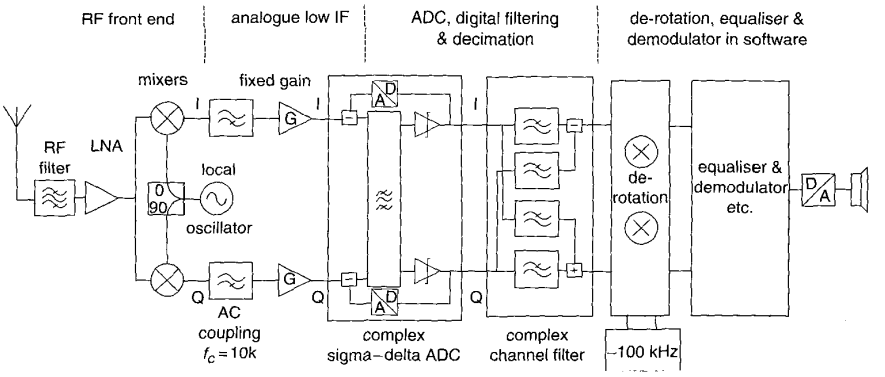

Fig. 1 *Complex signal processing in low-IF receiver architecture*

realised as a pair of cross-coupled ΣΔ modulators, which digitise the I and Q inputs into a pair of bit-streams of 1-bit resolution. These are, in turn, filtered by the digital channel filter whose dual roles are to remove any external interferers accompanying the wanted signal and also to remove the high-frequency quantisation noise generated by the ADC. The final step before equalisation and demodulation is to derotate the wanted signal back to an IF of zero.

There can be little doubt that eliminating the need for analogue channel filtering and AGC in this way is a significant step forward in terms of giving the receiver better multi-mode potential. However, moving the ADC function to such an advanced position in the signal chain carries the disadvantage of increasing the dynamic range requirement of the ADC. As will be explained later, the dynamic range required for GSM in these circumstances is in the region of 100 dB and, when this is combined with the complex aspect of the signal processing, the design of the ADC becomes a major challenge. There is also the disadvantage of needing a total of four FIR filter blocks in order to realise the asymmetrical frequency characteristics of the complex channel filters.

3 Performance requirements

The GSM standard is based on a mixture of time-division multiple access (TDMA) and frequency-division multiple access (FDMA). Each user is allocated a particular frequency channel of width 200 kHz and a time slot of duration 576.9 μs. Over the frequency range 915 to 960 MHz there are 175 available channels and over a period of 4.16 ms there are eight available time slots. The information rate is typically 9.6 kbit/s which, after channel coding and training bits are added, translates into a physical bit rate of 270.833 kbit/s. The type of modulation used is Gaussian minimum shift keying (GMSK) with a BT factor of 0.3. Responsibility for the GSM standard now lies with the 3rd-Generation Partnership Project (3GPP) [5].

Full details of the performance requirements relevant to the design of the receiver can be found in [6]. These relate to a 'small' mobile terminal receiving full-rate speech. There are several different fading conditions under which the terminal must operate, the most relevant of which are the static, TU50 and EQ50 profiles. With a static profile (i.e. no fading) the requirement on bit error rate (BER) is generally 2% unless specified otherwise. For the TU50 profile, which is intended to represent a typical urban situation where the terminal is limited to a velocity of 50 km/h, the BER requirement is 8%. A 3% BER usually applies to the EQ50 profile. The most important of the receiver characteristics for GSM are given in Table 1.

It should be noted that, although the GSM specification only calls for a reference sensitivity of −102 dBm, most receivers in current use actually achieve a sensitivity of −108 dBm and therefore this is now the more relevant performance objective.

4 Receiver dimensions

The receiver noise figure derives largely from the system requirement for sensitivity. The logical starting point for the calculation is the estimation of the signal-to-noise ratio (SNR) needed at the demodulator/equaliser of a pseudo-ideal receiver. According to basic system simulations, the E_b/N_o required for an 8% BER with a TU50 propagation channel is 5.2 dB. When a correction factor of 1.32 dB is applied to take account of the ratio of the bit rate to the channel bandwidth (i.e. 270.833/200), the SNR estimate becomes 6.5 dB. Hence, if the desired sensitivity, P_{sen}, is −108 dBm, the total noise power at the input to the receiver under these conditions, P_n, must be given by:

$$P_n = P_{sen} - SNR_{gmsk} = -108 - 6.5 = -114.5\,\text{dBm} \quad (1)$$

If this is compared with the thermal noise level (−173.83 dBm) raised by 53 dB to account for the 200 kHz channel bandwidth, the overall receiver noise

Table 1: Receiver characteristics for GSM

Maximum input	−15 dBm for 0.1% BER, static channel
Reference sensitivity	−102 dBm for 8% BER, TU50 channel (c.f. state of the art −108 dBm)
Co-channel interferer	−9 dB with respect to wanted signal at −82 dBm, 8% BER, TU50 channel
Adjacent-channel interferer	+9 dB with respect to wanted signal at −82 dBm, 8% BER, TU50 channel
Alternate-channel interferer	+41 dB with respect to wanted signal at −82 dBm, 8% BER, TU50 channel
Largest blocking signal (CW)	−23 dBm, 3 MHz offset, wanted signal at −99 dBm, 2% BER, static channel

figure, F_{db}, must then be:

$$F_{dB} = P_n - 10\log(200 \times 10^3) + 173.83 = 6.5\,\text{dB} \quad (2)$$

The front end alone needs a noise figure slightly less than this to allow for the quantisation noise contribution of the ADC. By assigning to the front end a noise figure of 6.0 dB, the degradation in receiver noise figure caused by the ADC must be approximately 0.5 dB, which corresponds to a referred ADC noise power, P_{adc}, of:

$$P_{adc} = P_n - 0.5 + 10\log_{10}\left[10^{\frac{0.5}{10}} - 1\right]$$
$$= -114.5 - 0.5 - 9.136 = -124.1\,\text{dBm} \quad (3)$$

In further references to this parameter the value will be rounded up to −125 dBm. Finally, if it is assumed that 2.5 dB of losses are to be tolerated in the passive RF parts of the front end, the noise figure of the active part must be further reduced to the value of 3.5 dB.

The adjacent-channel and alternate-channel rejection requirements of the receiver are illustrated by the curves plotted in Fig. 2. These represent the spectral envelopes of a wanted signal, a co-channel, an adjacent-channel and an alternate-channel interferer at the relative frequencies and levels stipulated in the GSM specification. For the tests in question, the wanted signal is at a relatively high level of −82 dBm, at which point the receiver noise can be ignored. Given that the receiver can achieve an 8% BER in a TU50 propagation channel with an SNR of 6.5 dB, there is generally no difficulty in meeting the co-channel rejection requirement of −9 dB. Then, on the basis that an adjacent-channel interferer at a level +9 dB above the wanted signal must be attenuated to the level of a co-channel interferer, the adjacent-channel rejection requirement must be at least 18 dB. Similarly, the alternate-channel rejection requirement must be of the order of 50 dB.

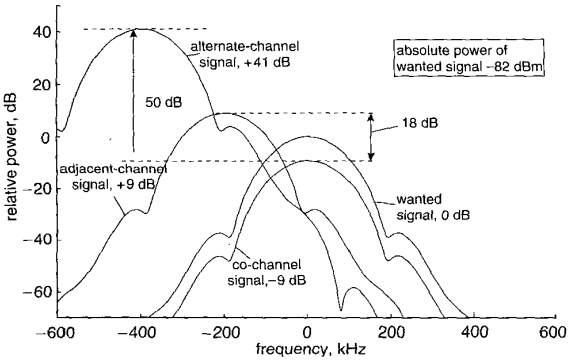

Fig. 2 *Channel filter rejection requirements*

Of the different blocking signals referenced in the 3GPP specification, it is the signal at a 3 MHz offset with a level of −23 dBm (P_{int}) that is generally regarded as the most demanding. Under the relevant test conditions the wanted signal is at a level of −99 dBm and if the required SNR of 6.5 dB is to be achieved, the residual power of the blocking signal after filtering must be no higher than −(99 + 6.5) = −105.5 dBm. At the level of −114.5 dBm, the receiver noise power can largely be ignored and the rejection requirement for the blocking interferer A_{blk} is then simply:

$$A_{blk} = P_{int} - P_{sig} + SNR_{gsm} = -23 + 99 + 6.5$$
$$= 82.5\,\text{dB} \quad (4)$$

The dynamic range requirement of the ADC in the receiver is determined by the level of this same blocking interferer and by the permitted level of the ADC quantisation noise P_{adc}. Hence the difference between the −23 dBm level of the blocking signal and the −125 dBm level of the noise gives a dynamic range requirement of 102 dB. Although substantial, this is known to be within the capability of the ΣΔ modulator type of ADC to be described. The design problem is also not quite so severe if the SINAD (signal-to-noise-and-distortion) requirement of the ADC is taken into consideration which, for the purposes of passing the blocking-interferer test, is a lower value of 85.5 dB. This is derived in much the same way as the filtering requirement for the blocking signal, i.e.

$$SINAD = P_{int} - P_{sig} + SNR_{gsm} + 3$$
$$= -23 + 99 + 6.5 + 3 = 85.5\,\text{dB} \quad (5)$$

the extra 3 dB being inserted to allow both the ADC noise and the residue of the blocking signal to contribute equally towards the maximum permitted noise residue mentioned above of −105.5 dBm.

5 The change to non-complex signal processing

A diagram of the revised low-IF receiver architecture that avoids the need for a complex ADC is given in Fig. 3. The basic idea is that, instead of processing both the I and Q components of the low-IF output from the front end, the Q component is discarded and only the I component is passed to a single, non-complex, ΣΔ modulator. The effect of this is to make the spectrum of the now real IF signal symmetrical about zero, as if the IF were itself zero (ref. spectrum at B in Fig. 3). Hence the spectrum is naturally aligned with that of the quantisation noise spectrum of the single ΣΔ modulator. It is then relatively easy to make the IF signal complex once again by performing the equivalent of a Hilbert transform in the digital channel filters that follow. The rest of the signal chain is the same as the previous system of Fig. 1.

An obvious consequence of processing only the I component of the IF signal is a complete loss of image rejection. Any interferer present in the lower adjacent channel will be folded over about zero frequency and become indistinguishable from the wanted signal. There is also a problem with the lower alternate channel as, when this signal becomes folded about zero, it falls into what is effectively the adjacent channel on the upper side of the wanted signal. In this position the lower tail of its spectrum falls into the band of the wanted signal and due to its relatively high power level the interference caused can degrade receiver sensitivity. Fortunately, both these problems can be easily overcome by filtering the output of the front end with a simple polyphase filter. The filter attenuates any interferers present in the lower adjacent and alternate channels to a sufficiently low level that they no longer have any significant effect. Except for some interstage buffers, the polyphase filter is a passive device and therefore consumes little DC power.

Like the original system of Fig. 1, the system of Fig. 3 uses no AGC and, despite the presence of the polyphase filter, the vast majority of the channel selectivity is implemented in the digital domain. The DC offsets from the mixers are removed by AC couplings, whose high-pass characteristics have the same 10 kHz cut-off frequency as used previously. The single ΣΔ modulator addresses the same dynamic range as before, but is now very much easier to design for optimum conversion efficiency and for improved adaptability. As will be shown, the dynamic range can be achieved with a fifth-order ΣΔ modulator, whose clock frequency is 26 MHz. The high levels of quantisation noise produced by the modulator outside the

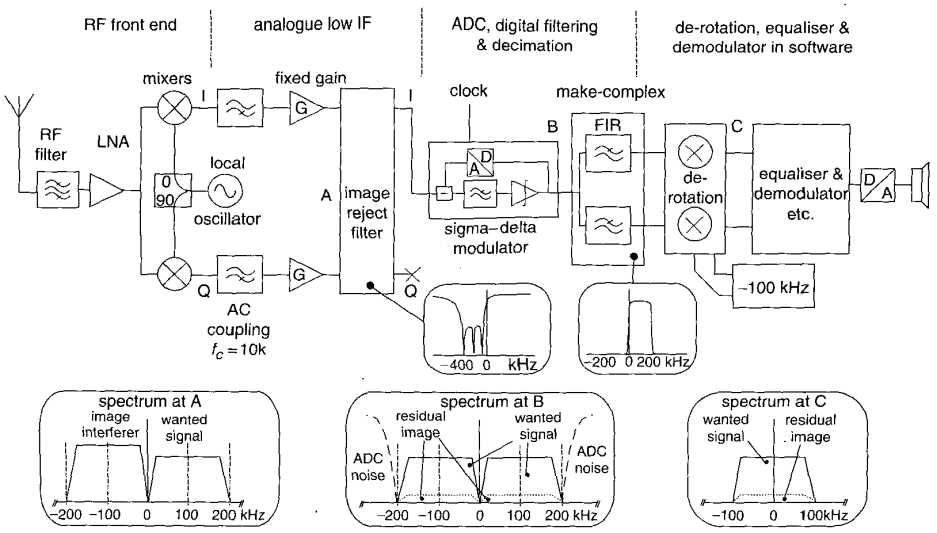

Fig. 3 *Non-complex signal processing in low-IF receiver architecture*

bandwidth of the wanted signal are heavily attenuated by the subsequent digital filters. This pair of FIR filters also provides the necessary channel filtering as well as reconstructing the Q component to make the IF signal complex once again. Only two FIR blocks are required because of the absence of a Q input. It is also important to note that the blocks decimate by a factor of 96 in one step, lowering the sampling frequency from 26 MHz at the input, to the bit rate of 270.8333 kHz at the output. Decimating in one step improves power efficiency by avoiding the need for digital multiplication. The signal processing then involves only changing the sign of the tap weights prior to summation in response to changes in the state of the binary input bit stream from the ΣΔ modulator.

Whilst improved adaptability is the main objective behind this non-complex signal processing, there will usually be some advantage to be gained in terms of power consumption over the alternative of a fully complex architecture. To explain this, it is helpful to split the power consumption of the whole ADC function into two parts, namely that associated with only the ΣΔ modulators P_1, and that associated with the decimation filters P_2. Furthermore, to establish a point of reference in this elaboration, the two powers P_1 and P_2 will be defined as the powers consumed by the two parts of the ADC function in an equivalent direct-conversion receiver operating with a zero IF and consuming a total power P_{zif}. In this scenario it is common for P_1 and P_2 to be of approximately the same magnitude.

To make the step from a zero-IF to a conventional low-IF configuration, some extra cross-branch circuitry is needed between the loop filters of the ΣΔ modulators to make the pair complex. There will be a very slight increase in power consumption associated with this but the increase is so small as to be ignored. Given the already large oversampling ratio, there should be no need to change either the clock speed or the bandwidth of the basic loop filters and hence the change in power consumption in switching from a zero IF to a low IF for the pair of ΣΔ modulators should be insignificant. As far as the digital filters are concerned, however, moving to the low-IF configuration will double the number of FIR filters required to provide the complex filtering function and hence for the same clock speed, the power consumption will typically double. This means that the power consumption for the conventional low-IF receiver, P_{nzif1}, will be approximately 50% greater than for the direct-conversion receiver, i.e.

$$P_{nzif1} = P_1 + 2 \times P_2 = P_{zif} \times 150\% \quad (6)$$

In moving to the low-IF receiver with non-complex signal processing, there is a need to double both the bandwidth of the loop filter in the ΣΔ modulator and the clock speed in order to maintain the same dynamic range in the band zero to 200 kHz. In a practical ΣΔ modulator, the power consumption and the noise output in the band of the wanted signal are dominated by the dimensions of the input stages of the loop filter and have only a weak dependency on the clock speed. If the loop filter is modified by just halving the area of the capacitors and not by any change in the size of the active devices, there should be no virtually no change in its power consumption. Hence, in needing only one instead of two modulators, there should be a saving of 50% in the power consumption figure P_1. Unfortunately, the same is not true of the power consumption of the digital filters since, despite the need for only two FIR filter blocks, doubling the clock speed doubles the number of taps required. This means the value of P_2 remains unchanged. If this analysis is valid, it can be concluded therefore, that the power consumption of the ADC function in the non-complex, low-IF receiver (P_{nzif2}) will be at least 17% higher than that for the direct-conversion receiver, but it could be of the order of 25% lower than that of the fully-complex low-IF receiver, i.e.:

$$P_{nzif2} = P_1/2 + 2 \times P_2 = P_{zif} \times 125\% = P_{nzif1} \times 83\% \quad (7)$$

This power saving should be worthwhile but remains to be fully verified in practice.

5.1 Polyphase image-rejection filter

Passive polyphase filters were studied some time ago by Gingell [7] and, as a prototype structure, take the form shown in Fig. 4. They are a cascade of RC sections each one of which is capable of creating a transmission zero at a frequency, ω_{zi}, such that $\omega_{zi} = -1/R_iC_i$. Whether the zero is at a positive or negative frequency will depend upon the relative polarities of the I and Q components of the input voltage. If each section were to be treated in isolation and driven by a pair of voltage sources, the frequency of the

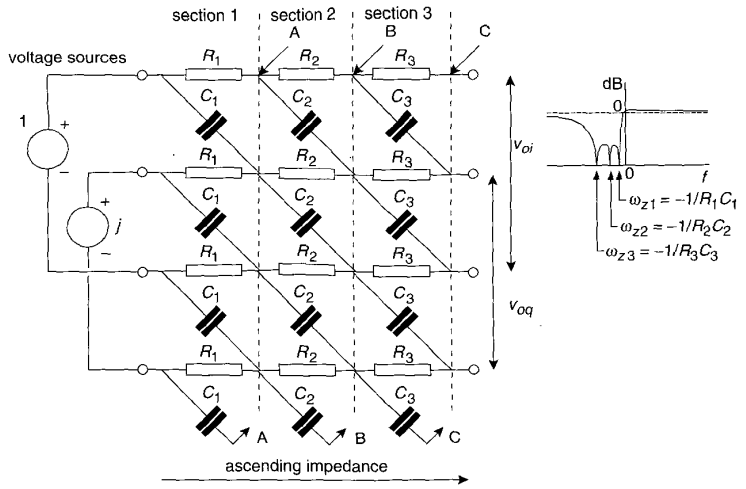

Fig. 4 *Passive polyphase filter prototype network*
$f_{z1} = -80$ kHz; $R_1 = 1$ kΩ; $C_1 = 2.0$ nF
$f_{z2} = 173$ kHz; $R_2 = 2$ kΩ; $C_2 = 0.46$ nF
$f_{z3} = -375$ kHz; $R_3 = 4$ kΩ; $C_3 = 0.11$ nF

transmission zero would uniquely define the whole of the frequency response and the impedance of the section would be of no consequence. However, because of the loading effect of each successive RC section on its preceding neighbour, the overall frequency response does become affected by the relative impedances and this substantially complicates the synthesis process. As a general rule of thumb, the impedance of the sections should increase in the direction of the output to minimise the loading effects, but it is usually necessary to adjust the impedances in a process of trial and error to achieve the most desirable frequency response. Hence, the design procedure involves choosing the transmission zeros to give the desired stopband response and the impedance levels to give the desired passband response. The desired passband response is one that is as flat as possible at positive frequencies close to zero in the region of the wanted signal.

Without the polyphase filter, the modified receiver would have no rejection in the lower adjacent channel and therefore the polyphase filter must provide all of the 18 dB required over the band −200 kHz to zero. If the problem with the lower alternate channel is to be avoided, it must also provide at least 32 dB of attenuation in the band −400 kHz to −200 kHz. This brings any interferer in the alternate channel at a relative level of +41 dB with respect to the wanted signal down to the maximum permitted level of an adjacent-channel interferer at +9 dB (Fig. 2). The remainder of the receiver selectivity can then be provided by the digital channel filters. For the purposes of designing the polyphase filter, the attenuation requirement is assumed to be at least 32 dB across both the lower adjacent and alternate channels as this carries no practical penalties and gives some useful performance margin.

To obtain the required attenuation over the approximate band −400 kHz to zero, the transmission zeros for the prototype network of Fig. 4 are set at the frequencies −80 kHz, −173 kHz and −375 kHz, whilst the corresponding resistor values are 1 kΩ, 2 kΩ and 4 kΩ. On analysis with a circuit simulator, the network produces a frequency response of the form plotted in Fig. 5 in which the stopband requirement is largely fulfilled over the band −400 kHz to 60 kHz. The response in the passband at positive frequencies between about 30 kHz and 1 MHz is also flat as required, the slight positive gain (4 dB) being a consequence of the impedance transformations in the filter and the use of ideal voltage sources. Difficulties with physical realisation and with group delay variation prevent the transmission zero at −80 kHz being moved closer to zero but the lack of rejection in this region has no significant impact on the ability of the network to reject an adjacent-channel interferer. In any case, the AC coupling elements elsewhere in the receiver chain will force a transmission zero at DC.

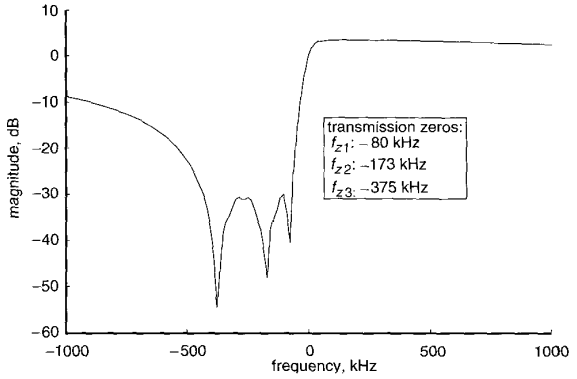

Fig. 5 *Frequency response of passive polyphase filter*

It should be noted that, in a practical implementation, the polyphase filter incorporates inter-stage buffer amplification to help reduce the loading effects of successive stages and to render the thermal noise generated by its resistors insignificant. The power consumption of the buffers is in the region of 10 mW which is a very small fraction of the total power consumption of the RF front end (typically 135 mW). In the forthcoming system simulations, the filter is modelled as a complex FIR device whose impulse responses are 500 samples in length at a sampling frequency of 26 MHz. This represents a significant computational overhead but is of no relevance to the practical implementation of the filter.

5.2 Make-complex channel filter

As previously stated, the output of the single ΣΔ modulator must be made complex once again and this is accomplished with a pair of FIR filters that perform the equivalent of a Hilbert transform [8]. A Hilbert transform of a real function in time $I(t)$ is given by:

$$Q(t) = \frac{1}{\pi} \int_{-\infty}^{\infty} \frac{I(\tau)}{t-\tau} d\tau \qquad (8)$$

where $Q(t)$ has a frequency spectrum whose amplitude components are the same as $I(t)$ but whose phase components are shifted by $-90°$ for positive frequencies and $+90°$ for negative frequencies. In the time domain, it can be interpreted as a convolution of $I(t)$ with the function $1/(\pi t)$ whose Fourier transform has a flat amplitude response over all frequencies but a phase response which has a step discontinuity between $+90°$ and $-90°$ at zero frequency. Hence the transform implements an ideal high-pass filter whose cut-off frequency is infinitesimally close to zero.

In practice, a close approximation to the transform can be implemented with a pair of filters of the form illustrated in Fig. 6. Here the FIR filter in the I signal path has a lowpass amplitude response, offering the additional benefit of some high-frequency selectivity. The FIR filter in the Q signal path has an identical amplitude response except for the presence of a hole at DC. The width of the hole is determined by the sampling rate and by the length of the impulse responses of the filters. The phase characteristic for the I component is preferably linear and has a slope determined by the delay of the filter. The phase characteristic of the Q component is identical except for the step discontinuity in the middle. Both filters must have the same delay.

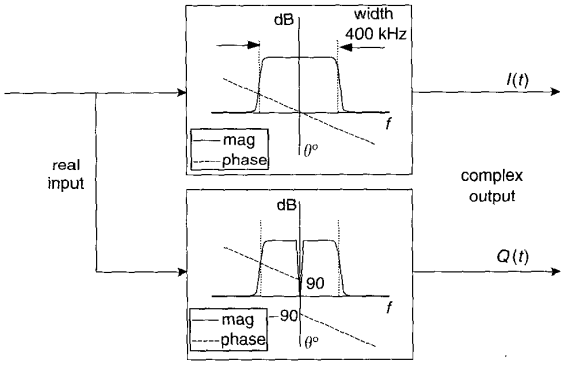

Fig. 6 *Digital make-complex and channel filter arrangement*

Whilst a suitable complex filter function can be derived by separate treatment of the two FIR components, the frequency response plotted in Fig. 7 was obtained by a slightly more direct route whereby a real, low-pass response was first synthesised with an appropriate shape and then simply translated in frequency by +100 kHz. It is then possible to calculate the two respective impulse responses for the I and Q components using an inverse, discrete Fourier transform. The delay of the filter is 18.2 μs, which is equivalent to 475 samples at a sampling frequency of 26 MHz. As shown in Fig. 7, the filter is substantially more selective than the attenuation template would suggest is necessary, but the extra selectivity and deep stopband floor are essential to attenuate the high levels of quantisation noise generated by the ΣΔ modulator.

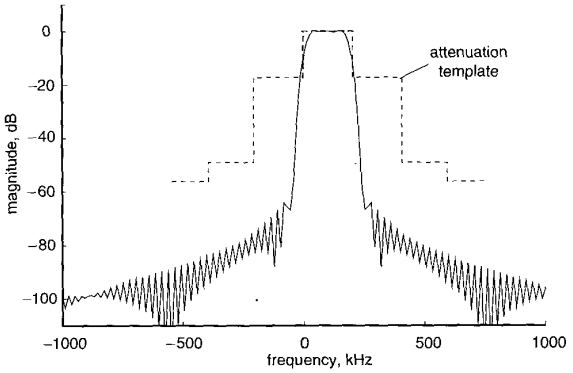

Fig. 7 *Frequency response of digital filter*
Sampling frequency, 26 MHz; no. of taps = 950; delay = 18.2 μs

5.3 ΣΔ modulator ADC

Sigma–delta modulators and their use as ADCs are discussed in some detail in [9] and [10]. As explained, they offer high conversion efficiency, excellent linearity and strong immunity to aliasing due to their high over-sampling ratio. Their basic principle of operation is illustrated by the diagram given in Fig. 8. There are three main parts to the modulator: the loop filter in the forward signal path; the

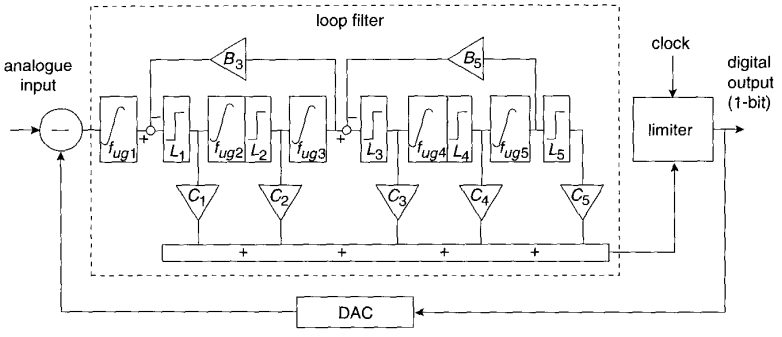

Fig. 8 *Behavioural model of fifth-order sigma–delta modulator*
Clock speed 26 MHz; poles of loop filter at 130 kHz and 210 kHz

output limiter; and the digital-to-analogue converter (DAC) in the feedback path. Signals entering the modulator are amplified by the loop filter and then quantised into a set of only two output levels (i.e. +1 and −1). The effect of the quantisation is to generate very large quantities of noise. However, by feeding the noisy output signal back into the input via the very simple DAC, the loop filter is able to alter the shape of the frequency spectrum of the noise and move most of its power to a very high frequency away from the vicinity of the wanted signal. It is then the task of the digital filter that follows to remove the quantisation noise and construct a multi-bit representation of the wanted signal with the required resolution.

The noise density at any point in the modulator output spectrum is a function of the sampling frequency and the gain of the loop filter. Hence, a high sampling frequency will reduce the noise density by spreading the noise over a wide bandwidth, whilst the high gain of the loop filter at low frequencies will give more effective cancellation and reduce the noise density in the region of the wanted signal. Typically, the loop filter comprises a cascade of integrators with unity-gain frequencies f_{ugi}. If these are realised as time-continuous circuits, the need for any anti-alias filters before the modulator can be largely avoided. In the fifth-order example shown in Fig. 8, the loop filter is of the so-called 'feedforward' type in which the outputs from all five integrators are suitably weighted by coefficients C_i before being added together at the common output. Two pairs of integrators are surrounded by feedback elements, B_3 and B_5 which generate conjugate pairs of transmission poles at ±130 kHz and ±210 kHz. The remaining integrator without feedback produces a single transmission pole at DC. Offsetting the poles in this way gives the loop filter a greater average gain over a 200 kHz bandwidth, leading to more effective noise shaping and a correspondingly lower level of in-band quantisation noise. Each integrator output passes through a clipping circuit that limits the output swing to a level of L_i. Their purpose is to help maintain loop stability under large-signal drive conditions by progressively reducing the effective loop gain. They also prevent the loop from entering a latch-up condition.

With suitable values for the set of parameters f_{ugi}, C_i, B_3, B_5 and the DAC gain, the fifth-order modulator produces an output spectrum of the form shown in Fig. 9 when its input is a pure tone of 100 kHz. In this case the tone is at the maximum permissible drive level for the modulator, which corresponds to a relative amplitude of 0.7 or a relative power level of −6 dBm. Any higher than this and the modulator becomes unstable. The clock speed is 26 MHz. As shown in the Figure, the tone is clearly present on both sides of the spectrum, as is to be expected with only the I component of the IF signal represented. The spectrum of the quantisation noise is also symmetrical about zero, the hole in the centre having a width of approximately 400 kHz. Fig. 9 also shows the spectrum of the modulator output after it has passed through the pair of digital channel filters. Not only has the pair of filters eliminated the majority of the quantisation noise, but it has also made the signal complex once more, as evidenced by the different levels of the tones now seen on either side of the spectrum. The tone on the right at +100 kHz is unchanged in magnitude but that on the left at −100 kHz has been attenuated by approximately 70 dB. This is the effective image rejection ratio of the make-complex filter function. By selective integration of the power in the spectrum, the dynamic range of the modulator and filter combination is found to be in the region of 100 dB.

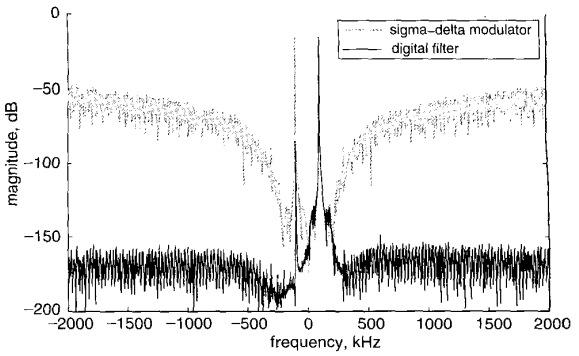

Fig. 9 *Output spectra from fifth-order sigma–delta modulator and digital filters*
Dynamic range 100 dB; sampling frequency 26 MHz; loop filter poles at 130 kHz and 210 kHz

6 System simulations

A series of system simulations have been carried out to verify the basic functionality of the modified receiver and its ability to meet the various GSM specifications. For increased confidence in the results, these simulations were carried out in two parallel exercises, one involving the coding of the various signal processing functions in FORTRAN and the other involving the use of the commercially-available software SPW [11]. The relevant system block diagram for the simulations is given in Fig. 10, the upper part of which is concerned with generating the receiver input signal, the middle part comprises the majority of the IF signal chain and the lower part deals with demodulation and equalisation. All the BER calculations are based on a comparison of physical (i.e. not coded) bits at the bit rate of 270.833 kbit/s. As shown, the receiver input comprises a wanted signal centred initially on a zero IF and an interferer shifted by an arbitrary frequency offset, both of which pass through independent, fading channels. On entry into the receiver, Gaussian noise is added at a level of −115 dBm to take account of the 6.0 dB noise figure of the front end. The whole spectrum is then translated by 100 kHz to position the wanted signal on the chosen IF.

All the filters of the receiver system are modelled as FIR devices, including the AC couplings whose cut-off frequency is 10 kHz. The gain of the amplifier shown at the input to the polyphase filter has a fixed value of 16 dB, which when the 4 dB gain of the polyphase filter and the 3 dB loss associated with dropping the Q channel are added, maps the maximum input level of a blocking signal at −23 dBm onto the −6 dBm maximum drive level of the single ΣΔ modulator.

The simulations for receiver sensitivity with a TU50 propagation channel yield the results plotted in Fig. 11. As shown, without the ΣΔ modulator present, the BER falls through a value of 8% for an input signal power of −108.5 dBm and continues to fall towards zero at an input power of −82 dBm. It remains zero for all higher input powers since without the ΣΔ modulator, the receiver is perfectly linear. With the ΣΔ modulator present, the degradation in receiver sensitivity for a BER of 8% is less than 0.5 dB, confirming that the quantisation noise power generated by the modulator must be at, or below, the intended value of −125 dBm. Hence, in terms of sensitivity, the receiver achieves its target performance of −108 dBm. At higher signal levels the ΣΔ modulator appears to cause some minor degradation in BER for input powers in the

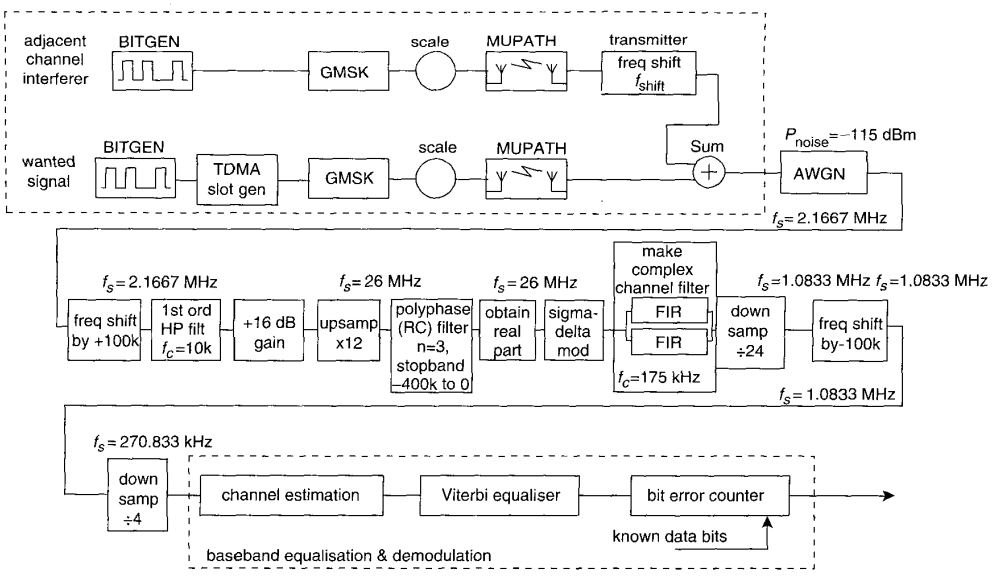

Fig. 10 *Block diagram for system simulations*

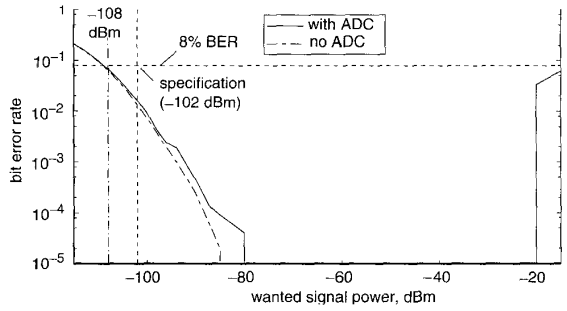

Fig. 11 *System simulations for receiver sensitivity*

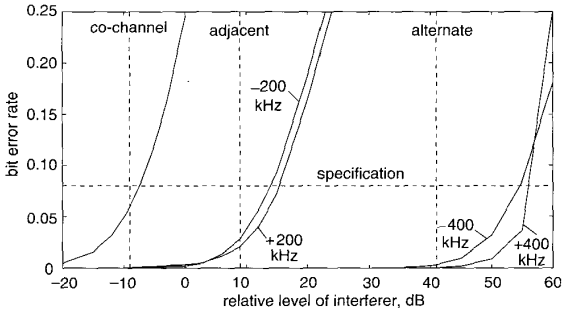

Fig. 12 *System simulations for selectivity*

region of −80 dBm. This effect is believed to be linked to the nonlinear behaviour of the channel equaliser for very low BERs, rather than just a simple loss of signal-to-noise ratio. In any case it is of little consequence. At still higher power levels the BER is substantially zero until it rises sharply at an input power of −20 dBm. The rise in BER is caused by an overdrive of the ΣΔ modulator. As the receiver must operate with a maximum input signal level of −15 dBm (static channel), this rise in BER is slightly premature. However, there is some doubt over the accuracy of the behavioural model used for the ΣΔ modulator when operating under such large-signal conditions, and results obtained in practice suggest that a real receiver is more likely to meet this particular performance requirement. If it does not, it would not be difficult to increase the dynamic range at the high end by introducing a simple one-step change in the gain of the front end.

Fig. 12 illustrates the selectivity performance of the receiver in dealing with co-channel, adjacent-channel and alternate-channel interferers. In each case, the BER for a TU50 propagation channel is plotted against the relative level of the interferer, whilst the wanted signal is held at a constant level of −82 dBm. For the co-channel interferer, the receiver passes the GSM specification by a margin of 1.5 dB, thereby confirming that the passband of the channel filters is well chosen and not unduly narrow. In the presence of the adjacent-channel interferers the receiver passes the specification by a margin of approximately 6 dB, the rejection of the interferer on the lower side being provided largely by the action of the polyphase filter and that on the upper side largely by the digital channel filters. For the alternate-channel interferers, the margin on the specification is even greater at a value of about 14 dB. This is despite the overdrive of the ΣΔ modulator that is the principal cause of the rise in BER at a relative interferer level of +55 dB.

7 Conclusions

The paper has presented a highly digitised, low-IF receiver architecture intended for use in a cellular radio application such as GSM. Its novel feature is that, by processing only the real part of the complex IF signal after the mixer, it avoids the need for a complex ADC, thereby resulting in a very much simpler and more adaptable ADC circuit design. Advancing the position of the ADC in a low-IF receiver already gives improved adaptability by moving the channel filtering into the digital domain. This overall adaptability is further improved in the proposed architecture, as well as offering the opportunity for a modest saving in power consumption. The non-complex signal processing causes an inevitable loss in image rejection but this problem is easily overcome by including a simple passive polyphase filter

before the ADC. The ADC itself is realised as a fifth-order $\Sigma\Delta$ modulator running with a clock speed of 26 MHz. Its bit-stream output is filtered extremely efficiently by a pair of digital FIR filters whose task is also to reconstruct the Q component of the complex baseband signal. System simulations demonstrate the effectiveness of the overall signal processing strategy and confirm that the level of performance needed to realise a competitive GSM product can be readily achieved.

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