An Evolved EDGE PHY ASIC Supporting Soft-Output Equalization and Rx Diversity

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***Abstract*—In this paper the first complete Evolved EDGE transceiver physical layer ASIC supporting receive diversity and soft-output Viterbi equalization is presented. It comprises transmitter and receiver with detector and a decoder with an autonomous incremental redundancy implementation. The ASIC reaches a measured sensitivity of -111.8 dBm for single antenna GSM voice channels and achieves the reference interference performance for adjacent channels 12 dB above 3GPP requirements. It occupies 6 mm^2 in 130 nm CMOS with a power consumption between 5 and 39 mW.**

I. Introduction

In multi-standard, LTE-enabled mobile platforms being fitted into the latest smart phones today the fallback solution outside major cities is still mostly provided by the EDGE mode, where the contrast in throughput between 100 Mb/s for LTE and 236 kb/s for EDGE is drastic in terms of user experience and service quality. Thus, improving the bottom-end of the data rate is as important as pushing the maximum further towards the Gb/s level. With potential throughput up to 1.2 Mb/s Evolved EDGE (E-EDGE) is such a standard, that fits well with LTE-enabled devices where a second antenna is already mandatory, so that E-EDGE can also freely take advantage of dual carrier or receive diversity to optimize throughput under interference dominated radio conditions. The interference suppression capability offered by receive diversity, in particular, also gives operators more flexibility to achieve a frequency re-use factor close to one, thus improving throughput and network coverage. Due to the ubiquitous coverage, such 2.75G networks, beyond providing a fallback solution for the latest smart phones, also play a key role for emerging low-bandwidth applications, such as machine-to-machine (M2M) communication or the internet of things (IoT).

However, interference cancellation and equalization algorithms for E-EDGE with Rx-diversity are prohibitively complex when implemented on dedicated DSPs, even though with the use of software-defined-radio (SDR) building-blocks they are said to be easily realizable on them in software today. However, no physical layer (PHY) has been realized to date.

Building on the first single-antenna E-EDGE receiver ASIC we presented recently [1], this contribution reports a complete PHY ASIC supporting additionally Rx-diversity, interference cancellation, soft-output Viterbi equalization (SOVE) and fully autonomous incremental redundancy (IR), as well as the necessary uplink functions of encoding, puncturing, interleaving and mapping in order to pass the correct symbols to the RF transmitter. The ASIC supports dual transfer mode (DTM), circuit- and packet-switched control- and traffic-channels up to multi-slot class 45 and 32 temporary block flows (TBFs), both the highest specified by 3GPP.

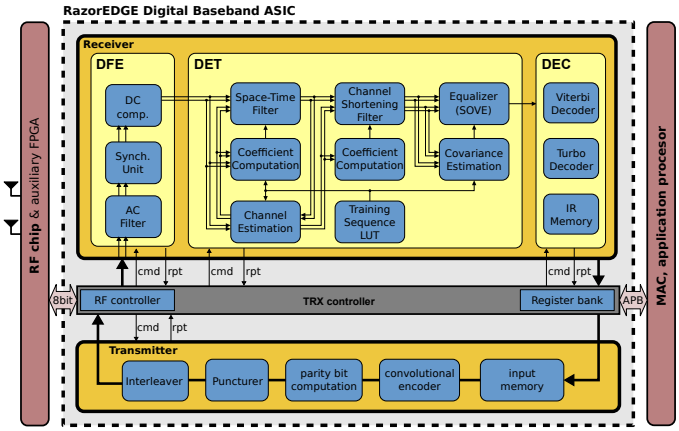

Fig. 1. Block diagram of RazorEDGE PHY with Receiver, Transmitter, TRX controller and configuration registers as well as attached system components.

II. PHY Architecture

Fig. 1 shows the top-level block diagram of the PHY ASIC, which includes: TRX controller, Receiver and Transmitter. The TRX controller is the top-level controller which holds the GSM PHY finite state machine and maintains the time base. Hence, no real-time awareness is required of the application processor interacting with the PHY, facilitating system integration. The core logic is also clocked independently from the interfaces to the application processor and RFIC. Besides the RF controller, it contains a register bank, whose registers are used to control the PHY ASIC and to read and write payload data of e.g, MAC blocks. The receiver is designed to have the digital front-end (DFE) operate symbol-wise, the detector (DET) burst-wise, and the decoder (DEC) radio-block-wise. This partitioning allows local data buffers to be deployed with minimum size along the RX chain instead of a global shared memory bank with complex access schedules which often forms the power and area bottleneck.

In the DFE signal processing tasks are performed on raw samples, such as sampling-rate conversion, synchronization

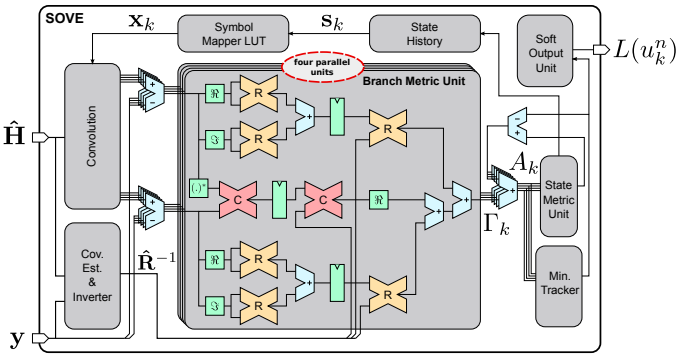

Fig. 2. Block diagram of soft-output Viterbi equalizer with four parallel branch metric units.

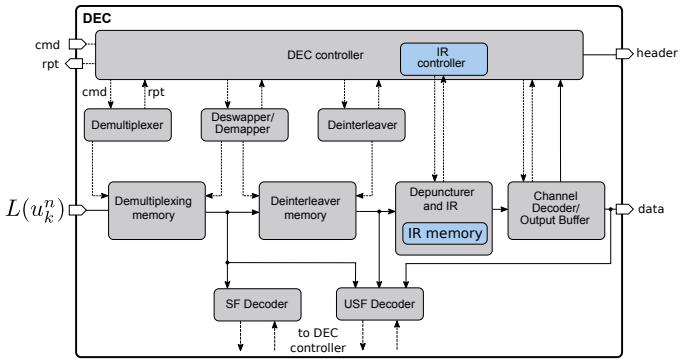

Fig. 3. Block diagram of decoder and incremental redundancy unit. The red arrows indicate the data flow, the blue arrows control signals.

in frequency and time, including frequency burst-detection and frequency offset estimation, as well as blind DC-offset compensation. It contains an adjustable decimation filter which can be adjusted by the TRX controller according to adjacent channel strength.

The DET performs the most complex signal processing tasks for symbol detection and interference cancellation across all modulation types. The support for RX-diversity increases performance, but requires computationally intensive signal processing algorithms to achieve the EGPRS-2A DARP II performance requirements [2]. On the one hand, co- and adjacent-channel interference must be mitigated using space-time processing. On the other hand, soft output ISI equalization based on trellis processing is required. Even though the latest GOps DSPs are capable of handling at its limits the vast number of complex additions and multiplications required for the interference cancellation and equalization of a 32-QAM burst affected by ISI over 7 symbols, as specified for GSM/EDGE, considerable area and power consumption is expected [3]. The core part of DET is therefore a hardwired arrangement of interference-canceller, channel-shortener and Viterbi equalizer. Interference is suppressed effectively by a space-time filter with coefficients derived in the MMSE-sense [4]. A structure consisting of four 5-tap FIR filters is used to suppress co- and adjacent-channel interference. The filter coefficients are derived by comparing the received training sequence and the actual training sequence convoluted with the channel estimate, as described in [4]. For the MMSE coefficient calculation, a dedicated application specific processor with a very reduced instruction set is employed. The actual filtering is done with four FIR filters, each consisting of a complex-valued multiply-accumulate unit.

Symbol detection is realized by a reduced-state soft output Viterbi equalizer in combination with the channel-shortening approach we proposed recently [5], where the coefficients are calculated in the cepstrum domain. Compared to our previous solution [1] based on hard-decisions, a 4 dB performance improvement is achievable by providing reliability information to the channel decoder. Traditional soft-output algorithms for trellis-based equalization, such as BCJR or its Max-Log approximation suffer from large memory requirements because a forward and a backward recursion through the trellis is performed. In this implementation we adopt an efficient SOVE architecture, where the backward recursion has been omitted [6]. Besides highly reduced complexity, a further advantage of omitting the backward recursion is that the demodulated symbols are forwarded to the channel decoder with less latency. This approach reduces complexity and still achieves close-to-optimal performance. Thanks to the minimum-phase property of the overall channel achieved by the shortening filter, only 32 trellis states are sufficient for the equalization of 32-QAM symbols.

III. SOVE Architecture

A block diagram of our SOVE architecture is shown in Fig. 2. It takes the estimated channel impulse response matrix $\hat{\mathbf{H}}$ and the received symbols $\mathbf{y}$ as input and delivers reliability information $L(u_k^n)$ as output. The matrix $\mathbf{y}$ contains the received samples from both Rx-streams arranged in two rows. Hereby, u_k^n is the transmitted bit sequence of a symbol with time index k and bit index n within the symbol. The soft values $L(u_k^n)$ are computed from the state metrics A_{k-1}^i and the branch metrics Γ_k^i according to [6] as shown in (1). D is the decision delay, which is an important design parameter for the SOVE, since it determines the number of trellis states for a given modulation order M by M^D.

$$\begin{aligned} L(u_{k-D}^n) &= \log \frac{p(u_{k-D}^n = 0|\mathbf{y})}{p(u_{k-D}^n = 1|\mathbf{y})} \\ &\approx \min_{i,u_{k-D}^n=1} \left(A_{k-1}^i - \Gamma_k^i\right) + \min_{i,u_{k-D}^n=0} \left(A_{k-1}^i + \Gamma_k^i\right) \end{aligned} \tag{1}$$

The approximation in (1) is a result of the max-log approximation of the SOVE algorithm and of neglecting the backward recursion. In the state metric unit the branch metrics Γ_k^i are added to the previous state metrics A_{k-1}^i and all new state metrics A_k^j are determined by selecting the most probable branch merging into the current state j as shown in (2).

$$A_k^j = \min_i \left(A_{k-1}^i + \Gamma_k^i\right) \tag{2}$$

Hereby, the branch metrics (3) are computed from the estimated inverse spatial covariance $\hat{\mathbf{R}}^{-1}$ of the received signal and the difference $\mathbf{d}_k$ between the received signal $\mathbf{y}_k$ and the convolution of the test symbols $\mathbf{x}_k$ with the estimated channel impulse responses in $\hat{\mathbf{H}}$. Since the spatial covariance has real-valued diagonal elements r_{11} and r_{22} as well as complex conjugated off-diagonal elements $r_{12} = r_{21}^*$, the branch metric

computation can be further simplified (cf. (3) and Fig. 2).

$$\begin{aligned}\Gamma_k^i &= \left(\mathbf{y}_k - \hat{\mathbf{H}}\mathbf{x}_k\right)^H \hat{\mathbf{R}}^{-1}\left(\mathbf{y}_k - \hat{\mathbf{H}}\mathbf{x}_k\right) = \mathbf{d}_k^H \hat{\mathbf{R}}^{-1}\mathbf{d}_k \\ &= |d_{1,k}|^2 r_{11} + |d_{2,k}|^2 r_{22} + 2\Re(d_{1,k}^* d_{2,k} r_{12}) \qquad (3)\end{aligned}$$

The test symbols $\mathbf{x}_k$ are determined by the specific branch and state, where each state has its own list of decision feedback symbols.

The branch metric unit is the block with the highest computational complexity in the equalizer. In order to achieve the required throughput for the 32 QAM case at a clock frequency of 100 MHz, 4 parallel branch metric units, each containing 14 real-value multipliers are deployed. In this setup, the processing of all branches for one trellis state takes only 8 clock cycles. While the branch metric unit computes the state metric of one trellis state, convolution of $\hat{\mathbf{H}}$ with the test symbols $\mathbf{x}_k$ of another state is performed, in order to ensure efficient hardware utilization. The inversion of the spatial covariance is computed using a divider-free approximation.

The test symbols $\mathbf{x}_k$ are obtained with a LUT from the hard-decision (binary) entries $\mathbf{s}_k$ obtained from the state history unit as shown in Fig. 2. A vector $\mathbf{s}_k$ is composed of the two symbols corresponding to the current trellis state and branch and the history of 6 decision feedback symbols for a channel length of 8 symbols. The state history is stored in a 32x20 bit RAM.

The dynamic range of the state metrics is kept small by subtracting the minimum state metric at every trellis stage. Furthermore, all winning state metrics are forwarded to the soft-output unit, where metrics corresponding to different hypotheses for all modulated bits are compared to obtain their respective log-likelihood ratios as shown in (1).

IV. Decoder and Incremental Redundancy Unit

The decoder block of the transceiver is depicted in Fig. 3. It consists of a controller and the necessary units for decoding, depuncturing, deinterleaving and demultiplexing of MAC data blocks and a fully autonomous IR implementation. With IR, which aims at achieving a higher throughput, if decoding of a received block fails, the mobile station stores the soft values of the data block and requests a re-transmission from the base-station. Due to our dedicated hardware IR implementation the PHY ASIC is capable of doing the entire IR processing, whereas the software running the MAC layer does not need to be aware of IR processing anymore. No additional resources of the processor running the MAC layer will be occupied.

The IR controller initiates and controls the necessary operations according to the parameters extracted from the header field of a block, such as block sequence number and modulation and coding scheme. To ease memory access and control, fragmented memories were employed. We use a demultiplexing memory, a deinterleaver memory and an IR memory to store the blocks of previous transmissions as shown in Fig. 3. The dedicated IR implementation uses 50 kGE and a total memory size of 183 kbit and complies with the 3GPP throughput requirements.

The channel decoder itself comprises a 64 state Viterbi decoder and a 3GPP turbo decoder [7]. This flexible solution allows efficient Viterbi/turbo decoding for a variable number of trellis states, code rates and code-block lengths.

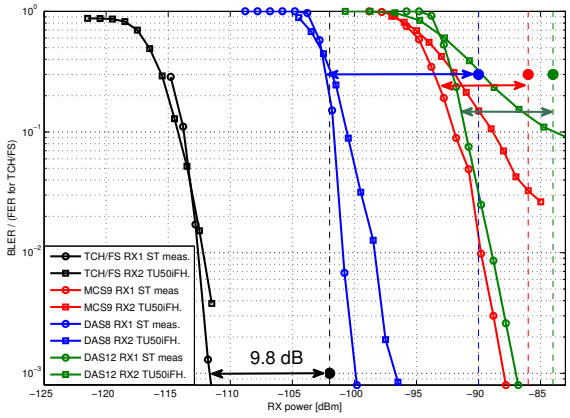

Fig. 4. Measured and simulated BLER performance, single antenna for static (ST) and RX-diversity for typical urban (TU50) channel profile.

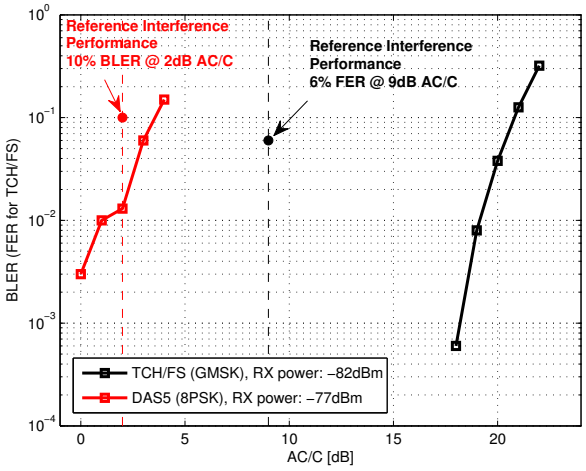

Fig. 5. Measured performance as a function of the adjacent channel power over desired channel power ratio (AC/C).

V. Testbed, Performance and Power Consumption

As part of a complete E-EDGE solution the ASIC was connected to an RF subsystem based on one of our RF-transceivers [8] and verified in a real-time testbed as shown in Fig. 6. The testbed comprises a PowerPC on a Virtex4 FPGA acting as application processor connected via Ethernet/SSH to a host PC. The PHY interface has been simplified that the communication to the application processor only requires a minimum of basic PHY commands. For the downlink performance evaluation either over-the-air signals are captured or sample data from R&S measurement equipment is used.

Simulated and measured frame erasure rate (FER) for voice channel (TCH/FS) and block-error rate (BLER) performance for EGPRS (MCS9) and EGPRS2 (DAS8, DAS12) modes have been assessed for sensitivity and interference scenarios. The sensitivity performance plots for single antenna on the static channel (ST) profile and RX-diversity on the TU50 channel

profile are shown in Fig. 4. The performance requirements of 0.1% FER, 10% and 30% BLER, respectively, are fulfilled for all modes and indeed exceeded by a large margin in most cases. The margin for the voice case, for example, is close to 10 dB even in the single antenna measurement, which corresponds to the best reported sensitivity of any GSM receiver to date. From Fig. 4 it can also be seen that the use of RX-diversity achieves nearly the same performance in a TU50 channel profile as the single antenna receiver for the static channel. In addition to the sensitivity performance, the adjacent channel interference performance has been measured for TCH/FS and DAS5 as shown in Fig. 5. Thanks to the interference cancellation combined with the SOVE, more than 10 dB margin has been achieved for GMSK and 2.5 dB for DAS5 mode despite the challenge of additional ISI caused by channel filtering. Table I summarizes the performance results compared to state-of-the-art GSM/EDGE transceivers [9], [10].

The power consumption for the highest throughput EGPRS2-A mode with different time slot configurations has been measured. The highest clock frequency (104 MHz) is required when the specified maximum of 6 time slots are used or when RX-diversity is enabled. In these modes, timing margins still allow voltage to be scaled to push the power consumption from 56 mW to 39 mW (-30%) and from 41 mW to 26 mW (-36%) with and without Rx-diversity, respectively. For configurations with less than 6 timeslots both voltage and frequency scaling can be applied, leading to 5 mW for processing a single 32QAM EGPRS2-A time slot.

TABLE I. RAZOREDGE PERFORMANCE RESULTS

	3GPP	[9]	[10]	This work
Sensitivity Performance [dBm] Measurement, Static ch. profile				
TCH/FS (GMSK)	-102	-110.1	-111.3	**-111.8**
MCS9 (8PSK)	-86	N/A	N/A	**-93.6**
DAS8 (16QAM)	-90	N/A	N/A	**-101**
DAS12 (32QAM)	-84	N/A	N/A	**-92.7**
RX-diversity sensitivity performance [dBm] Simulation Ant. Corr. = 0, AGI = 0, DARP II, TU50nFH ch. profile, ** = 30% BLER				
TCH/FS (GMSK)	-105	N/A	N/A	**-111**
MCS9 (8PSK)	-89**	N/A	N/A	**-92****
DAS8 (16QAM)	[t.b.d.]	N/A	N/A	**-102****
DAS12 (32QAM)	[t.b.d.]	N/A	N/A	**-90****
Interference performance [dB] Measurement 6% FER, adjacent ch. above desired signal level (-82 dBm), TU50nFH ch. profile				
TCH/FS (GMSK)	9	N/A	N/A	**21**

VI. CONCLUSION

The reported ASIC is the first 32-QAM capable Evolved EDGE PHY with downlink diversity. Thanks to sophisticated signal processing in all modes, it meets the standard requirements with significant margin in all modes. Specifically, it achieves the best GSM voice sensitivity in standard single antenna mode, when combined with an RF subsystem complete with antenna switches, receive SAW filters and the RFIC. At the same time, the dedicated hardware implementation maintains extremely low power consumption, fitting into a die area of 6 mm^2 in 130 nm SMIC. The die micrograph is shown in Fig. 6 and the main chip characteristics are summarized in Table II.

TABLE II. PHYSICAL CHARACTERISTICS

Technology / Package	SMIC 130 (0.13μm CMOS) / QFN56
Core size	6mm^2 ($6002500\mu\text{m}^2$)
Gate count	800 kGE
RAM size	400 kbit
Supply voltage V_{DD}	1.2 V
Core operating frequency: f_{C}	104 MHz

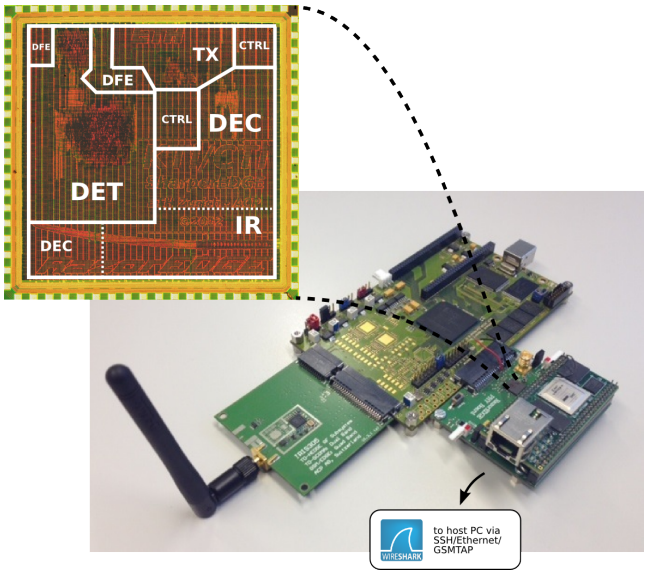

Fig. 6. Testbed and die micrograph of the RazorEDGE ASIC for the single antenna case.

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