A Multicarrier GMSK Modulator

Jouko Vankka, *Student Member, IEEE*, Mauri Honkanen, and Kari A. I. Halonen

***Abstract*—A multicarrier Gaussian minimum shift keying (GMSK) modulator has been developed and implemented. The design contains four GMSK modulators, which generate GMSK modulated carriers at the specified center frequencies. Utilization of the redundancy in the stored waveforms reduces the size of the GMSK trajectory look-up table to less than one-quarter of the original size in the modulator. Conventionally, the power ramping and output power level controlling are performed in the analog domain. A novel digital ramp generator and output power level controller perform both the burst ramping and the dynamic power control in the digital domain. The power control is realized by scaling the ramp curve, which follows a raised cosine/sine curve. The four GMSK modulated signals are combined together in the digital domain. The digital multicarrier GMSK modulator is designed to fulfill the spectrum and phase error specifications of the GSM 900 and DCS 1800 base stations.**

***Index Terms*—Direct digital synthesizer, GMSK modulator, multicarrier, power control.**

I. Introduction

IN CONVENTIONAL base station solutions, the transmitted carriers are combined after the power amplifier (PA) as shown in Fig. 1. This paper describes an architecture, where a multicarrier GMSK modulated IF signal is upconverted to RF by two mixers and bandpass filters (BPFs) as shown in Fig. 2. This saves a huge number of analog components, many of which require production tuning. Consequently, an expensive and tedious part of the manufacturing will be eliminated. The proposed multicarrier GMSK modulator does not use an analog I/Q modulator; therefore, the difficulties of adjusting the dc offset, the phasing, and the amplitude levels between the in-phase and quadrature phase signal paths are avoided. A single linearized multicarrier power amplifier replaces a bank of individual amplifiers whose high-power outputs are conventionally combined by using selective cavities. Hence, power losses inherent to cavity-filter combiners are avoided which results in space and cost savings as well as greater reliability. The GMSK modulation method used in the GSM 900 and DCS 1800 is a constant envelope modulation scheme. As a number of these GMSK carriers are combined to produce a multicarrier signal, the beneficial properties are lost. Because of the strongly varying envelope of the composite signal, very stringent linearity requirements are imposed on the wide-band D/A converter, upconversion mixers, and the PA.

This paper only concentrates on the parameters of the digital multicarrier GMSK modulator, which generates the IF signal in

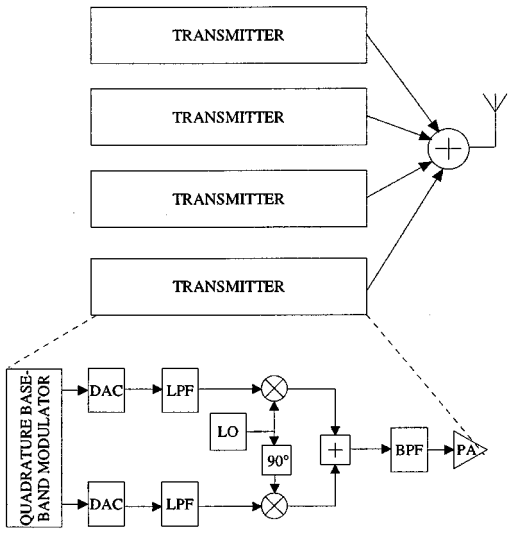

Fig. 1. Conventional multicarrier transmitter in the base station.

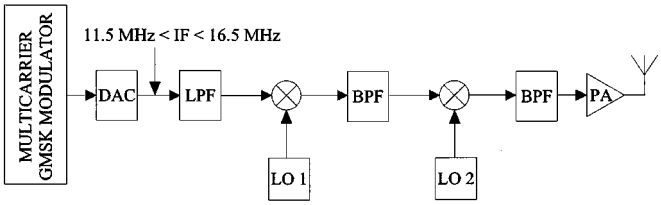

Fig. 2. Multicarrier GMSK modulator and upconversion chain.

Fig. 2. The block diagram of the multicarrier GMSK modulator is shown in Fig. 3. The analysis of spurs, harmonics, and noise from the filters, mixers, and PA is left out of the scope of this paper.

II. GMSK Modulator

The interface FPGA in Fig. 3 extracts data bits, power level indications, frequency control words, initialization, and control data from the base station backend. The FPGA feeds necessary data and control bits to the multicarrier GMSK modulator. The block diagram of the GMSK-modulator is shown in Fig. 4. The system consists of a shift register, counter, frequency trajectory look-up table (LUT), adder/subtracter, phase accumulator, carrier frequency register, phase-to-amplitude converter (conventionally a sine ROM), and D/A-converter. The use of the LUT as a digital filter has been described in [1] and [2]. Incoming data symbols to the Gaussian low-pass filter [3] are stored in the shift register (see Fig. 4). The LUT generates a frequency path with intersymbol interference over $(w-1)T$ [1], where T is the symbol duration, and w is the number of the symbol stages in the shift register in Fig. 4. The simulation shows that in order to meet modulation spectrum requirements, the number

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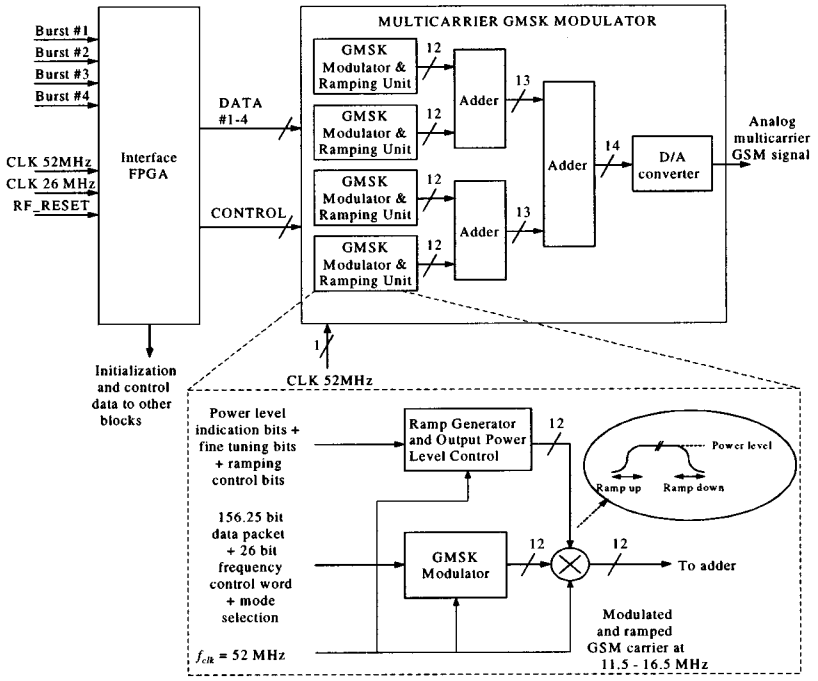


Fig. 3. Multicarrier GMSK modulator.

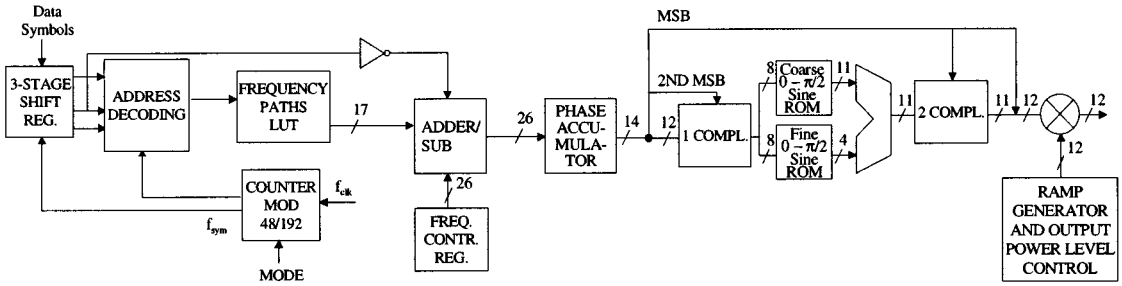


Fig. 4. Details of the single GMSK modulator and ramping unit in the multicarrier GMSK modulator (Fig. 3).

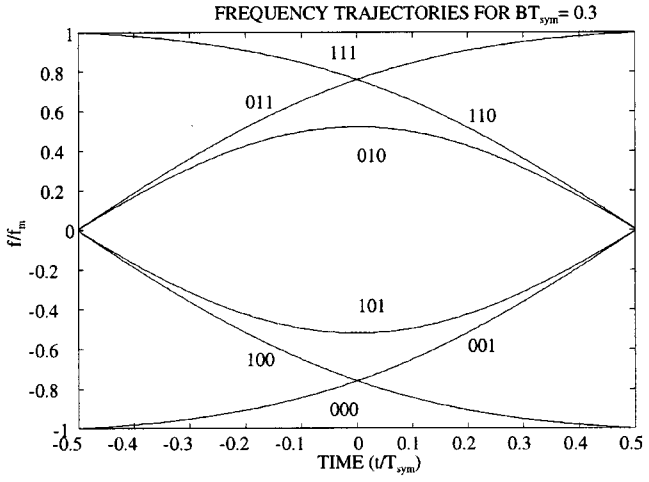


Fig. 5. Frequency trajectories for $BT = 0.3$.

of the symbol stages in the shift register should be three (see Table II). Therefore, we limit the pulse response to only the two nearest neighbors in Fig. 5. As the pulses can have one of two possible values (0 or 1), we can have $2^3 = 8$ possible curves. The frequency trajectories for $BT = 0.3$, where B is the 3-dB bandwidth, are shown in Fig. 5. Other frequency trajectories can be obtained from [000, 001, 101, 100] by sign changes. The frequency trajectory LUT takes the advantage of this symmetry in Fig. 4. The absolute values of the GMSK frequency trajectories are saved in the frequency path LUT. If the second bit is inverted, it can be used as a sign bit, as shown in Fig. 5. Therefore, there is no need to save the sign bits in the LUT (see Fig. 4). The frequency trajectories are symmetric around the time axes in Fig. 5. The frequency trajectory is constant when the address of the frequency trajectory LUT is [000] or [111]. The required LUT size is reduced to less than one-quarter of the original size (1 : 5.3) by eliminating the redundant data. Of course, the complexity of the address decoder has increased, but the decrease of the LUT size compensates more than enough.

The number of samples per symbol is 192 (see Section IV). The burst length is 156.25 bits in GSM 900 and DCS 1800 systems [4]. One-quarter of a guard bit ($=0.25 \times 192 = 48$ samples) is inserted after each burst after the eight guard bit ones [4]. Therefore, the counter has 48/192 modes in Fig. 4.

The output of the adder/subtracter is $N_n = (C_n \pm L_n)$, where C_n is the carrier frequency ($\pm$ carrier offset) control word, L_n is the frequency modulation control word (the LUT output), N_n is the input to the phase accumulator, with n being the time index.

The phase value of the phase accumulator is $P_n = (N_n + P_{n-1})$ mod 2^j, where j is the phase accumulator width. The phase accumulator acts as a digital integrator followed by a modulo 2^j operator. The output frequency is

$$f_{\text{out}} = \frac{\Delta P_n}{\Delta T} = \frac{N_n f_{\text{clk}}}{2^j} \tag{1}$$

where f_{clk} is the clock frequency. The input to the phase accumulator, N_n, can only have integer values, therefore the frequency resolution is found setting $N_n = 1$

$$\Delta f = \frac{f_{\text{clk}}}{2^j}. \tag{2}$$

The phase accumulator addresses the sine read only memory (ROM), which converts the phase information into the values of a sine wave. A straightforward implementation of the sine memory requires a $2^{14} \times 12$ b ROM. Therefore, a sine memory compression technique is applied to reduce the size and access time of the sine ROM [5]. This DDS architecture takes advantage of the symmetry of a sine wave to reduce ROM storage requirements. One only needs to store sine samples from 0 to $\pi/2$, as shown in Fig. 4. The coarse sine ROM provides low resolution samples, and the fine sine ROM gives additional resolution by interpolating between the low resolution samples in Fig. 4. The $2^{14} \times 12$ sine samples are compressed into $2^8 \times 11$ coarse samples and $2^8 \times 4$ fine samples, resulting in a compression ratio of 51 : 1. An FFT of the compressed ROM contents gives a worst case digital output spectral purity of -87 dBc. The multiplier controls the envelope of the digital GMSK modulated IF signal in Fig. 4. The four GMSK modulated signals are combined together in the digital domain as shown in Fig. 3. Next, the signal is presented to the D/A converter, which develops an analog signal.

III. Ramp Generator and Output Power Level Controller

A. Conventional Solutions

Multicarrier transmission with digital carrier combining necessitates power control to be implemented in the digital domain. Otherwise, it would not be possible to adjust the relative power of a single carrier with respect to the others. Therefore, a digital ramp generator and output power level controller is proposed in Fig. 4.

The conventional ramp generator and output power level controller is based on the look-up table (LUT). The size of the LUT is about $(f_{\text{clk}} \times T_r) \times \text{out}w$, where f_{clk} is the digital IF modulator clock frequency (sampling frequency), T_r is the pulse duration, and $\text{out}w$ is the raised cosine LUT output width. The clock frequency is high in the digital IF modulators; therefore, the size of the LUT is large. For example, if the clock frequency is 52 MHz and the ramp duration is 14 μs, as shown in Table I, then the size of the LUT will be about 728 $\times$ 12 bits. Furthermore, the multiplier is needed to set the output power level.

Another conventional method for implementing the ramp generator and output power controller is to use an FIR-filter. The number of FIR filter taps is $(f_{\text{clk}} \times T_r)$, where f_{clk} is the digital IF modulator clock frequency and T_r is the pulse duration. Due to the high clock frequency in the IF modulators, there are many taps in the FIR. For example, if the clock frequency is 52 MHz and the ramp duration is 14 μs, as shown in Table I, then the number of the FIR filter taps will be 728. Multistage implementations may reduce the number of the taps somewhat.

TABLE I
ASSUMED MULTICARRIER GMSK MODULATOR SPECIFICATIONS

Symbol rate	270.833 Kbit/s
Frequency error	2 Hz
Hopping bandwidth	5 MHz
Output Bandwidth	11.5 – 16.5 MHz
Hopping Frequency	1.733 kHz (GSM burst-by-burst)
System Clock Frequency	52 MHz
Number of Carriers	Four
Carrier Spacing	200 kHz
Modulation	GMSK with BT = 0.3
Phase error rms	1.5°
Phase error peak	2.5°
Spurious Free Dynamic Range	76 dB
Ramp-up time	14 µs
Ramp-down time	14 µs
Ramp curve type	Raised cosine/sine
Output word length	12 bits
Power control range	0...-32 dB
Power control step	2 dB
Power control fine tuning step	0.25 dB

B. Novel Ramp Generator and Output Power Level Controller

The downlink dynamic power control in the GSM 900/DCS 1800 uses 16 power levels with 2-dB separation. The power control range of the proposed design is $0 \cdots -32$ dB, where the 0-dB level is the nominal maximum power. The additional 2-dB range is introduced to assist the gain stabilization of the transmitter analog parts. Furthermore, a power control fine tuning step (0.25 dB) is introduced for this purpose (see Table I). The power level can be changed burst by burst. The digital GMSK modulated IF signal is multiplied by the ramp signal for a smooth rise and fall of the burst in Fig. 4. The power control is realized by scaling the ramp curve, which follows a raised cosine/sine curve. Hence, the ramp-up curve starts from the minimum power level but settles to the level specified by the power level indication as shown in Fig. 6.

The burst signal can be considered to be a product of an original modulated signal $m(t)$ and a periodical switching signal $sw(t)$. The spectrum of the burst signal is the square of the absolute value of convolution of these two signals in the frequency domain.

For rectangular switching, we get

$$\begin{aligned} W(f) &= |M(f - f_c) * SW(f)|^2 \\ &= K \left| \sum_{n=-\infty}^{\infty} M(f - f_c - nf_g) \frac{\sin \pi n f_g T_b}{\pi n f_g T_b} \right|^2 \end{aligned} \tag{3}$$

where

$*$ convolution;
f_c carrier frequency;
f_g burst gating rate;

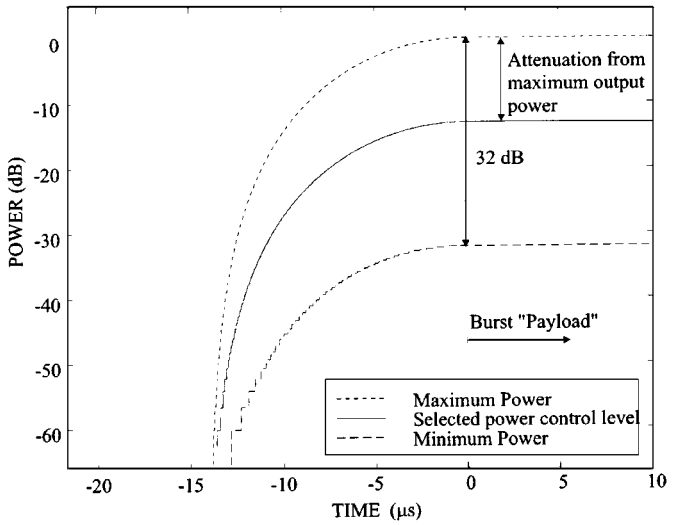


Fig. 6. Power control feature combined to the power ramping.

T_b burst length;
K proportional constant.

For raised cosine/sine switching, we get

$$W(f) = L\left|\sum_{n=-\infty}^{\infty} M(f - f_c - nf_g) \cdot \frac{\sin \pi n f_g (T_b - T_r)}{\pi n f_g (T_b - T_r)} \frac{\cos \pi T_r n f_g}{1 - (2T_r n f_g)^2}\right|^2 \quad (4)$$

where T_r is the ramp duration, and L is a proportional constant.

The spectrum of the periodic burst signal consists of infinite numbers of secondary spectral lobes which have the same shape as $M(f)$, separated by the burst gating rate f_g, and have decreasing amplitudes. The secondary spectral lobes decay faster in (4) than in (3), and for this reason the raised cosine/sine switching is used. The following function is used to smooth out the rise of the burst:

$$(A - dc)\sin(\frac{\pi t}{2T_r})^2 + dc = \frac{1}{2}\left((A + dc) + (A - dc)\cos(\frac{\pi t}{T_r} + \pi)\right) \quad (5)$$

where

T_r ramp duration;
t [0 T_r];
A envelope of the GMSK-modulated signal;
dc dc offset (determines the starting power level).

On the right side of the above equation, the cosine/sine term is not raised, and so it could be implemented by a sinusoidal oscillator. The following function is used to smooth out the fall of the burst:

$$(A - dc)\cos(\frac{\pi t}{2T_r})^2 + dc = \frac{1}{2}\left((A + dc) + (A - dc)\cos(\frac{\pi t}{T_r})\right) \quad (6)$$

where dc is the dc offset (sets the power level after the ramp).

The novel ramp generator and output power level controller is shown in Fig. 7(a). The core of this structure is a well-known second-order direct-form feedback structure. The constant $(A+dc)$ in (5) and (6) is added to the sinusoidal oscillator output. The amplitude of the cosine term is $(A-dc)$ from (5) and (6). The binary shift (2^{-1}) is implemented with wiring. During the ramp period, the signal sel is low in Fig. 7(a), and the multiplexer conducts the ramp signal to the multiplier (Fig. 4). After the ramp duration (T_r) the signal sel becomes high; and the output of the multiplexer is connected to the input of the multiplexer, and the output power level is constant. The cosine term is implemented by the second-order difference equation in Fig. 7(a) [6]. Fig. 7(a) shows the signal flow graph of the second-order direct-form feedback structure with state variables $x_1(n)$ and $x_2(n)$. The corresponding difference equation for this system is given by

$$x_2(n+2) = \alpha x_2(n+1) - x_2(n). \quad (7)$$

The two state variables are related by $x_1(n) = x_2(n+1)$. Solving the one-sided z transform of (7) for $x_2(n)$ leads to

$$X_2(z) = \frac{(z^2 - \alpha z)x_2(0) + z x_1(0)}{z^2 - \alpha z + 1} \quad (8)$$

where $x_1(0)$ and $x_2(0)$ are the initial values of the state variables. Identifying the second state variable as output variable $y(n) = x_2(n)$, as shown in Fig. 7(a), and choosing the denominator coefficient α to be $\alpha = 2\cos\theta_0$ and $\theta_0 = \omega_0 T = 2\pi f_0 / f_{\text{clk}}$, with f_0 being the oscillator frequency, and f_{clk} being the sampling frequency, then choosing the initial values of the state variables to be $x_1(0) = A'\cos\theta_0$ and $x_2(0) = A'$, we obtain from (8) a discrete-time sinusoidal function as the output signal

$$Y(z) = \frac{A'(z^2 - \cos\theta_0 z)}{z^2 - 2\cos\theta_0 z + 1}. \quad (9)$$

The equation has complex-conjugate poles at

$$z = \exp(\pm j\theta_0) \quad (10)$$

and a unit sample response

$$y(n) = A'\cos(n\theta_0), \qquad n \geq 0. \quad (11)$$

Thus, the impulse response of the second-order system with complex-conjugate poles on the unit circle is a sinusoidal waveform.

An arbitrary initial phase offset φ_0 can be realized [7], namely,

$$y(n) = A'\cos(\theta_0 n + \varphi_0) \quad (12)$$

by choosing the initial values

$$x_1(0) = A'\cos(\theta_0 + \varphi_0) \quad (13)$$
$$x_2(0) = A'\cos(\varphi_0). \quad (14)$$

Thus, any real-valued sinusoidal oscillator signal can be generated by the second-order structure shown in Fig. 7(a). The digital oscillator amplitude (A') is $(A - dc)$ from (5) and (6). The initial phase offsets of the digital oscillator are 0 for the ramp down

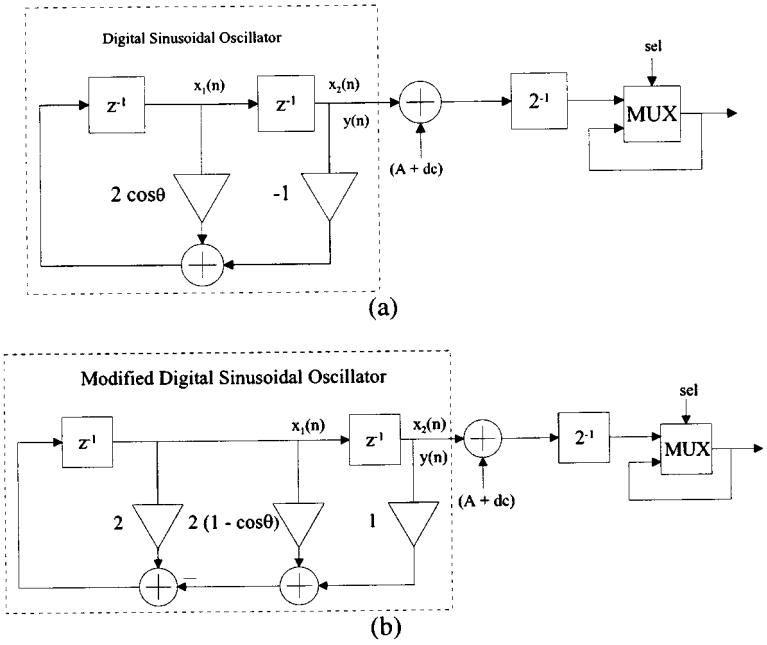


Fig. 7. (a) Ramp generator and output power level controller. (b) Modified [see (15)].

and π for the ramp up, from (5) and (6). Hence, for the falling ramp ($\varphi_0 = 0$), the initial values are $x_1(0) = (A - dc)\cos(\theta_0)$ and $x_2(0) = (A - dc)$. For the rising ramp ($\varphi_0 = \pi$) $x_1(0) = -(A - dc)\cos(\theta_0)$, $x_2(0) = -(A - dc)$. The initial values for the rising ramp are the negatives of the initial values for the falling ramp.

The output sequence $y(n)$ of the ideal oscillator is a sampled version of a pure sine wave. The angle θ_0 represented by the oscillator coefficient is given by $\theta_0 = 2\pi f_0/f_{\rm clk}$, where f_0 is the desired frequency in cycles per second. In an actual implementation, the multiplier coefficient $2\cos(\theta_0)$ is assumed to have $b + 2$ bits. In particular, one bit is for the sign, one bit for the integer part, and b bits for the remaining fractional part in fixed-point number representation. Then the largest value of the coefficient $2\cos(\theta_0)$ which can be represented is $(2 - 2^{-b})$. This value of the coefficient gives the smallest value of $\theta_{\rm min}$, which can be implemented by the direct form digital oscillator using b bits: $\theta_{\rm min} = \cos^{-1}[1/2(2 - 2^{-b})]$. Therefore, the smallest frequency that the oscillator can generate is $f_{\rm min} = (\theta_{\rm min}/2\pi)f_{\rm clk}$, where $f_{\rm clk}$ is the clock frequency (sampling frequency). As an example, let $b = 25$ bits. The largest oscillator coefficient $[2\cos(\theta_0)]$ is 67108863/33554432 and $\theta_{\rm min} = \cos^{-1}(67108863/67108864) \approx 0.00017263$. For $f_{\rm clk} = 52$ MHz and $b = 25$, $f_{\rm min} \approx 1.43$ kHz.

During the ramp, the phase change is π in (5) and (6), and therefore the required output frequency is $f_0 = 1/2T_r$. The smallest frequency $(f_{\rm min})$ should be below f_0. For $T_r = 14\ \mu$s, $f_0 \approx 35.71$ kHz.

The power control is realized by scaling the ramp curve. The amplitude of the sinusoidal is controlled by A' in (13) and (14). The downlink dynamic power control in GSM 900/DCS 1800 uses 16 power levels with 2–dB separation. The power control range is $0 \cdots -32$ dB, where the 0-dB level is the nominal maximum power. Therefore, the amplitude (A') value range of the initial values is from 0.0251 to 0.999. The simulated power control resolution (see the Appendix) is below 0.25 dB (see Table I).

If the ramp time is variable, then a fully parallel multiplier is needed. For applications with fixed ramp time, a fully parallel multiplier is not required and it would indeed be a waste of silicon area. A multiplication by a fixed binary number can be accomplished with $(N - 1)$ adders, where N is the number of nonzero bits in the coefficient. If the clock frequency is 52 MHz, the output frequency of the oscillator is 35.71 kHz and b is 25, and the coefficient $2\cos(2\pi f_0/f_{\rm clk})$ is 1.99998137757162 $(01111111111111111110110001111)_2$. This requires 21 adders. One way to reduce the hardware complexity of the direct-form digital oscillator was proposed in [8] and can be obtained

$$2\cos(\theta) = 2 - 2^{-b1}[2^{b1}(2 - 2\cos(\theta))]$$

where

$$b1 = \left[\log_2 \frac{1}{2(1 - \cos\theta)}\right] \tag{15}$$

and $[r]$ is the smallest integer greater than or equal to r. The coefficient $(2 - 2\cos(2\pi f_0/f_{\rm clk}))$ is 0.00001862 $(00000000000000000001001110000)_2$. The total number of adders required to implement the coefficient $2\cos(2\pi f_0/f_{\rm clk})$ is reduced from 21 to 4. The coefficient is formed by multiplying the small fraction $(2 - 2\cos(2\pi f_0/f_{\rm clk}))$ by the factor 2^{b1}, where $b1$ is 16. This reduces hardware complexity by reducing the maximum word length needed in adders. The output of the adders must be multiplied by 2^{-b1} to keep the overall gain unchanged. The number of adders could be reduced further using the canonic signed digit (CSD) numbers. The block diagram of the modified ramp generator and output power level controller is shown in Fig. 7(b). The novel ramp generator and output power level controller in Fig. 7(b) can be implemented with the aid of three two-input adders, two

delays, one multiplexer, and one fixed multiplier, which can be accomplished with $(N-1)$ adders, where N is the number of nonzero bits in the coefficient. The novel ramp generator and output power level controller needs neither a memory nor a fully parallel multiplier as in the case of the look-up table method, so it can be easily implemented with standard cells.

The D/A converter usually exhibits a fully sample-and-hold output that causes the $\sin x/x$ rolloff function on the spectrum of the converted analog signals. In the multicarrier GMSK modulator, the output band is from 11.5 MHz to 16.5 MHz. This introduces a droop of -0.779 dB, which is not acceptable. One method to compensate the $\sin x/x$ rolloff is the use of the inverse $\sin x/x$ filter in the IF frequency [9]. The digital ramp generator and output power level controller could compensate for this droop when the bandwidth of the single carrier is narrow. The $\sin x/x$ rolloff is taken into account when the power level value of the carrier is calculated.

The dynamic range in the transmission could be optimized digitally by setting the multicarrier signal peak value equal to the D/A converter full scale. However, this approach is not utilized in this design due to required power compensation in the analog domain. The problem with the analog solutions is the inaccuracy due to aging, temperature, and component variations. Furthermore, the analog solutions are complex, and stability might be a problem. This design enables digital fine-tuning of the carrier power level with adjustable accuracy.

IV. Design Example

In this section, an investigation will be carried out in which parameter values of the digital GMSK modulator are required to accomplish the system specifications for a base station modulator [10].

1) Determine the number of samples per symbol and the clock frequency $f_{\mathrm{clk}} = S \times f_{\mathrm{symr}}$, when S is 192, and f_{symr} is 270.833 kb/s, f_{clk} is 52 MHz.
2) The frequency resolution will be 0.77 Hz by (2), when f_{clk} is 52 MHz, and j is 26. The frequency resolution is better than the target frequency error specification in Table I.
3) Determine the LUT output wordlength (e)

$$\frac{2^e f_{\mathrm{clk}}}{2^j} > f_d \tag{16}$$

where f_d is the maximum absolute value of the frequency deviation due to the modulation, and f_d is $f_{\mathrm{symr}}/4$ in this design example. If e is equal to 17, then (16) is true.

Other wordlengths in the multicarrier GMSK modulator are shown in Figs. 3 and 4. The D/A converter wordlength is 14 bits, which is the maximum wordlength in state-of-the-art IF D/A converters [11]. After the four carriers are combined together in Fig. 3, the power per carrier is not changed, but the noise floor is increased by 6 dB. Thus, the carrier-to-noise ratio is decreased 6 dB. Increasing the wordlengths of the sine ROM and the multiplier, and doing the quantization after the carrier combination, could reduce this degradation. In the GMSK IF modulator, most of the spurs are generated less by digital errors (quantization errors) and more by analog errors in the D/A converter. Hence, the spectral improvement in the digital output would not be visible in the D/A converter IF output. The wordlengths used are sufficient to fulfill the spectrum requirements due to the modulation as shown in Fig. 10(a) and (b). The increased wordlengths of the multipliers and sine ROMs will add complexity and enlarge core area. Therefore, it was decided that the wordlengths shown in Figs. 3 and 4 should be used.

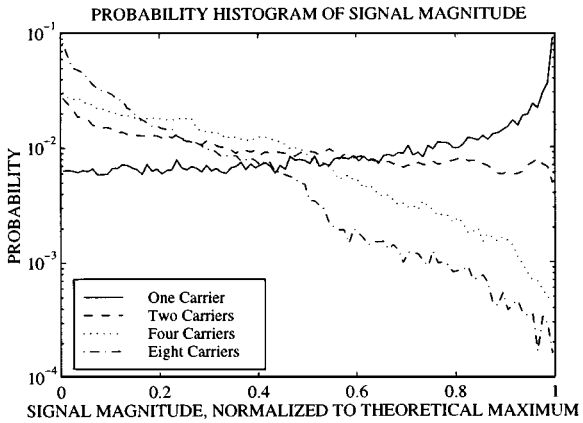
V. Multicarrier GSM Signal Characteristics

The GMSK modulation method used in the GSM 900 and DCS 1800 is a constant envelope modulation scheme. This property is very desirable from the linearity point of view in single carrier transmission because, as such, it allows usage of fairly nonlinear components in the transmission chain [12]. On the other hand, the multicarrier signal has very unfavorable characteristics because signals with constant envelope quite often sum up in phase. Therefore, the multicarrier signal has a high ratio of peak value to rms value of a waveform (a high crest factor).

In order to discover the multicarrier GSM signal characteristics, simulations were carried out using the modulator model. The simulation length was 1800 symbols, and 192 amplitude samples per one symbol were taken. The multicarrier GMSK simulation employed a regular carrier spacing of 600 kHz and a data rate $1/T = 270.833$ kb/s, together with a Gaussian low-pass pulse shaping filter with a normalized bandwidth BT of 0.3. In the simulations, the burst structure is three tail bits (0's), 58 payload bits (random 0s and 1s), 26 training sequence bits [eight different (here TS 0)] [13], 58 payload bits (random 0s and 1s), three tail bits (0s), eight guard timing bits (1's), one-quarter guard bit (1). Different pseudorandom number generators are used to generate each digital modulation source, thus ensuring a low correlation between the resulting carriers.

In the case of the multicarrier GSM 900/DCS 1800, the crest factors are given in Fig. 8 for one to eight carriers. The disadvantageous behavior of the multicarrier-GSM signal is clearly revealed by Fig. 8. For a large number of carriers, the peak power in the signal is significantly higher than the rms power (increased crest factor). An increasing amount of the signal energy is concentrated around the midscale values of the D/A converter in the multicarrier GMSK modulator. As a result, a "small-scale" dynamic and static linearity of the D/A converter becomes increasingly critical in obtaining low intermodulation distortion, and maintaining sufficient carrier-to-noise ratios. Since the power amplifier is normally most nonlinear in saturation at high powers, peaks in signal amplitude signify nonlinear amplification. This, in turn, dictates intermodulation and spectral regrowth. However, the analysis of spurs, harmonics, and noise from the filters, mixers, and power amplifier are beyond the scope of this paper.

Nevertheless, the crest factors do not characterize the signal comprehensively. What really matters is how often the signal amplitude lies in the range of high values, i.e., how probable it is that peak powers will actually occur. Magnitude probability densities of multicarrier signals are shown in Fig. 8. The magnitude probability density presented confirms that the probability of the amplitude magnitude reaching the theoretical maximum (during a given time period) decreases for an increasing number of carriers.



CREST FACTORS OF MULTICARRIER GSM 900/DCS 1800 SIGNALS

Number of carriers	Simulated Crest Factor [dB]	Theoretical Crest Factor [dB]
1	3.0122	3.0103
2	6.0229	6.0206
4	9.0294	9.0309
8	12.0396	12.0412

Fig. 8. Magnitude probability density of multicarrier GMSK signals and crest factors.

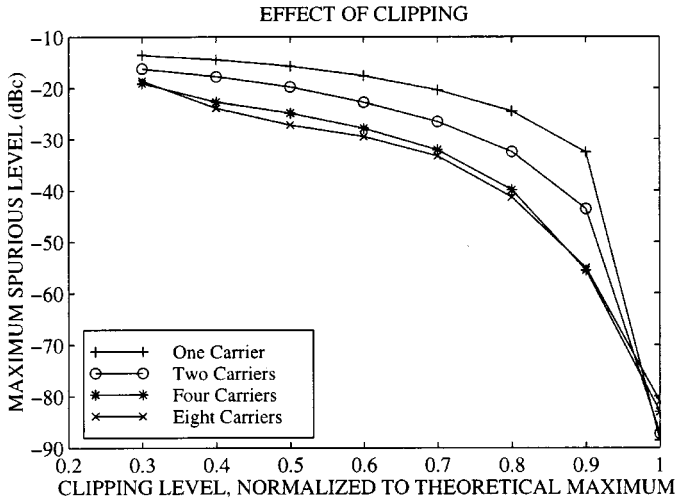


Fig. 9. Maximum spurious level due to clipping.

If the peak values of the signal were reduced, then the dynamic range requirements of the D/A converter would be alleviated. One method of decreasing the peak values is to use clipping [14]. Fig. 9 clearly illustrates the effect of clipping. The harder the clipping is done, the higher is the distortion level. The distortion generated by clipping would have to conform to the spectral purity specifications of −76 dBc (see Table I). Therefore, the clipping level must be set near the theoretical maximum magnitude in order to meet the spectral purity requirements, as shown in Fig. 9. Hence, clipping cannot be used to reduce the dynamic range of the signal.

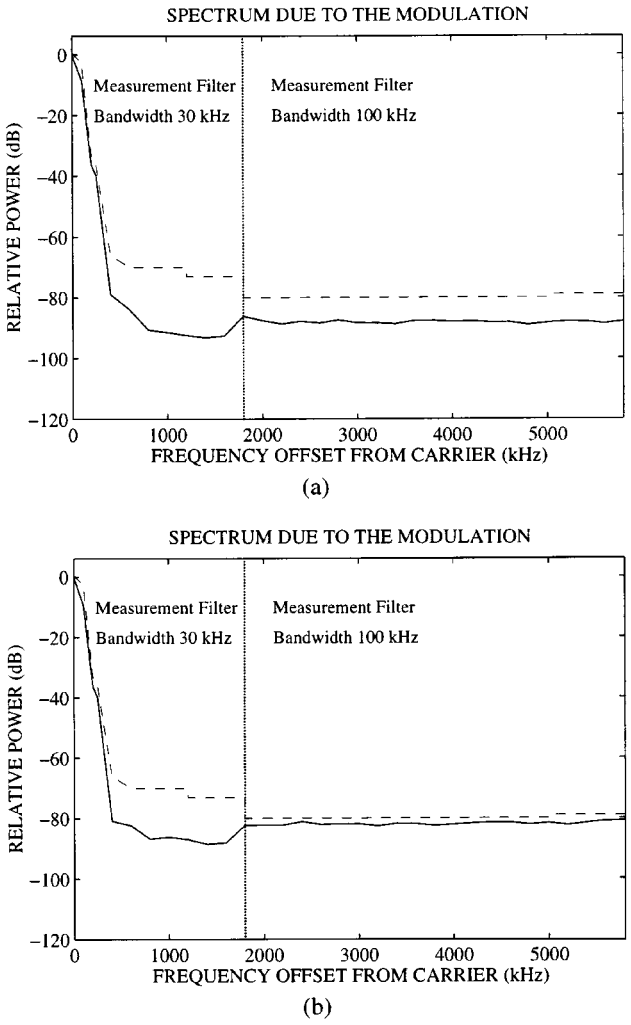


Fig. 10. Spectrum due to the modulation in the case of (a) the single carrier and (b) the multicarrier. Some margin (6 dB) has been left between the most stringent modulation spectrum requirement defined for GSM 900 and DCS 1800 BTS in [10] and the values specified in Fig. 10 at offsets larger than 1800 kHz, because in the case of the multicarrier digital modulator it is not possible to use steep analog bandpass filters (Fig. 2) around each carrier.

VI. Simulation Results

A computer model of the digital GMSK modulator has been built to simulate the effect of the parameters on the output signal. The phase trajectory of the GMSK-modulated signal generated by the digital GMSK modulator is compared to the mathematically computed ideal phase trajectory to determine the phase difference between the transmitted signal and the ideal signal. The phase difference is fitted to a linear regression line [10]. The slope of the regression line provides an estimate of the frequency error of the transmitter, and the regression line subtracted from the phase difference provides an estimate of the phase error. The phase error target is specified to be 1.5° rms with the peak at 2.5° (see Table I). The pseudorandom bit stream will be any 148-bit subsequence of the 511-bit pseudorandom bit stream [15]. Table II shows phase errors with different numbers of symbol stages in the shift register. Other wordlengths in the GMSK modulator are shown in Fig. 4. The "Spectrum Req." column of Table II indicates whether the spectrum requirements shown in Fig. 10(a) with a dashed line are fulfilled or not. The

TABLE II
NUMBER OF SYMBOL STAGES (w) IN SHIFT REGISTER

w	Rms Phase Error	Peak Phase Error	Spectrum Req.	Transient Req.	The Size of the LUT †
2	6.138°	11.537°	No	No	768 × 17 bits
3	0.931°	1.754°	Yes	Yes	1536 × 17 bits
4	0.039°	0.090°	Yes	Yes	3072 × 17 bits
5	0.006°	0.012°	Yes	Yes	6144 × 17 bits

† The size of the uncompressed LUT is 2^(w)×192×17 bits, where w is the number of the symbol stages in the shift register in Fig. 4.

TABLE III
SPECTRUM DUE TO SWITCHING TRANSIENTS (PEAK-HOLD MEASUREMENT, 30 kHz FILTER BANDWIDTH, REFERENCE (300 kHz WITH ZERO OFFSET)

Offset (kHz)	Maximum Power Limit (dBc)		Simulated Maximum Power (dBc)
	GSM 900	DCS 1800/1900	
400	- 60	- 53	-71.20
600	- 70	- 61	-78.09
1200	- 77	- 69	-84.97
1800	- 77	- 69	-86.23

"Transient Req." column of Table II shows whether the requirements of the switching transient spectrum (given in Table III) are met. If the number of the symbol stages in the shift register is three, then the phase error levels (see Table II) meet the assumed specifications (see Table I).

The modulation and power level switching spectra can produce significant interference to adjacent bands. The spectrum due to the modulation in the case of the single carrier is shown in Fig. 10(a), where the dashed line shows the spectrum requirements due to the modulation. Fig. 10(b) shows the spectrum due to the modulation in the case of the multicarrier transmission. The wordlengths in the simulation are shown in Figs. 3 and 4. After the four carriers are combined together in Fig. 3, the power per carrier is not changed but the noise floor is increased by 6 dB. Therefore, the noise floor is about 6 dB higher in Fig. 10(b) than in Fig. 10(a).

In simulations, the ramp-up and the ramp-down profiles of a transmitted time slot satisfy the GSM 900/DCS 1800 masks for the burst-by-burst power ramping [10]. The power measured due to switching transients, which determines allowed spurious responses originating from the power ramping before and after the bursts, will not exceed the values shown in Table III [10]. Some margin (3 dB) has been left between the values in [10] and the values specified in Table III. This margin should take care of the other transmitter stages that might degrade the spectral purity of the signal. The power levels simulated are well below the limits shown in Table III.

The problem with a digital ramp generator and output power level controller is reduced carrier-to-noise ratio at low power levels, because the dynamic power control is realized by scaling in the digital domain. According to specifications, modulation spectrum is measured at maximum dynamic power level [10], so that the reduced carrier-to-noise ratio at low power levels presents no problems in meeting the specifications. Of course, the base station performance will be degraded due to the reduced carrier-to-noise ratio.

VII. IMPLEMENTATION

The multicarrier GMSK modulator design was synthesized by Synopsys software from the VHDL description using the 0.35 μm CMOS standard cell library. Functional and timing verifications have been performed at all levels. A die/digital core area is 26.8 mm^2/18.1 mm^2. The power dissipation of the digital part is 0.7 W at 52 MHz at 3.3 V.

VIII. MEASUREMENT RESULTS

In the GMSK IF modulator, most of the spurs are generated less by digital errors (quantization errors) and more by analog errors in the D/A converter such as clock feedthrough, intermodulation, and glitch energy. The simulation results were saved in the pattern generator memory. These data were transferred to the D/A converter [16]. The output wordlength of the single GMSK modulator is 12 bits as shown in Fig. 3. Fig. 11(a) shows the single carrier output, when the resolution and video bandwidth is 30 kHz. The output signal in Fig. 11(a) fulfills the spectrum mask requirements [10], when the measurement bandwidth is 30 kHz. Fig. 11(b) shows the single carrier output, when the resolution and video bandwidth is 100 kHz. The increased spur level around the Nyquist frequency is removed by the analog low-pass filter in Fig. 2. Therefore, the output signal in Fig. 11(b) fulfills the spectrum mask requirements [10], when the measurement bandwidth is 100 kHz. Fig. 12(a) shows the multicarrier output, when the resolution and video bandwidth is 30 kHz. The noise floor level with respect to the carrier in Fig. 12(a) is about 10 dB higher than in Fig. 11(a), which could be explained by the higher crest factor (see Fig. 8). Fig. 12(b) shows the multicarrier output, when the resolution and video bandwidth is 100 kHz. The noise floor in Fig. 12(b) has increased about 10 dB compared to Fig. 11(b). The four carrier GMSK modulator does not fulfill GSM 900/DCS 1800 spectrum specifications, because Fig. 12(a) and (b) does not

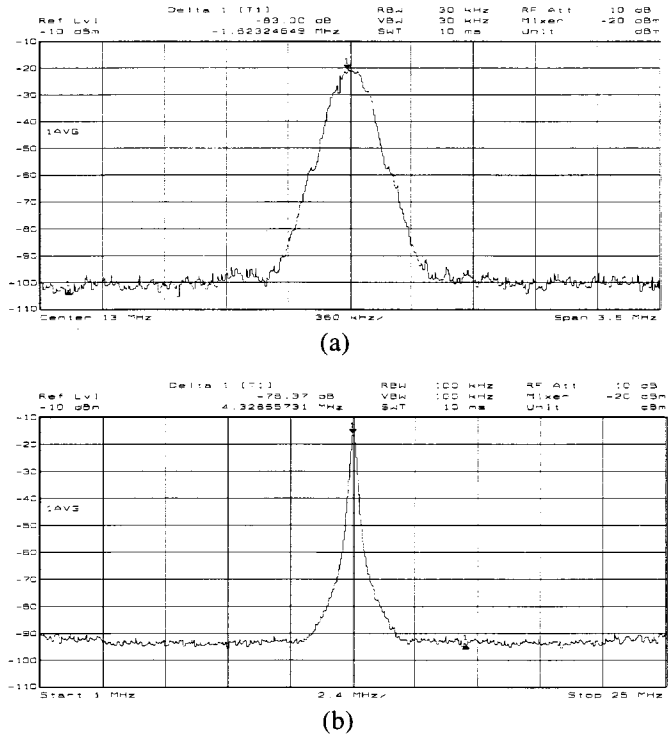


Fig. 11. GMSK-modulated signal. The sweep time is 10 ms and averaging is used. The resolution and video bandwidth is (a) 30 kHz and (b) 100 kHz.

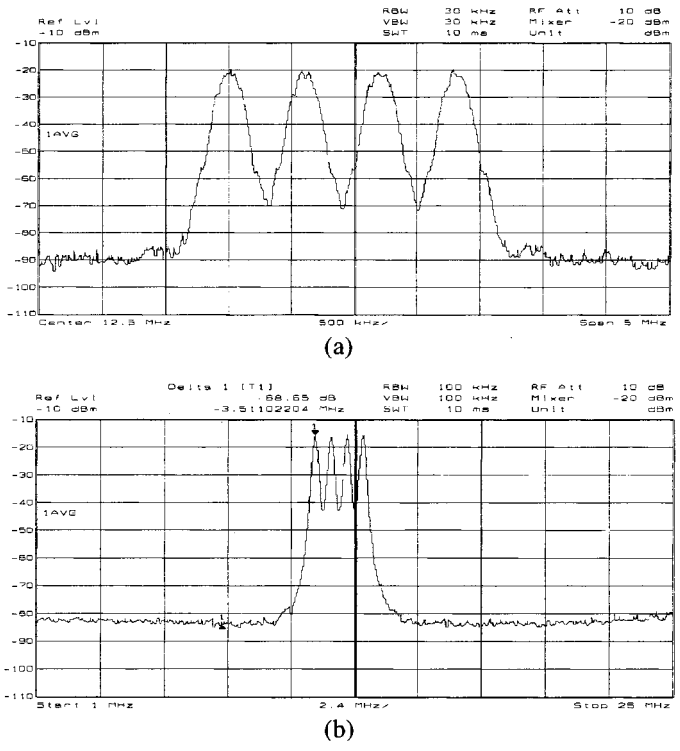


Fig. 12. Multicarrier GMSK-modulated signal, the channel spacing is 600 kHz. The sweep time is 10 ms and averaging is used. The resolution and video bandwidth is (a) 30 kHz and (b) 100 kHz.

fulfill the spectrum mask requirements [10]. However, if the D/A converter's static and dynamic nonlinearity performance is improved, then a successful implementation of the multicarrier GMSK modulator might be possible in the IF frequency.

IX. Conclusion

A multicarrier GMSK modulator has been developed and implemented. It comprises four GMSK modulators, which generate GMSK modulated carriers at the specified center frequencies. Utilization of the redundancy in the stored waveforms reduces the size of the GMSK trajectory LUT to less than one-quarter of the original size in the modulator. The novel digital ramp generator and output power level controller performs both the burst ramping and the dynamic power control in the digital domain. The four GMSK modulated signals are combined together in the digital domain. Thus, only one upconversion chain is needed, which results in huge savings in the number of the required analog components.

Appendix
Finite Wordlength Effects in Ramp Generator and Output Power Level Controller

The error at the ramp generator and output power level controller output consists of two components, $e(n) = e_1(n) + e_2(n)$, where $e_1(n)$ is the error due to the ramp generator and output power level controller output quantization, and $e_2(n)$ is the error that has been accumulated as a result of the recursive computations in the digital oscillator.

The bounds for $e_1(n)$ are given by

$$-2^{-c} < e_1 \leq 0 \tag{17}$$

for truncation, and $-(2^{-c}/2) < e_1 \leq 2^{-c}/2$ for rounding, where c is the number of fractional bits in the output of the ramp generator and output power level controller. No sign bit is needed because the ramp signal is always positive [see (5) and (6)].

In the digital oscillator, besides the zero-input response $y(n)$ of the second-order system, we get a zero-state response $y_{\rm err}(n)$ due to the random sequence $e_2(n)$ acting as an input signal. From (7), we obtain

$$y(n+2) = \alpha y(n+1) - y(n) + e_2(n+2) \tag{18}$$

and by z transformation

$$Y(z) = Y_{\rm ideal}(z) + Y_{\rm err}(z) \tag{19}$$

with $Y_{\rm ideal}(z)$ derived from (8). The z transform of the output error $y_{\rm err}(n)$ is given by

$$Y_{\rm err}(z) = \frac{z^2 E_2(z) - z^2 e_2(0) - z e_2(1)}{z^2 - 2\cos\theta_0 z + 1} \tag{20}$$

with $E_2(z)$ being the z transform of the quantization error signal $e_2(n)$. Transforming $Y_{\rm err}(z)$ back into the time domain results in an output error sequence

$$y_{\rm err}(n) = \frac{1}{\sin\theta_0} \sum_{k=2}^{n} e_2(k) \sin(\theta_0(n-k+1)), \quad \text{for } n \geq 2 \tag{21}$$

when $e_2(0)$ and $e_2(1)$ are assumed to be zero. Equation (21) shows that the output error is inversely proportional to $\sin(\theta_0)$; thus, the output error increases with the decreasing digital oscillator frequency. If truncation is used, the right-hand side of (20) is negative, since $e_2(k)$ is negative [see (17)], and $\sin(\theta_0(n-k+$

$1))$ is positive, because the digital oscillator generates only half of the sine wave period [see (5) and (6)]. The fact that the error is a deterministic signal [7] forces us to investigate the worst case, which corresponds to the case where every truncation suffers from the maximum absolute error value. In this case, the digital oscillator generates one-half of the period, and thus the upper limit for the output error becomes

$$y_{\max\mathrm{err}}(M) = \frac{e_{\max}}{\sin\theta_0}\sum_{k=2}^{M}\sin(\theta_0(M-k+1)) \approx \frac{-2^{-b}}{\sin\theta_0\sin(\theta_0/2)} \approx \frac{-2^{-b+1}}{\theta_0^2} \qquad (22)$$

where $e_{\max} = -2^{-b}$ is the worst-case truncation error, b is the number of fractional bits in the digital oscillator, $0 < \theta_0 \ll 1$, $M = [\pi/\theta_0]$, and $[r]$ is the smallest integer greater than or equal to r.

If the rounding is used, the $e_2(k)$ will acquire positive and negative values and so the output error sequence will have lower values than in the case of truncation. The simulations indicate the accumulated error is below the output quantization error when rounding is used, b is 25, and c is 12.

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