An Evolved GSM/EDGE Baseband ASIC Supporting Rx Diversity

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***Abstract*—In this paper, a baseband ASIC which supports receive diversity and soft-output Viterbi equalization for enhanced 2G networks is presented. It includes a transmitter and receiver with a symbol detector and a decoder with a dedicated incremental redundancy implementation, as well as the necessary control capability to autonomously communicate with the RF-IC. The ASIC is connected to an RF-IC to build a complete Evolved EDGE transceiver system. The transceiver system reaches a measured sensitivity close to −112 dBm for single-antenna GSM voice channels and achieves the reference interference performance for adjacent channels 11.4 dB above 3GPP requirements. It is the first reported solution which fulfills the most demanding 3GPP Downlink Advanced Receive Performance Phase 2 testcases specified for Rx-diversity. The ASIC occupies 6 mm² in 130 nm CMOS with a power consumption between 3.9 and 14 mW.**

***Index Terms*—Baseband ASIC, enhanced 2G networks, evolved EDGE (E-EDGE), evolved EDGE testbed, GSM/EDGE, hybrid ARQ, incremental redundancy, interference cancellation, internet of things (IoT), machine-to–machine (M2M), Rx diversity, space-time processing.**

I. Introduction

In multistandard, LTE-enabled mobile platforms being fitted into the latest smart phones today, the fallback solution outside major cities is still mostly provided by the EDGE mode, where the contrast in throughput between 100 Mb/s for LTE and 236 kb/s for EDGE is drastic in terms of user experience and service quality. Thus, improving the bottom-end of the data rate is as important as pushing the maximum further towards the Gb/s level. With potential throughput up to 1.2 Mb/s, Evolved EDGE (E-EDGE) is such a standard that fits well with LTE-enabled devices where a second antenna is already mandatory, so that E-EDGE can also freely take advantage of dual carrier or receive diversity to increase throughput under interference dominated radio conditions. The interference suppression capability offered by the second antenna, in particular, also gives operators more flexibility to achieve a frequency re-use factor closer to one, thus improving the capacity of the network. Due to the ubiquitous coverage, such enhanced 2G networks, beyond providing a fallback solution for the latest smart phones, also play a key role for emerging low-bandwidth applications, such as machine-to-machine (M2M) communication or the Internet of things (IoT). For applications of this type, e.g., asset tracking or fleet management, low power consumption to ensure long battery life, as well as worldwide coverage is indispensable.

To make E-EDGE a suitable and reliable fallback solution or even a stand-alone solution, several technical features have been introduced, such as diversity techniques and higher order modulation schemes (16-QAM and 32-QAM).

Unfortunately, interference cancellation and equalization algorithms for E-EDGE also result in prohibitively complex[1] and power-hungry designs, especially implemented on dedicated DSPs. Moreover, the latest EDGE transceivers, e.g., [1], are not supporting any E-EDGE features.

In [2], we presented the first (and so far only reported) single-antenna E-EDGE receiver ASIC based on a hard-output equalizer. Unfortunately, it does not allow the channel decoder to achieve maximum performance, which can only be achieved by providing soft output values. These can be obtained under ISI conditions by Viterbi equalization. However, for the high modulation orders of E-EDGE, using the full trellis is impracticable, and a reduced-state Viterbi equalizer in combination with a channel shortening filter is a favorable choice [3]. Compared with our previous solution [2] based on hard-decisions, a significant performance improvement of 3–4 dB is achievable by providing reliability information to the channel decoder.

Moreover, our implementation of [2] is not able to take advantage of Rx-diversity, which allows to provide an array-gain of up to 3 dB and a diversity gain in case of two independent fading channels

Beyond that, for mobile stations supporting Rx-diversity, 3GPP introduced a new set of stringent performance requirements labeled Downlink Advanced Receiver Performance Phase 2 (DARP2). Moreover, Rx-diversity also improves the robustness to interference, and hence increase the throughput in areas of strong congested areas. Besides the lack of Rx-diversity and soft-output equalization, our work of [2] was a standalone digital baseband receiver ASIC without transmitter and without any controlling capability of an attached RF transceiver.

[1]SOVE Equalization of one 32-QAM burst requires 193k complex-valued multiplications.

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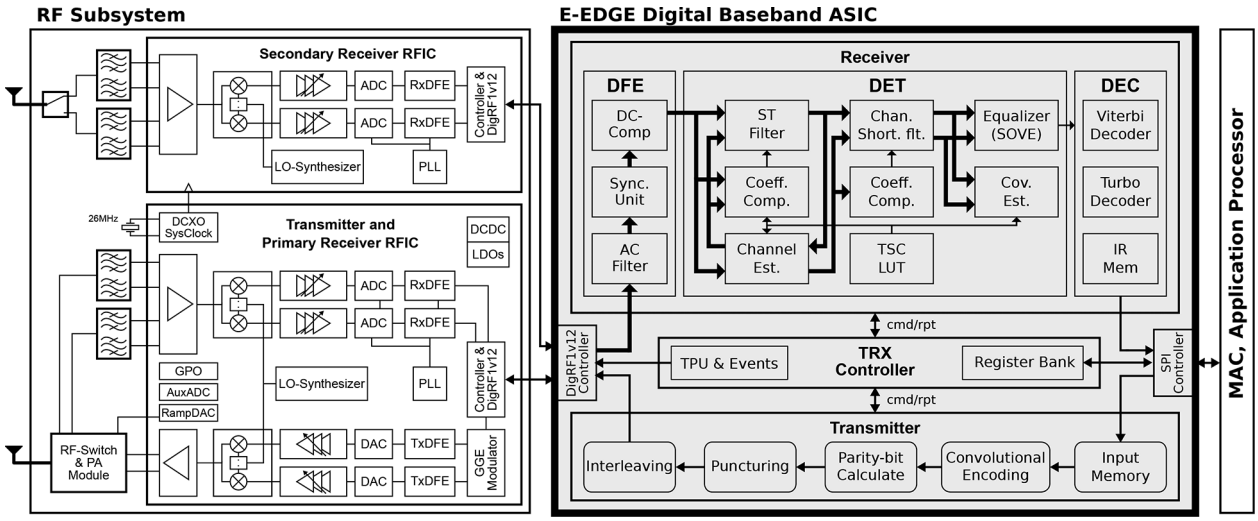

Fig. 1. Block diagram of the two/three-chip E-EDGE solution with RF transceiver chip, BB-ASIC with receiver, transmitter, TRX controller, and configuration registers as well as attached system components.

A. Contributions

In this paper, we present an Rx-diversity enabled baseband ASIC (BB-ASIC), which performs the entire baseband processing, including interference cancellation, soft-output Viterbi equalization (SOVE) and fully autonomous incremental redundancy (IR) management. We propose a highly parallelized SOVE equalizer architecture which allows a performance improvement of up to 4 dB compared to hard-output equalizers. The ASIC is used to build the first complete E-EDGE system by connecting it to an existing RF transceiver chip (RF-IC). In addition to the measured sensitivity, we show the first measured interference performance for a DARP2 testcase.

B. Outline

The remainder of this paper is organized as follows. Section II provides an overview over the building blocks of the BB-ASIC and the surrounding E-EDGE system. In Section III, the subsequent digital building blocks responsible for symbol detection are presented. Then, in Section IV. the channel decoder and the IR unit is explained. Section V presents the measured performance results and compares them with other reported GSM/EDGE solutions.

II. ASIC Architecture and System Overview

Fig. 1 shows the top-level block diagram of the BB-ASIC and the E-EDGE system, into which the ASIC is embedded. The BB-ASIC includes a BB-transmitter and a BB-receiver with a top-level controller in between, labeled as TRX controller. The dedicated TRX controller is responsible for sending commands and evaluating reports from and to the BB-receiver, BB-transmitter, RF-subsystem, and application processor. A key problem in E-EDGE is the tight schedule and real-time constraints which impose stringent throughput and delay requirements on the signal processing algorithms, especially on the symbol detection and decoding blocks. To solve this issue, we implemented a time processing unit (TPU), which hosts the GSM time-base as the main time reference for the baseband. Hence, no real-time awareness is required for the external application processor when interacting with the baseband, which greatly facilitates system integration. The core logic is also clocked independently from the interfaces to the application processor and RF-IC.

The BB-transmitter contains all of the necessary uplink functions of encoding, puncturing, interleaving and mapping in order to pass the correct symbols to the RF transmitter. The baseband processing of the transmitter includes convolutional encoding, parity bit computation, puncturing and interleaving to support all modulation and coding schemes defined for GSM/EDGE/E-EDGE.

The receiver part of the BB-ASIC contains three main blocks, the digital front-end (DFE), the detector (DET) and the decoder (DEC). The DFE's responsibility is to provide samples whose impairments have been compensated to the DET, which performs the symbol detection and interference cancellation.

The DFE is the first signal processing unit on the BB-ASIC. The task of the DFE is to decimate the oversampled data from the RF-IC, to compensate the DC offset and to estimate the carrier frequency offset and the power of the received signal. As shown in Fig. 2, the architecture of this block is arranged in such a way that the samples flow in a continuous stream through the processing stages allowing for highly parallel processing and minimizing the storage requirements. The decimation filter is implemented in a sequential architecture as shown in Fig. 2. The purpose of the decimation filter, besides avoiding aliasing, is to suppress the adjacent channels which have not been completely suppressed by the analog filters in the RF-IC. Therefore, the cutoff frequency of the decimation filter is adjusted from the TRX controller according to the strength of the GSM channel in the adjacent band. For this, a lookup-table (LUT) with various FIR coefficient sets is implemented. A coefficient set can be set according to the power of the adjacent channel, which is estimated in the ac detection block in Fig. 2, or manually. Besides sampling rate conversion, the DFE is responsible for the compensation of the DC-offset from the RF-IC. The dc-offset is estimated blindly on the oversampled signal by taking the mean

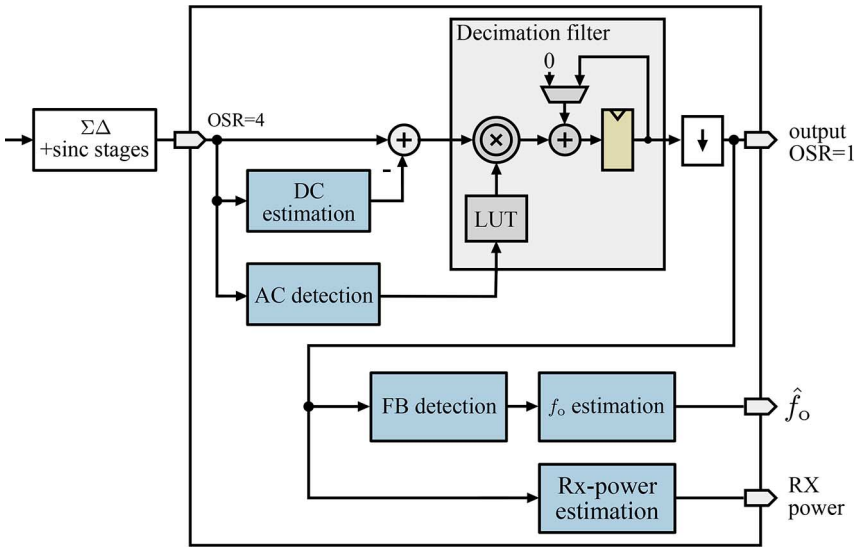

Fig. 2. Digital front-end block diagram.

of successive input samples, or by the method of [4], where a first-order IIR filter is used. The estimated dc-offset is then subtracted from the signal. The carrier frequency offset caused by the inaccuracy of the crystal oscillator is estimated via our proposed low-complexity method in [5] in two stages on the down-sampled signal.

The DET feeds reliability information about the detected bits to the decoder, which performs channel decoding on the received data. The receiver is designed to have the DFE operate symbol-wise, the DET burst-wise, and the DEC code-block-wise. This partitioning allows local data buffers to be deployed with minimum size along the Rx-chain instead of a global shared memory bank with complex access schedules which often forms the power and area bottleneck.

III. Symbol Detection and Equalization

The task of the detector (DET) is to deliver estimates of the transmitted bits in form of reliability information based on the received samples obtained from the DFE to the decoder. Even if many impairments have been mitigated in the DFE, the samples are still distorted by intersymbol interference (ISI) caused by the multipath channel and the pulse-shaping filter in the transmitter and by co-channel interference (CCI) coming from users in neighboring cells. Due to the different energy levels of CCI and ISI, a joint elimination would suppress ISI more and leave the CCI at a high level. Hence, CCI and ISI are most effectively combatted separately in a two-stage approach as proposed in [6]. First, CCI must be mitigated using a space-time filter as introduced in Section III-C. Second, soft-output signal detection under ISI must be performed by considering all possible transmitted symbol sequences which are represented by a trellis where each state is defined by the symbols in the channel memory. The recursive processing of all paths in this trellis is efficiently done by the Viterbi algorithm [7]. However, the number of states in the trellis grows exponentially with the number of bits per symbol and the channel length. Hence, for the high modulation orders of E-EDGE, only a reduced-state trellis is considered and decision feedback is used for the symbols that

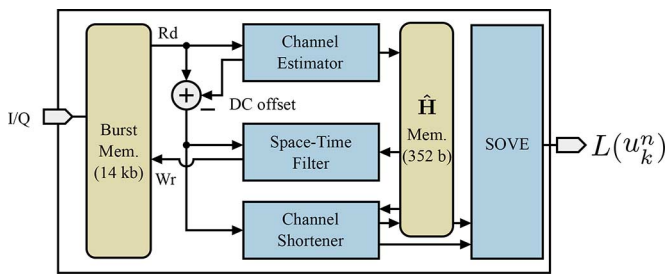

Fig. 3. Hardware architecture of DET.

are not covered by the state [8]. To concentrate the energy of the channel impulse response (CIR) in the channel taps which are covered by the equalizer, a channel shortening filter is used. The combination of channel shortening filter and reduced-state Viterbi equalization has already been shown to be suitable for 8-PSK (EDGE) in [9] and it is even more advantageous for the 32-QAM alphabet of E-EDGE since the complexity of the linear filter does not depend on the modulation order.

The DET block is implemented by a hardwired arrangement of interference-canceller (Space-Time Filter), channel shortener and soft-output Viterbi equalizer (SOVE) as shown in Fig. 3. In contrast to the stream-based processing in the DFE, the architecture of the DET has a central memory which holds a complete burst and which is accessed by most of the processing blocks in a mutually exclusive way.

A. System Model for Symbol Detection

For symbol detection, the baseband model for the received symbols is given by

$$\mathbf{y}_k = \mathbf{H}\mathbf{x}_k + \mathbf{n}_k. \tag{1}$$

The DET input for the two receive antennas at time k is arranged in the two-element column vector $\mathbf{y}_k$. The effect of the multipath channel is modeled by the multiplication of the eight last transmitted symbols $\mathbf{x}_k = [x_k \dots x_{k-7}]^T$ and the channel matrix $\mathbf{H}$ which consists of the CIRs arranged in two rows.

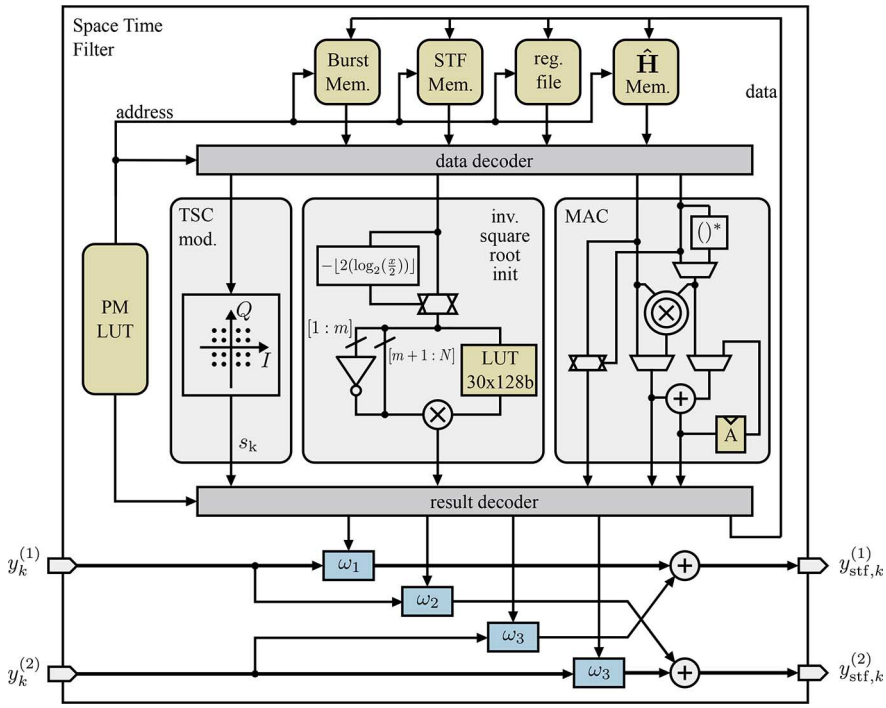

Fig. 4. Space-time filter and coefficient computation architecture with dedicated datapaths for symbol modulation and inverse square-root computation.

Thermal noise and interference is summarized in the additive term $\mathbf{n}_k$.

B. Channel Estimation and Residual DC-Offset Compensation

Each burst contains a known midamble which is used to derive a least-squares estimate of the two CIRs in $\mathbf{H}$. To this end, the Moore–Penrose pseudo-inverse of a matrix consisting of shifted versions of the midamble must be computed. By extending this matrix with an additional column of ones, the residual dc-offset is also estimated [10] and subtracted from the data in the burst memory as shown in Fig. 3. In our BB-ASIC, the inverted matrix of the least squares estimator equation is pre-computed and stored in a LUT such that computation of the estimation $\hat{\mathbf{H}}$ takes only a few cycles.

C. Space-Time Interference Cancellation Processing Unit

Space Time interference cancellation is an effective way to combat co-channel interference in presence of Rx-diversity. The interference is suppressed by a space–time filter with coefficients derived in the MMSE-sense [6]. The error function of the MMSE estimation is given by the difference of the training symbols convoluted with the estimated CIR and the received signal. In this way, the ISI is not taken into account in this estimation. The filter coefficient matrix $\mathbf{W}$ is obtained from the MMSE solution $\mathbf{W} = \hat{\mathbf{H}}\mathbf{S}\mathbf{X}^{\mathrm{H}}(\mathbf{X}\mathbf{X}^{\mathrm{H}})^{-1}$, where $\mathbf{X}$ is a matrix with the received symbols on the position of the training sequence, and $\mathbf{S}$ is a matrix with the modulated training symbols. The computation of $\mathbf{W}$ contains a mixture of multiply-accumulate operations, a matrix inversion and the computation of the modulated training symbols in the matrix $\mathbf{S}$. Therefore, $\mathbf{W}$ is calculated with a dedicated processor architecture with a very reduced instruction set which covers all of the operations necessary, as shown in Fig. 4. The matrix inversion is performed by first computing the lower triangular matrix of $\mathbf{X}\mathbf{X}^{\mathrm{H}}$ by using the Cholesky triangularization.

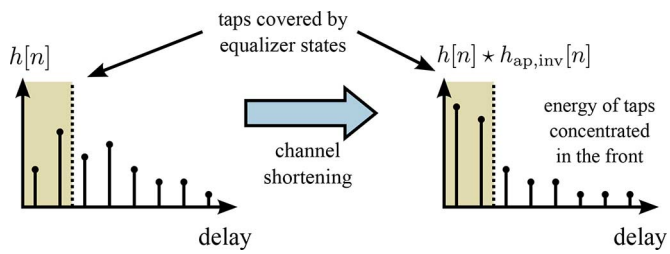

Fig. 5. Reduced-state Viterbi equalization requires the energy of the CIR to be concentrated in the first two taps.

The resulting lower triangular matrix is then inverted with the Gauss–Jordan Algorithm. The Cholesky decomposition includes taking the square root of the diagonal elements. The subsequent Gauss-Jordan algorithm requires the inversion of the diagonal elements. Hence, from an architectural point of view it is favorable to compute the inverse square root directly instead of computing the square root and the division separately. In addition, the need for an expensive fixed-point divider circuit is avoided. The computation of $(1)/(\sqrt{(\cdot)})$ is done with an initial guess according to two factors [11] in a custom instruction, as as shown in the datapath in Fig. 4. One factor is obtained from a 3×128 b LUT and the second factor is obtained from bitwise inversions of part of the shifted input signal. The value is refined by 3 Newton–Raphson iterations which are carried by the multiply-accumulate datapath of the processor. Evaluations have shown that three iterations are sufficient to obtain an implementation loss below 0.05 dB.

The matrix $\mathbf{S}$ contains the modulated training symbols which are obtained by mapping the bits of the training-sequence onto

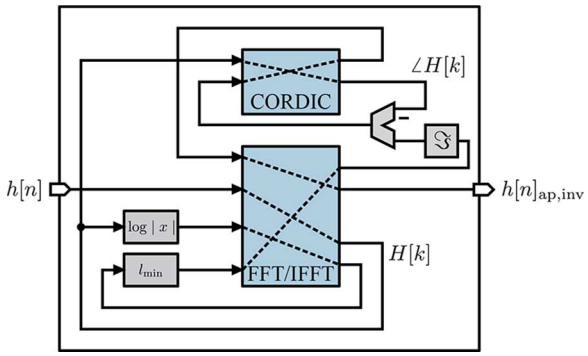

Fig. 6. Time-shared architecture of the channel shortener with FFT/IFFT and CORDIC unit.

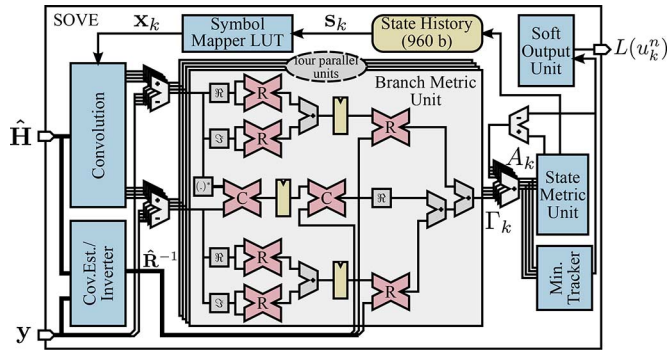

Fig. 7. Block diagram of SOVE with four parallel branch metric units.

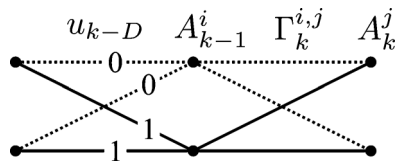

Fig. 8. Trellis example for binary modulation and $D = 1$. Dashed lines correspond to the branch metrics $\Gamma_k^{i,j}$ with $u_{k-D} = 0$.

constellation points. With a custom instruction the symbols are mapped according to the modulation scheme and the phase rotation. A LUT is used to store the constellation points for every modulation type and training sequence number.

The actual filtering is done with four 5-tap FIR filters in Fig. 4, labeled as ω_1 to ω_4, each consisting of one complex-valued multiply-accumulate unit.

D. Homomorphic Channel Shortening

Reduced-state Viterbi equalization shows the best performance if the energy of the CIR is concentrated in the front. At the same time, noise enhancement due to the frequency responseof filters in the processing chain must be avoided. A filter which transforms the CIR into its minimum phase equivalent provides exactly the desired behavior as it does not modify the magnitude response, but transforms the signal in time domain as illustrated in Fig. 5. It has been shown in [2] that a coefficient computation based on linear prediction (LP) is suitable for integration in dedicated hardware for a filter order of $p = 32$. However, the equalization performance for the closely spaced 32-QAM constellation can be improved by providing even higher filter orders. Since the complexity of the LP algorithm grows very quickly with $\mathcal{O}(p^2)$, we employ the solution which we have proposed recently [12] with a complexity growing with only $\mathcal{O}(p \cdot \log_2 p)$. This approach is based on the fact that minimum-phase in time domain corresponds to causality in the cepstrum domain—a homomorphic property that is easily achieved. The computation of the filter coefficients requires a total of four (inverse) Fourier transforms along with logarithm computations and cartesian-to-polar conversions. In our implementation, a single time-shared FFT/IFFT and one CORDIC unit is used to carry out all the operations as shown in Fig. 6. A low silicon area is achieved by a highly sequential hardware architecture consisting of only a single butterfly unit for the Fourier transform and one sequential CORDIC for the angle computation and vector rotation. Even with the highly sequential architecture, computing 32 coefficients requires only 7% of the duration of one GSM burst at the aimed clock frequency of 104 MHz, which is a small amount compared with the time which the equalizer requires.

E. SOVE Algorithm and Architecture

The well-known soft-output algorithms for trellis-based equalization, such as BCJR [13] suffer from large memory requirements because the results of the forward recursion must be kept until the backward recursion is done. This drawback can be mitigated by using a sliding-window trellis processing approach as we do in our turbo decoder solution (Section IV), but for equalization, numerical simulations confirmed the result of [14] that the backward recursion can be omitted with only little performance loss. Thanks to the minimum-phase property of the overall channel achieved by the channel shortening filter, only 32 trellis states are sufficient for the equalization of 32-QAM symbols.

A block diagram of our SOVE architecture is shown in Fig. 7. It takes the estimated channel $\hat{\mathbf{H}}$ and the received symbols $\mathbf{y}$ as input and delivers reliability information $L(u_k^n)$ as output. The soft values $L(u_k^n)$ are computed from the state metrics A_{k-1}^i and the branch metrics $\Gamma_k^{i,j}$ according to [14], as given by

$$\begin{aligned} L\left(u_{k-D}^n\right) &= \log \frac{p(u_{k-D}^n = 0|\mathbf{y})}{p(u_{k-D}^n = 1|\mathbf{y})} \\ &\approx \min_{i,j,u_{k-D}^n=1} \left(A_{k-1}^i + \Gamma_k^{i,j}\right) \\ &\quad - \min_{i,j,u_{k-D}^n=0} \left(A_{k-1}^i + \Gamma_k^{i,j}\right) \end{aligned} \tag{2}$$

where u_k^n denotes the bit of the symbol with time index k and bit index n within the symbol, and $p(u_{k-D}^n = 0|\mathbf{y})$ is the probability of that bit being 0 given the received sequence $\mathbf{y}$. The approximation in (2) is a result of the common max-log approximation of the SOVE algorithm and of neglecting the backward recursion. D is the decision delay, which is an important design parameter for the SOVE, since it determines the number of trellis states for a given modulation order M by M^D. The two groups of branches for $u_{k-D}^n = 0$ and $u_{k-D}^n = 1$ in (2) are illustrated in the tiny trellis example in Fig. 8 for binary modulation and $D = 1$.

In the state metric unit, the branch metrics $\Gamma_k^{i,j}$ are added to the previous state metrics A_{k-1}^i and all new state metrics A_k^j

are determined by selecting the most probable branch merging into the current state j as given by

$$A_k^j = \min_i \left(A_{k-1}^i + \Gamma_k^{i,j} \right). \tag{3}$$

The branch metrics

$$\begin{aligned} \Gamma_k^{i,j} &= (\mathbf{y}_k - \hat{\mathbf{H}} x_k)^H \hat{\mathbf{R}}^{-1} (\mathbf{y}_k - \hat{\mathbf{H}} x_k) \\ &= \mathbf{d}_k^H \hat{\mathbf{R}}^{-1} \mathbf{d}_k \\ &= |d_{1,k}|^2 r_{11} + |d_{2,k}|^2 r_{22} + 2\Re(d_{1,k}^* d_{2,k} r_{12}) \end{aligned} \tag{4}$$

are computed from the estimated inverse spatial covariance matrix $\hat{\mathbf{R}}^{-1}$ of the received signal and the difference $\mathbf{d}_k$ between the received signal $\mathbf{y}_k$ and the convolution of the test symbols $\mathbf{x}_k$ with the estimated CIRs in $\hat{\mathbf{H}}$. Since $\hat{\mathbf{R}}^{-1}$ has real-valued diagonal elements r_{11} and r_{22} as well as complex conjugated off-diagonal elements $r_{12} = r_{21}^*$, the branch metric computation can be simplified (see (4) and Fig. 7). The test symbols $\mathbf{x}_k$ are determined by the specific branch and state, where each state has its own list of decision feedback symbols.

The branch metric unit is the block with the highest computational complexity in the equalizer. In order to achieve the required throughput at our baseband circuit clock frequency of 104 MHz, four parallel branch metric units, each containing 14 real-valued multipliers are deployed. In this setup, the processing of all branches for one trellis state takes only eight clock cycles. While the branch metric unit computes the state metric of one trellis state, convolution of $\hat{\mathbf{H}}$ with the test symbols $\mathbf{x}_k$ of another state is performed, to ensure efficient hardware utilization.

The test symbols $\mathbf{x}_k$ are obtained with a LUT from the binary vector $\mathbf{s}_k$, which is composed of the two symbols corresponding to the current trellis state and branch and the history of six decision feedback symbols. The state history is stored in a 32×30 b RAM.

The dynamic range of the state metrics is kept small by subtracting the minimum state metric at every trellis stage. Furthermore, all winning state metrics are forwarded to the soft-output unit, where metrics corresponding to different hypotheses for all modulated bits are compared to obtain their respective log-likelihood ratio (LLR) values, as shown in (2).

IV. Channel Decoder and Incremental Redundancy

The DEC block of the BB-ASIC is depicted in Fig. 9. It consists of a controller and the signal processing units for channel decoding and autonomous IR processing. To ease memory access and control, fragmented memories were employed. Depending on the current code block, either a Viterbi or a turbo decoder is used. Legacy GSM/GPRS/EDGE modes use the Viterbi decoder, whereas E-EDGE uses the turbo decoder. Fig. 10 shows the high-level block diagram of the channel decoder architecture. It comprises an input buffer, dedicated turbo and Viterbi decoder cores, and an output buffer. Since only one of the two decoder cores is active at a time, we can reduce the overall memory overhead by a single intermediate memory instance. The turbo decoder core is based on our efficient turbo decoder implementation described in [15], which has been optimized for the binary parallel-concatenated 8-state

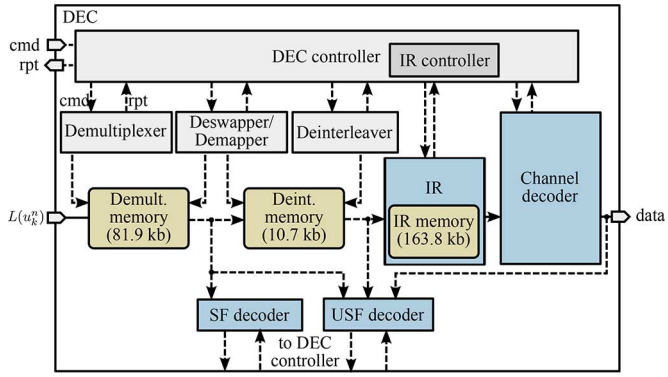

Fig. 9. Block diagram of decoder with channel decoder and autonomous incremental redundancy signal processing units.

convolutional turbo codes specified by the standard [16]. When decoding of a code block fails, the mobile station stores the corresponding LLRs and requests a retransmission from the base station. In the retransmission, the base station applies a different puncturing pattern. Thus, additional (redundant) information is available at the channel decoder input. This mechanism is called IR and aims to achieve a higher throughput. Our autonomous IR implementation relieves the software running the RLC/MAC layer from the burden of this process. The IR controller extracts relevant IR parameters from the header code block of a radio block. The controller is capable of uniquely identifying the remaining code blocks of the radio block. In addition, the controller holds information of each code block stored within the IR memory. In case of a match (new code block already exists in IR memory), the controller informs the IR processing unit accordingly. Otherwise, the IR processing unit is informed to only depuncture the block. The combination of LLRs is done by addition (chase combining).

V. Implementation and Measurement Results

The fabricated BB-ASIC is the key part of a complete E-EDGE solution comprising RF subsystem and an application processor. The RF subsystem is shown on the left-hand side of Fig. 1. It comprises all necessary components that make up a complete quad-band GSM RF transceiver platform. The RF subsystem exhibits state-of-the-art, field-proven performance in both the receiver and the transmitter. The RF-IC, which is an enhanced derivative of [17], is commercially available and under mass production for GSM and EDGE systems, but also supports the E-EDGE standard. The key characteristics of the BB-ASIC and the RF-IC are summarized in Table I. The ASIC can be connected to one or two of our RF transceivers [17] described in Section II to support single-antenna only or Rx-diversity.

A. Measurement and Testbed Setup

In this work, the single-antenna testbed of [18] which is shown in Fig. 11 has been extended to support Rx-diversity operation. The testbed of the first generation comprises a PowerPC processor on a Virtex4 FPGA which is acting as application processor connected via Ethernet/SSH to a host PC. In the latest testbed of the second generation, shown in Fig. 12,

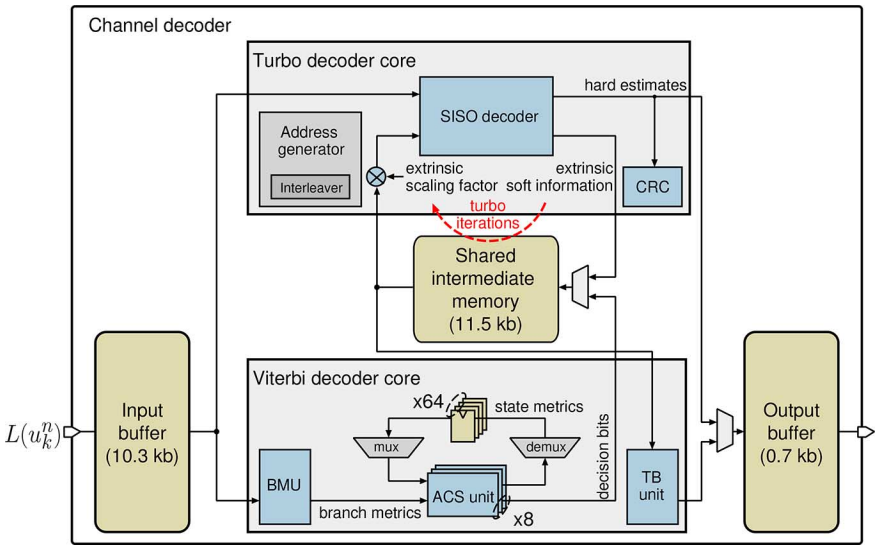

Fig. 10. High-level block diagram of channel decoder architecture.

TABLE I
PHYSICAL CHARACTERISTICS OF THE BB-ASIC AND THE ATTACHED RF-IC

	BB-ASIC	RF-IC
Technology	SMIC 130	SMIC 130
Package	QFN56	BGA 5x5
Core size	6 mm^2	n.a.
Gate count	800 kGE	-
RAM size	400 kbit	-
Supply voltage V_{DD}	1.2 V	3.7 V
Core operating frequency: f_C	104 MHz	26 MHz

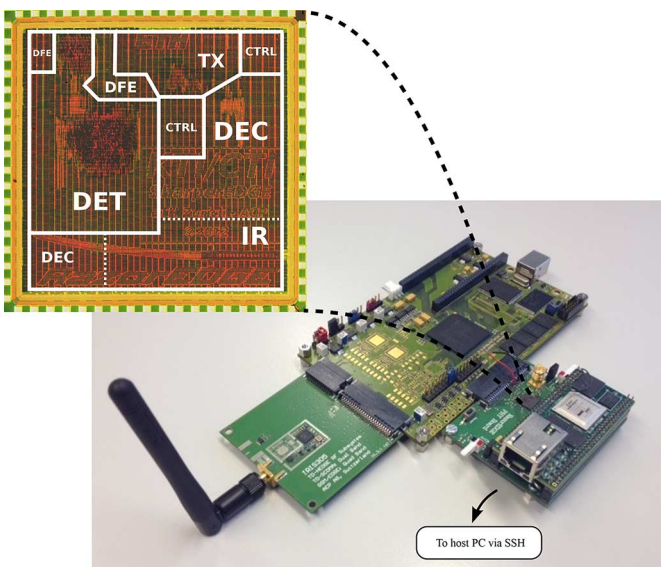

Fig. 11. Testbed of the first generation and die micrograph of the BB-ASIC for the single antenna case.

the RF-ICs are connected to a Xilinx Zynq development board and to a ML605 FPGA board, which hosts the logic of the BB-ASIC described in this paper. One core of the Zynq runs a real-time operating system controlling the BB-ASIC via L1CTL commands over an SPI interface. The second core runs

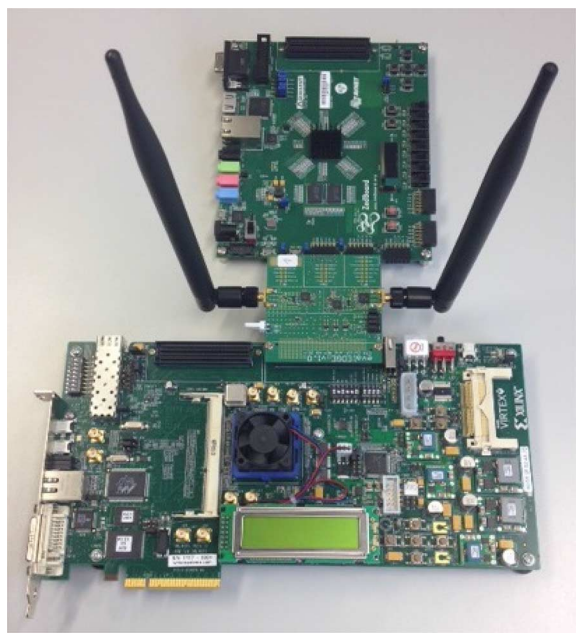

Fig. 12. Testbed of the second generation for Rx-diversity measurements with zynq (on Zedboard) and ASIC logic on the ML605 FPGA board.

an embedded Linux OS which displays or forwards the data to the higher layers in the protocol stack or to a connected PC for evaluation purposes.

At the antenna input of the RF transceiver, standard compliant RF signals are supplied, which are generated by a channel emulator (Propsim C8) and a wireless protocol tester (Agilent 8960). For the performance and power measurements, the testcases shown in Table II are chosen. These testcases are a representative subset of the vast amount of requirements specified in [19].

In order to achieve the rigorous 3GPP requirements, a joint configuration of RF transceiver and the baseband is essential. Our configuration approach is explained in Section V-B.

TABLE II
MEASURED TESTCASES FOR SINGLE-ANTENNA (RX1) AND DUAL-ANTENNA (RX2) OPERATION

Nr.	Rx-div.	payload	impairment	scheme	mod.	channel	Fig.
1	RX1	voice	sensitivity	TCH/FS	GMSK	ST	13
2	RX1	data	sensitivity	MCS9	8PSK	ST	14
3	RX1	data	AC interference	DAS5	8PSK	TU50nFH	17
4	RX1	data	sensitivity	DAS10	32-QAM	TU50nFH	16
5	RX2	voice	sensitivity	TCH/FS	GMSK	ST	13
6	RX2	data	sensitivity	MCS9	8PSK	ST	14
7	RX2	data	CC interference	MCS1	GMSK	TU50nFH	18
8	RX2	data	sensitivity	DAS10	32-QAM	TU50nFH	16

TABLE III
JOINT CONFIGURATION PARAMETERS FOR THE BB-ASIC AND THE RF-IC

	RF-IC	BB-ASIC				power consumption	
Testcase	gain	channel shortening	DFE coeff. set	space-time filter	SOVE (states / D)	RF-IC [mW]	baseband [mW]
1	max.	on	6	off	8 / 3	35.3	3.9
2	max. - 18 dB	on	6	off	8 / 1	35.3	3.9
3	max. - 11 dB	on	3	off	8 / 1	35.3	3.9
4	max. - 19 dB	on	6	off	32 / 1	35.3	5.5
5	max.	on	6	off	8 / 3	52.7	10.9
6	max. - 16 dB	on	3	off	8 / 1	52.7	10.9
7	max. - 15 dB	off	6	on	8 / 3	52.7	10.9
8	max. - 15 dB	on	6	off	32 / 1	52.7	14.0

B. Joint Configuration of RF Transceiver and BB-ASIC

Different testcases require different settings of the RF-IC and the BB-ASIC. In Table III the settings of both components are shown for the different testcases of Table II. The configuration parameters for the BB-ASIC include enabling or disabling of channel shortening and space time filtering as well as the configuration of the SOVE. The configuration of the SOVE is given by the number of trellis states and the decision delay D. Both SOVE parameters are set according to the detected modulation type or can be set manually. The configuration of the DFE is given by the selection of one of the eight pre-programmed FIR filter coefficient sets, whose cut-off frequency ranges from 54 to 135 kHz. The cutoff frequency is linearly mapped to the strength of the detected adjacent channel (AC). A narrow filter is favorable for AC interference suppression, but deteriorates the sensitivity performance, due to the inserted inter-symbol-interference. The narrowest 54 kHz filter allows an AC to be 21 dB stronger than the desired signal, at a sensitivity loss of 1.2 dB. The coefficient set can be set automatically according to the result of the AC detection, or manually. On the RF-IC the gain is adjusted adaptively according to the Rx power estimation in the DFE of the BB-ASIC.

C. Performance Measurement Results

The measured frame erasure rate (FER) for voice channel (TCH/FS) and block-error rate (BLER) performance for packet data channels has been assessed for the testcaes in Table II. Figs. 13–18 show the measured performance plots for the testcases. *RX1* denotes single-antenna measurement, while *RX2* denotes measurements, where the signal is received on both antennas. The bold markers in the figures denote the 3GPP reference performance requirements. The testcase belonging to each performance plot is notated in the respective legend.

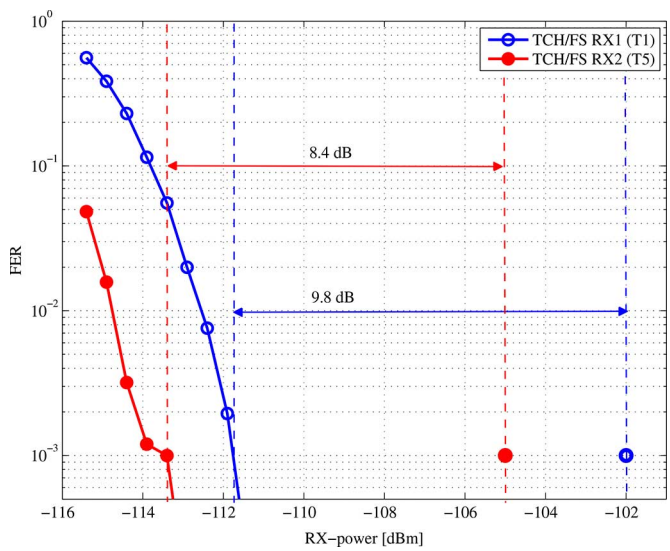

Fig. 13. Measured sensitivity performance for the GMSK modulated GSM voice. Static channel.

1) Sensitivity Performance: The measurements for single antenna and Rx-diversity on the static channel (ST) profile are shown in Fig. 13. The margin for the voice case is close to 10 dB even in the single-antenna measurement. From Fig. 13, it can also be seen that the use of Rx-diversity pushes the sensitivity performance further down to −113.4 dBm due to the array gain. In Table IV, the sensitivity is compared with state-of-the-art GSM/EDGE transceivers. Since this work is the first reported

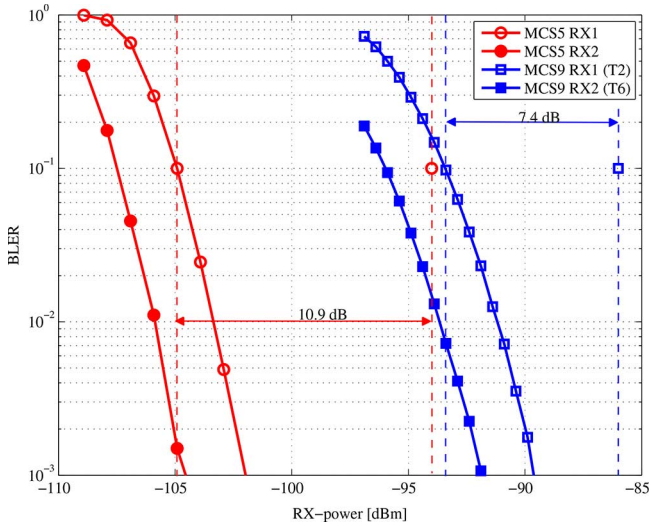

Fig. 14. EDGE measured sensitivity performance for the 8-PSK modulated schemes MCS5 and MCS9. Static channel.

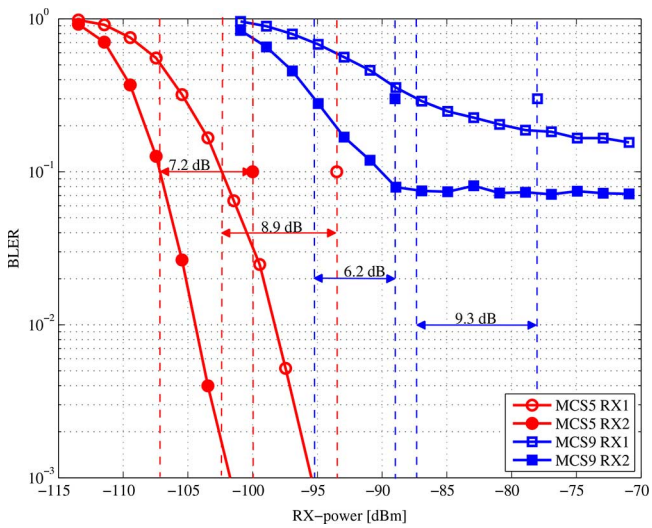

Fig. 15. EDGE measured sensitivity performance for the 8-PSK modulated schemes MCS5 and MCS9. TU50 channel, no frequency hopping.

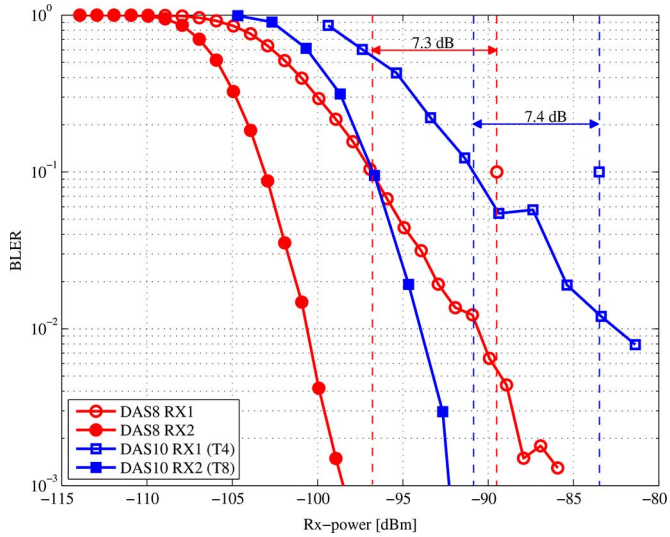

Fig. 16. E-EDGE measured sensitivity performance for the 16-QAM modulated DAS8 scheme and the 32-QAM modulated DAS10 scheme. TU50 channel, no frequency hopping.

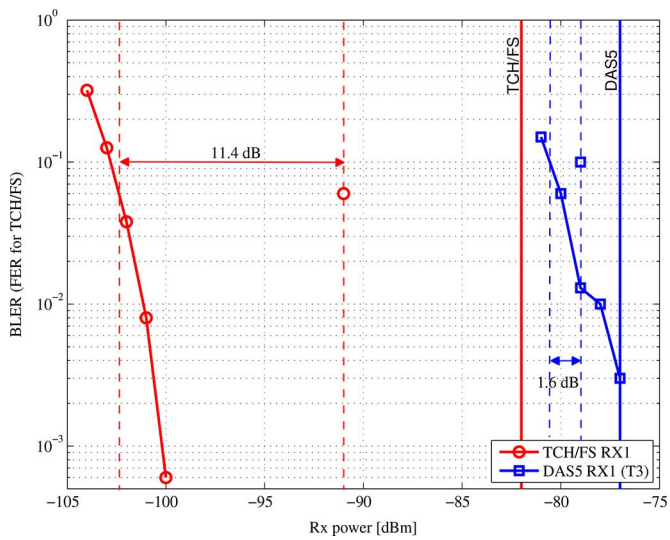

Fig. 17. Measured interference performance for a TCH/FS and a DARP1 scenario for the 8-PSK modulated DAS5 scheme in single-antenna mode. The solid vertical lines indicate the power of the interferer.

E-EDGE solution, comparison is only possible for the voice sensitivity (testcase 1). The sensitivity performance of our E-EDGE solution lies in a competitive range and shows better sensitivity than [20], [1], [21]. Our system shows a sensitivity of 1.2 dB below the transceiver of [22], which reports a sensitivity of −113 dBm (Class II RBER) and is based on a noise figure of 2.4 dB, while our RF-IC has a noise figure of 4 dB [17] including front-end insertion loss. Figs. 14 and 15 show the performance in EDGE mode for the static and the TU50 channel profiles, respectively. In both cases, the requirements are exceeded by a margin of at least 6.4 dB. Fig. 16 shows the performance of the E-EDGE mode with the highest order modulation (32-QAM), represented by testcases 4 and 8. In these testcases, a substantial diversity gain is observable.

2) Interference Performance: The adjacent- and co-channel interference performance has been measured for TCH/FS, MCS1 and DAS5. In Fig. 17 the interference performance is shown. Thanks to the interference cancellation combined with the SOVE, more than 11 dB margin has been achieved for GMSK and 1.6 dB for the DAS5 mode despite the challenge of additional ISI caused by the narrow AC-filter bandwidth. The toughest performance requirements are the DARP 2 testcases [19], which allow a co-channel interferer of up to 11.5 dB stronger than the desired channel for the MCS1 (GMSK) case. This testcase is shown in Fig. 18, where it can be seen that the use of space-time interference cancellation allows even such a requirement to be exceed by 4.5 dB. In this testcase, the channel shortening filter is bypassed and the space time filter is turned on. Furthermore our solution exceeds the most demanding co-channel testcase by a margin of 4.5 dB.

D. Power Measurement Results

The power consumption of the BB-ASIC was measured on an ASIC tester (Verigy 93000) for different timeslot

TABLE IV
SENSITIVITY PERFORMANCE COMPARISON [dBm]

Testcase	3GPP BLER/FER [%]	3GPP	[20]	[1]	[23]	[24]	[21]	[22]	This work
1	0.1	-102	-110	-110.1	-111.4	-111	-111.3	-113[a]	**-111.8**
2	10	-86	not available						**-93.4**
3	10	-79 (AC: -77)	not supported						**-80.6**
4	10	-84							**-91.4**
5	0.1	-105	not supported						**-113.4**
6	10	-89							**-96**
7	10	-92.4 (CC: -89.9)							**-96.9**
8	10	[t.b.d.]							**-97.1**

[a]Residual bit error rate (RBER) Class II. No FER given.

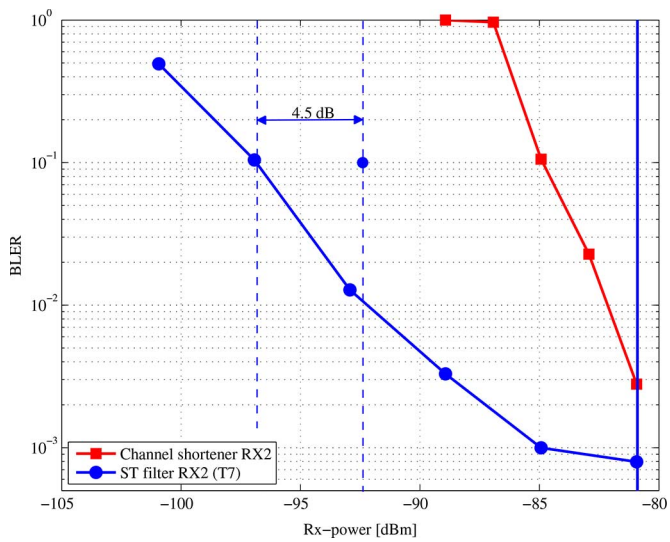

Fig. 18. Impact of space-time interference cancellation in Rx-diversity mode. Measured interference performance for a DARP2 scenario with GMSK modulated MCS1. The solid vertical line indicates the power of the interferer.

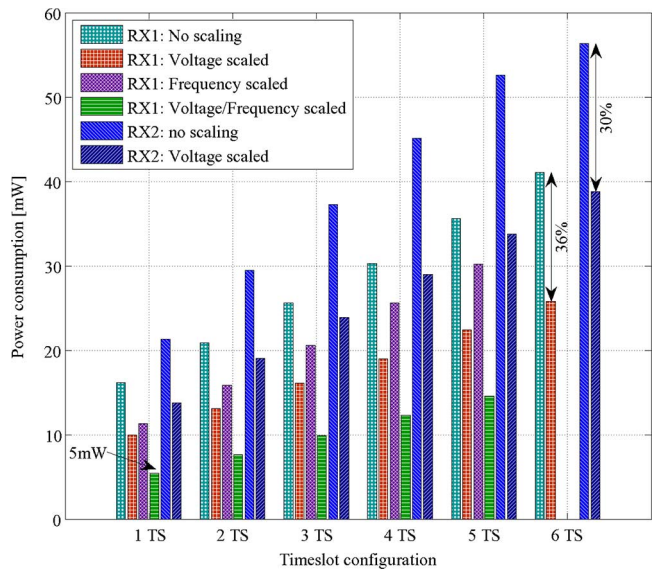

Fig. 19. Power consumption of the BB-ASIC for different Rx and timeslot configurations in a 32-QAM testcase.

configurations and modulation and coding schemes. The highest clock frequency (104 MHz) is required when the specified maximum of six time slots are used or when Rx-diversity is enabled. In these modes, timing margins still allow the voltage to be scaled from 1.2 V to 0.83 V to push the power consumption from 56 to 39 mW (-30%) and from 41 to 26 mW (-36%) with and without Rx-diversity, respectively. For configurations with less than six timeslots, both voltage- and frequency-scaling from 104 to 52 MHz can be applied, leading to 5.5 mW for processing a single 32-QAM EGPRS2-A timeslot. Fig. 19 shows the power consumption of the ASIC for different timeslot configurations with and without scaling. The minimum power consumption for the different testcases is summarized in Table III. It can be seen, that the power consumption for the 32-QAM mode is higher than for GMSK and 8PSK modes, due to the higher equalization and decoding effort. The power consumption of the RF-IC has been measured in the testbed, and is also shown in Table III. In single antenna mode, power consumption of the BB-ASIC ranges from 3.9 to 5.5 mW at $V_{\mathrm{DD}} = 0.83$ V and $f_{\mathrm{C}} = 52$ MHz, which is below 15% of the power consumption of the RF-IC. In Rx-diversity mode the power consumption of the BB-ASIC ranges from 10.9 to 14.5 mW at $V_{\mathrm{DD}} = 0.96$ V and $f_{\mathrm{C}} = 104$ MHz, which is below 26 % of the power consumption of the RF-IC.

VI. CONCLUSION

In this paper, we have shown that, with a dedicated hardware architecture, the baseband processing of E-EDGE using complex high-performance DSP algorithms can be optimized to reduce power consumption to vanish in comparison to that of a low-power RF-IC solution. The reported ASIC is the first 32-QAM capable Evolved EDGE baseband with downlink diversity. Thanks to sophisticated signal processing in all modes, it meets the standard requirements with significant margin in all modes. It achieves the stringent DARP2 requirements for Rx-diversity and achieves GSM voice sensitivity close to -112 dB in standard single-antenna mode, when combined with an RF subsystem complete with antenna switches, receive SAW filters and the RF-IC. At the same time, the dedicated hardware implementation maintains extremely low power consumption, fitting into a die area of 6 mm^2 in 130 nm SMIC.

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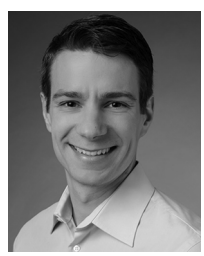

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