Sitronix

ST7565P

65 x 132 Dot Matrix LCD Controller/Driver

FEATURES

- Directly display RAM data through Display Data RAM
- RAM capacity : 65 x 132 = 8580 bits
- Display duty selectable by select pin
  1/65 duty : 65 common x 132 segment
  1/49 duty : 49 common x 132 segment
  1/33 duty : 33 common x 132 segment
  1/55 duty : 55 common x 132 segment
  1/53 duty : 53 common x 132 segment
- High-speed 8-bit MPU interface:
  ST7565P can be connected directly to both the 80x86 series MPUs and the 6800 series MPUs.
  Serial interface (SPI-4) is also supported.
- Abundant command functions:
  Display data read/write, display ON/OFF, Normal/ Reverse display mode, page address set, display start line set, column address set, status read, display all points ON, LCD bias set, electronic volume, read-modify-write, set segment driver direction, power save mode, set common output direction, set V0 regulator internal resistor ratio.
- Built-in low power consumption power circuits: Booster, Regulator and Follower.
- Booster circuit supports 2X/3X/4X/5X/6X boost level. External reference voltage (VDD2) for booster circuits.
- High-accuracy Regulator with contrast control (EV) and built-in V0 voltage regulator resistors. (Thermal gradient = –0.05%/℃)
- Built-in Follower for LCD bias voltages.
- Embedded R-C oscillation circuit. Support external clock input.
- Extremely low power consumption:
  60uA (operating, bare chip with internal power)
  (V_{DD}–V_{SS} = V_{DD2}–V_{SS} = 3V, Booster x4, V0 = 11V).
  Condition: display pattern is “OFF”; use normal mode.
- Wide application voltage range:
  Logic power: V_{DD} – V_{SS} = 1.8V to 3.3V (typical)
  Analog power: V_{DD2} – V_{SS} = 2.4V to 3.3V (typical)
  Maximum Booster limitation: V_{OUT} = 13.5V
  LCD Vop: V0 – V_{SS} = 3.0V to 12.0V
- Wide operation temperature range: –30 to 85℃
- CMOS process.
- Package type: Bare chip (COG) and TCP.
- ST7565P is not designed for resistance to light or resistance to radiation.

GENERAL DESCRIPTION

ST7565P is a single-chip dot-matrix LCD driver that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal Display Data RAM and this chip generates LCD driving signals independent of the microprocessor. Each data bits (65x132) of the internal Display Data RAM is 1-to-1 correspondence with each pixels (65x132) on the LCD panel, therefore, ST7565P enables displays with a high degree of freedom.

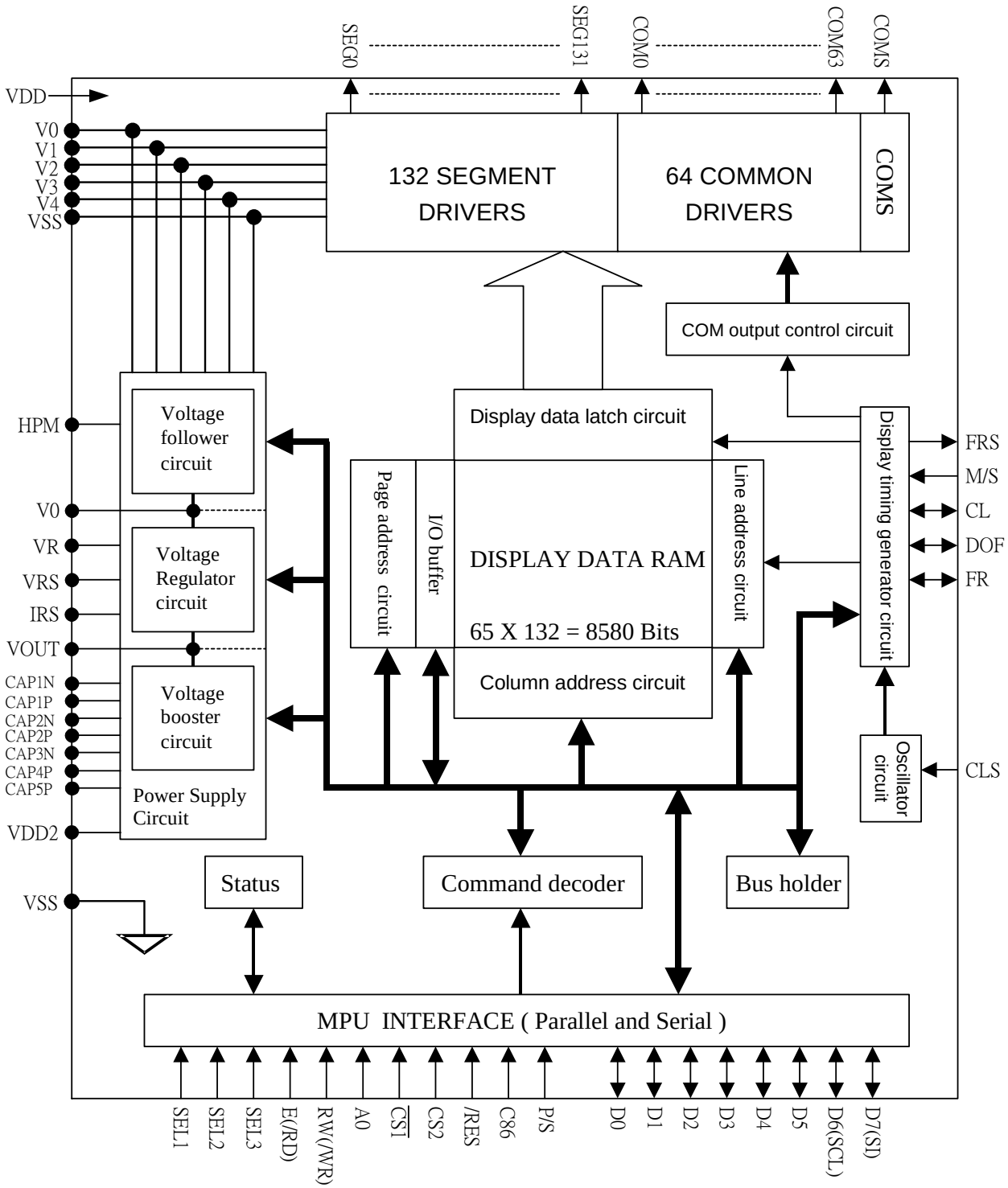
Moreover, the display area can be extended horizontally by using Master/Slave feature.

With the abundant embedded circuits (2~6 times booster circuit, V0 regulator with contrast control for LCD voltage adjustment, voltage follower with bias selection and R-C oscillation circuit), ST7565P can be used to create a display system with the lowest power consumption and the fewest external components for high-performance portable devices.

PART NO.	VRS temperature gradient	VRS range
ST7565P	-0.05%/℃	2.1V ± 0.03V

ST7565P	**6800 , 8080 , 4-Line interface**	

BLOCK DIAGRAM



PIN DESCRIPTIONS

Power Supply Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>VDD</td><td>Power Supply</td><td>Power supply</td><td>13</td></tr>
<tr><td>VDD2</td><td>Power Supply</td><td>Power supply</td><td>10</td></tr>
<tr><td>VSS</td><td>Power Supply</td><td>Ground</td><td>2</td></tr>
<tr><td>VRS</td><td>Power Supply</td><td>This is the internal-output VREG power supply for the LCD power supply voltage regulator.</td><td>2</td></tr>
<tr><td>V0, V1, V2, V3, V4,Vss</td><td>Power Supply</td><td>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below.

V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧Vss

When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/65 DUTY</th><th>1/49 DUTY</th><th>1/33 DUTY</th><th>1/55 DUTY</th><th>1/53 DUTY</th></tr>
<tr><td>V1</td><td>8/9*V0,6/7*V0</td><td>7/8*V0,5/6*V0</td><td>5/6*V0,4/5*V0</td><td>7/8*V0,5/6*V0</td><td>7/8*V0,5/6*V0</td></tr>
<tr><td>V2</td><td>7/9*V0,5/7*V0</td><td>6/8*V0,4/6*V0</td><td>4/6*V0,3/5*V0</td><td>6/8*V0,4/6*V0</td><td>6/8*V0,4/6*V0</td></tr>
<tr><td>V3</td><td>2/9*V0,2/7*V0</td><td>2/8*V0,2/6*V0</td><td>2/6*V0,2/5*V0</td><td>2/8*V0,2/6*V0</td><td>2/8*V0,2/6*V0</td></tr>
<tr><td>V4</td><td>1/9*V0,1/7*V0</td><td>1/8*V0,1/6*V0</td><td>1/6*V0,1/5*V0</td><td>1/8*V0,1/6*V0</td><td>1/8*V0,1/6*V0</td></tr>
</table>
</td><td>10</td></tr>
</table>

LCD Power Supply Pins

Pin Name	I/O	Function	No. of Pins
CAP1P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	4
CAP1N	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.	2
CAP2P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	2
CAP2N	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.	2
CAP3P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	2
CAP4P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	2
CAP5P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	2
VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD	2
VR	I	Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider. IRS = “L” : the V0 voltage regulator internal resistors are not used. IRS = “H” : the V0 voltage regulator internal resistors are used.	2

System Bus Connection Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>D5 to D0
D6 (SCL)
D7 (SI)</td><td>I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface (SPI-4) is selected (P/S = “L”) :
D7 : serial data input (SI) ; D6 : the serial clock input (SCL).
D0 to D5 should be connected to VDD or floating.
When the chip select is not active, D0 to D7 are set to high impedance.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command.
A0 = “H”: Indicates that D0 to D7 are display data.
A0 = “L”: Indicates that D0 to D7 are control data.</td><td>1</td></tr>
<tr><td>/RES</td><td>I</td><td>When /RES is set to “L”, the register settings are initialized (cleared).
The reset operation is performed by the /RES signal level.</td><td>1</td></tr>
<tr><td>/CS1
CS2</td><td>I</td><td>This is the chip select signal. When /CS1 = “L” and CS2 = “H”, then the chip select becomes active, and data/command I/O is enabled.</td><td>2</td></tr>
<tr><td>/RD
(E)</td><td>I</td><td>• When connected to 8080 series MPU, this pin is treated as the “/RD” signal of the 8080 MPU and is LOW-active.
The data bus is in an output status when this signal is “L”.
• When connected to 6800 series MPU, this pin is treated as the “E” signal of the 6800 MPU and is HIGH-active.
This is the enable clock input terminal of the 6800 Series MPU.</td><td>1</td></tr>
<tr><td>/WR
(R/W)</td><td>I</td><td>• When connected to 8080 series MPU, this pin is treated as the “/WR” signal of the 8080 MPU and is LOW-active.
The signals on the data bus are latched at the rising edge of the /WR signal.
• When connected to 6800 series MPU, this pin is treated as the “R/W” signal of the 6800 MPU and decides the access type :
When R/W = “H”: Read.
When R/W = “L”: Write.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>This is the MPU interface selection pin.
C86 = “H”: 6800 Series MPU interface.
C86 = “L”: 8080 Series MPU interface.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin configures the interface to be parallel mode or serial mode.
P/S = “H”: Parallel data input/output.
P/S = “L”: Serial data input.
The following applies depending on the P/S status:
<table><tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr><tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>X</td></tr><tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table>When P/S = “L”, D0 to D5 must be fixed to “H”.
/RD (E) and /WR (R/W) are fixed to either “H” or “L”.
The serial access mode does NOT support read operation.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>CLS</td><td>I</td><td>Selection pin to enable or disable the internal display clock oscillator circuit.
CLS = “H” : use internal oscillator circuit .
CLS = “L” : use external clock input (internal oscillator is disabled).
When CLS = “L”, input the external display clock through the CL terminal.</td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the ST7565P Series chips.
Master operation outputs the timing signals that are required for the LCD display, while slave operation input the timing signals required for the liquid crystal display.
That synchronized the liquid crystal display system between Master and Slave.
M/S = “H” Master operation
M/S = “L” Slave operation
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>DOF</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Enabled
Disabled</td><td>Enabled
Enabled</td><td>Output
Input</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Disabled
Disabled</td><td>Disabled
Disabled</td><td>Input
Input</td><td>Input
Input</td><td>Input
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the M/S and CLS status.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Output
Input</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Input
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>O</td><td>This is the liquid crystal alternating current signal terminal.</td><td>1</td></tr>
<tr><td>/DOF</td><td>O</td><td>This is the LCD blanking control terminal.</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>Reserved</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V0 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal</td><td>1</td></tr>
<tr><td>/HPM</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
/HPM = “H”: Normal mode
/HPM = “L”: High power mode</td><td>1</td></tr>
<tr><td>SEL3
SEL2
SEL1</td><td>I</td><td>These pins are DUTY selection.
<table>
<tr><th>SEL 3 , 2 , 1</th><th>DUTY</th><th>BIAS</th></tr>
<tr><td>0 , 0 , 0</td><td>1/65</td><td>1/9 or 1/7</td></tr>
<tr><td>0 , 0 , 1</td><td>1/49</td><td>1/8 or 1/6</td></tr>
<tr><td>0 , 1 , 0</td><td>1/33</td><td>1/6 or 1/5</td></tr>
<tr><td>0 , 1 , 1</td><td>1/55</td><td>1/8 or 1/6</td></tr>
<tr><td>1 , 0 , 0</td><td>1/53</td><td>1/8 or 1/6</td></tr>
<tr><td>1, X , X</td><td>-----</td><td>-----</td></tr>
</table></td><td>3</td></tr>
<tr><td>TEST0 ~ 5</td><td>I</td><td>These are terminals for IC testing.
They are set to open.</td><td>6</td></tr>
</table>

LCD Driver Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>These are the LCD segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from Vss, V3, V2 and V0.
<table>
<tr><th rowspan="2">RAM DATA</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td>Power save</td><td></td><td colspan="2">Vss</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0
to
COMn</td><td>O</td><td>Through a combination of the contents of the scan data and with the FR signal, a single level is selected from Vss, V4, V1 and V0.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>Vss</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td>Power save</td><td></td><td>Vss</td></tr>
</table></td><td>67</td></tr>
<tr><td>COMS</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.</td><td>2</td></tr>
</table>

ST7565P I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
TEST0…5	**Floating**
V_{DD}, V_{DD2}, V_{SS}, V_{OUT}, VR, VRS	**<100Ω**
V0, V1, V2, V3, V4, CAP1P, CAP1N, CAP2P, CAP2N, CAP3P, CAP4P, CAP5P	**<500Ω**
/CS1, CS2, CL, E, R/W, A0, D0…D7,	**<1KΩ**
FR, /DOF, C86, P/S, M/S, /HPM,SEL1…SEL3, CLS, IRS	**<5KΩ**
/RES	**<10KΩ**

DESCRIPTION OF FUNCTIONS

The MPU Interface

Selecting the Interface Type

With the ST7565P chips, data transfers are done through an 8-bit parallel data bus (D7 to D0) or through a serial data input (SI). By setting the P/S terminal to “H” or “L”, it sets the access mode to be either parallel or serial mode as shown in Table 1.

Table 1

P/S	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
H: Parallel mode	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L: Serial mode	/CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

“—” indicates fixed to either “H” or to “L”

The Parallel Interface

When the parallel interface has been selected (P/S =“H”), the interface can be connected directly to either 8080 or 6800 Series MPU (as shown in Table 2) by setting the C86 terminal to either “H” or “L”.

Table 2

C86 (P/S=H)	/CS1	CS2	A0	E(/RD)	R/W(/WR)	D7~D0
H: 6800 Series	/CS1	CS2	A0	E	R/W	D7~D0
L: 8080 Series	/CS1	CS2	A0	/RD	/WR	D7~D0

Moreover, data bus signals are recognized according to the combination of A0, /RD (E), /WR (R/W) signals. The functions are shown as below in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	R/W	/RD	/WR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

The Serial Interface

When the serial interface has been selected (P/S = “L”) then when the chip is in active state (/CS1 = “L” and CS2 = “H”) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = “H”, the data is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is a serial interface signal chart.

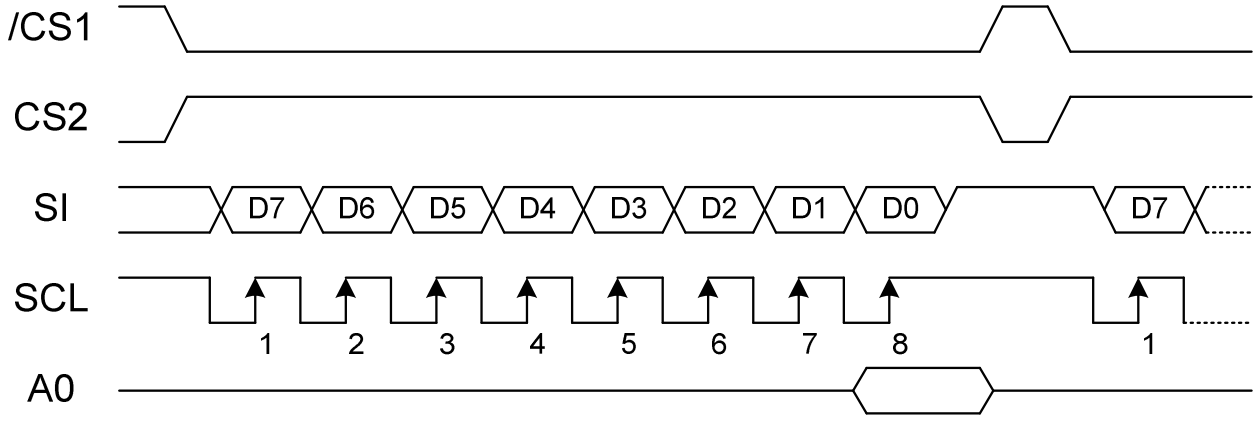


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The ST7565P have two chip select terminals: /CS1 and CS2. The MPU interface or the serial interface is enabled only when /CS1 = “L” and CS2 = “H”.

When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, /RD, and /WR inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

The Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (tCYC) requirement alone in accessing the ST7565P. Wait time may not be considered. And, in the ST7565P, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. Internal data bus.
For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.
There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.
This relationship is shown in Figure 2.

The Busy Flag

When the busy flag is “1” it indicates that the ST7565P is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (tCYC) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

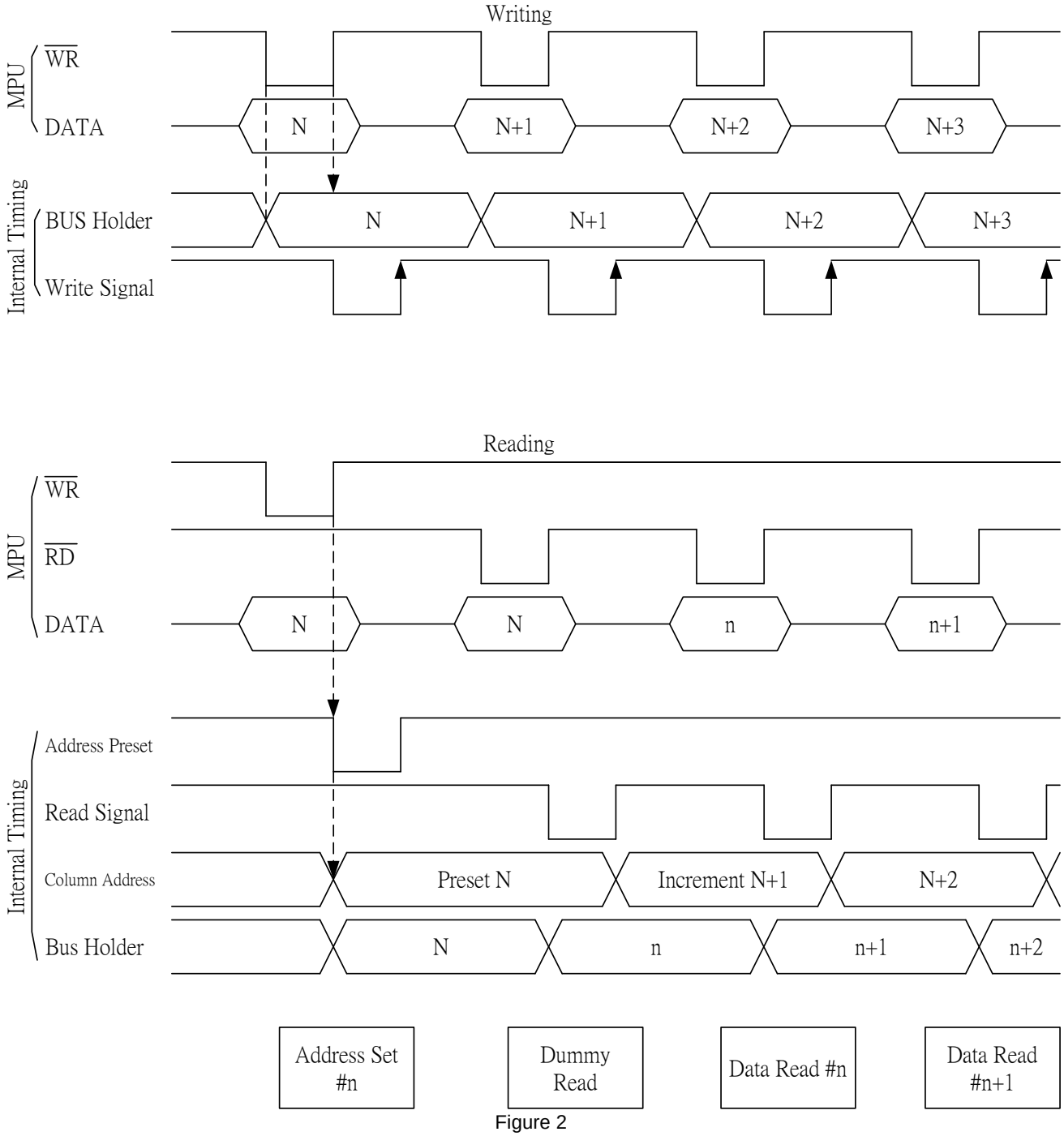


Figure 2

Display Data RAM

The display data RAM stores the dot data for the LCD. It has a 65 (8 page x 8 bit +1) x 132 bit structure. As is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD display common direction; there are few constraints at the time of display data transfer when multiple ST7565P are used, thus and display structures can be created easily and with a high degree of freedom.

Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

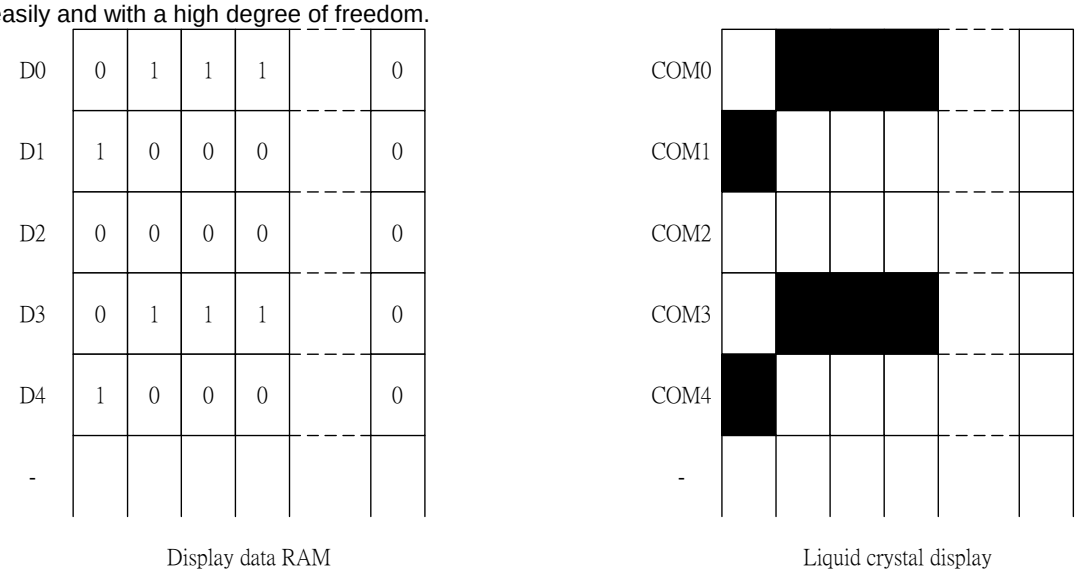


Figure 3

The Page Address Circuit

Page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is a special RAM for icons, and only display data D0 is used (refer to Figure 4)

The Column Addresses

The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementing of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respective both the page address and the column address.

Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized. As is shown in Figure 4.

Table 4

SEG Output ADC	SEG0		SEG 131
(D0) "0"	0 (H)	→ Column Address →	83 (H)
(D0) "1"	83 (H)	← Column Address ←	0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for ST7565P , the detail is shown page.11 The display area is a 65 line area for the ST7565P. If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

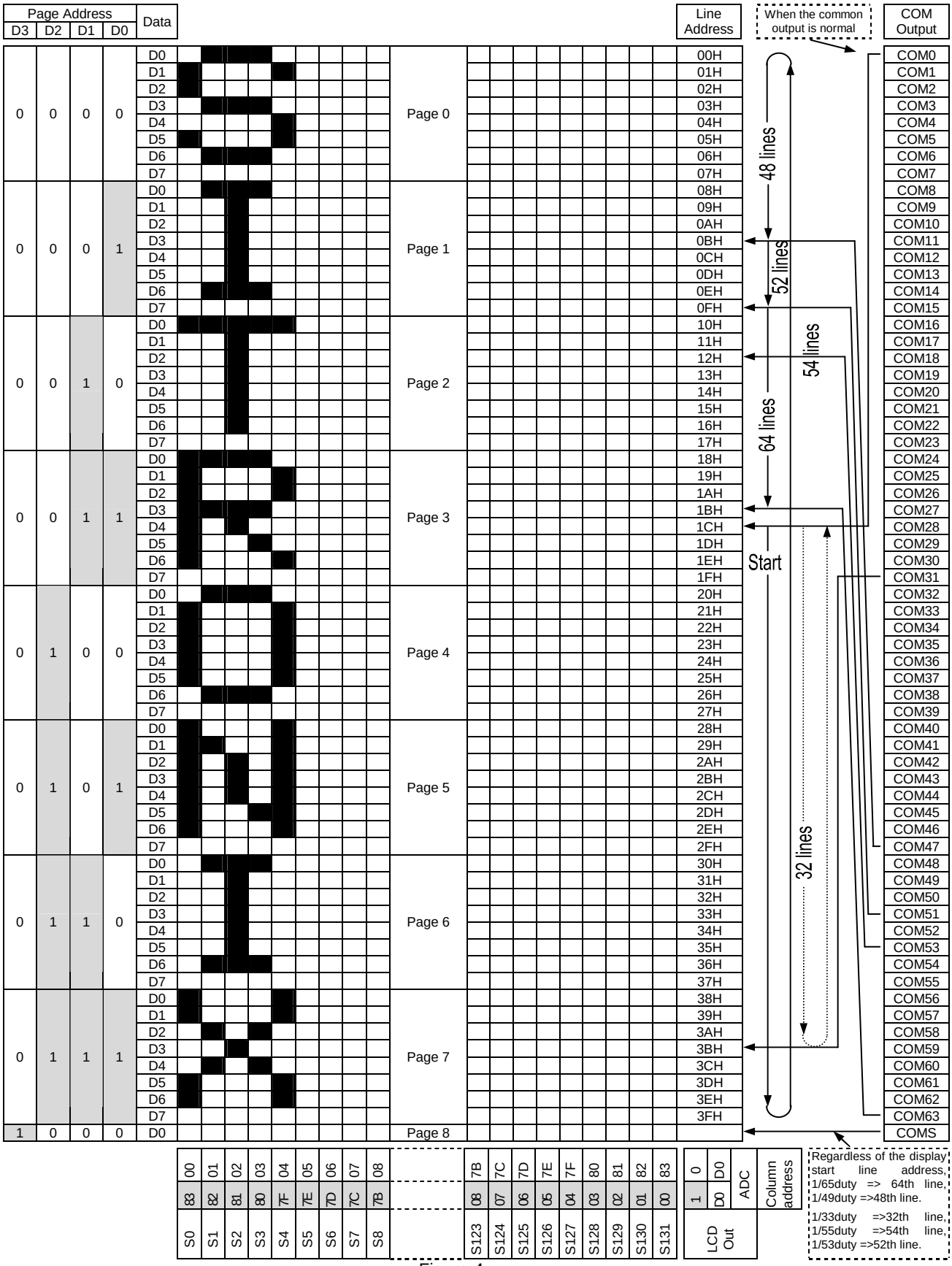

Page Address
D3 D2 D1 D0
Data
Line Address
When the common output is normal
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
48 lines
52 lines
54 lines
64 lines
32 lines
Start
COMS
Column address
ADC
LCD Out
Regardless of the display start line address,
1/65duty => 64th line,
1/49duty =>48th line.
1/33duty =>32th line,
1/55duty =>54th line,
1/53duty =>52th line.

Figure 4

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.

Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator is only enabled when M/S= “H” and CLS = “H”.

When CLS = “L” the oscillation stops, and the external clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive waveform

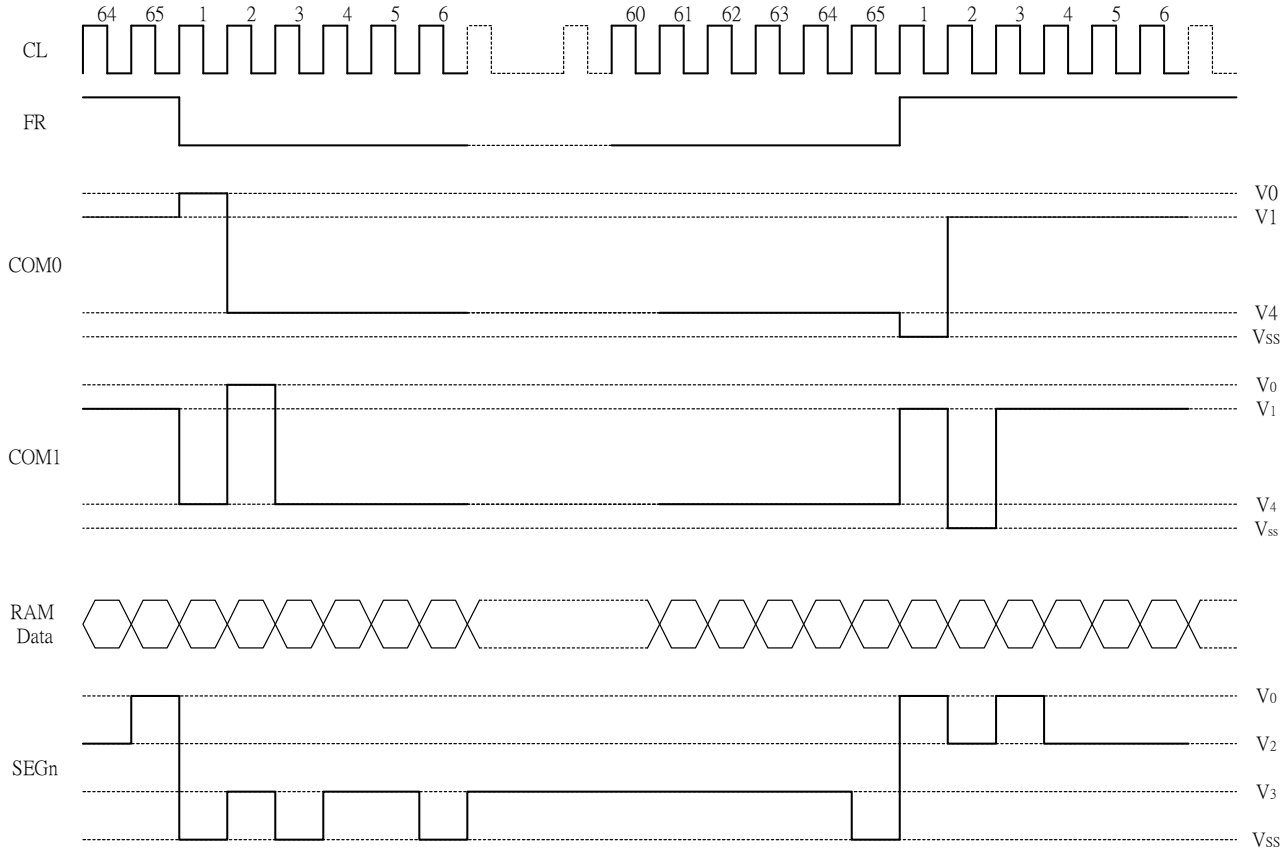


Figure 5

The Common Output Status Select Circuit

In the ST7565P chips, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

Status	COM Scan Direction				
	1/65 DUTY	**1/49 DUTY**	**1/33 DUTY**	**1/55 DUTY**	**1/53 DUTY**
Normal Reverse	COM0 → COM63 COM63 → COM0	COM0 → COM47 COM47 → COM0	COM0 → COM31 COM31 → COM0	COM0 → COM53 COM53 → COM0	COM0 → COM51 COM51 → COM0

Duty	COM dir	Common output pins							
		COM[0:15]	**COM[16:23]**	**COM[24:26]**	**COM[27:36]**	**COM[37:39]**	**COM[40:47]**	**COM[48:63]**	**COMS**
1/65	0	COM[0:63]							COMS
	1	COM[63:0]							COMS
1/49	0	COM[0:23]			reserve		COM[24:47]		COMS
	1	COM[47:24]			reserve		COM[23:0]		COMS
1/33	0	COM[0:15]		reserve				COM[16:31]	COMS
	1	COM[31:16]		reserve				COM[15:0]	COMS
1/55	0	COM[0:26]			reserve		COM[27:53]		COMS
	1	COM[53:27]			reserve		COM[26:0]		COMS
1/53	0	COM[0:25]			reserve		COM[26:51]		COMS
	1	COM[51:26]			reserve		COM[25:0]		COMS

The LCD Driver Circuits

The LCD driver circuits generates four voltage levels to drive the LCD. The combination of the display data, the COM scan signal and the FR signal produces the drive voltage of LCD.

Figure 6 shows examples of the SEG and COM output wave form.

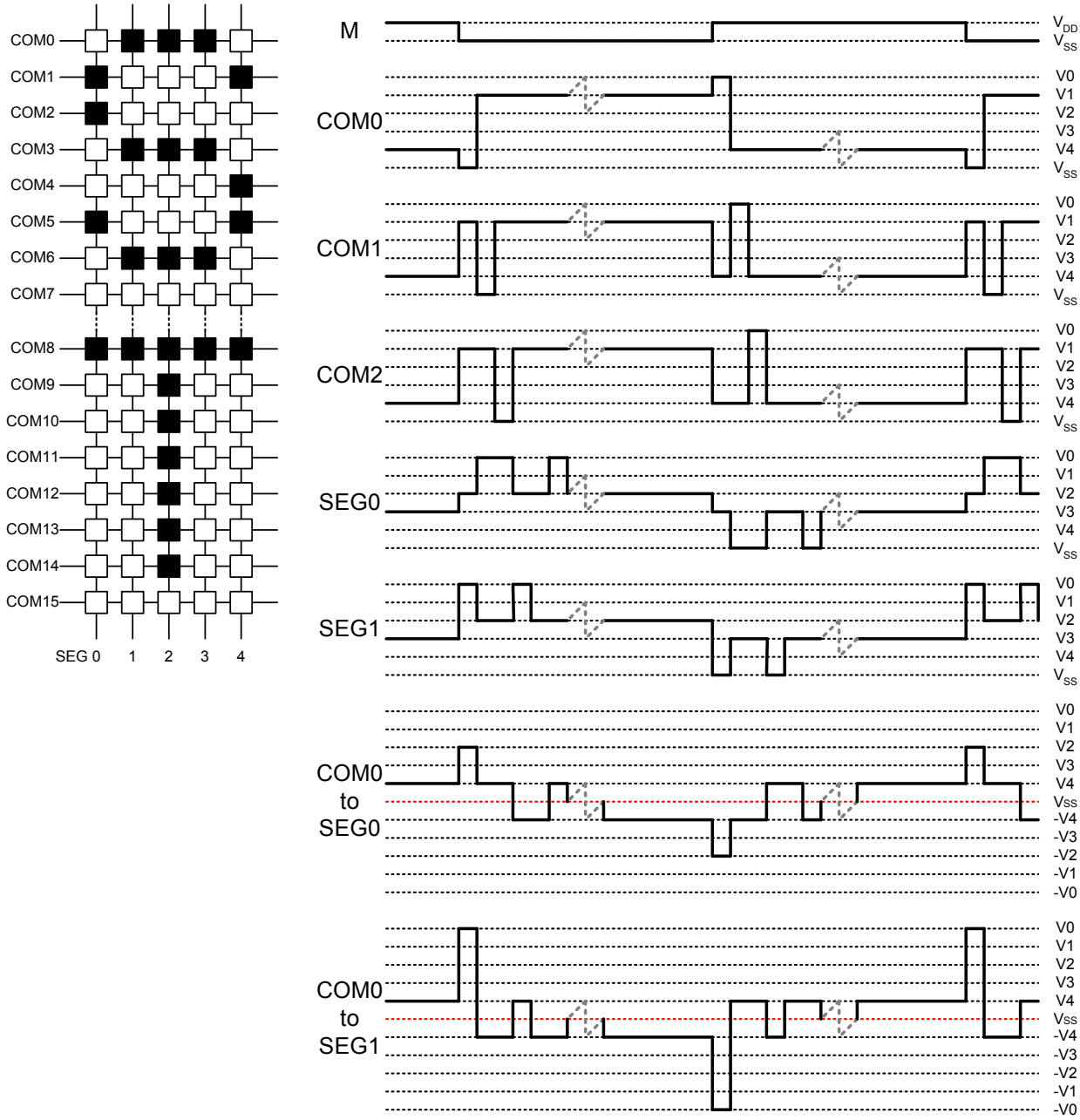


Figure 6

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 7

bit	function	Status "1"	Status "0"
D2	Booster circuit control bit	ON	OFF
D1	Voltage regulator circuit control bit (V/R circuit)	ON	OFF
D0	Voltage follower circuit control bit (V/F circuit)	ON	OFF

The Control Details of Each Bit of the Power Control Set Command

Table 8

Use Settings	D2	D1	D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Step-up voltage
Only the internal power supply is used	1	1	1	ON	ON	ON	V_{DD2}	Used
Only the voltage regulator circuit and the voltage follower circuit are used	0	1	1	OFF	ON	ON	V_{OUT}, V_{DD2}	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V_0, V_{DD2}	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V_0 to V_4	Open

Reference Combinations

* The "step-up system terminals" refer CAP1N, CAP1P, CAP2N, CAP2P, and CAP3N.
* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the ST7565P chips it is possible to product a 2X,3X,4X,5X or 6X step-up of the VSS – VDD2 voltage levels.
The step-up voltage relationships are shown in Figure 7.

6X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,between CAP1N and CAP5P, and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 6 times the voltage level between VSS and VDD2.

5X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 5 times the voltage level between VSS and VDD2.

4X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 4 times the voltage level between VSS and VDD2.

3X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P and between VDD2 and VOUT, and short between CAP3P and VOUT to produce voltages level in the positive direction at the VOUT terminal that is 3 times the voltage difference between VSS and VDD2.

2X step-up: Connect capacitor C1 between CAP1N and CAP1P, and between VDD2 and VOUT, leave CAP2N open, and short between CAP2P, CAP3P and VOUT to produce a voltage in the positive direction at the VOUT terminal that Is twice the voltage between VSS and VDD2.

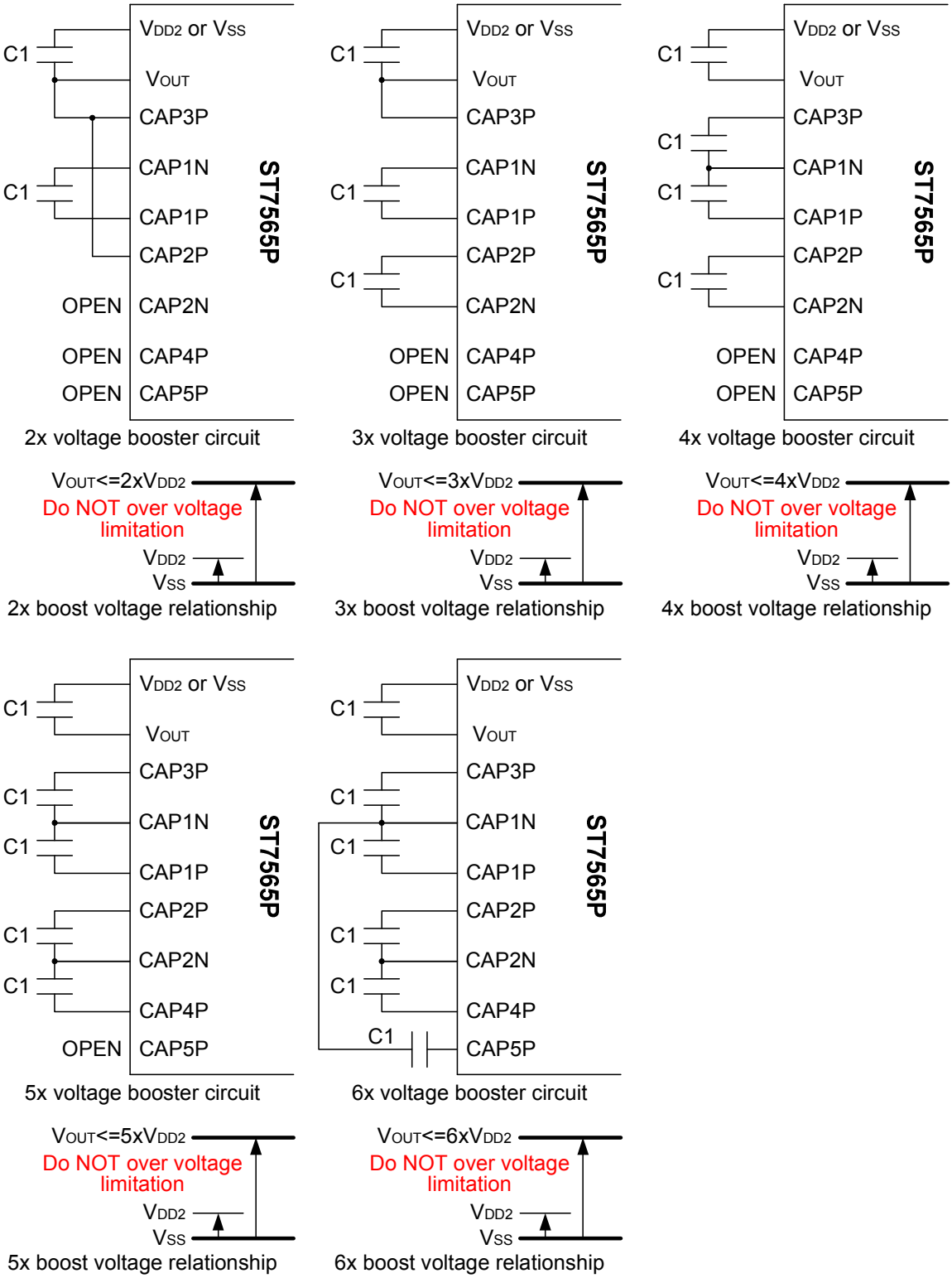


Figure 7

* The VDD2 voltage range must be set so that the VOUT terminal voltage does not exceed the absolute maximum rated value.
* The maximum voltage of the booster capacitor terminals are :
  VMAX: CAP5P > CAP4P > CAP3P > CAP2P > CAP1P > CAP2N = CAP1N.

The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V0 through the voltage regulator circuit. Because the ST7565P chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. (VREG thermal gradients approximate -0.05%/℃)

(A) When the V0 Voltage Regulator Internal Resistors Are Used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where | V0 | < | VOUT |.

$$V_0 = \left(1 + \frac{Rb}{Ra}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb}{Ra}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

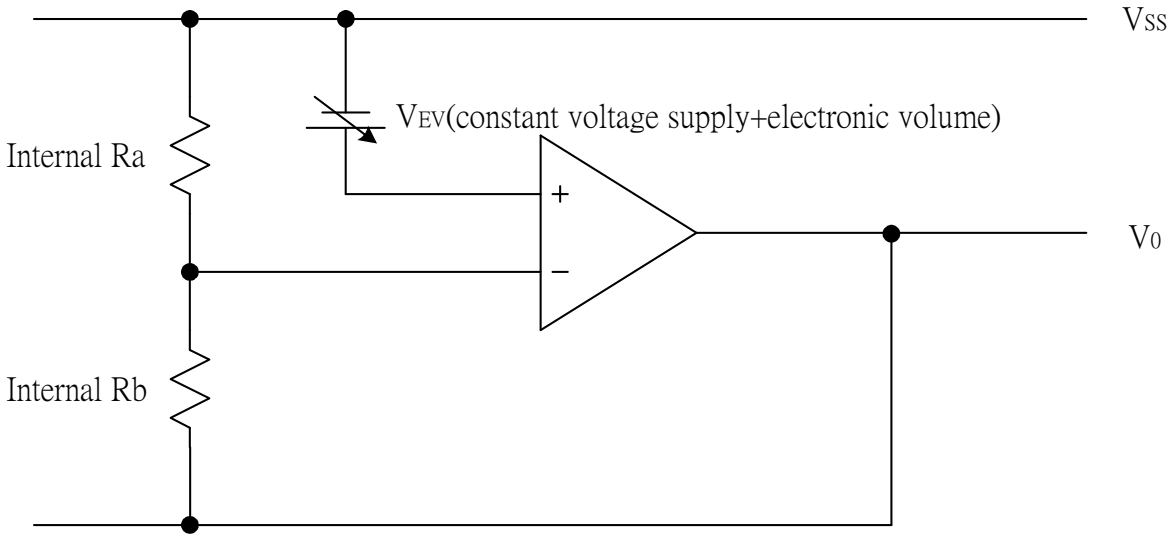


Figure 8

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25℃ is as shown in Table 9.

Table 9

Part no.	Equipment Type	Thermal Gradient	VREG
ST7565P	Internal Power Supply	–0.05 %/℃	2.1V

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume registers. Table 10 shows the value for α depending on the electronic volume register settings.
Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			:			:
			:			:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V0 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			ST7565P
D2	D1	D0	(1) –0.05 %/℃
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

Figures 9, 10 show V0 voltage measured by values of the internal resistance ratio resistor for V0 voltage adjustment and electric volume resister for each temperature grade model.

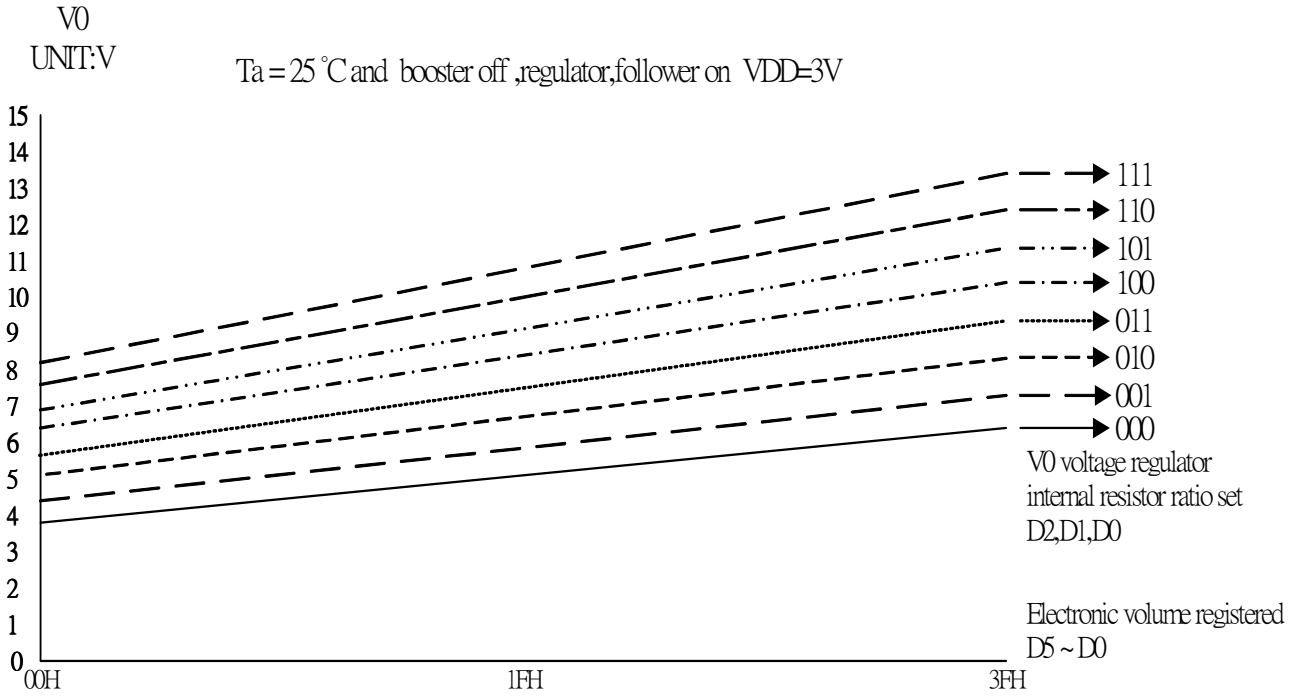


Figure 9 : (1) For ST7565P the Thermal Gradient = -0.05%/℃

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25℃ and V0 = 7V f or an ST7565P on which Temperature gradient = –0.05%/℃.
Using Figure 9 and the equation A-1, the following setup is enabled.
At this time, the variable range and the notch width of the V0 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 12

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V_0 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

Table 13

V_0	Min	Typ	Max	Units
Variable Range	5.1 (63 levels)	7.0 (central value)	8.4 (0 level)	[V]
Notch width		51		[mV]

(B) When an External Resistance is Used (The V0 Voltage Regulator Internal Resistors Are Not Used) (1)

The liquid crystal power supply voltage V0 can also be set without using the V0 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra' and Rb' between VDD and VR, and between VR and V0, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V0 through commands.
In the range where | V0 | < | VOUT |, the V0 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

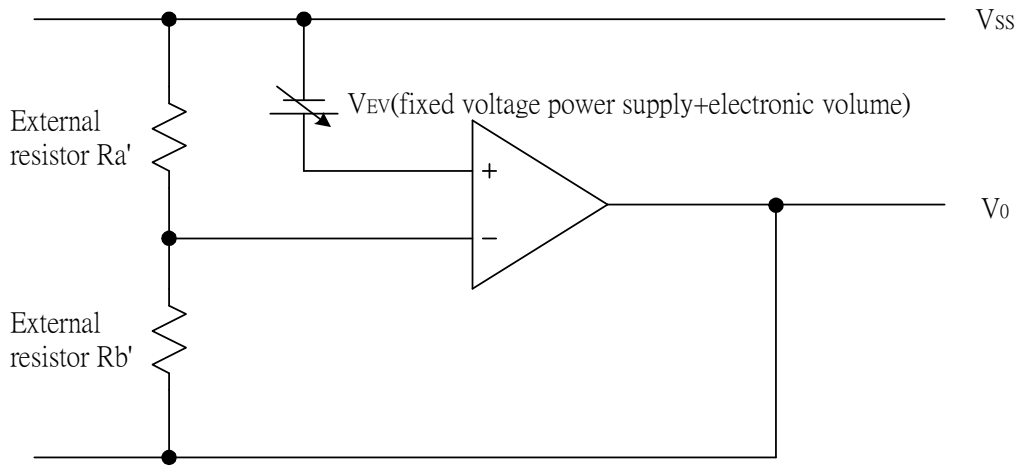


Figure 11

Setup example: When selecting Ta = 25℃ and V0 = 7 V for ST7565P the temperature gradient = –0.05%/℃.
When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = 2.1V so, according to equation B-1,

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$7V = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (2.1)$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 uA,
Ra' + Rb' = 1.4MΩ ..... (Equation B-3)

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$

$$Ra' = 340k\Omega$$

$$Rb' = 1060k\Omega$$

At this time, the V0 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

Table 14

V0	Min	Typ	Max	Units
Variable Range	5.3 (63 levels)	7.0 (central value)	8.6 (0 level)	[V]
Notch width		52		[mV]

(C) When External Resistors are Used (The V0 Voltage Regulator Internal Resistors Are Not Used) (2)

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V0. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V0 by commands to adjust the liquid crystal display brightness.

In the range where | V0 | < | VOUT | the V0 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistor) and R3 settings, where R2 can be subjected to fine adjustments (△ R2).

$$V_0 = \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

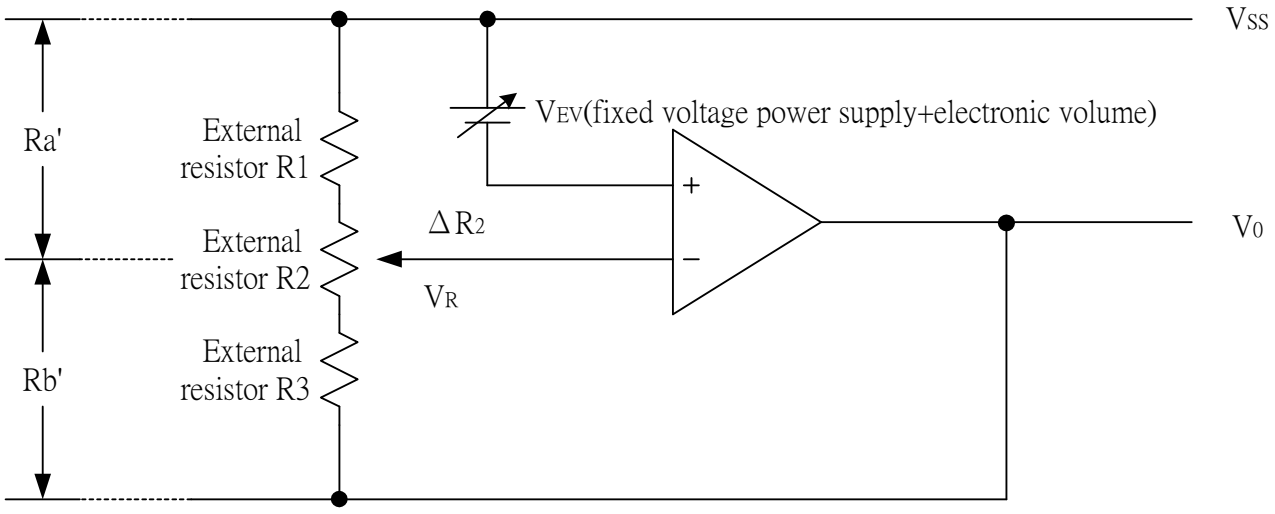


Figure 12

Setup example: When selecting Ta = 25℃ and V0= 5 to 9 V (using R2) for an ST7565P the temperature gradient = –0.05%/℃.
When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = 2.1 V so, according to equation C-1, when ΔR2 = 0 Ω, in order to make V0 = 9 V,

$$9V = \left(1 + \frac{R3+R2}{R1}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet \quad (2.1)$$

When △R2 = R2, in order to make V = –5 V,

$$5V = \left(1 + \frac{R3}{R1+R2}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet \quad (2.1)$$

When the current flowing VDD and V0 is set to 5 uA,

R1 + R2 + R3 = 1.4MΩ.....(Equation C-4)

With this, according to equation C-2, C-3 and C-4,

$$R1 = 264k\Omega$$

$$R2 = 211k\Omega$$

$$R3 = 925k\Omega$$

The V0 voltage variable range and notch width based on the electron volume function is as shown in Table 15.

Table 15

V0	Min	Typ	Max	Units
Variable Range	5.5 (63 levels)	7.3 (central value)	9 (0 level)	[V]
Notch width		56		[mV]

* When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.
* The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal = “L”). When the V0 voltage regulator internal resistors are used (i.e. when the IRS terminal = “H”), then the VR terminal is left open.
* Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The LCD Voltage Generator Circuit

The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3 and V4 to the liquid crystal drive circuit.

High Power Mode

The power supply circuit equipped in the ST7565P chips has very low power consumption (normal mode: HPM = “H”). **However, for LCD panels with large loads (size), this low-power power supply may cause display quality to degrade. When this occurs, set the HPM terminal to “L” (high power mode) can improve the display quality.** SITRONIX recommends that the display should be checked on actual equipment to determine whether or not to use this mode. Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 13 is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

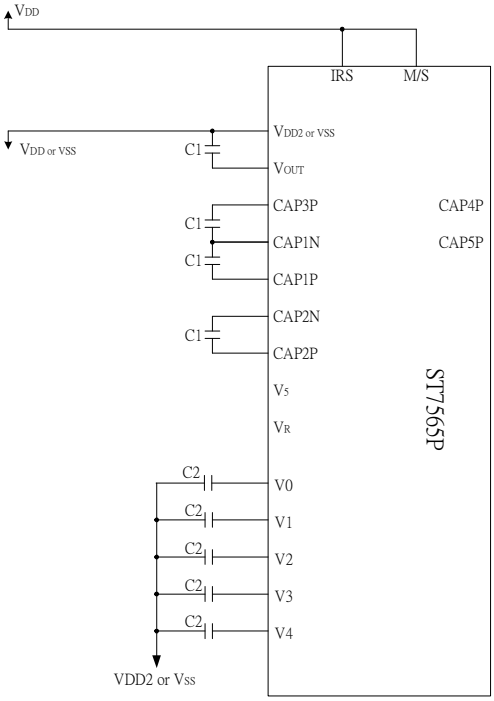
Sequence	Details (Command, status)	Command address D7 D6 D5 D4 D3 D2 D1 D0	
Step1	Display OFF	1 0 1 0 1 1 1 0	Power saver
Step2	Display all points ON	1 0 1 0 0 1 0 1	commands
End	Internal power supply OFF		(compound)

Figure 13

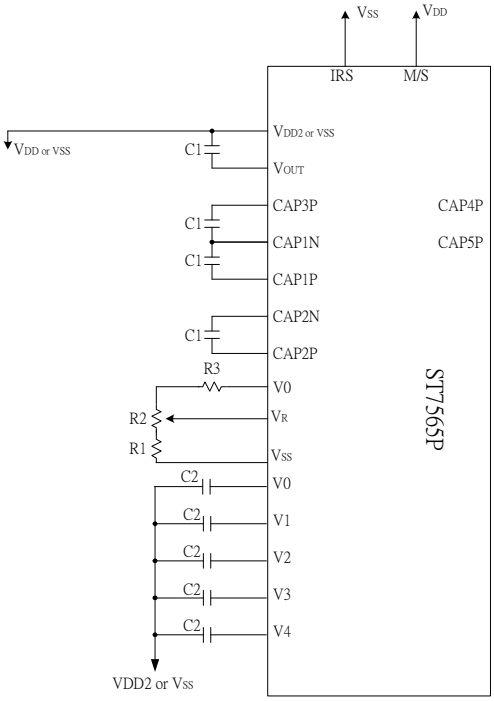
Reference Circuit Examples

1. When used all of the step-up circuit, voltage regulating circuit and V/F circuit

(1) When the voltage regulator internal resistor is used.
(Example where VDD2 = VDD, with 4x step-up)

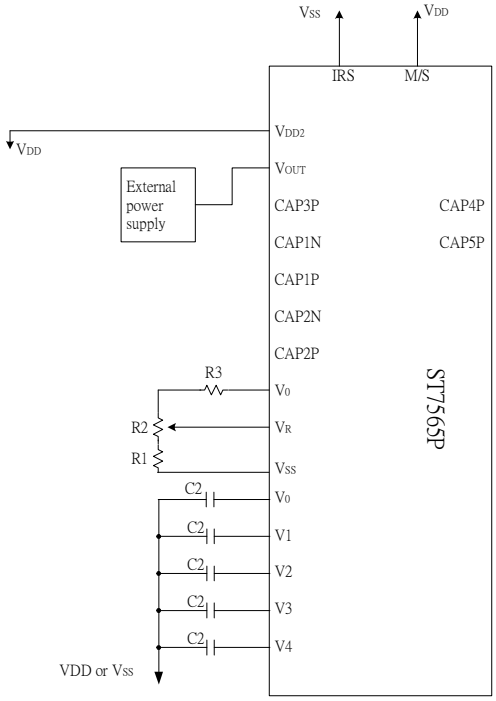


(2) When the voltage regulator internal resistor is not used.
(Example where VDD2 = VDD, with 4x step-up)

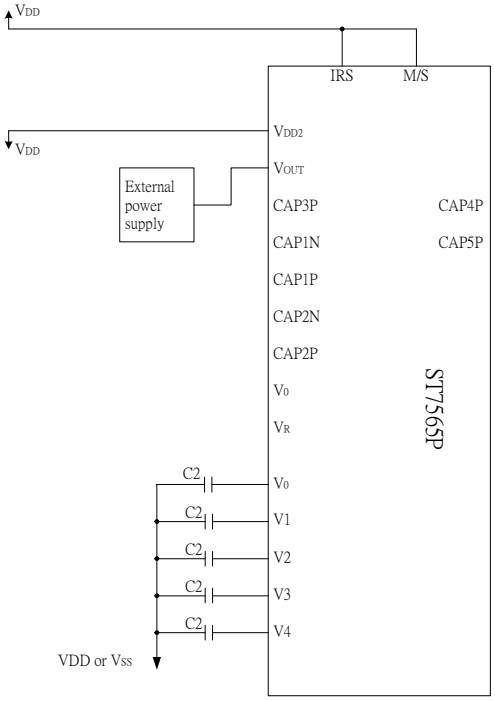


2. When the voltage regulator circuit and V/F circuit alone are used

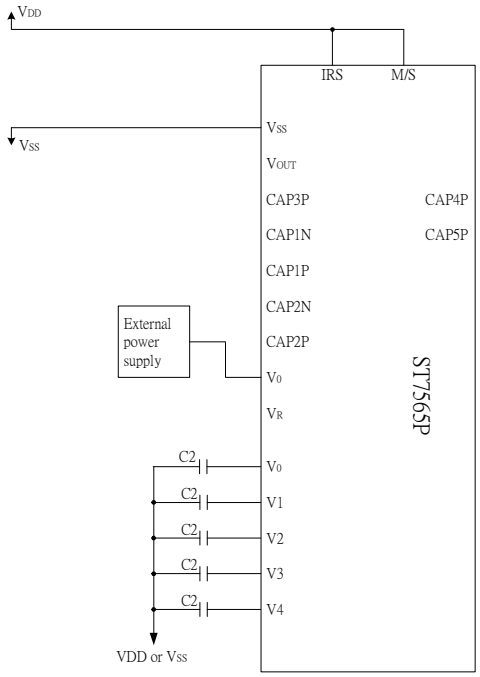
(1) When the V0 voltage regulator internal resistor is NOT used.



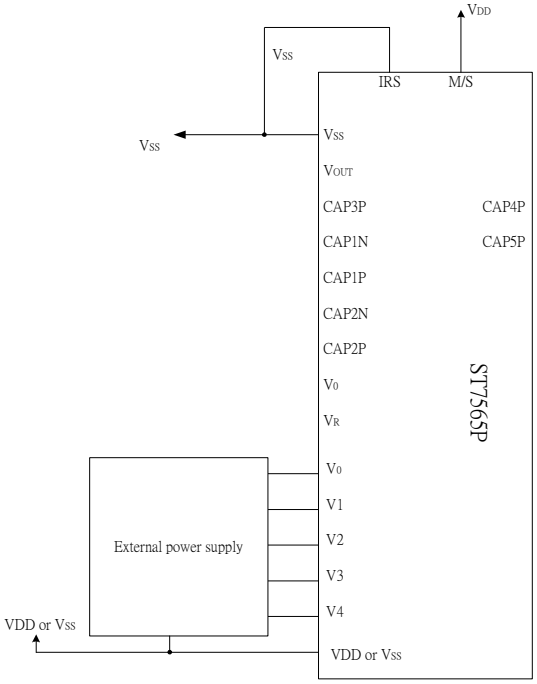
(2) When the V0 voltage regulator internal resistor is used.



(3) When the V/F circuit alone is used



(4) When the built-in power is not used



Item	Set value	units
C1	1.0 to 4.7	uF
C2	0.1 to 4.7	uF

C1 and C2 are determined by the size of the LCD being driven.

* 1. Because the VR terminal input impedance is high, use short leads and shielded lines.
* 2. C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the process which determines the capacitor values:
* Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to VOUT from the outside.
* Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V0 to V4). Note that all C2 capacitors must have the same capacitance value.
* Next turn all the power supplies ON and determine C1.

The Reset Circuit

When the /RES input comes to the “L” level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC command D0 = “L”)
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias rate:
   1/65 DUTY = 1/9 bias
   1/49,1/55,1/53 DUTY = 1/8 bias
   1/33 DUTY = 1/6 bias
7. All-indicator lamps-on OFF (All-indicator lamps ON/OFF command D0 = “L”)
8. Power saving clear
9. V0 voltage regulator internal resistors Ra and Rb separation
10. Output conditions of SEG and COM terminals SEG=VSS , COM=VSS
11. Read modify write OFF
12. Display start line set to first line
13. Column address set to Address 0
14. Page address set to Page 0
15. Common output status normal
16. V0 voltage regulator internal resistor ratio set mode clear
17. Clear Electronic volume register :
    (D5, D4, D3, D2, D1, D0) = (1, 0. 0, 0, 0,0)
18. Test mode clear

On the other hand, when the reset command is used, the above default settings from 11 to 18 are only executed.

When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the /RES terminal. After the initialization, each input terminal should be controlled normally.
Moreover, when the control signal from the MPU is in the high impedance, an over current may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state.
If the internal liquid crystal power supply circuit is not used on ST7565P,it is necessary that /RES is “H” when the external liquid crystal power supply is turned on. This IC has the function to discharge V0 when /RES is “L,” and the external power supply short-circuits to Vss when /RES is “L.” This means that an internal resistor is connected between VSS and V0.
While /RES is “L,” the oscillator works but the display timing generator stops, and the CL, FR and /DOF terminals are fixed to “H.” The terminals D0 to D7 are not affected. The VSS level is output to SEG and COM output terminals after a success hardware reset.

COMMANDS

The ST7565P identify the data bus signals by a combination of A0, /RD (E), /WR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.
In the 8080 MPU interface, commands are launched by inputting a low pulse to the RD terminal for reading, and inputting a low pulse to the /WR terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an “H” signal is input to the R/W terminal and placed in a write mode when a “L” signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read /RD (E) becomes “1(H)”. In the explanations below the commands are explained using the 8080 Series MPU interface as the example. When the serial interface is selected, the data is input in sequence starting with D7.

<Explanation of Commands>

Display ON/OFF

This command turns the display ON and OFF.

	E	R/W								
A0	**/RD**	**/WR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Setting**
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in “The Line Address Circuit”.

	E	R/W								
A0	**/RD**	**/WR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Line address**
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
								↓			↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

	E	R/W								
A0	**/RD**	**/WR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Page address**
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in “The Column Address Circuit,” for details.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

Status Read

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	BUSY = 1: it indicates that either processing is occurring internally or a reset condition is in process. BUSY = 0: A new command can be accepted . if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n ↔ SEG n) 1: Normal (column address n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by “1” after the write, the MPU can write the display data.

A0	E /RD	R/W /WR	D7 D6 D5 D4 D3 D2 D1 D0
1	1	0	Write data

Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H" LCD ON voltage (normal)
										1	RAM Data "L" LCD ON voltage (reverse)

Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the Power Save section.

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Select Status 1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

Read/Modify/Write

This command is used paired with the “END” command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

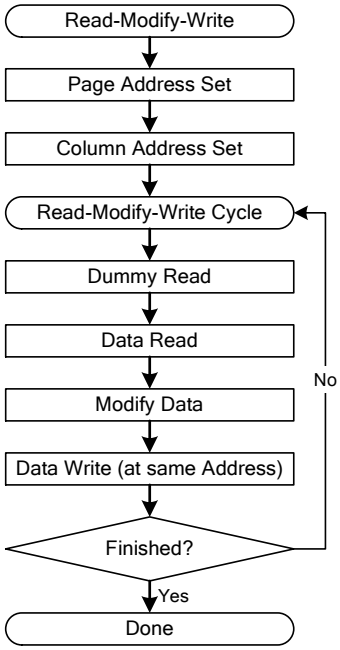


Figure 24 Command Sequence For read modify write

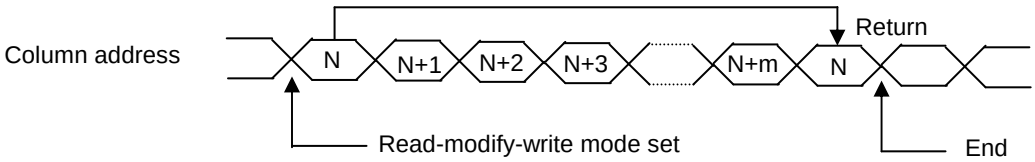


Figure 25

End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V0 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in “Reset” for details. The reset operation is performed after the reset command is entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in “Common Output Mode Select Circuit.”

E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode					
											1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
A0															
0	1 0	1	1	0	0	0 1	*	*	*	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
										Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

* Disabled bit

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in “The Power Supply Circuit,” for details.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see the function explanation is “The Voltage Regulator circuit " and Table 11.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	1	
								1	1	1	Large

The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V0 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	| V0 |
0	1	0	*	*	0	0	0	0	0	1	Small
			*	*	0	0	0	0	1	0	
			*	*	0	0	0	0	1	1	
							↓				↓
			*	*	1	1	1	1	1	0	
			*	*	1	1	1	1	1	1	Large

* Inactive bit (set “0”)
When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

The Electronic Volume Register Set Sequence

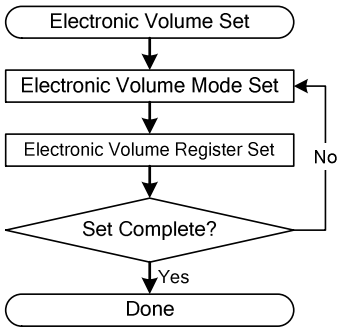


Figure 26

Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered. In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM. Refer to figure 28 for power save off sequence.

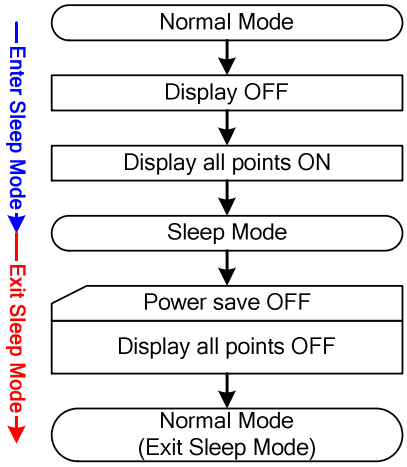


Figure 28

Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VSS level.
3. The static drive system does not operate.

The Booster Ratio (Double Byte Command)

This command makes it possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte command used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

Booster Ratio Select Mode Set

When this command is input, the Booster ratio register set command becomes enabled. Once the booster ratio select mode has been set, no other command except for the booster ratio register command can be used. Once the booster ratio register set command has been used to set data into the register, then the booster ratio select mode is released.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

Booset Ratio Register Set

By using this command to set two bits of data to the booster ratio register, it can be select what kind of the booster ratio can be used. When this command is input, the booster ratio select mode is released after the booster ratio register has been set.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Booster ratio select
0	1	0	*	*	*	*	*	*	0	0	2x,3x,4x
			*	*	*	*	*	*	0	1	5x
			*	*	*	*	*	*	1	1	6x

* Inactive bit (set “0”)
When the booster ratio select function is not used, set this to (0, 0) 2x,3x,4x step-up mode.

The booster ratio Register Set Sequence

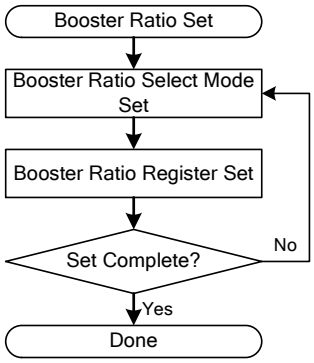


Figure 29

NOP

Non-Operation Command

	E	R/W							
A0	**/RD**	**/WR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a “L” signal to the /RES input by the reset command or by using an NOP.

	E	R/W							
A0	**/RD**	**/WR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	1	1	1	*	*

* Inactive bit

Note: The ST7565P maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the ST7565P . Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16: Table of ST7565P Commands (Note) *: disabled data

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the V_0 output voltage electronic volume register
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

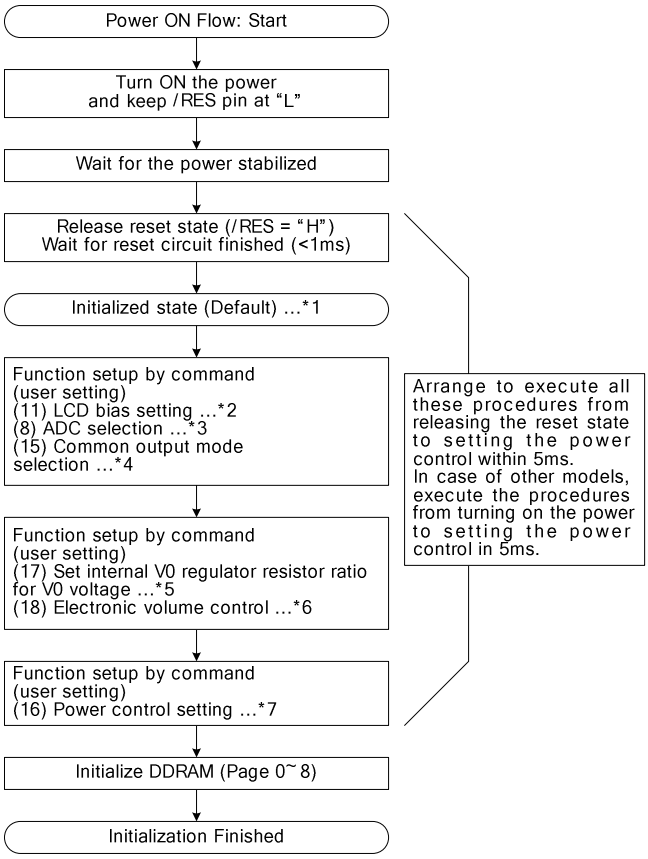
COMMAND DESCRIPTION

Instruction Setup: Reference

(1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 ~ V4) and the VSS pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

1. When the built-in power is being used immediately after turning on the power:

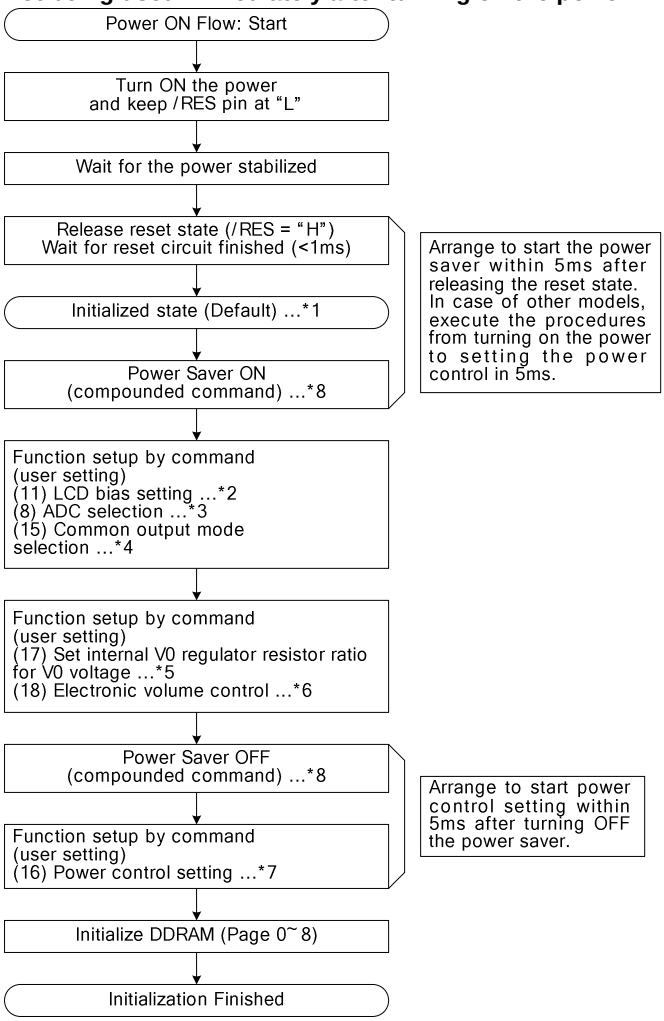


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V0 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting

2. When the built-in power is not being used immediately after turning on the power:

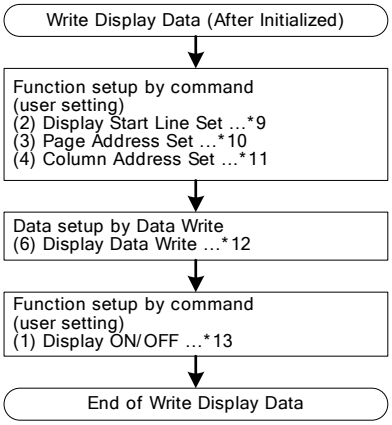


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V0 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting
*8: The power saver ON state can either be in sleep state or stand-by state.
Command description; Power saver START (multiple commands)

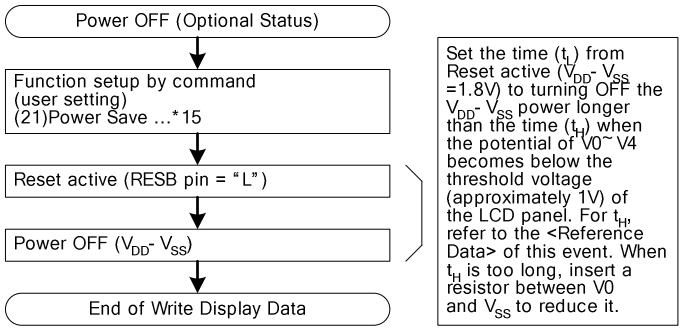
(2) Data Display



Notes: Reference items

*9: Command Description; Display start line set
*10: Command Description; Page address set
*11: Command Description; Column address set
*12: Command Description; Display data write
*13: Command Description; Display ON/OFF
Avoid displaying all the data at the data display start (when the display is ON) in white.

(3) Power OFF *14



Notes: Reference items

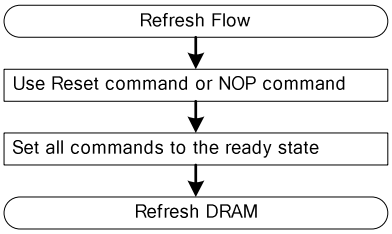
*14: The logic circuit of this IC's power supply VDD - VSS controls the driver of the LCD power supply VSS – V0. So, if the power supply VDD - VSS is cut off when the LCD power supply VSS – V0 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:
• After turning off the internal power supply, make sure that the potential V0 ~ V4 has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (VDD - VSS). 6. Description of Function, 6.7 Power Circuit

*15: After inputting the power save command, be sure to reset the function using the /RES terminal until the power supply VDD - VSS is turned off. 7. Command Description (20) Power Save

*16: After inputting the power save command, do not reset the function using the /RES terminal until the power supply VDD - VSS is turned off. 7. Command Description (20) Power Save

Refresh

It is recommended to turn on the refresh sequence regularly at a specified interval.



Precautions on Turning off the power

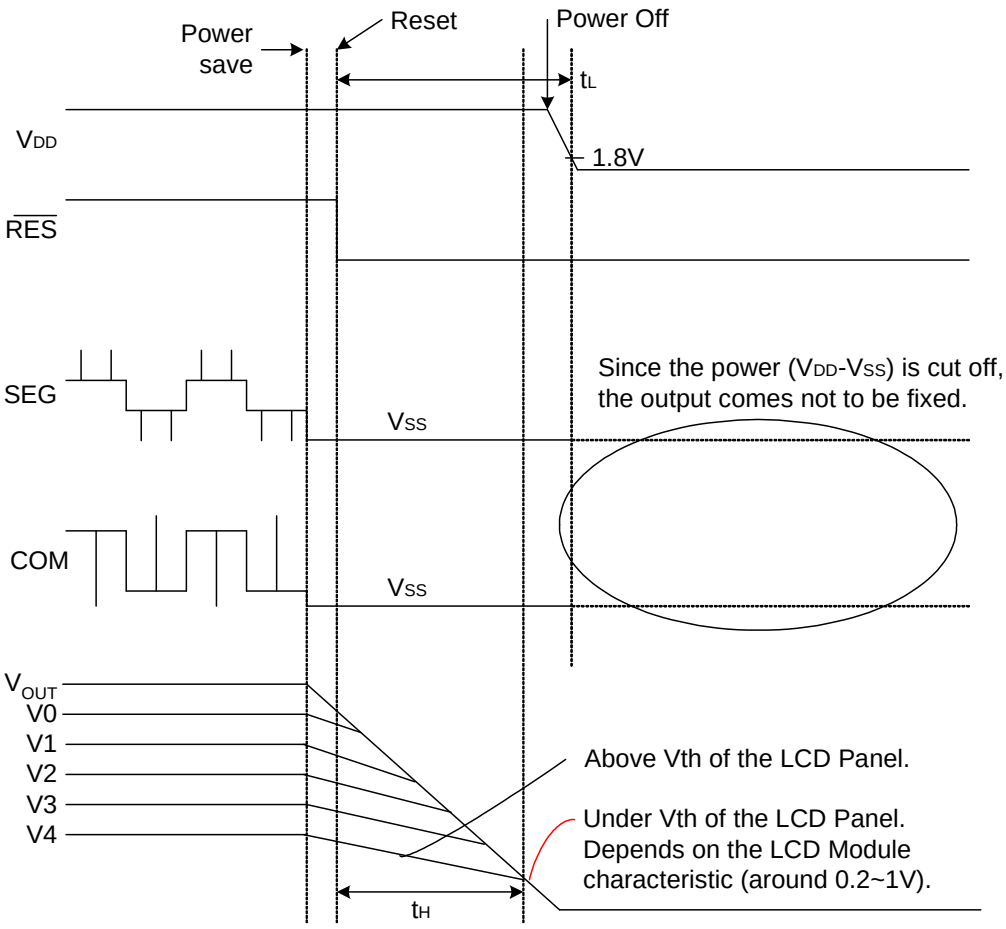
<Turning the power (V_{DD} - V_{SS}) off>

1) Power Save (The LCD powers (V_0 - V_{SS}) are off.) → Reset input → Power (V_{DD} - V_{SS}) OFF

• Observe $t_L > t_H$.

• **When $t_L < t_H$, an irregular display may occur.**

Set t_L on the MPU according to the software. t_H is determined according to the external capacitor C2 (smoothing capacitor of V_0 ~ V_4) and the driver's discharging capacity.



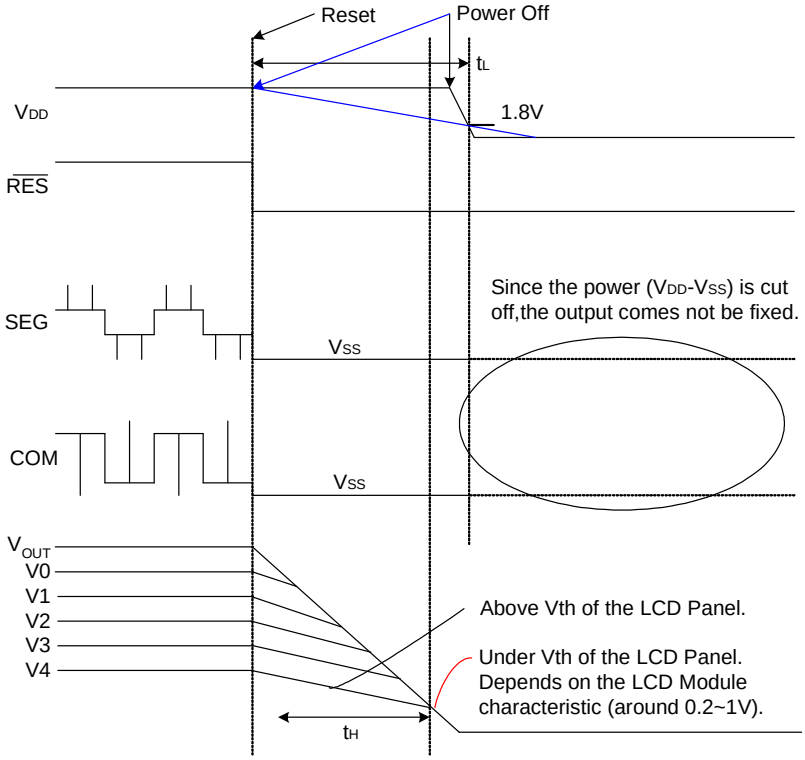
<Turning the power (VDD - VSS) off : When command control is not possible.>
2) Reset (The LCD powers (V_{DD} - V_{SS}) are off.) → Power (V_{DD} - V_{SS}) OFF

• Observe $t_L > t_H$.

• **When $t_L < t_H$, an irregular display may occur.**

For t_L, make the power (V_{DD} - V_{SS}) falling characteristics longer or consider any other method.

t_H is determined according to the external capacity C2 (smoothing capacity of V_0 to V_4) and the driver's discharging capacity.



<Reference Data>

V_0 voltage falling (discharge) time (t_H) after the process of operation → power save → reset.

V_0 voltage falling (discharge) time (t_H) after the process of operation → reset.

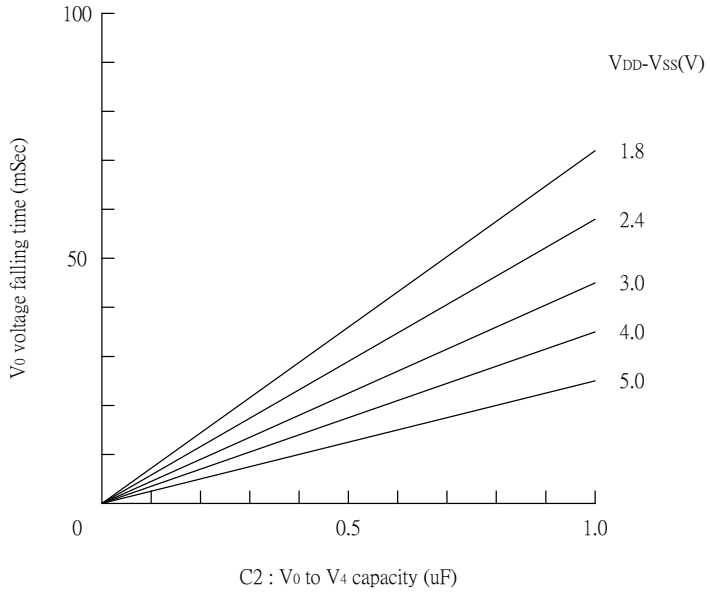


Figure 31

ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified, VSS = 0V

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 ~ 3.6	V
Power supply voltage (VDD standard)		V_{DD2}	–0.3 ~ 3.6	V
Power supply voltage (VDD standard)		V0, VOUT	–0.3 ~ 14.5	V
Power supply voltage (VDD standard)		V1, V2, V3, V4	–0.3 ~ V0+0.3	V
Input Voltage	(Digital Pads)	V_{IN}	–0.3 ~ VDD+0.3	V
Output Voltage		V_O	–0.3 ~ VDD+0.3	V
Operating temperature	Bare chip	T_{OPR}	–30 to +85	℃
Storage temperature		T_{STR}	–65 to +150	℃

Table 17

Notes and Cautions

1. The voltages are relative to VSS = 0V unless otherwise specified.
2. The ranges listed in this section are stress only. It is recommended that the normal operating condition of this device should be in the ranges listed in “DC Characteristics” (the next section).
3. Stress over the listed ranges in “Absolute Maximum Ratings” may cause permanent damage to this device.
4. If this device is operated out of these conditions and ranges, it may not only result in malfunctions, but may have a negative impact on the reliability as well.
5. Insure that the voltage levels of V1, V2, V3, and V4 are always such that VOUT ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4.

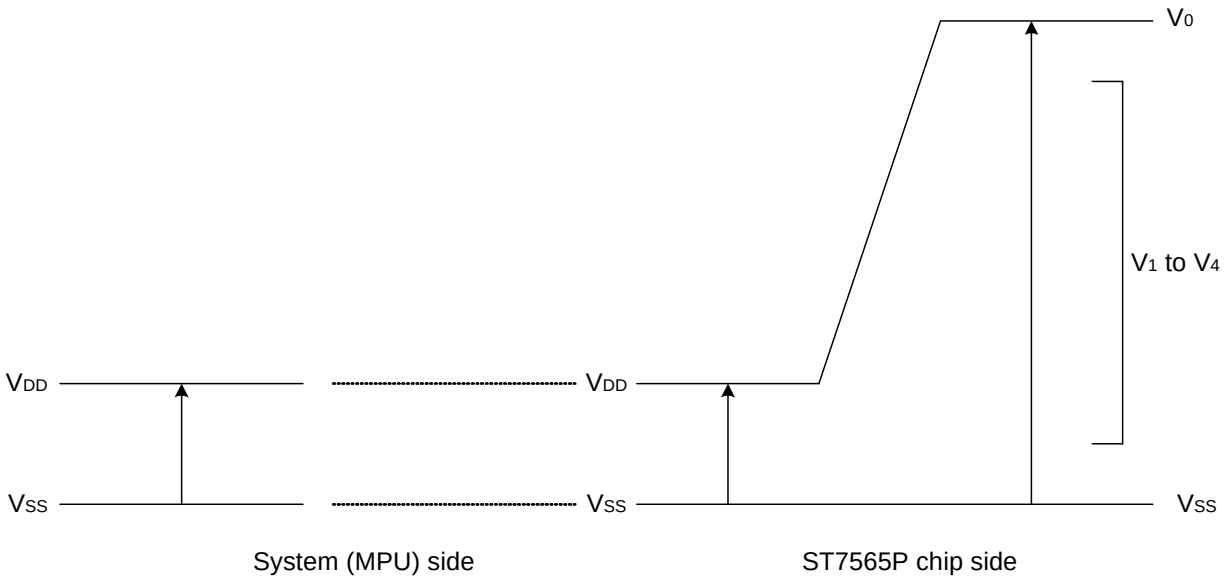


Figure 30

DC CHARACTERISTICS

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, Ta = –30 to 85℃

Table 18

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		V_{DD}			1.8	—	3.3	V	V_{SS}*1
Operating Voltage (2)		V_{DD2}	(Related to V_{SS})		2.4	—	3.3	V	V_{SS}
High-level Input Voltage		V_{IHC}			0.8 x V_{DD}	—	V_{DD}	V	*3
Low-level Input Voltage		V_{ILC}			V_{SS}	—	0.2 x V_{DD}	V	*3
High-level Output Voltage		V_{OHC}	I_{OH} = –1 mA		0.8 x V_{DD}	—	V_{DD}	V	*4
Low-level Output Voltage		V_{OLC}	I_{OL} = 1 mA		V_{SS}	—	0.2 x V_{DD}	V	*4
Input leakage current		I_{LI}	V_{IN} = VDD or VSS		–1.0	—	1.0	µA	*5
Output leakage current		I_{LO}	V_{IN} = VDD or VSS		–3.0	—	3.0	µA	*6
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25℃ (Related to V_{SS})	V0 = 13.0V	—	2.0	3.5	KΩ	SEGn COMn *7
				V0 = 8.0V	—	3.2	5.4		
Static Consumption Current		I_{SSQ}	V0 = 13.0 V (Related to V_{SS})		—	0.01	2	µA	V_{DD}, V_{DD2}
Output Leakage Current		I_{5Q}			—	0.01	10	µA	V0
Input Terminal Capacitance		C_{IN}	Ta = 25℃ , f = 1 MHz		—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	f_{OSC}	1/65 duty 1/33 duty	Ta = 25℃	17	20	24	kHz	*8
	External Input	f_{CL}			17	20	24	kHz	CL
	Internal Oscillator	f_{OSC}	1/49 duty 1/53 duty 1/55 duty	Ta = 25℃	25	30	35	kHz	*8
	External Input	f_{CL}			25	30	35	kHz	CL

Table 19

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	V_{DD2}	(Relative to V_{SS})	2.4	—	3.3	V	V_{SS}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative to V_{SS})	—	—	13.5	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative to V_{SS})	6.0	—	13.5	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V0	(Relative to V_{SS})	4.0	—	13.0	V	V0 * 9
	Base Voltage	V_R	Ta = 25℃ , (Relative to V_{SS}) –0.05%/℃	2.07	2.10	2.13	V	*10

• Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used .

Table 20

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern OFF	I_{DD}	V_{DD} = 3.0 V, V0 – V_{SS} = 11.0 V	—	16	27	µA	*11
Display Pattern Checker	I_{DD}	V_{DD} = 3.0 V, V0 – V_{SS} = 11.0 V	—	19	32	µA	*11

• Dynamic Consumption Current : During Display, with the Internal Power Supply ON

Table 21

Test pattern	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
Display Pattern OFF	I_{DD}	V_{DD} = 3.0 V, Quad step-up voltage. V0 –V_{SS} = 11.0 V	Normal Mode	—	90	130	µA	*12
			High-Power Mode	—	128	193		
Display Pattern Checker	I_{DD}	V_{DD} = 3.0 V, Quad step-up voltage. V0 –V_{SS} = 11.0 V	Normal Mode	—	100	147	µA	*12
			High-Power Mode	—	135	205		

• Consumption Current at Time of Power Saver Mode : VSS = -3.0 V ± 10%

Table 22

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Sleep mode	I_{DD}	Ta = 25℃	—	0.1	4	µA	
Standby Mode	I_{DD}	Ta = 25℃	—	5	10		

• **The Relationship Between Oscillator Frequency fOSC, Display Clock Frequency fCL and the Liquid Crystal Frame Rate Frequency fFR**

Table 23

Item		fCL	fFR
1/65 DUTY	Used internal oscillator circuit	fOSC / 4	fOSC / (4*65)
	Used **external** display clock	External input (fCL)	fCL / 260
1/49 DUTY	Used internal oscillator circuit	fOSC / 4	fOSC / (4*49)
	Used **external** display clock	External input (fCL)	fCL / 196
1/33 DUTY	Used internal oscillator circuit	fOSC / 8	fOSC / (8*33)
	Used **external** display clock	External input (fCL)	fCL / 264
1/55 DUTY	Used internal oscillator circuit	fOSC / 4	fOSC / (4*55)
	Used **external** display clock	External input (fCL)	fCL / 220
1/53 DUTY	Used internal oscillator circuit	fOSC / 4	fOSC / (4*53)
	Used **external** display clock	External input (fCL)	fCL / 212

(fFR is the liquid crystal alternating current period, and not the FR signal period.)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The operating voltage range for the VSS system and the V0 system is. This applies when the external power supply is being used.

*3 The A0, D0 to D5, D6 (SCL), D7 (SI), /RD (E), /WR (R/W), /CS1, CS2, CLS, CL, FR, M/S, C86, P/S, /DOF, /RES, IRS, and /HPM terminals.

*4 The D0 to D7, FR, /DOF, and CL terminals.

*5 The A0, /RD (E), /WR (R/W), /CS1, CS2, CLS, M/S, C86, P/S, /RES, IRS, and /HPM terminals.

*6 Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, FR, and /DOF terminals are in a high impedance state.

*7 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage (3) range. RON = 0.1 V / △I (Where △I is the current that flows when 0.1 V is applied while the power supply is ON.)

*8 See Table 23 for the relationship between the oscillator frequency and the frame rate frequency.

*9 The V0 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

*10 This is the internal voltage reference supply for the V0 voltage regulator circuit. In the ST7565P , the temperature range approximately –0.05%/℃.

*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on. The ST7565P is 1/9 biased. Does not include the current due to the LCD panel capacity and wiring capacity. Applicable only when there is no access from the MPU.

*12 It is the value on a ST7565P having the VREG temperature gradient is –0.05%/℃ when the V0 voltage regulator internal resistor is used.

TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

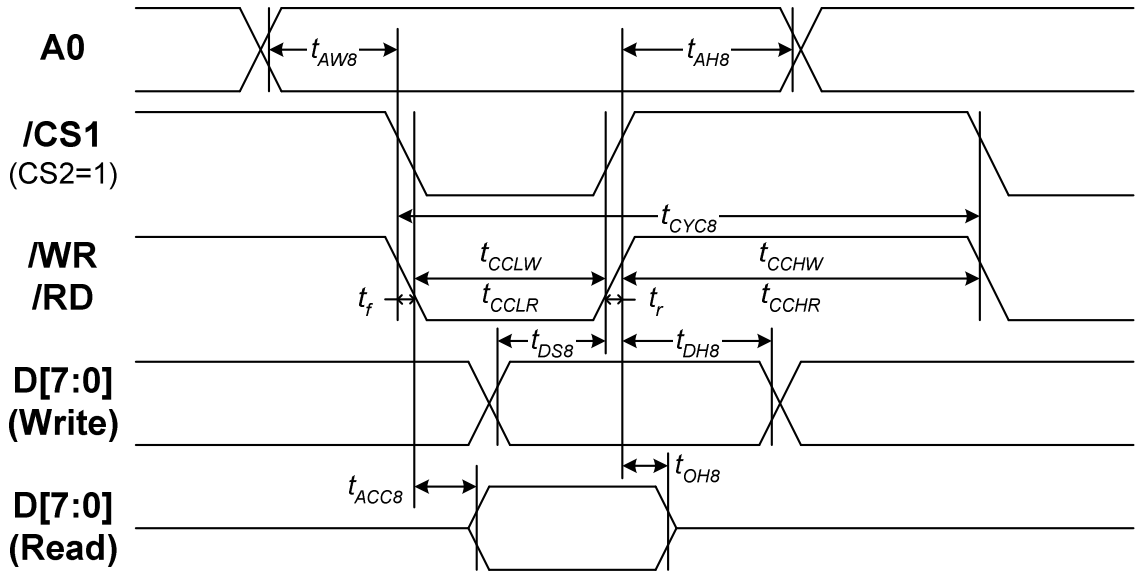


Figure 37

Table 24

(V_{DD} = 3.3V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	Ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Write L pulse width	/WR	t_{CCLW}		80	—	
Write H pulse width		t_{CCHW}		80	—	
Read L pulse width	/RD	t_{CCLR}		140	—	
Read H pulse width		t_{CCHR}		80		
Write Data setup time	D0 to D7	t_{DS8}		40	—	
Write Address hold time		t_{DH8}		0	—	
Read access time		t_{ACC8}	C_L = 100 pF	—	70	
Read Output disable time		t_{OH8}	C_L = 100 pF	5	50	

Table 25

(V_{DD} = 2.7V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		400	—	
Write L pulse width	WR	t_{CCLW}		220	—	
Write H pulse width		t_{CCHW}		180	—	
Read L pulse width	RD	t_{CCLR}		220	—	
Read H pulse width		t_{CCHR}		180	—	
Write Data setup time	D0 to D7	t_{DS8}		40	—	
Write Address hold time		t_{DH8}		0	—	
Read access time		t_{ACC8}	C_L = 100 pF	—	140	
Read Output disable time		t_{OH8}	C_L = 100 pF	10	100	

Table 26

(V_{DD} = 1.8V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		640	—	
Write L pulse width	WR	t_{CCLW}		360	—	
Write H pulse width		t_{CCHW}		280	—	
Read L pulse width	RD	t_{CCLR}		360	—	
Read H pulse width		t_{CCHR}		280		
Write Data setup time	D0 to D7	t_{DS8}		80	—	
Write Address hold time		t_{DH8}		0	—	
Read access time		t_{ACC8}	C_L = 100 pF	—	240	
Read Output disable time		t_{OH8}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{CCLW} and t_{CCLR} are specified as the overlap between /CS1 being “L” (CS2 = “H”) and /WR and /RD being at the “L” level.

System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)

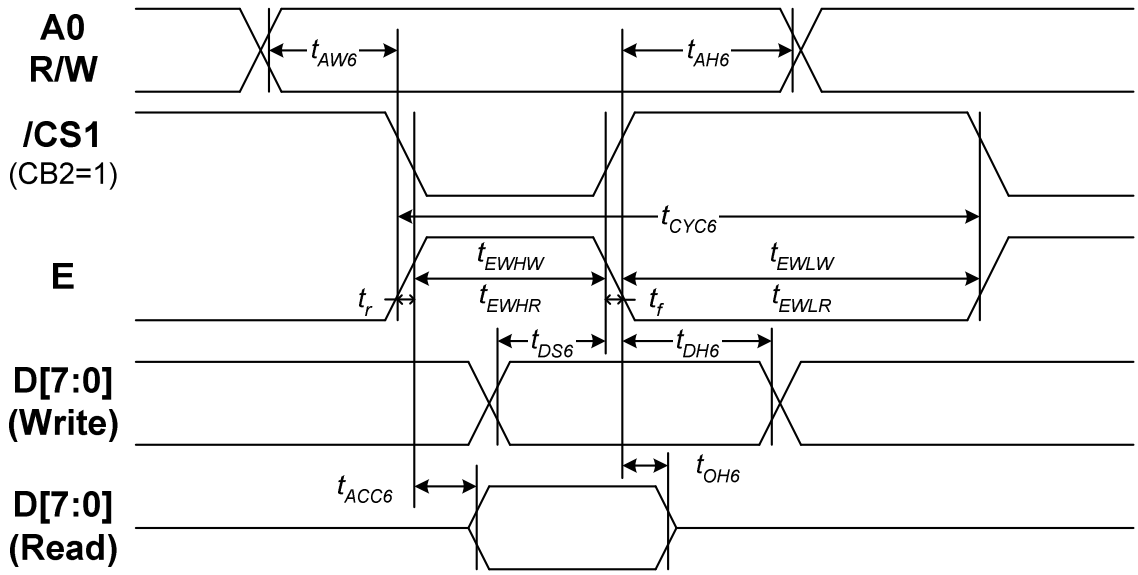


Figure 38

Table 27

(VDD = 3.3V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	E	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)		tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

Table 28

(V_{DD} = 2.7V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	E	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)		t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	100	

Table 29

(V_{DD} = 1.8V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		640	—	
Enable L pulse width (WRITE)	E	t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)		t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280	—	
WRITE Data setup time	D0 to D7	t_{DS6}		80	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being “L” (CS2 = “H”) and E.

The Serial Interface

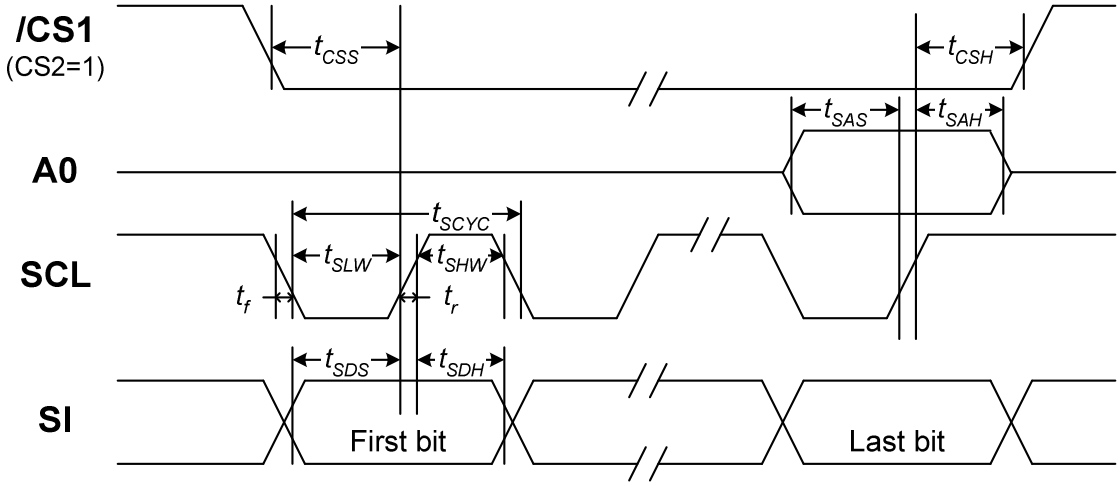


Figure 39

Table 30

(V_{DD} = 3.3V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		50	—	ns
SCL “H” pulse width		t_{SHW}		25	—	
SCL “L” pulse width		t_{SLW}		25	—	
Address setup time	A0	t_{SAS}		20	—	
Address hold time		t_{SAH}		10	—	
Data setup time	SI	t_{SDS}		20	—	
Data hold time		t_{SDH}		10	—	
CS-SCL time	CS	t_{CSS}		20	—	
CS-SCL time		t_{CSH}		40	—	

Table 31

(V_{DD} = 2.7V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		100	—	ns
SCL “H” pulse width		t_{SHW}		50	—	
SCL “L” pulse width		t_{SLW}		50	—	
Address setup time	A0	t_{SAS}		30	—	
Address hold time		t_{SAH}		20	—	
Data setup time	SI	t_{SDS}		30	—	
Data hold time		t_{SDH}		20	—	
CS-SCL time	CS	t_{CSS}		30	—	
CS-SCL time		t_{CSH}		60	—	

Table 32

(V_{DD} = 1.8V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		200	—	ns
SCL “H” pulse width		t_{SHW}		80	—	
SCL “L” pulse width		t_{SLW}		80	—	
Address setup time	A0	t_{SAS}		60	—	
Address hold time		t_{SAH}		30	—	
Data setup time	SI	t_{SDS}		60	—	
Data hold time		t_{SDH}		30	—	
CS-SCL time	CS	t_{CSS}		40	—	
CS-SCL time		t_{CSH}		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

Reset Timing

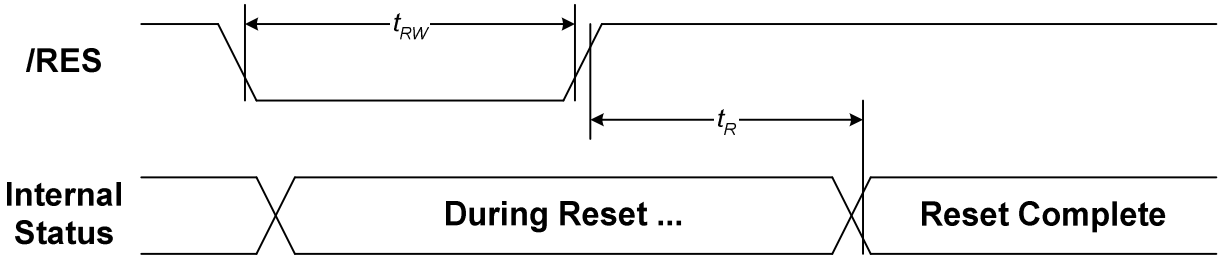


Figure 41

Table 36

(V_{DD} = 3.3V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RES	t_R		—	—	1.0	μs
Reset “L” pulse width		t_{RW}		1.0	—	—	μs

Table 37

(V_{DD} = 2.7V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RES	t_R		—	—	2.0	μs
Reset “L” pulse width		t_{RW}		2.0	—	—	μs

Table 38

(V_{DD} = 1.8V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RES	t_R		—	—	3.0	μs
Reset “L” pulse width		t_{RW}		3.0	—	—	μs

*1 All timing is specified with 20% and 80% of V_{DD} as the standard.

THE MPU INTERFACE (REFERENCE EXAMPLES)

ST7565P can be connected to either 80X86 series MPUs or 68000 series MPU. Moreover, by using the serial interface, it is possible to operate ST7565P with fewer signal pins.

The display area can be extended horizontally by using two ST7565P chips. Two chip select signals can be used to select the individual ICs to access.

(1) 8080 Series MPUs

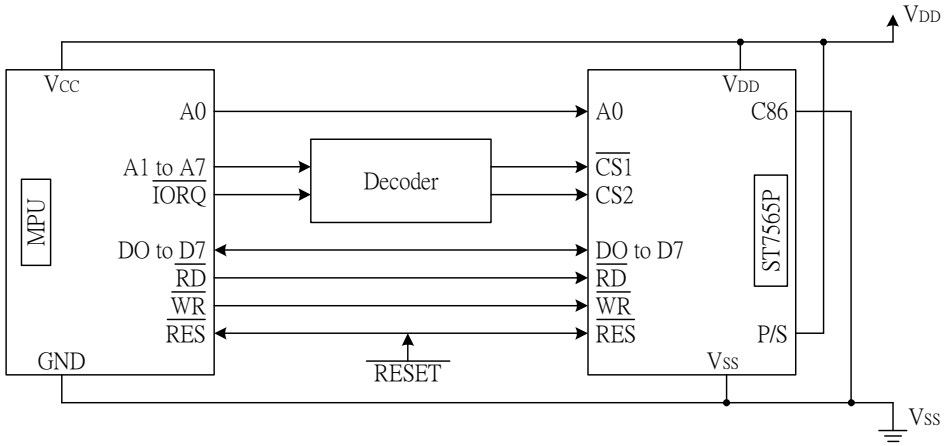


Figure 42-1

(2) 6800 Series MPUs

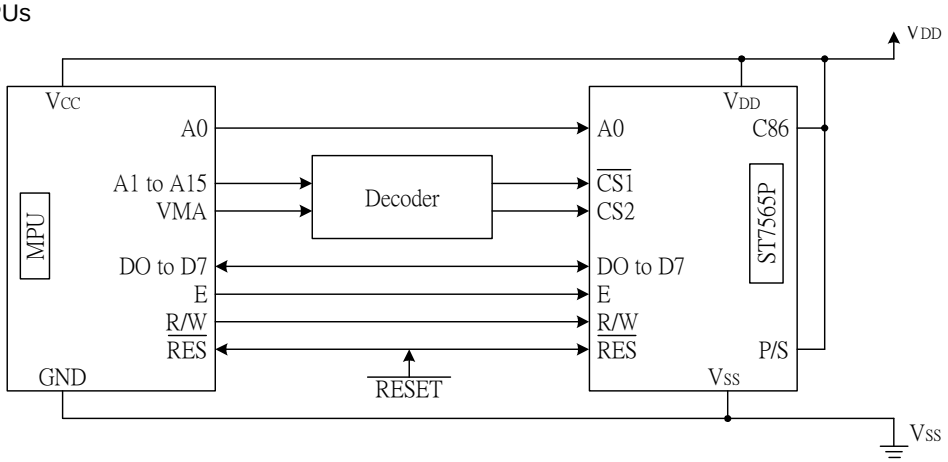


Figure 42-2

(3) Using the Serial Interface

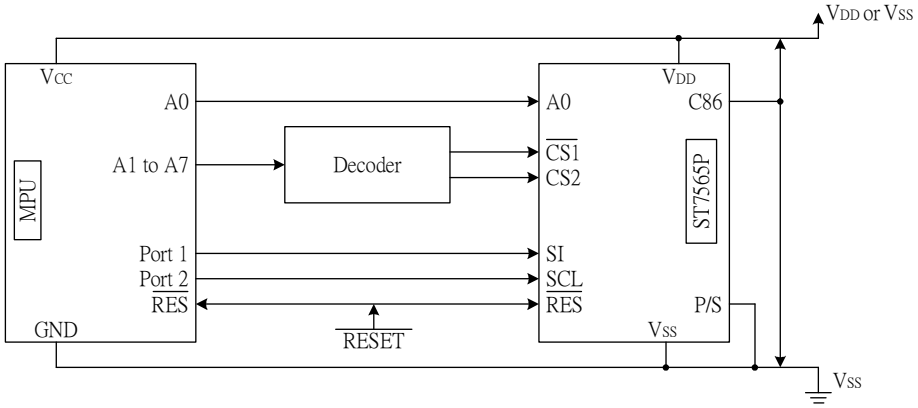


Figure 42-3

CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLE)

The display area of LCD panel can be extended horizontally by using two ST7565P chips. Use a same equipment type.

(1) ST7565P (master) → ST7565P (slave)

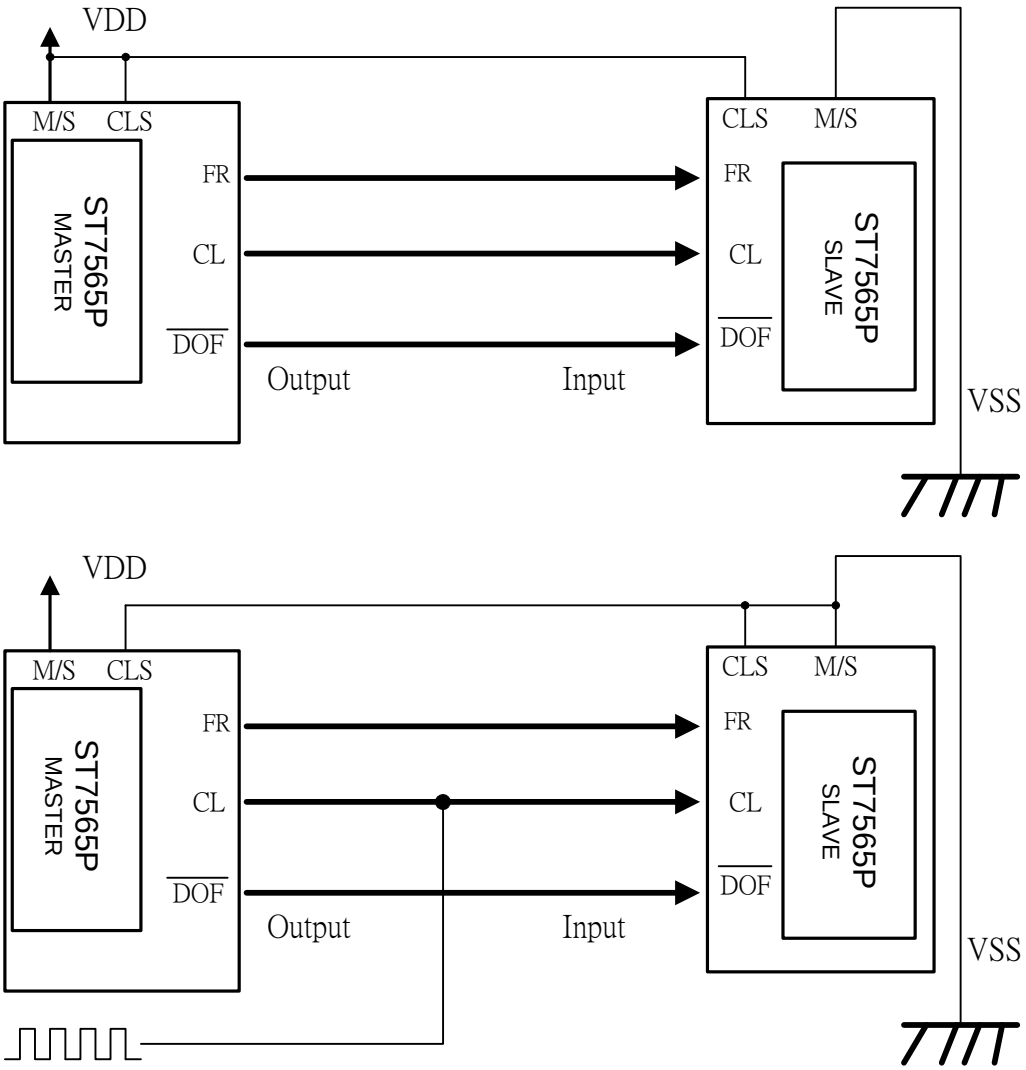


Figure 43-1

(2) Single-chip Structure

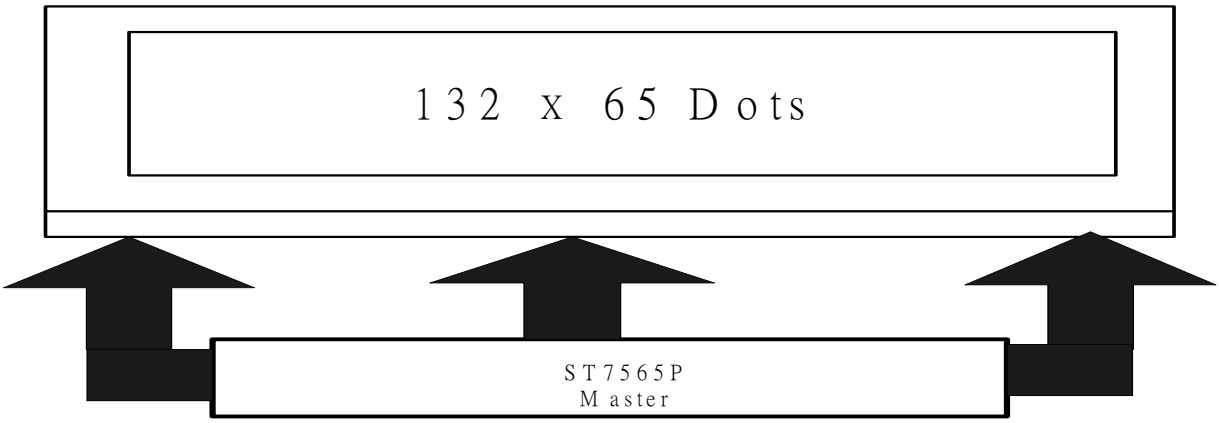


Figure 43-2

(3) Double-chip Structure

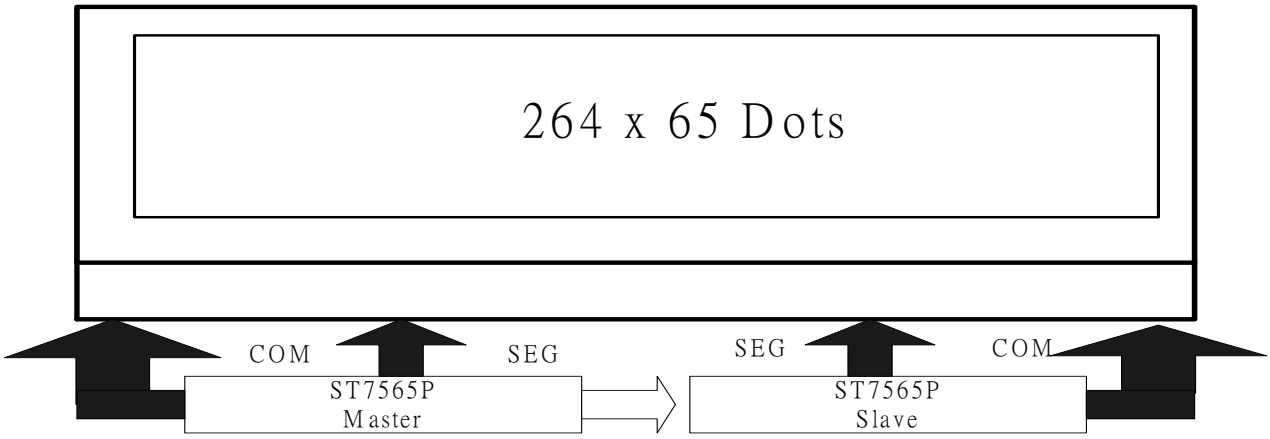


Figure 43-3

Change Notes

2004.04.05	Ver 1.2a	● Modify Serial interface Timing Character.
2004.05.18	Ver 1.3	● Change Temperature compensation rate to -0.05%/^{O}C.
2004.05.31	Ver 1.4	● Add I/O pin ITO resistor limitation.
2004.06.24	Ver 1.5	● Modify Page 2 PAD Diagram.
2004.07.14	Ver 1.6	● Modify Page 19 V1~V4 voltage setting with different bias set command.
2005.09.22	Ver 1.7	● Modify Feature Description; ● Modify operating temperature; ● Modify PIN Name: PAD 80~85 to TEST0~5; ● Modify Absolute Maximum Ratings; ● Modify Ta of DC Characteristics and Reset Timing; ● Remove redundant Page 28; ● Modify reference voltage to Vss (Page 58, 59).
2006.02.13	Ver 1.8	● Modify the description of DC characteristics. ● Modify function description. ● Redraw figures. ● Redraw the PAD DIAGRAM. ● Highlight the HPM (High Power Mode) description. ● Put emphasis on the power OFF procedure (Page 56-57).
2006/03/10	Ver 1.9	● Fix Ver. 1.8: Booster Circuit mistake (Booster X6, Page 32).
2007/11/06	Ver 1.9a	● Modify PAD pitch between COM[40] and alignment mark of PAD DIAGRAM. (Page 2).
2008/02/19	Ver 1.9b	● Modify Page 2 information: PAD 115, 290 and alignment mark drawing. ● Modify some description for easy understanding.
2008/03/14	Ver 1.9c	● Modify Ver 1.9c mistake: alignment mark coordinate. ● Add V_{IN} and V_O in Absolute Maximum Ratings. ● Modify description in Absolute Maximum Ratings.
2008/04/10	Ver 2.0	● Remove Static Indicator function and command. ● Reserved FRS pin function. ● Truncated Alignment mark coordinate. ● Rewrite some description. ● Update timing figures and naming.
2008/07/15	Ver 2.1	● Modify Page 2 information: bump size of PAD 115, 290.
2009/02/23	Ver 2.1a	● Modify mistake of Status Read.
2009/09/14	Ver 2.1b	● Modify the mistake of The Reset Circuit.