



EECS 2070 02 Fall 2022

Vivado Tutorial for FPGA Implementation

黃稚存

Chih-Tsun Huang

cthuang@cs.nthu.edu.tw



國立清華大學
NATIONAL TSING HUA UNIVERSITY

資訊工程學系
Computer Science

Lecture 03



聲明

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Hello FPGA

- » The very first lab to bring up FPGA board with Vivado

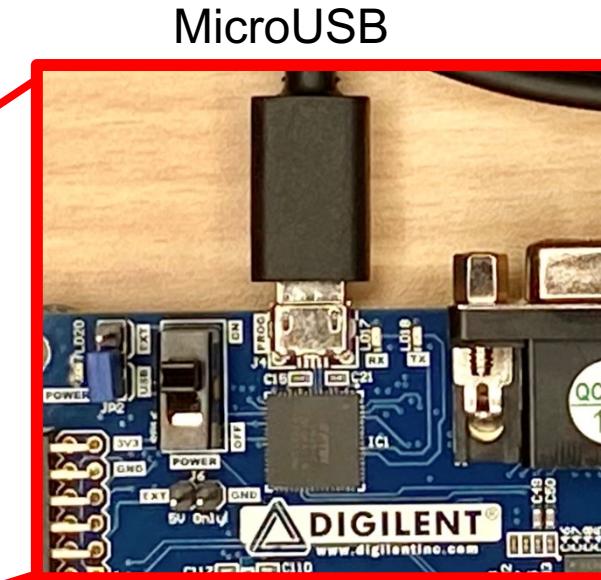
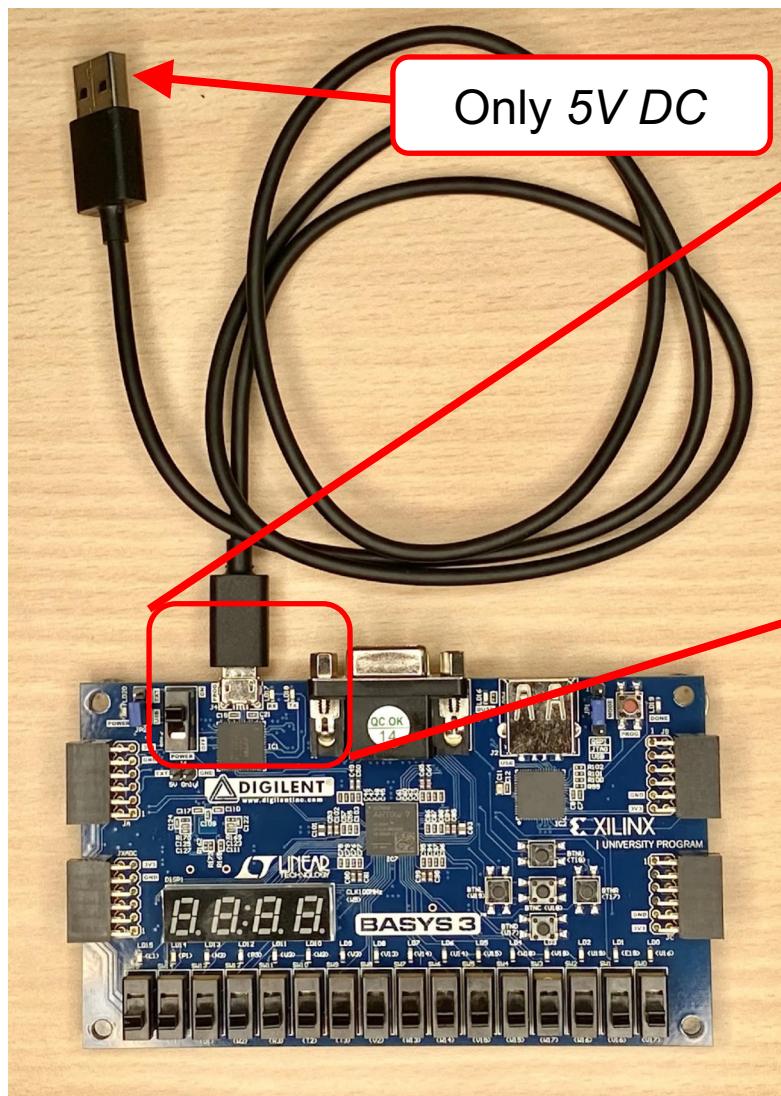


Lab 0 and Vivado Tutorial

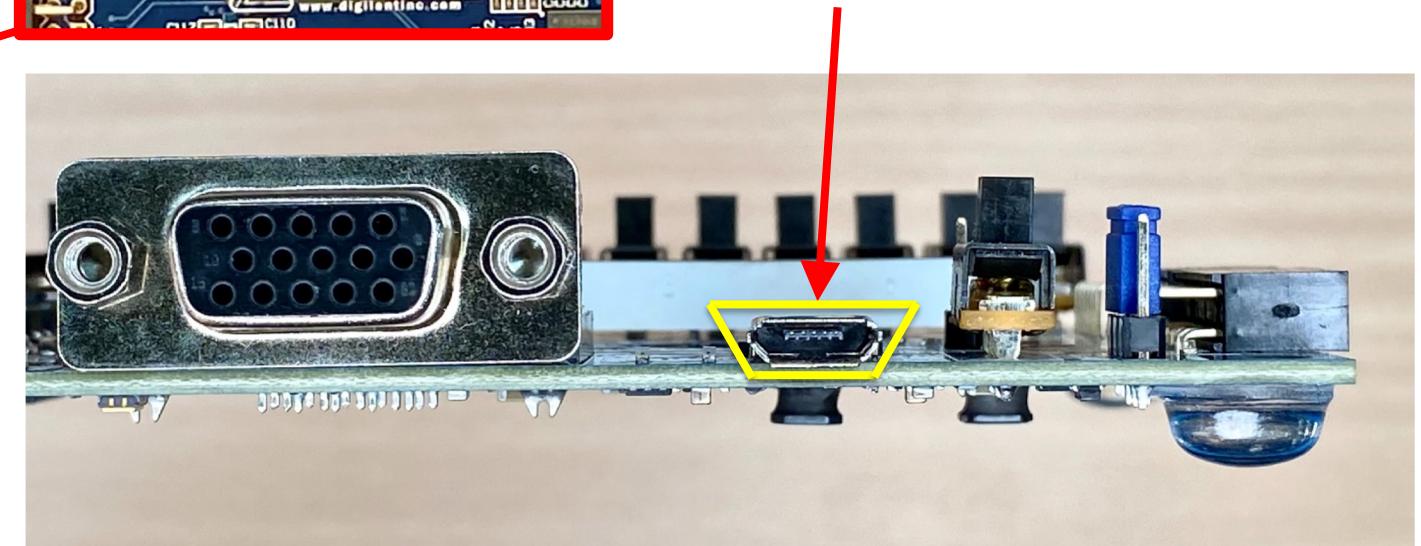
- 1. Get the FPGA board and USB cable**
 - ◆ Sign your name after receiving the board
 - ◆ Make sure both of them work
(You can use your own USB cable)
- 2. Perform Lab 0**
 - ◆ Following the instructions of Lab 0 for the two samples
 - A rock-paper-scissors game: tutorial of simulation and FPGA demo
 - A test-your-own-FPGA demo
 - ◆ **If you fail to complete Lab 0 with its report, you will get zero score for all the lab**
 - ◆ You have to write a report for every lab



Attention with Cable Connector!!!



Please mind
the **DIRECTION!!**





Introduce Basys3 Demo Board

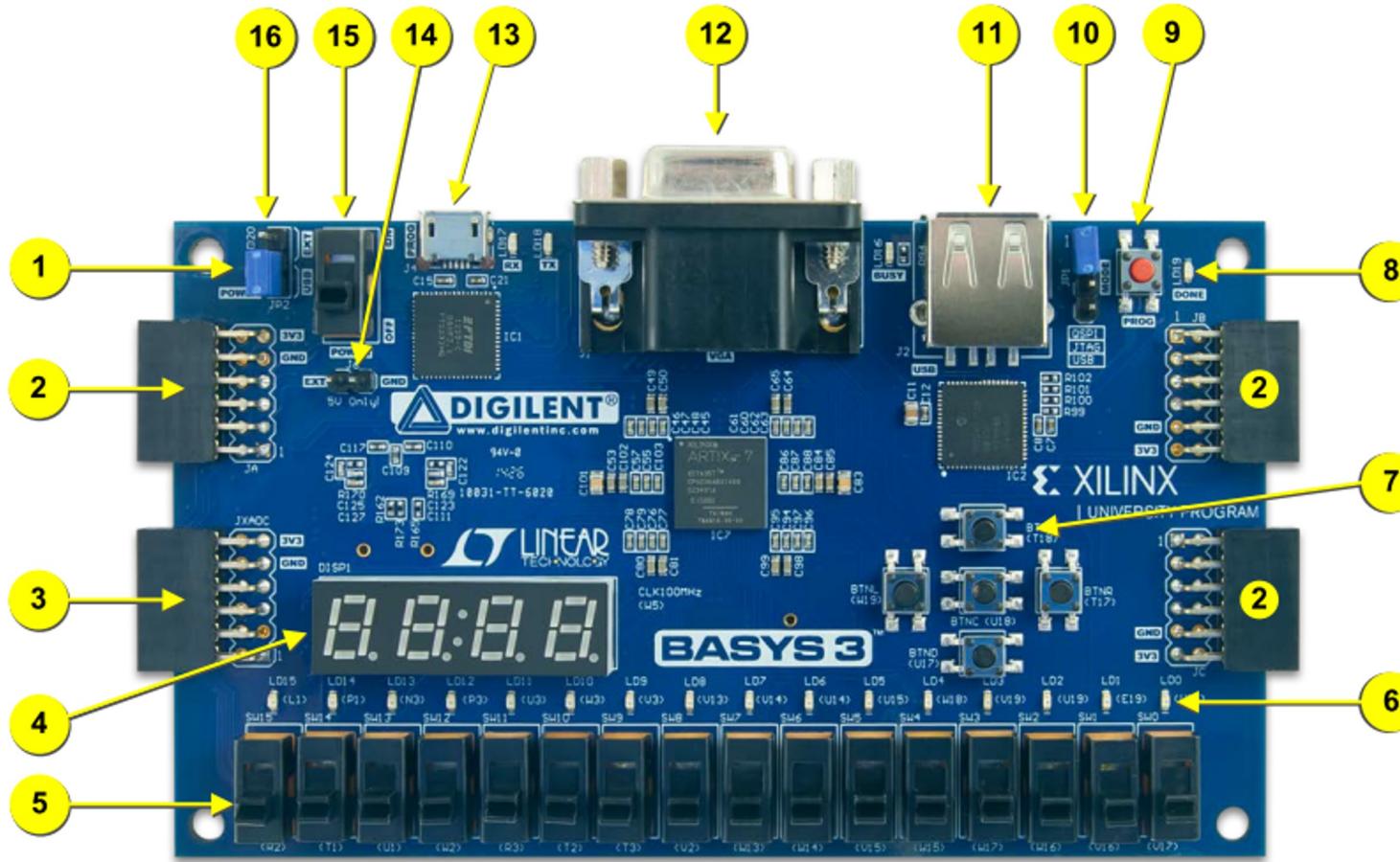


Figure 1. Basys3 FPGA board with callouts.

Callout	Component Description
1	Power good LED
2	Pmod connector(s)
3	Analog signal Pmod connector (XADC)
4	Four digit 7-segment display
5	Slide switches (16)
6	LEDs (16)
7	Pushbuttons (5)
8	FPGA programming done LED
9	FPGA configuration reset button
10	Programming mode jumper
11	USB host connector
12	VGA connector
13	Shared UART/ JTAG USB port
14	External power connector
15	Power Switch
16	Power Select Jumper



General Design Flow





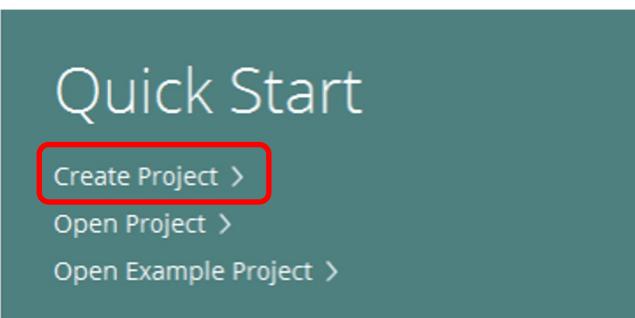
Create New Project (1/8)

1.

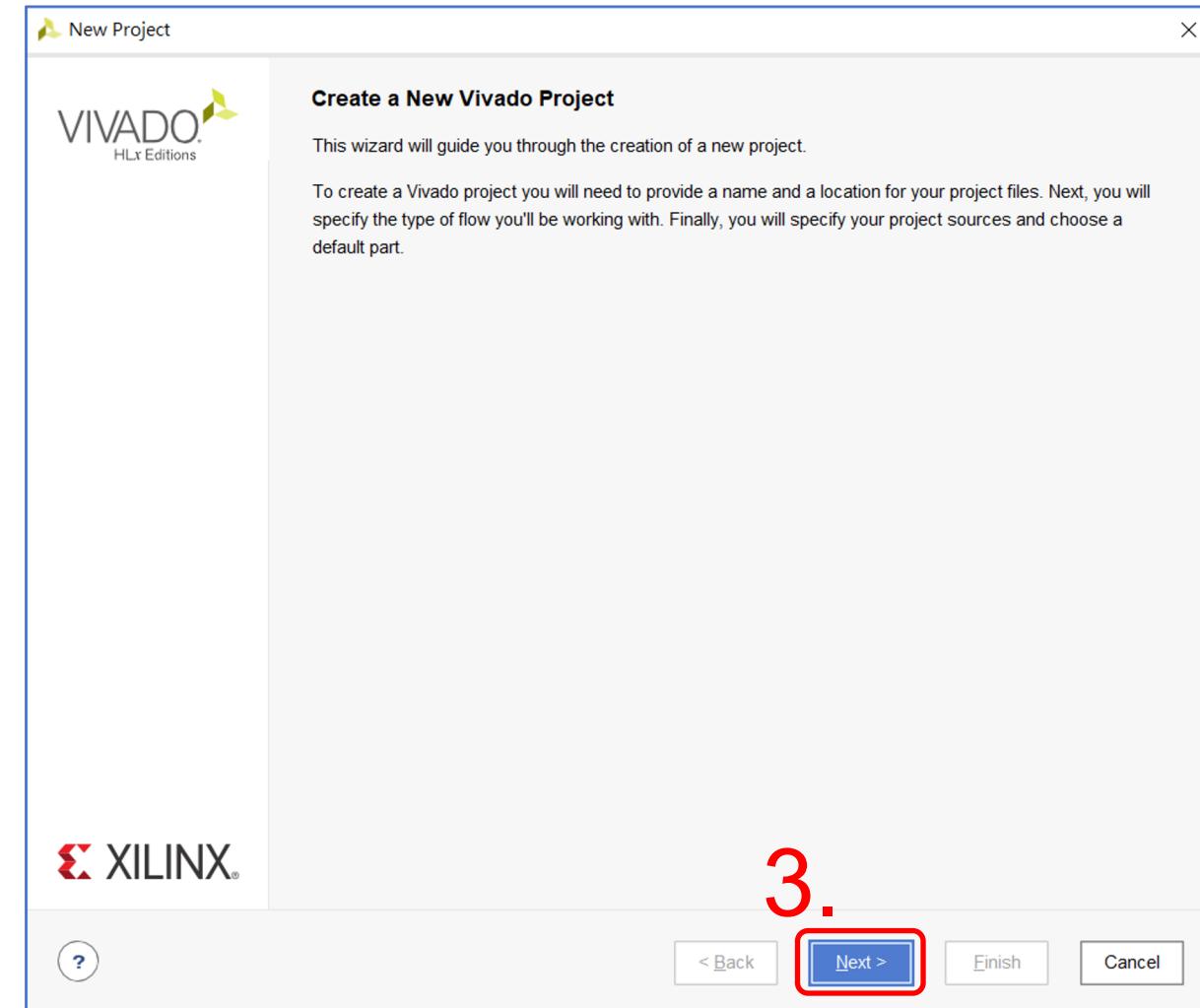


Launch Vivado

2.



Create Project



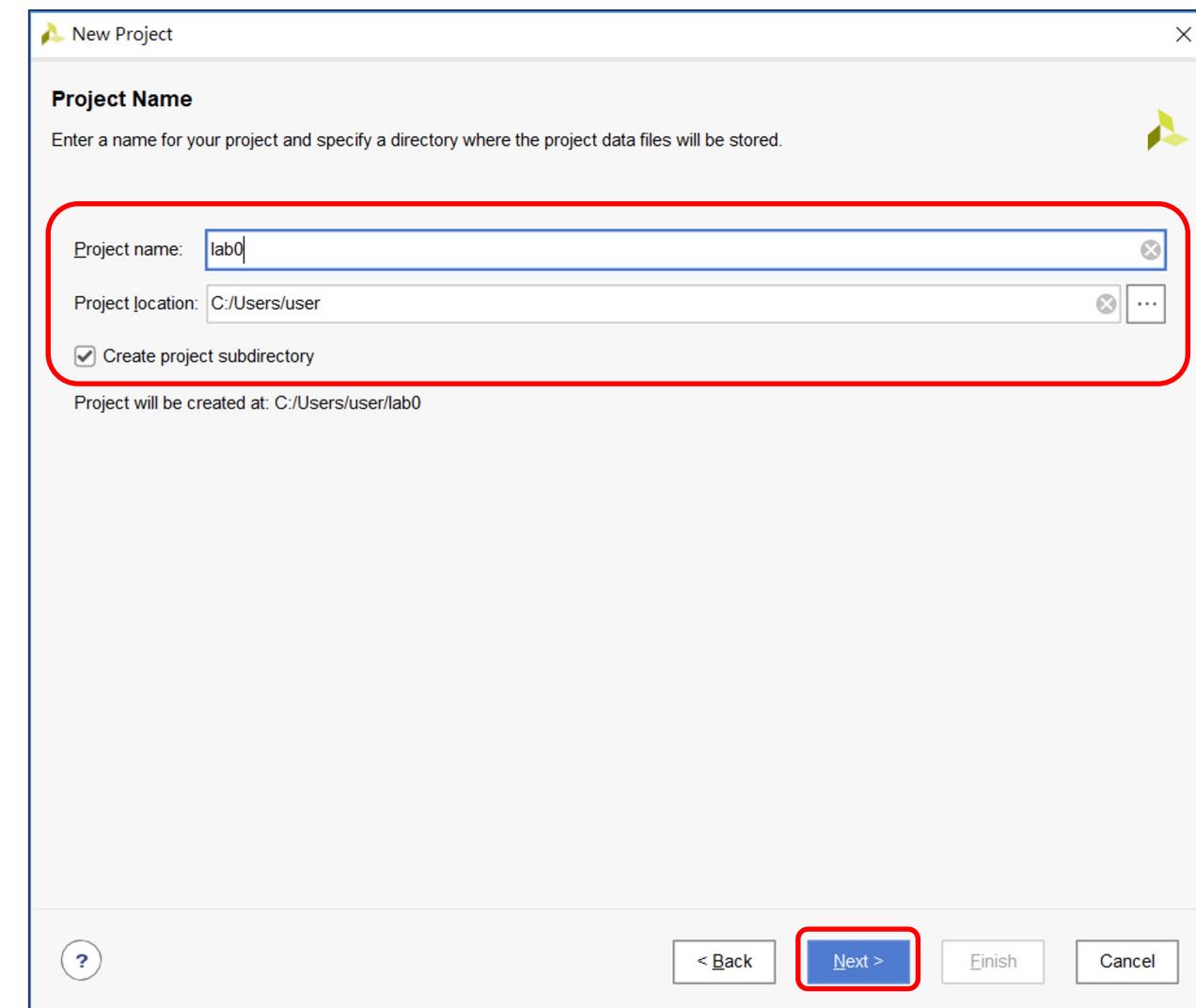
3.

Note: Vivado may check remote license so you may need Internet connection during its execution.



Create New Project (2/8)

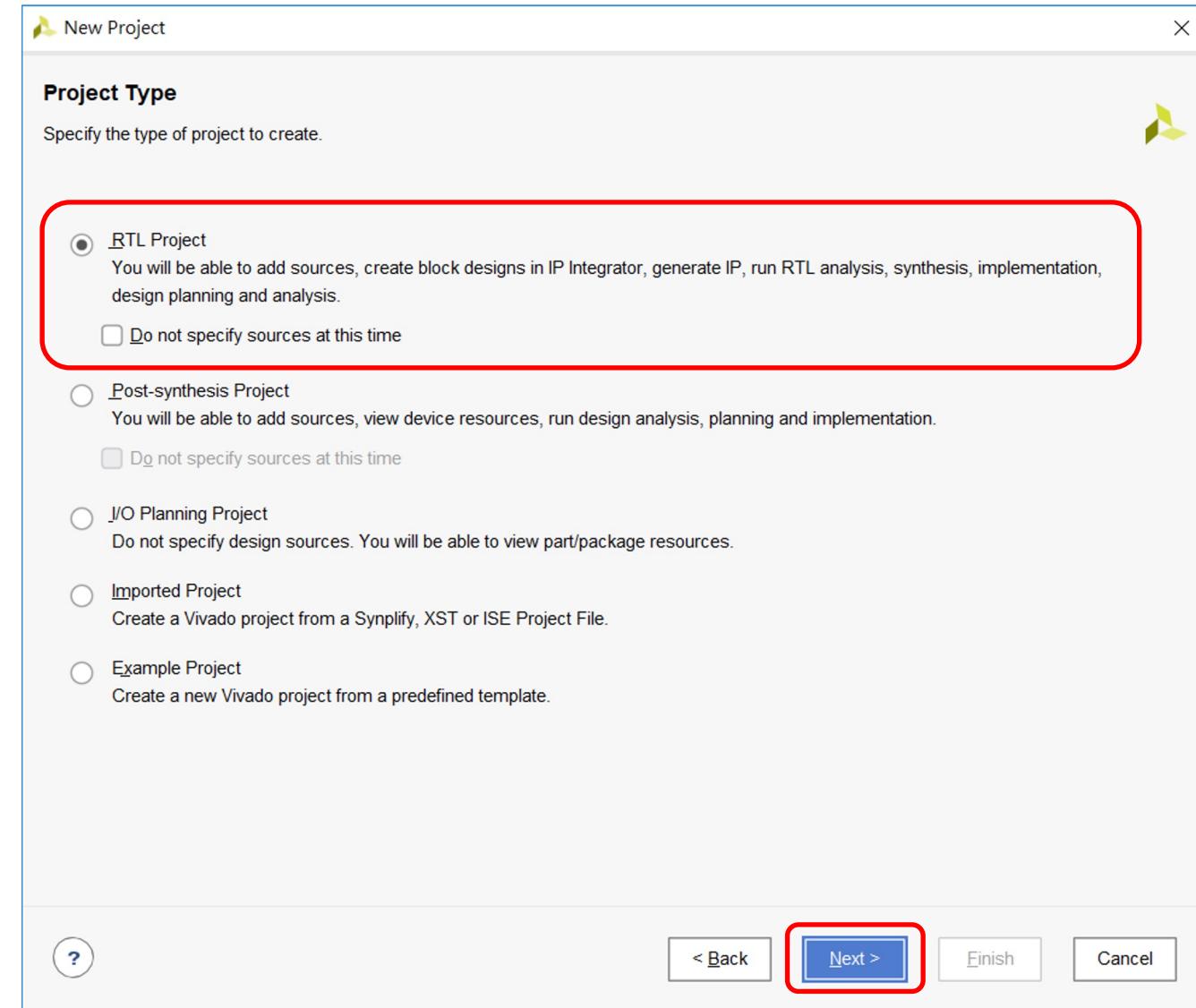
- Set *project name* and *location*





Create New Project (3/8)

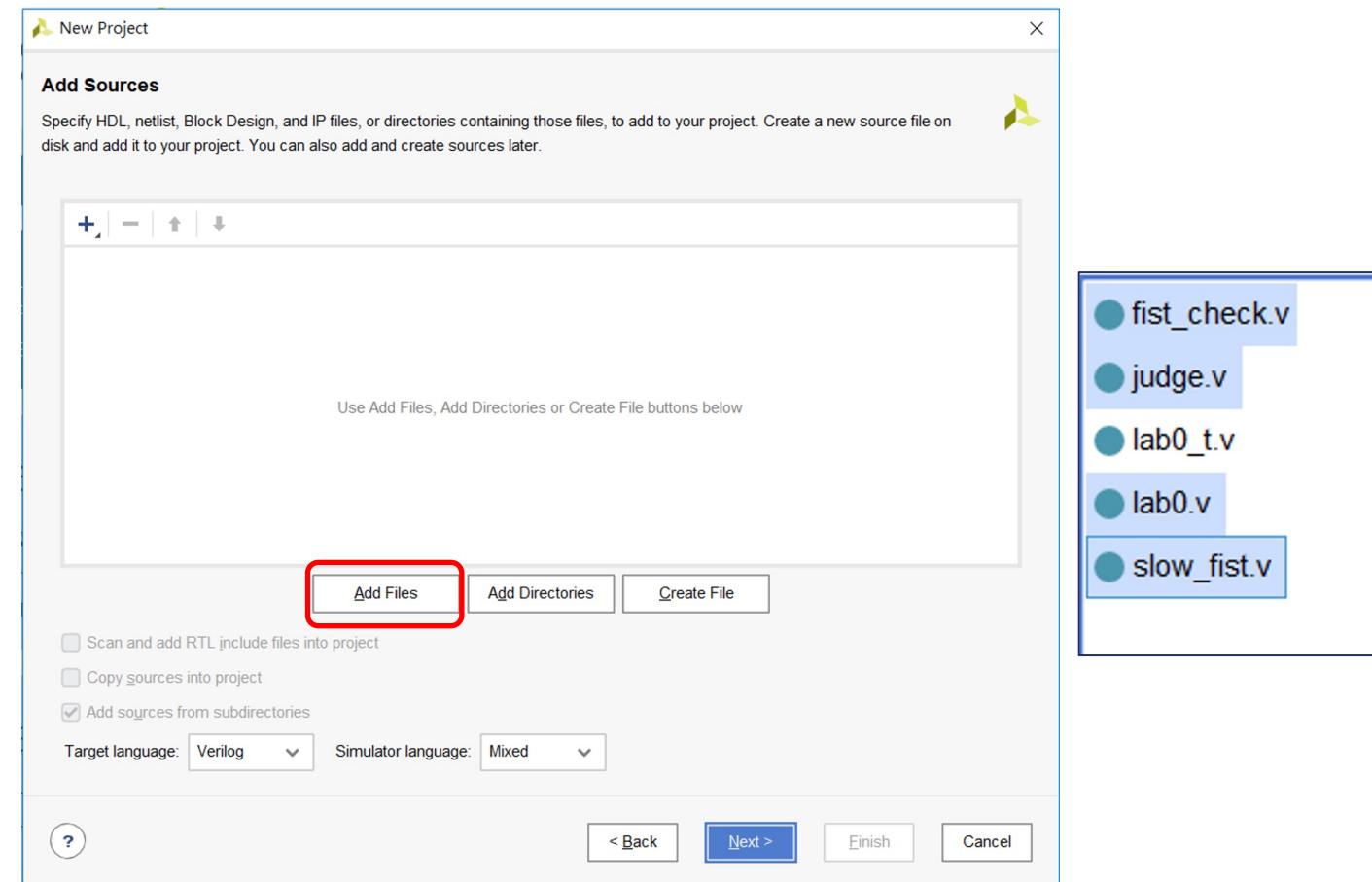
① Choose *project type*





Create New Project (4/8)

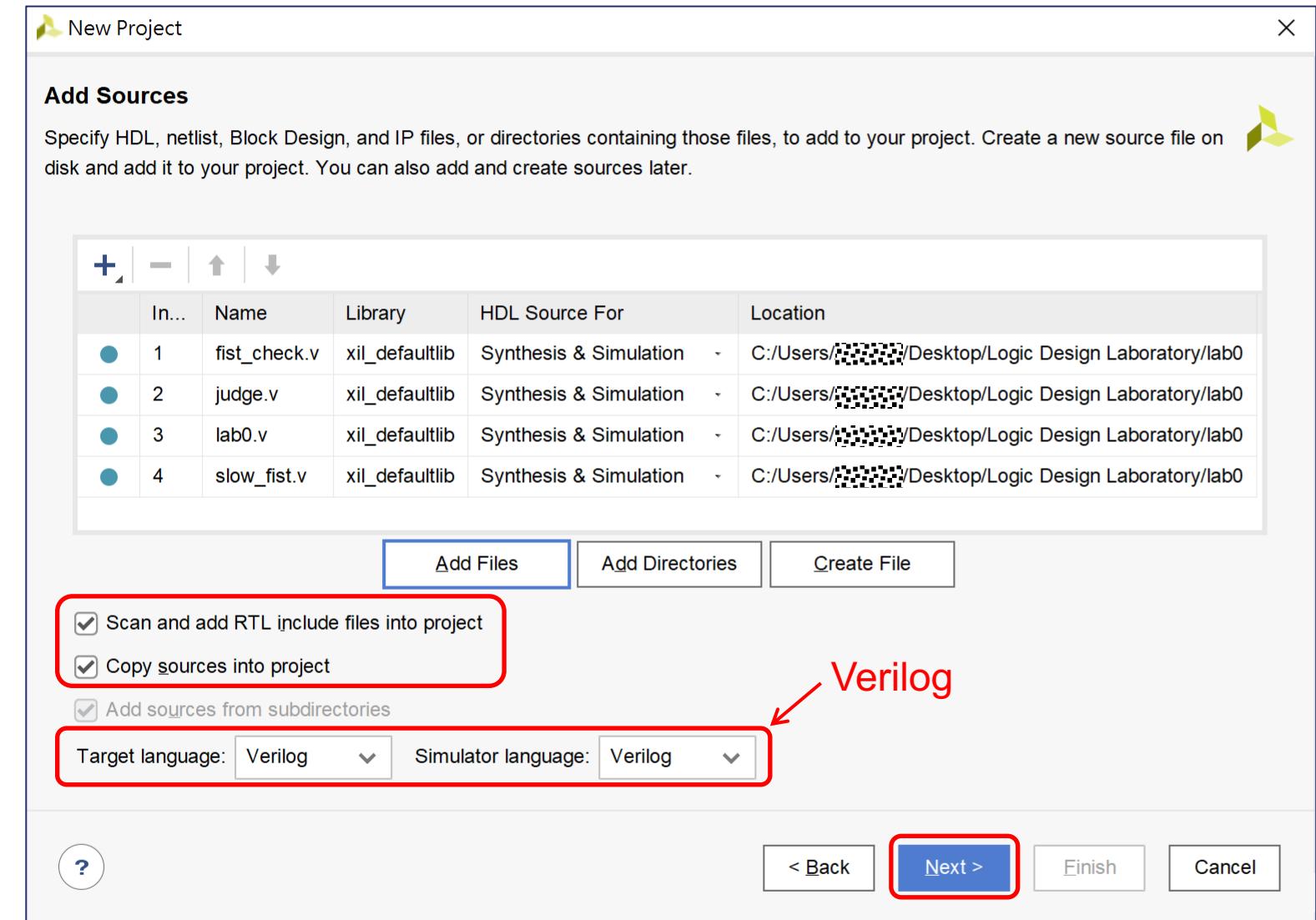
- Add all .v files except “lab0_t.v”





Create New Project (5/8)

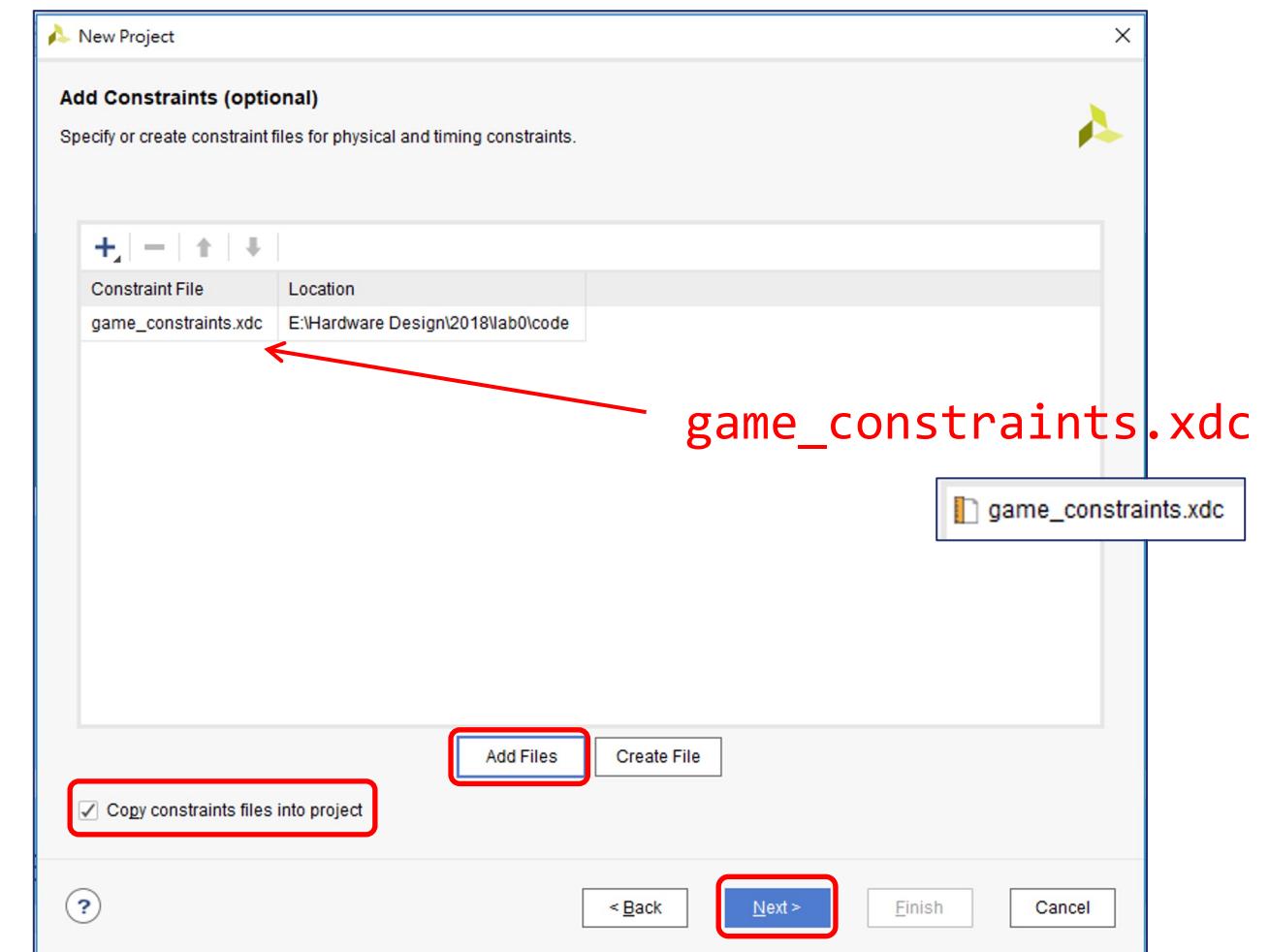
- Add all .v files except “lab0_t.v”





Create New Project (6/8)

- Add constraints (*.xdc)
 - ◆ Connections between Verilog ports and FPGA IOs
 - ◆ Timing spec such as
 - ▣ Clock port
 - ▣ Clock frequency
 - ▣ Etc.





Create New Project (7/8)



Part Number of
Our FPGA
xc7a35tcp236-1

New Project

Default Part

Choose a default Xilinx part or board for your project.

Family: Artix-7 Package: cpg236 Speed: -1

Parts | Boards

Reset All Filters

Category:	All	Package:	cpg236	Temperature:	All Remaining
Family:	Artix-7	Speed:	-1	Static power:	All Remaining

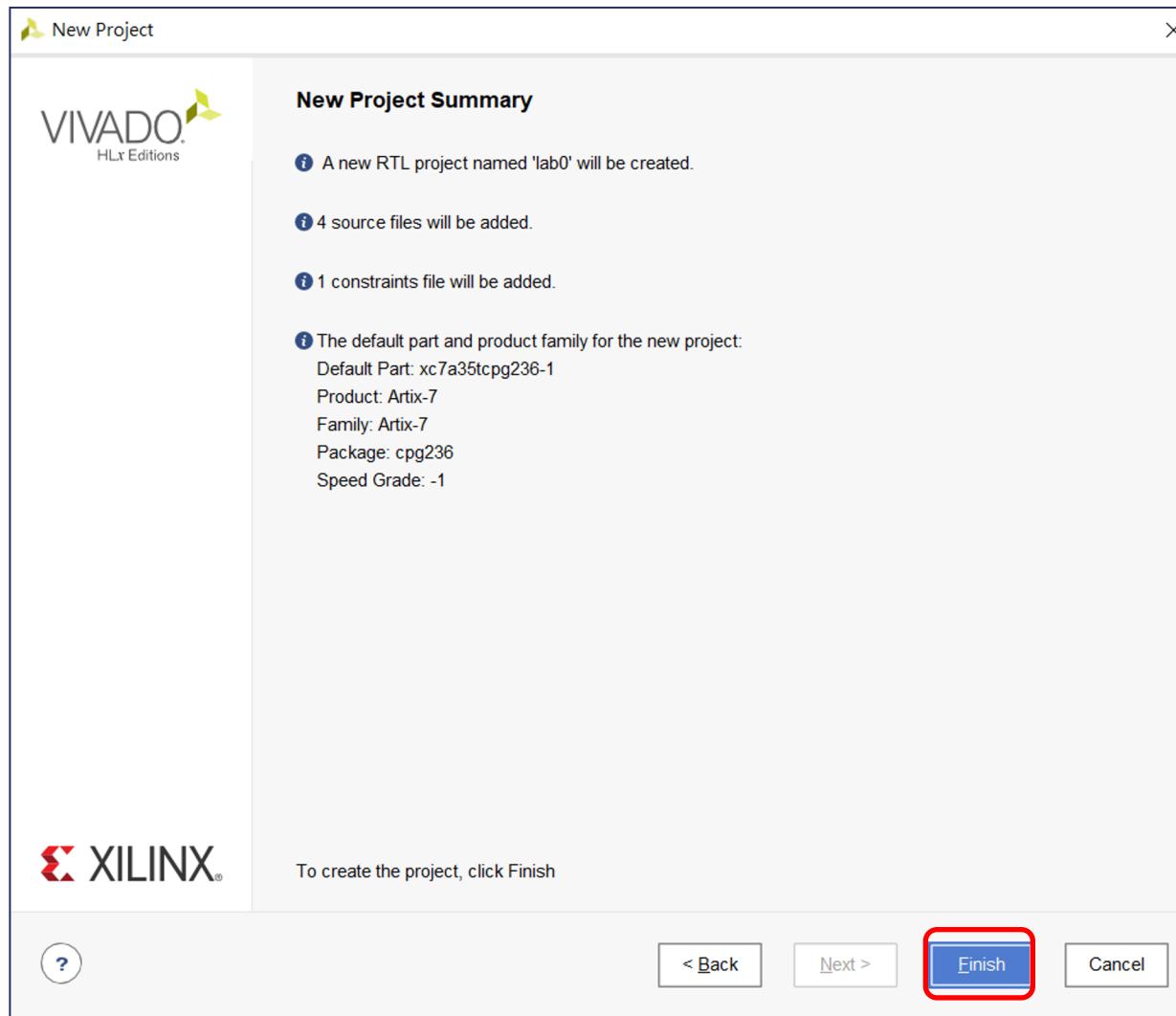
Search:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transce
xc7a15tcp236-1	236	106	10400	20800	25	0	45	2
xc7a35tcp236-1	236	106	20800	41600	50	0	90	2
xc7a50tcp236-1	236	106	32600	65200	75	0	120	2

< Back **Next >** Finish Cancel



Create New Project (8/8)



Note: If it takes forever in initializing the project creation, check your Internet connection.



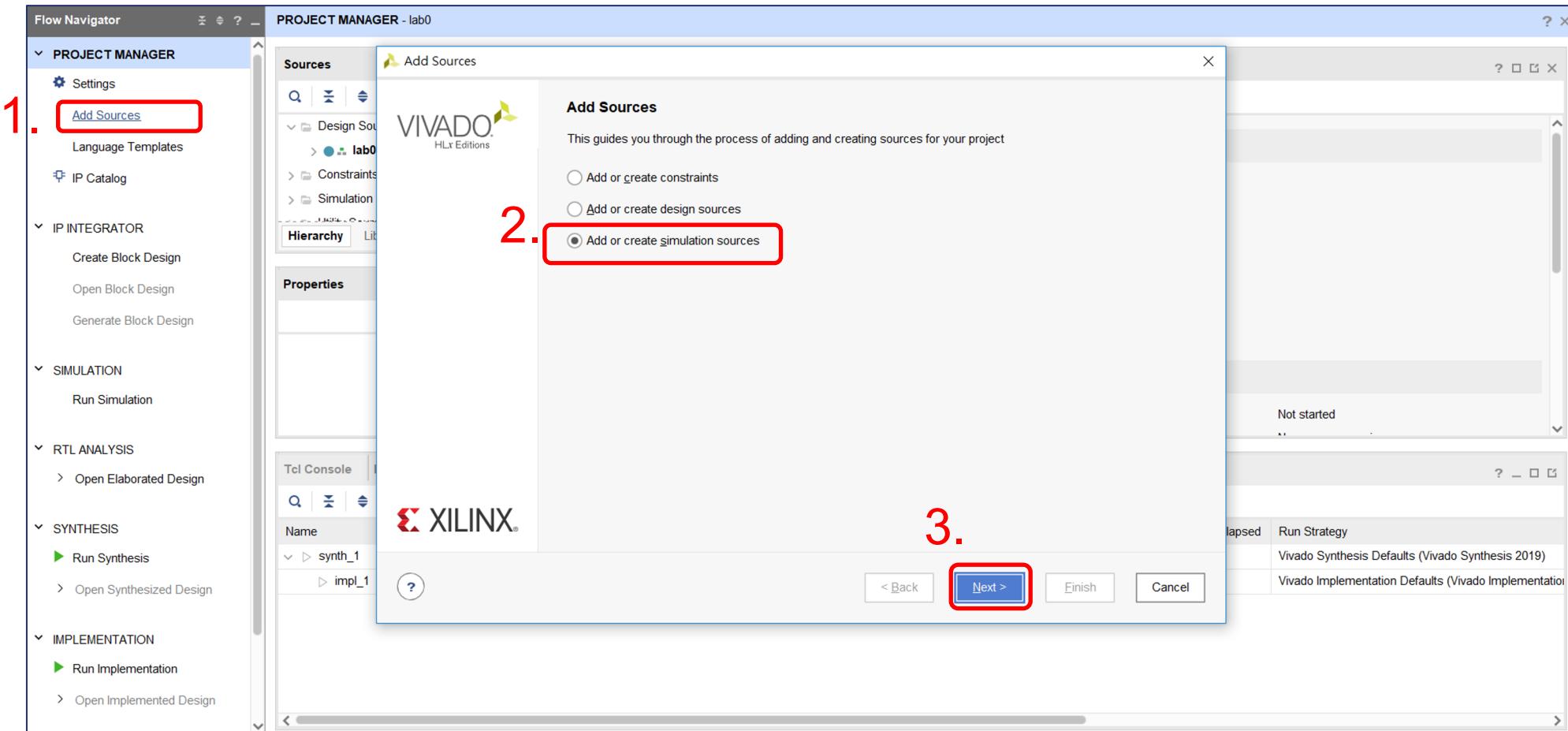
Simulation

- » Verilog simulation: RTL design + testbench



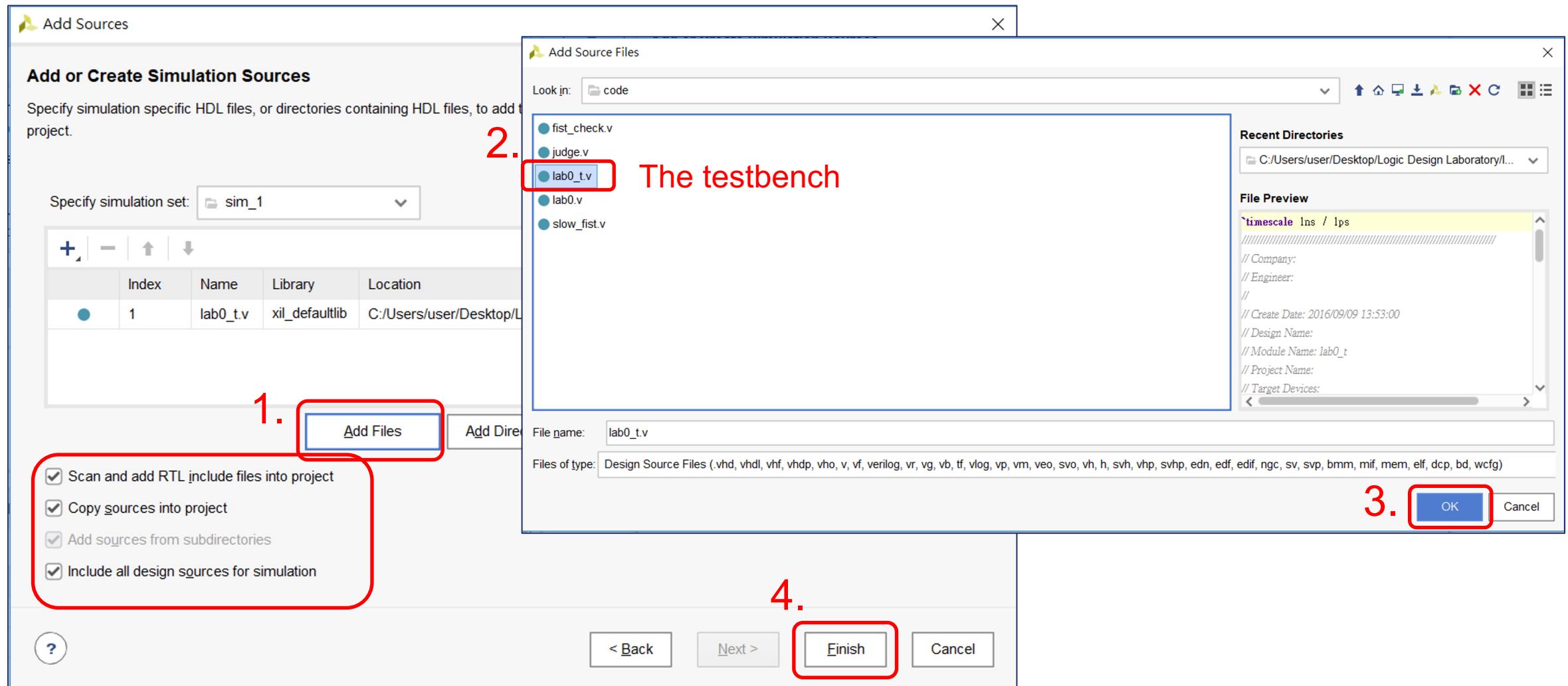
Simulation (1/5): Add Sources

- Add sources (e.g., design, testbench, etc.)



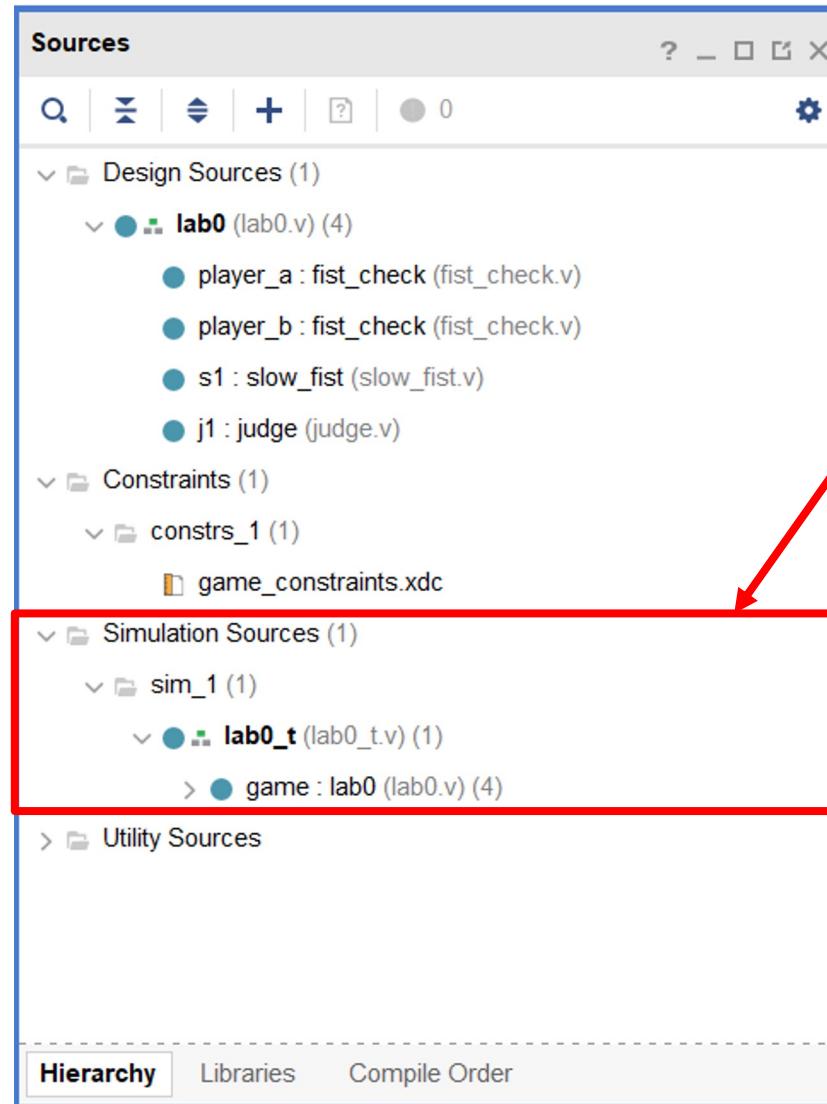


Simulation (2/5): Add Files





Simulation (3/5): Add Files



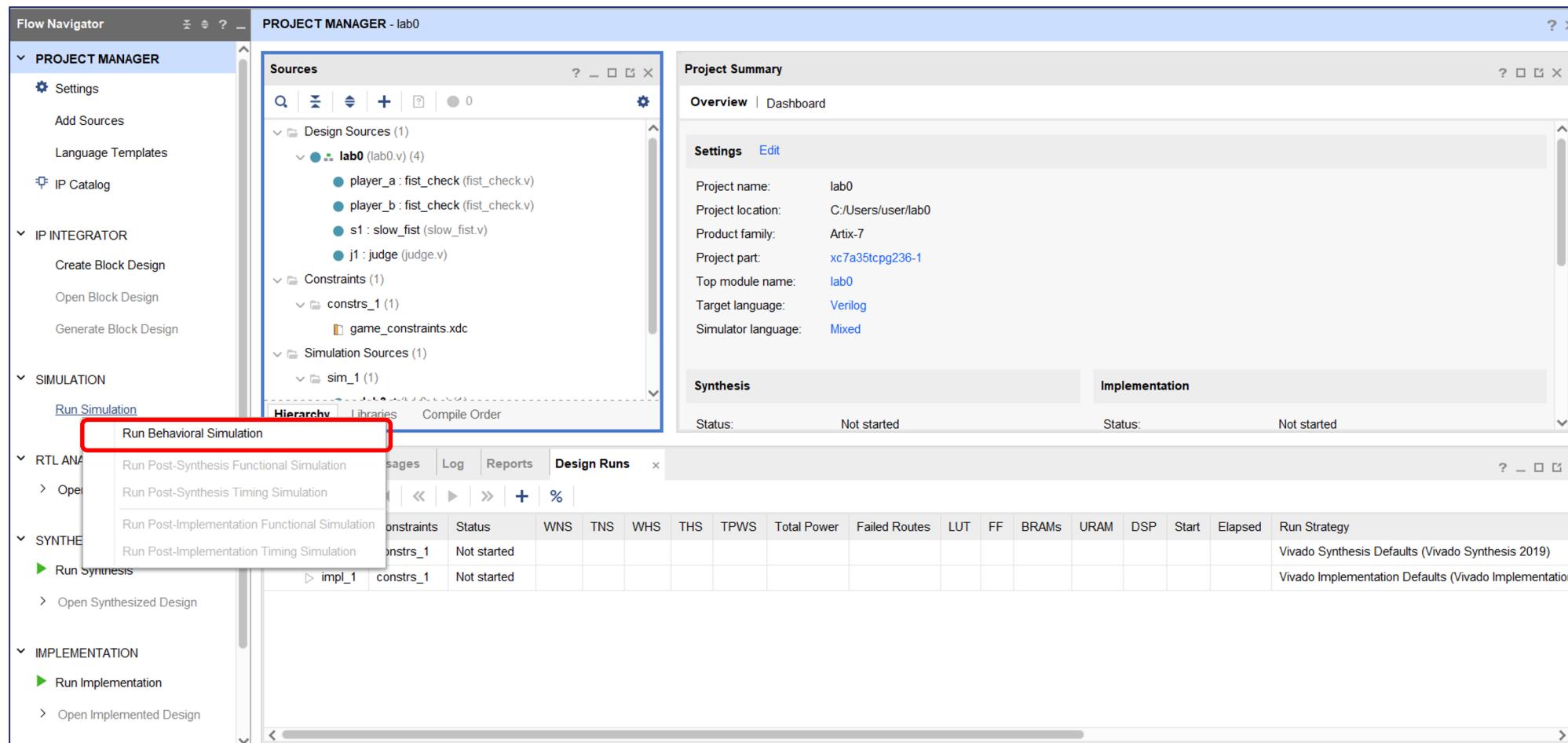
You may add more than one testbenches (and different versions of the specific design) and switch among them.

Simply right-click the mouse, and **enable/disable** the sources accordingly.



Simulation (4/5): Run Simulation

Run Simulation → Run Behavioral Simulation

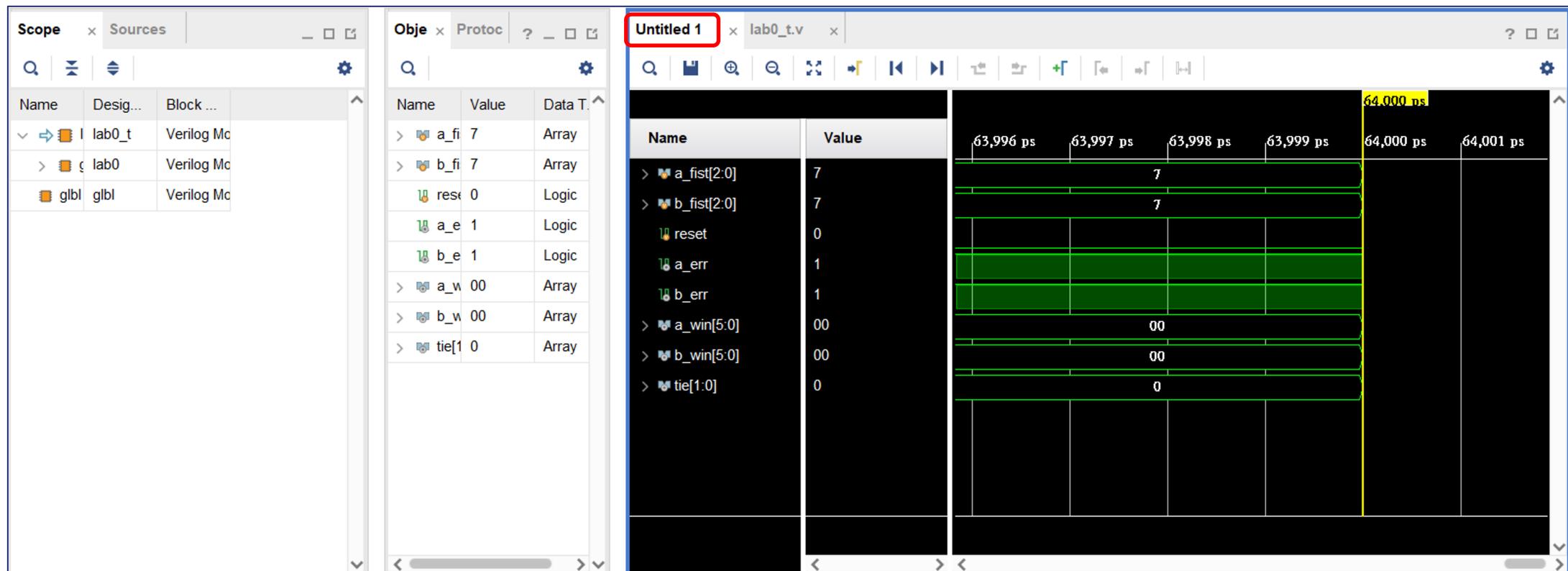




Simulation (5/5): Check Signals

○ Show waveform

Click



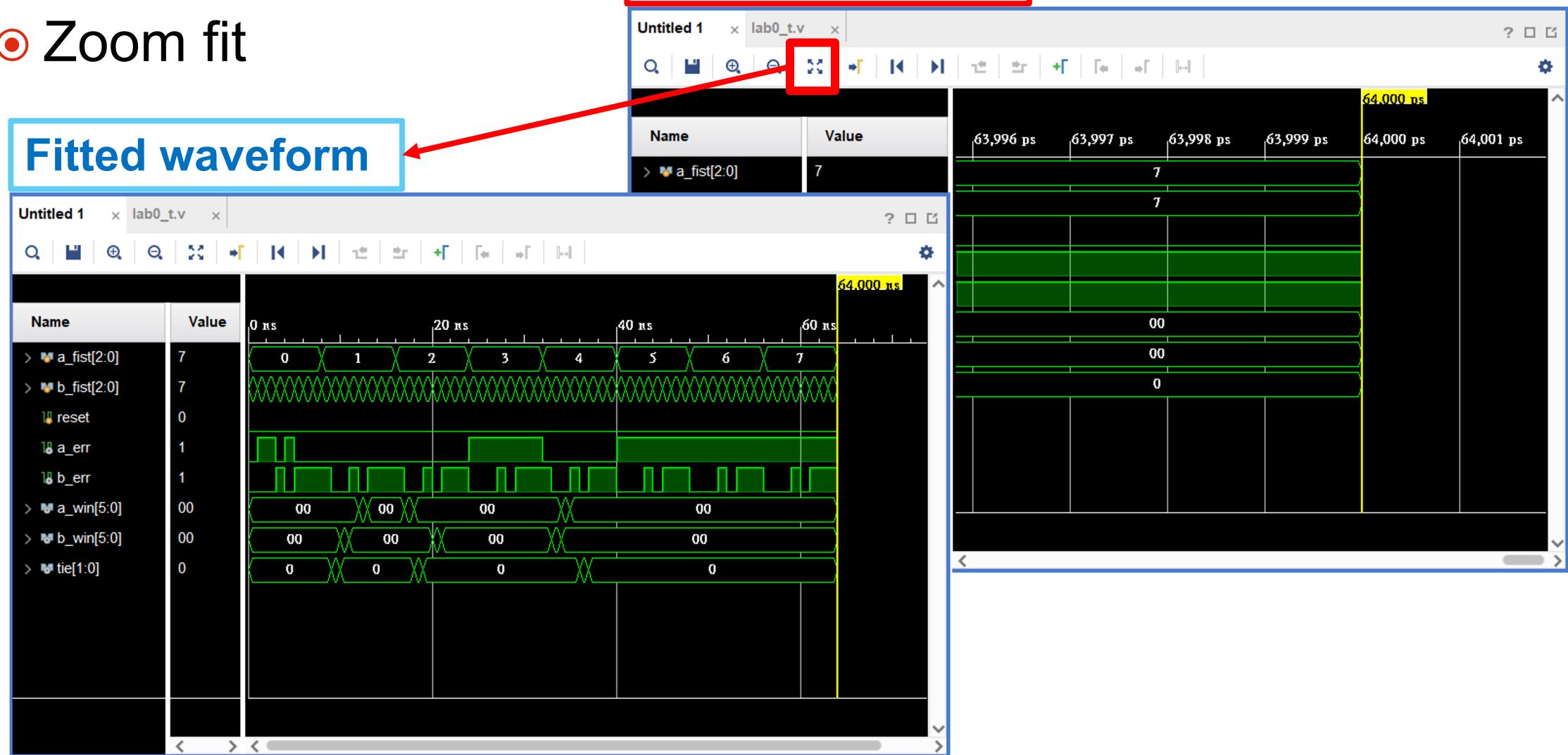


Debugging (1/4)

Zoom fit

Fitted waveform

Unfitted waveform

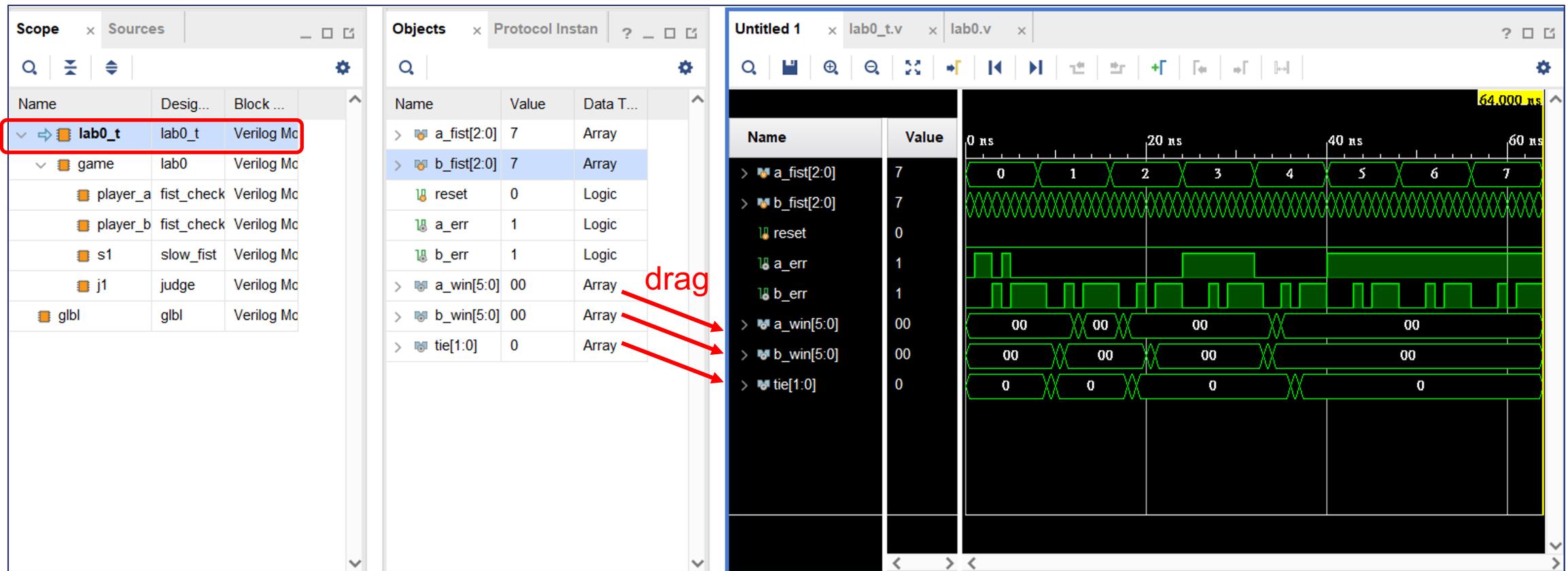




Debugging (2/4)

- Reorder (and/or modify) the signals by  and delete.

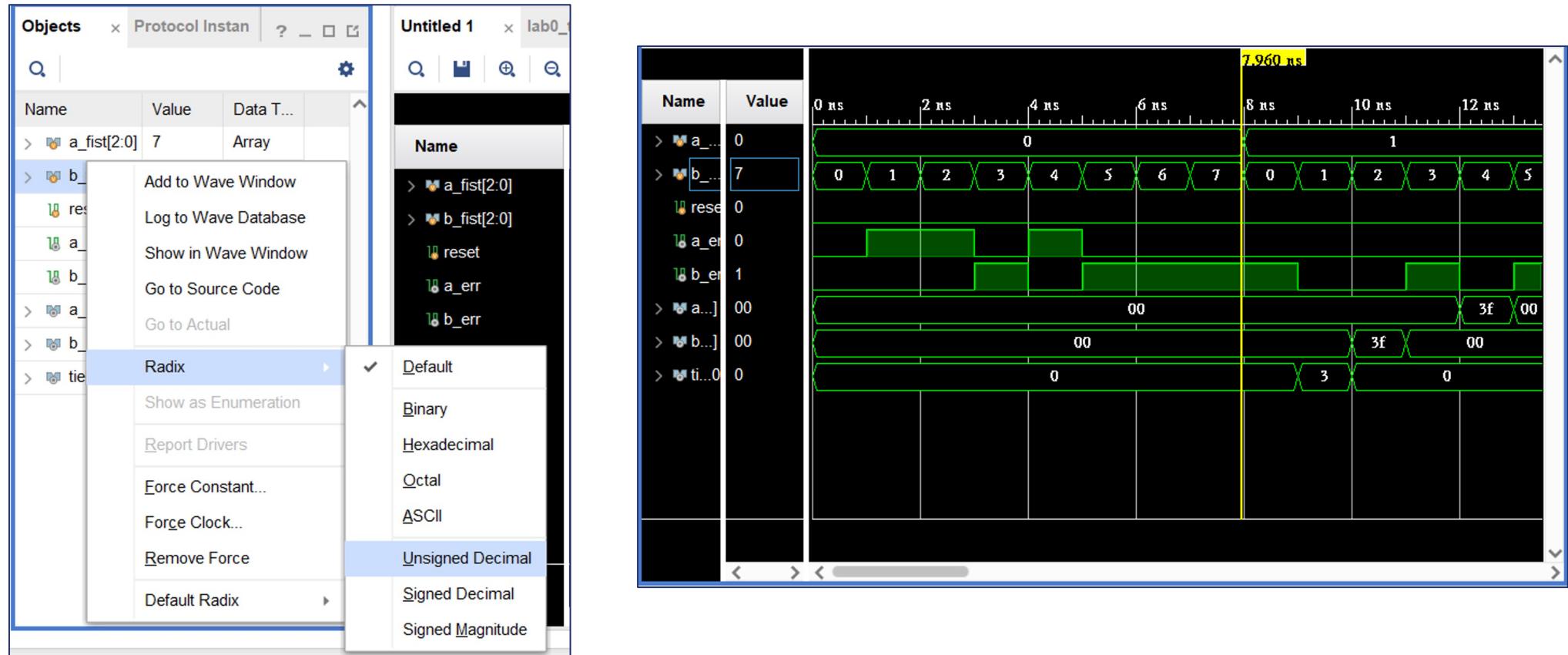
Choose the **block** that you want to see





Debugging (3/4)

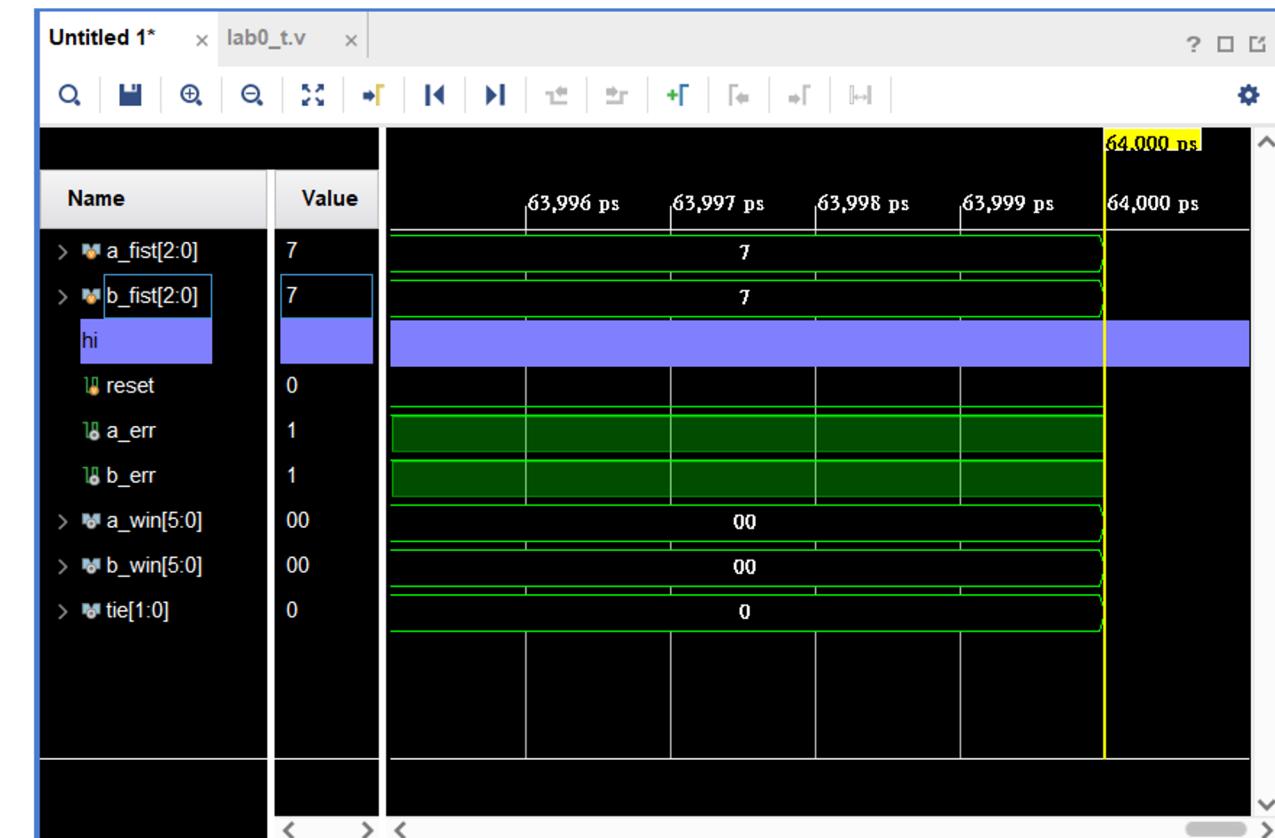
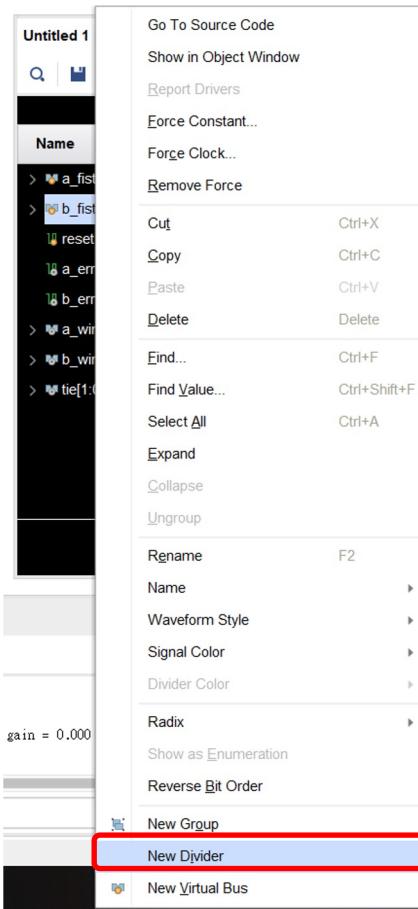
- Right click to open the popup menu again, and select Radix → Unsigned Decimal





Debugging (4/4)

- Right click to open the popup menu again, and select *New Divider*



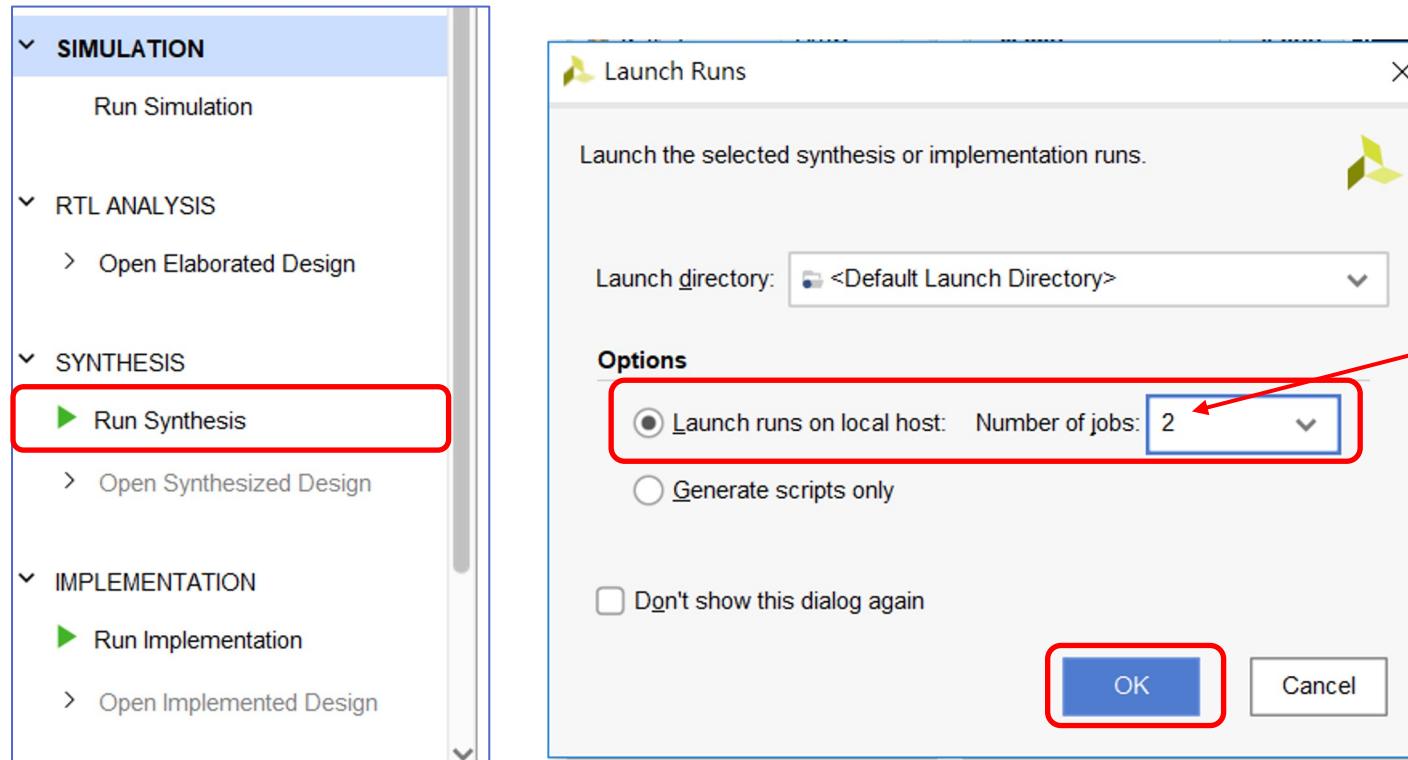


Synthesis

- » RTL design → gate-level design
- » RTL code only (no testbench)



Synthesis (1/2)

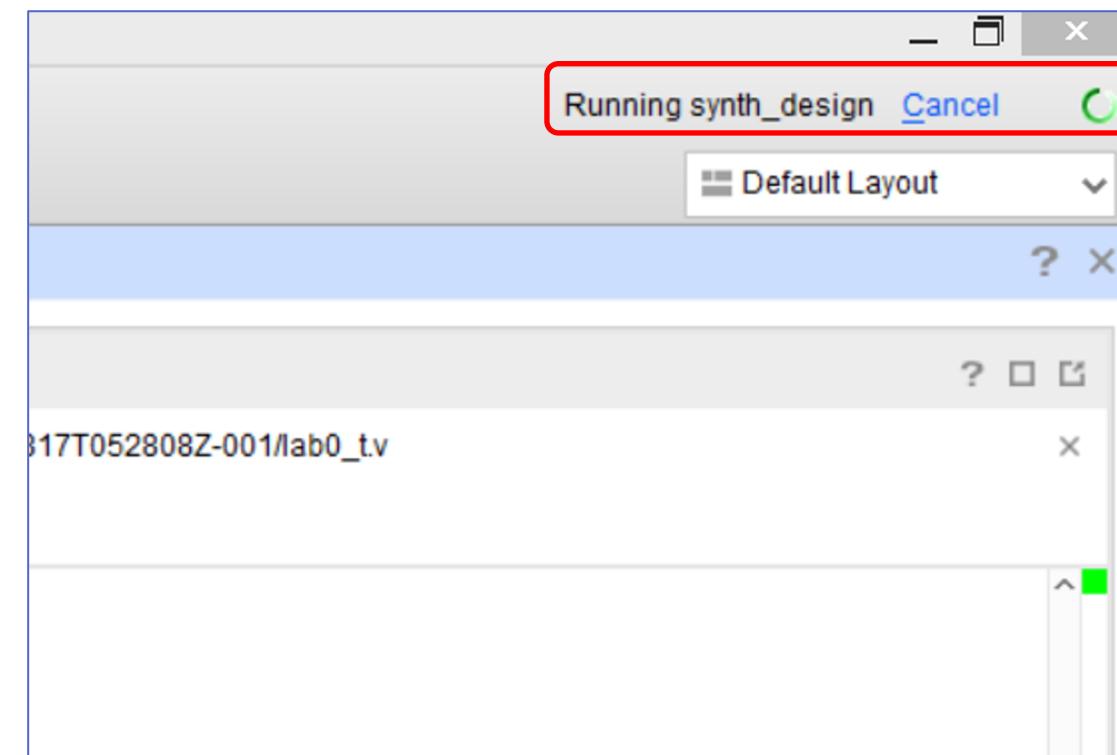


You may increase to 8 or 12 or more (depending on your CPU) to speed up the synthesis!



Synthesis (2/2)

- Wait for a while



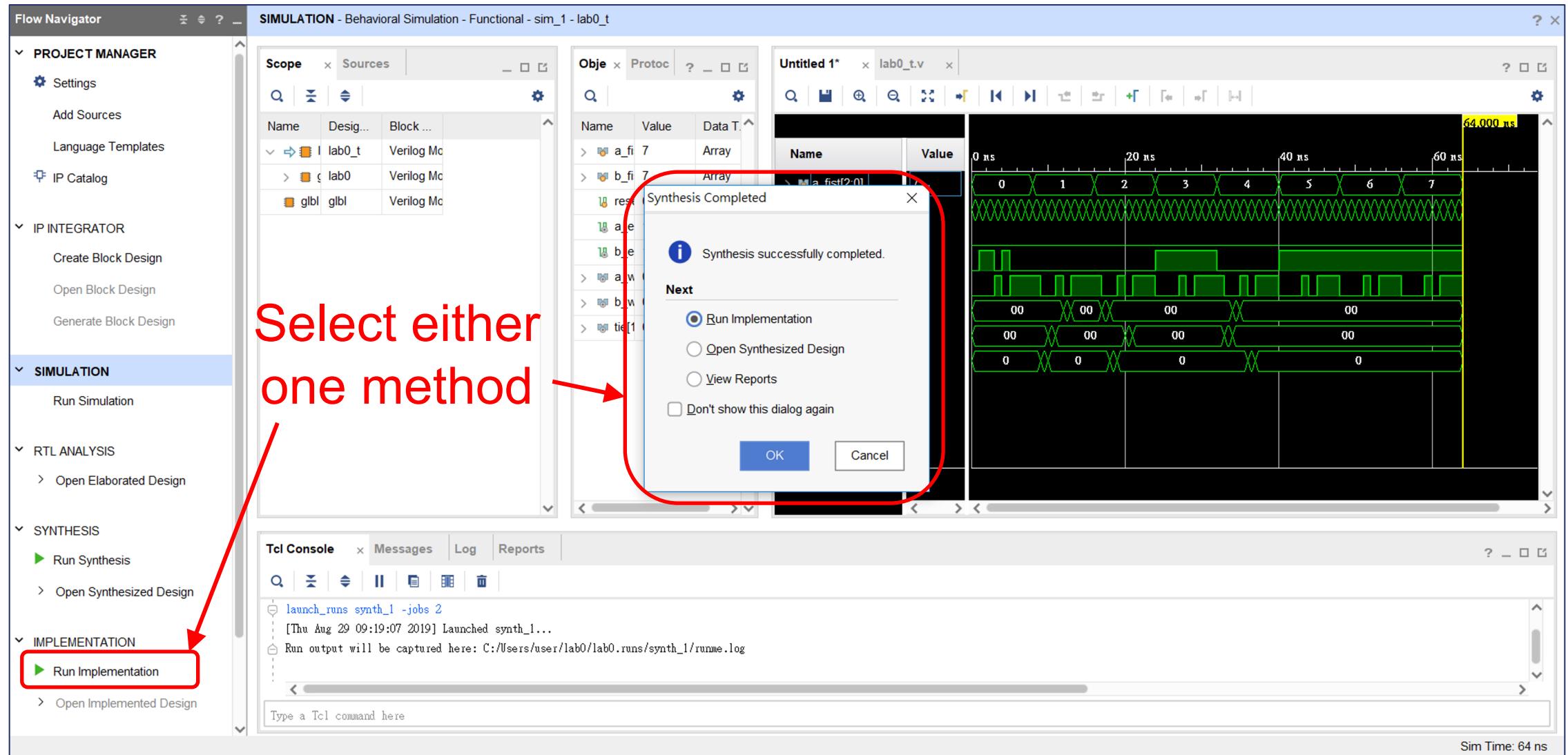


Implementation

- » Gate-level design → mapped into FPGA



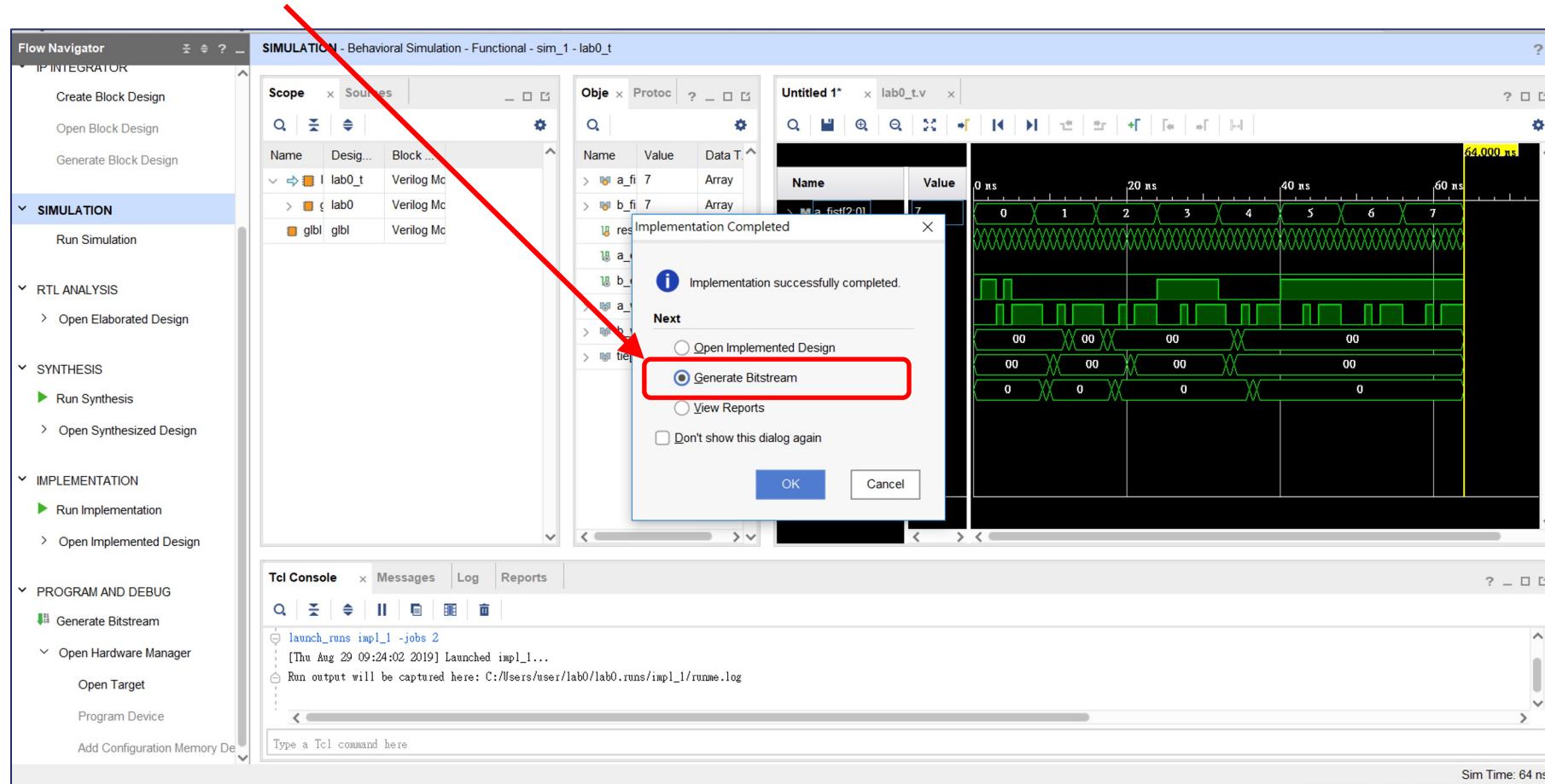
Run Implementation





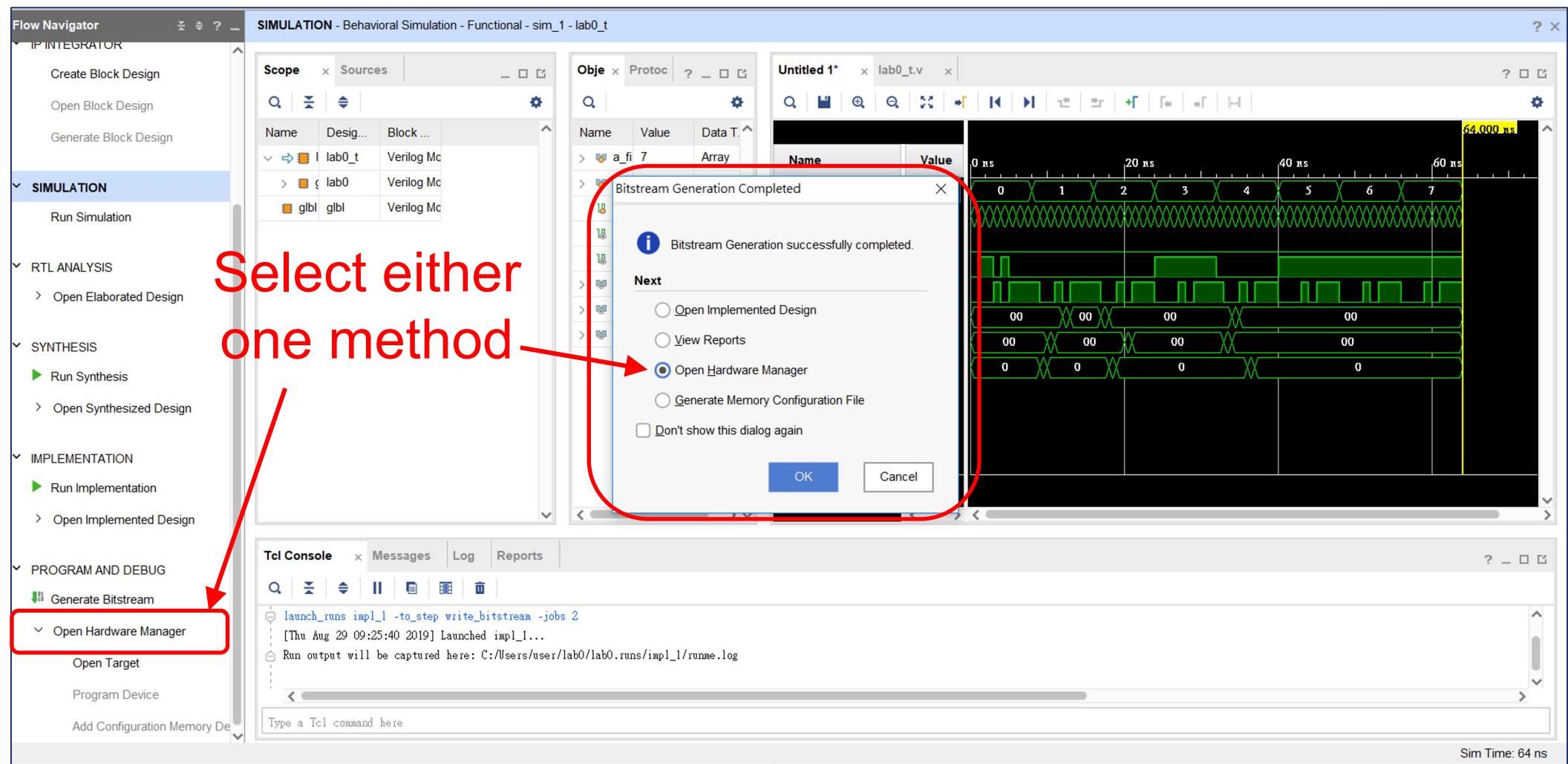
Generate Bitstream (Bit File)

NOTE: Once synthesized, you can generate Bitstream directly without going through the synthesis and implementation again!





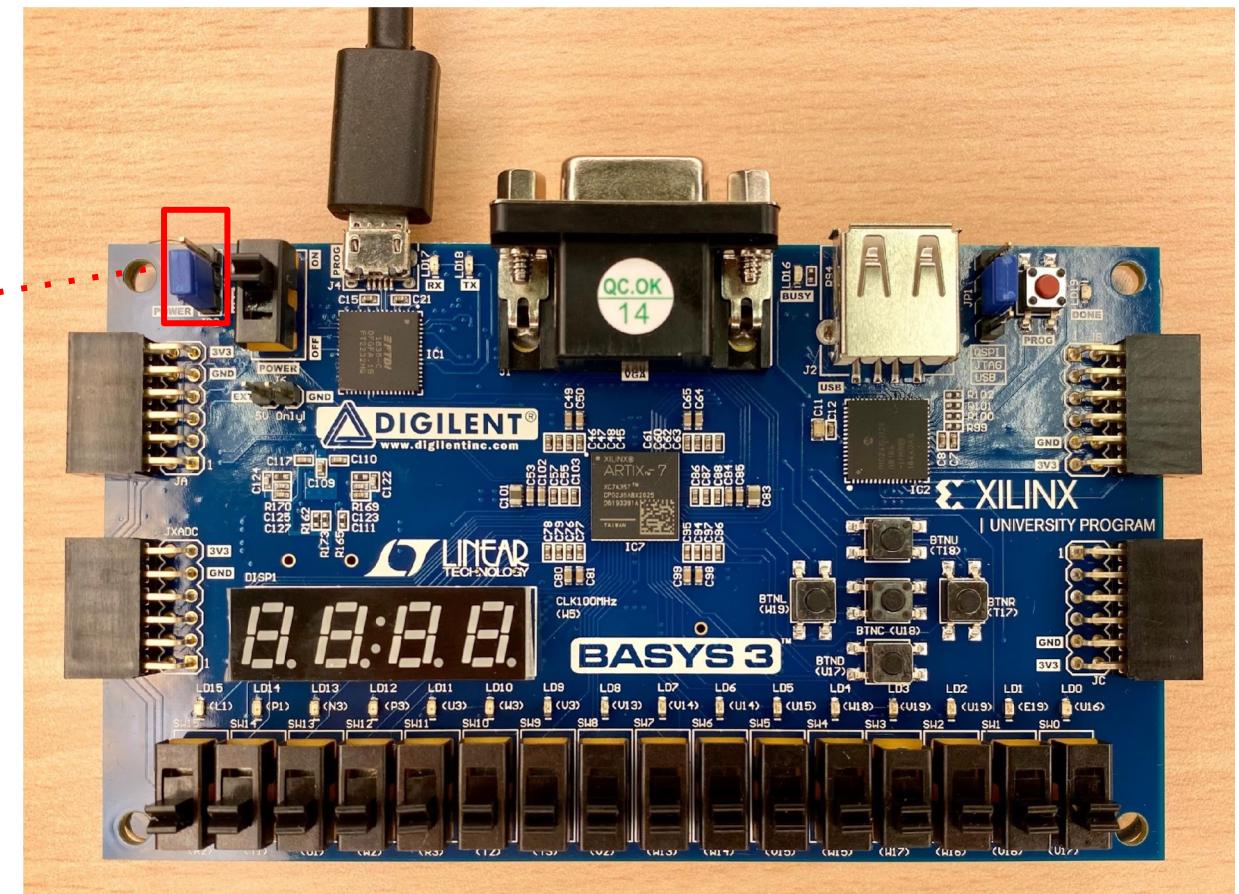
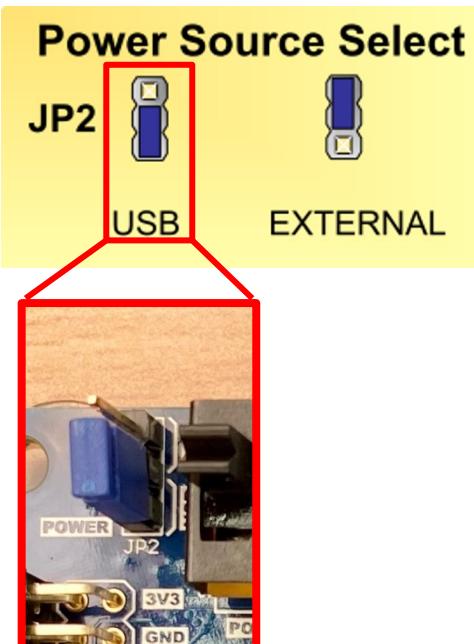
Open Hardware Manager





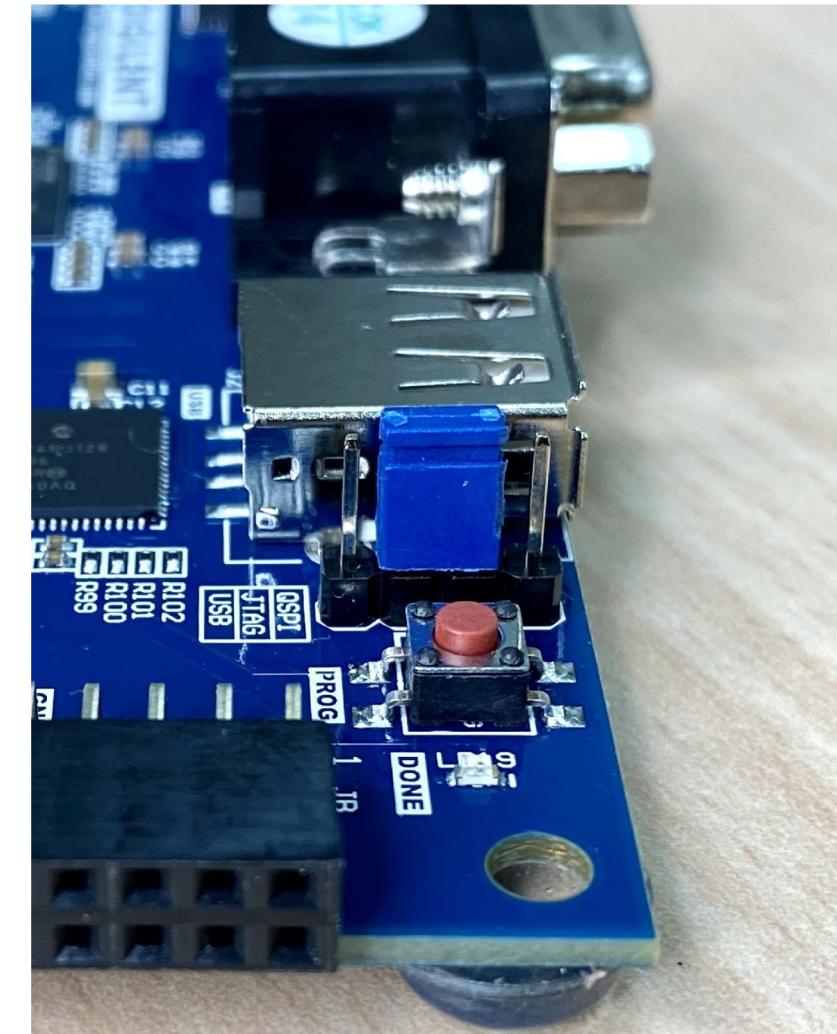
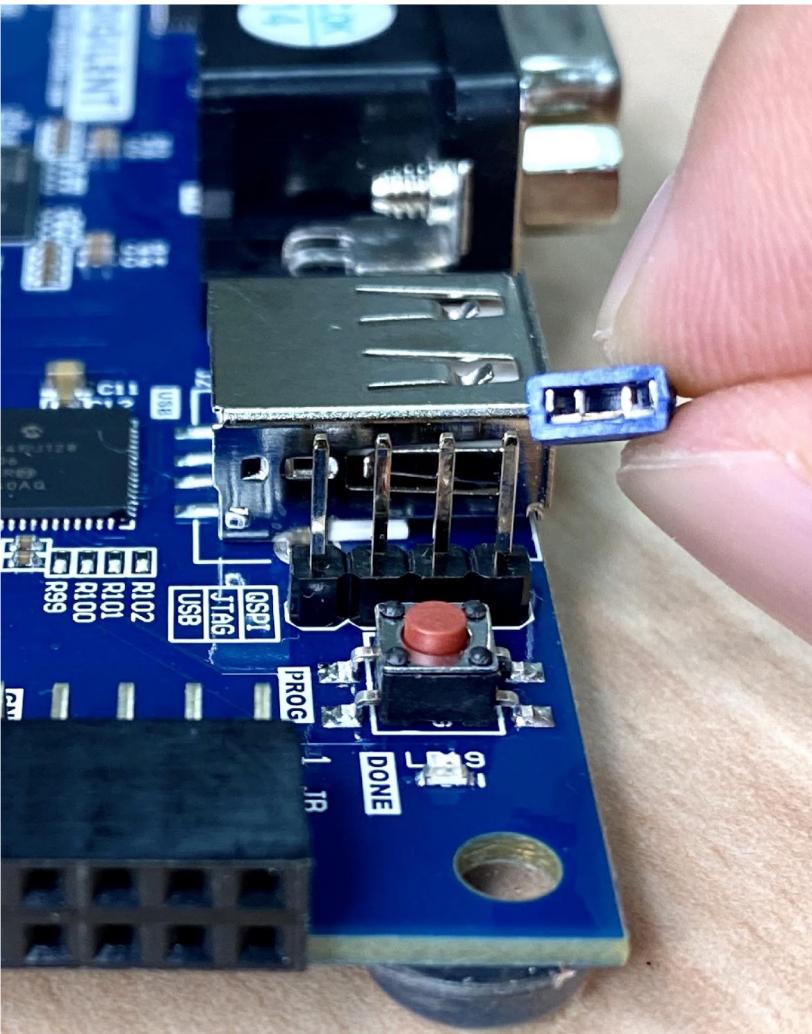
Power Supply to FPGA Board

- FPGA board receives power from either
 - ◆ MicroUSB port (default), or
 - ◆ A 5V external power supply





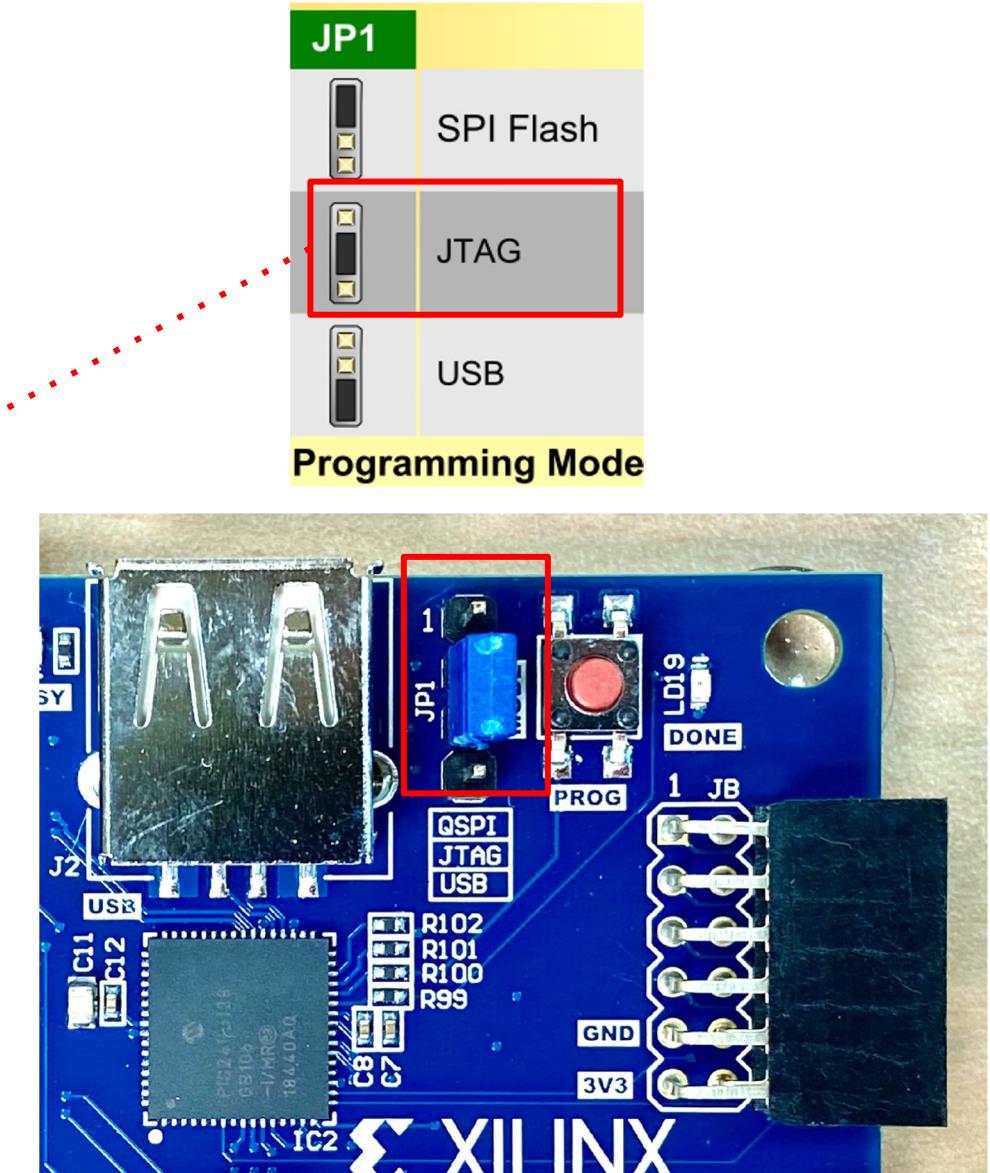
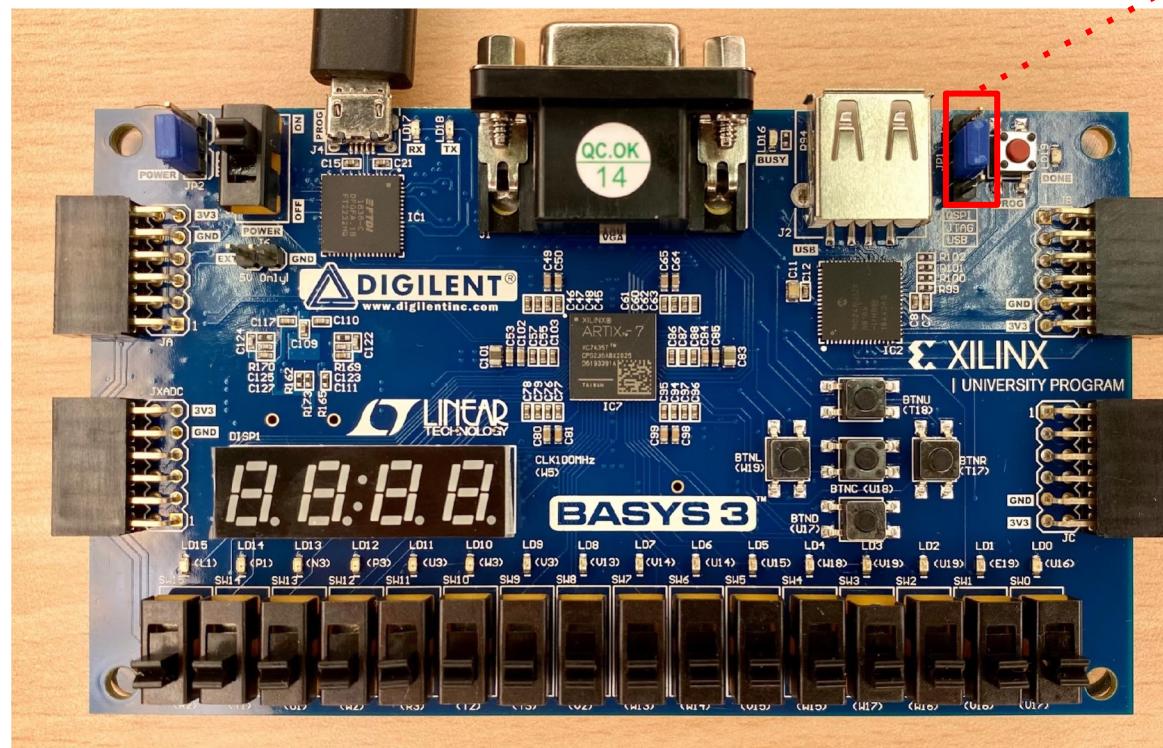
Jumper (跳線) Setting





Bitstream Downloading

- FPGA board receives **Bitstream** from:
 - ◆ Flash
 - ◆ JTAG (Default)
 - ◆ USB Drive

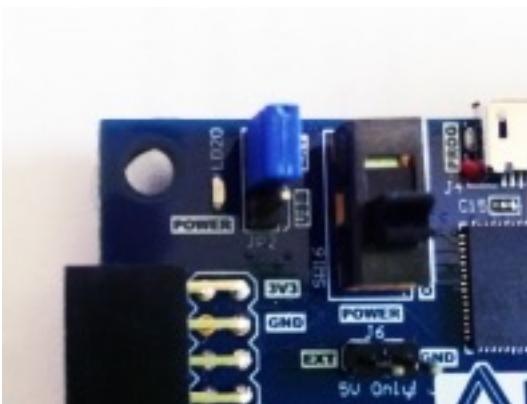
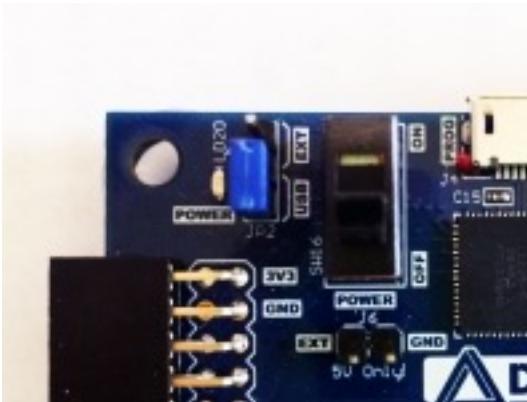




Jumper Settings of JP2 and JP1

① JP2

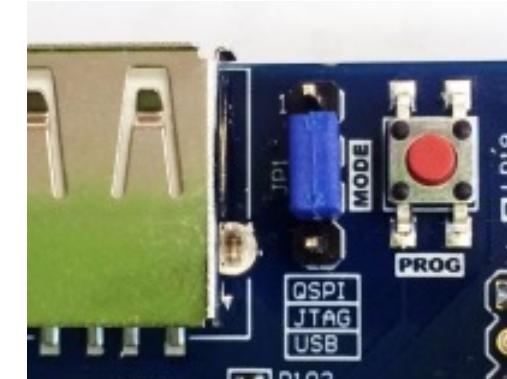
USB
Power



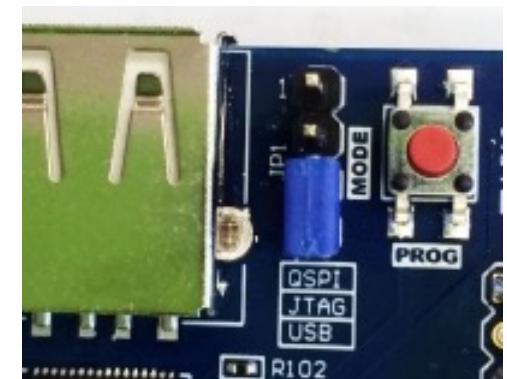
External
Power

① JP1

JTAG
Programming



Quad SPI (Flash)
Programming

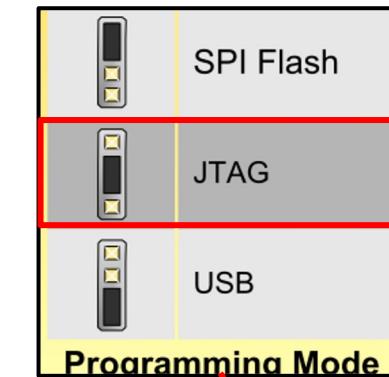


USB Host
Programming

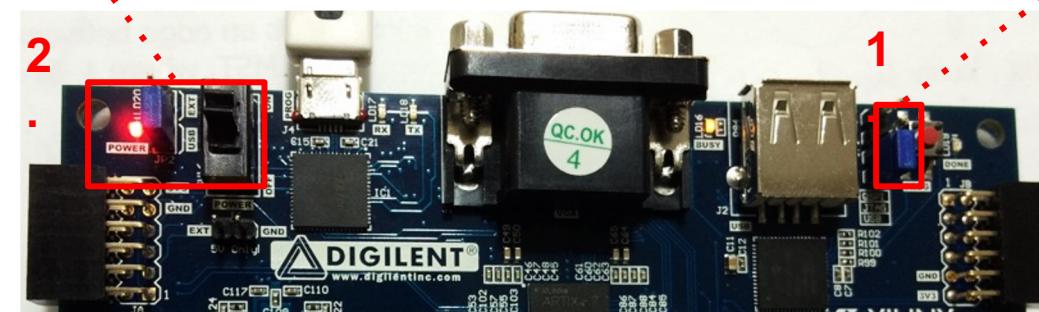


Power On

Step 1:
Set the blue jumper JP1 to [**JTAG**] mode



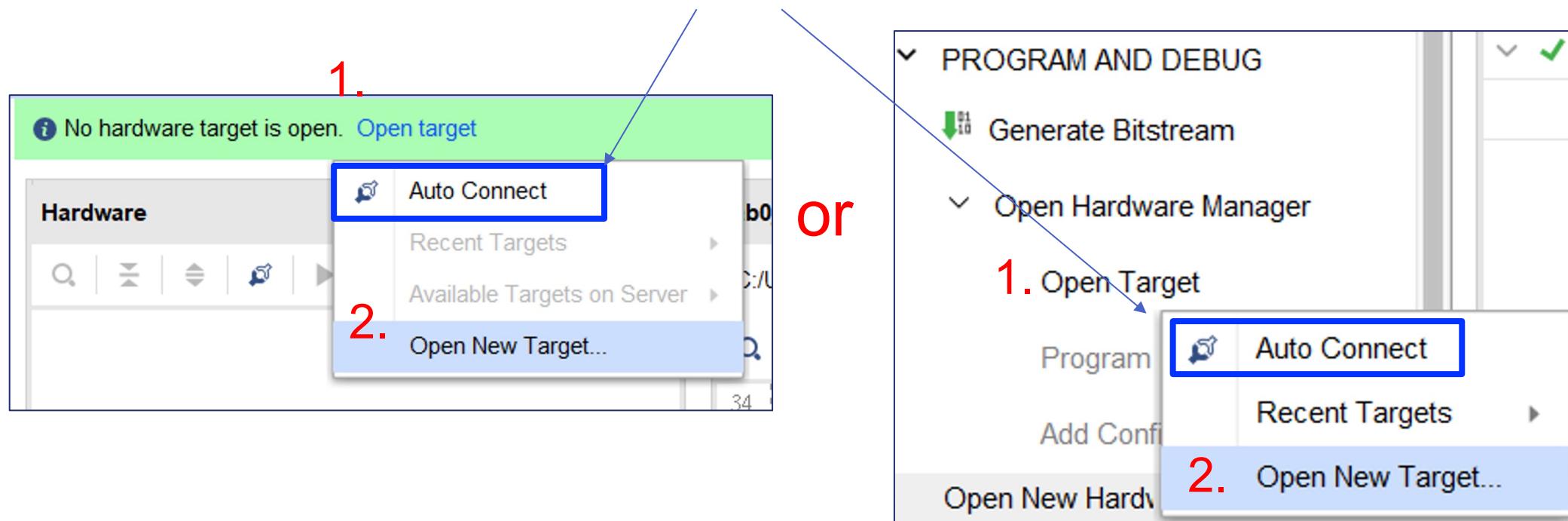
Step 2:
Turn the power switch to [**ON**]





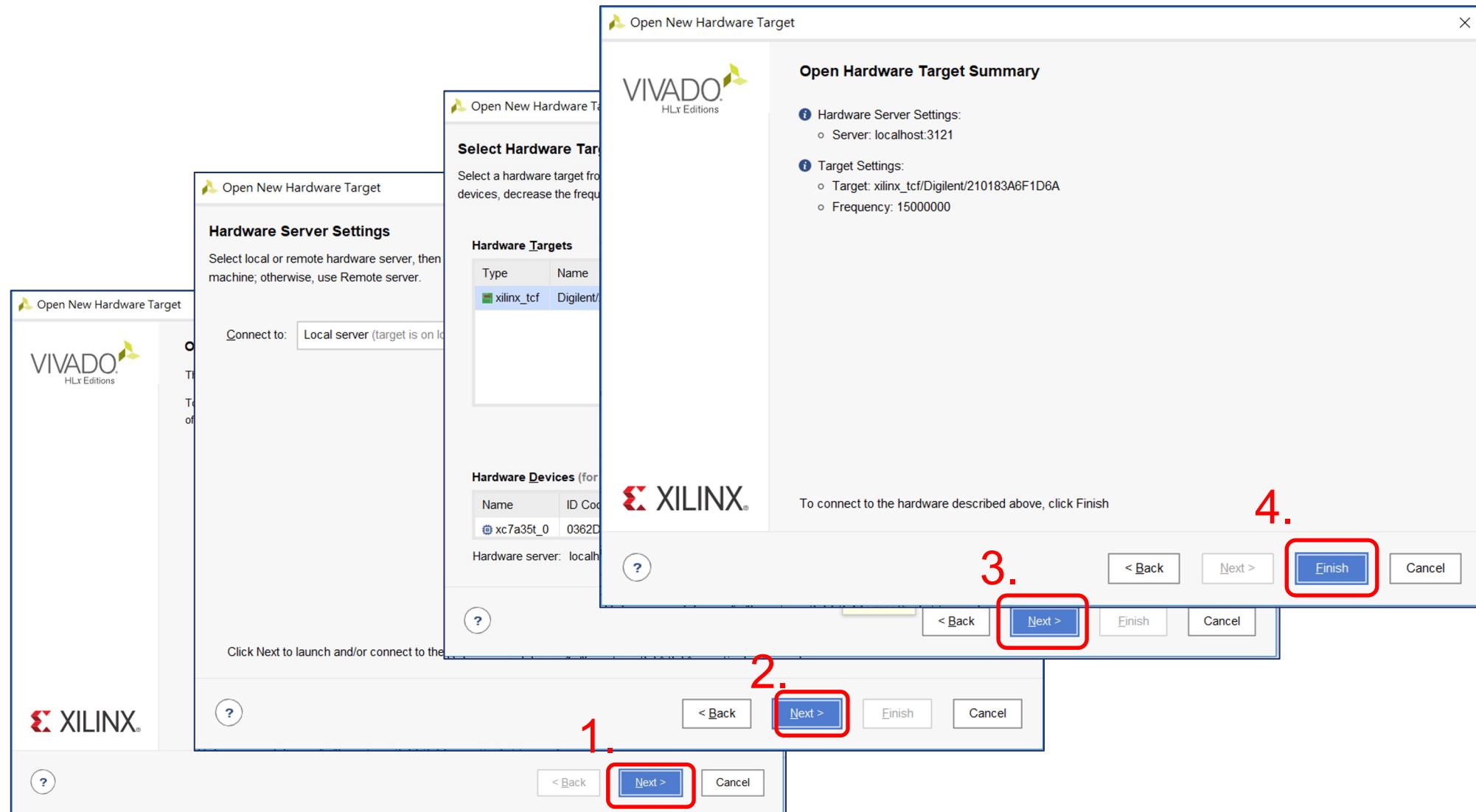
Open Target and Auto Connect (1/2)

Use "Auto Connect" which is simpler.





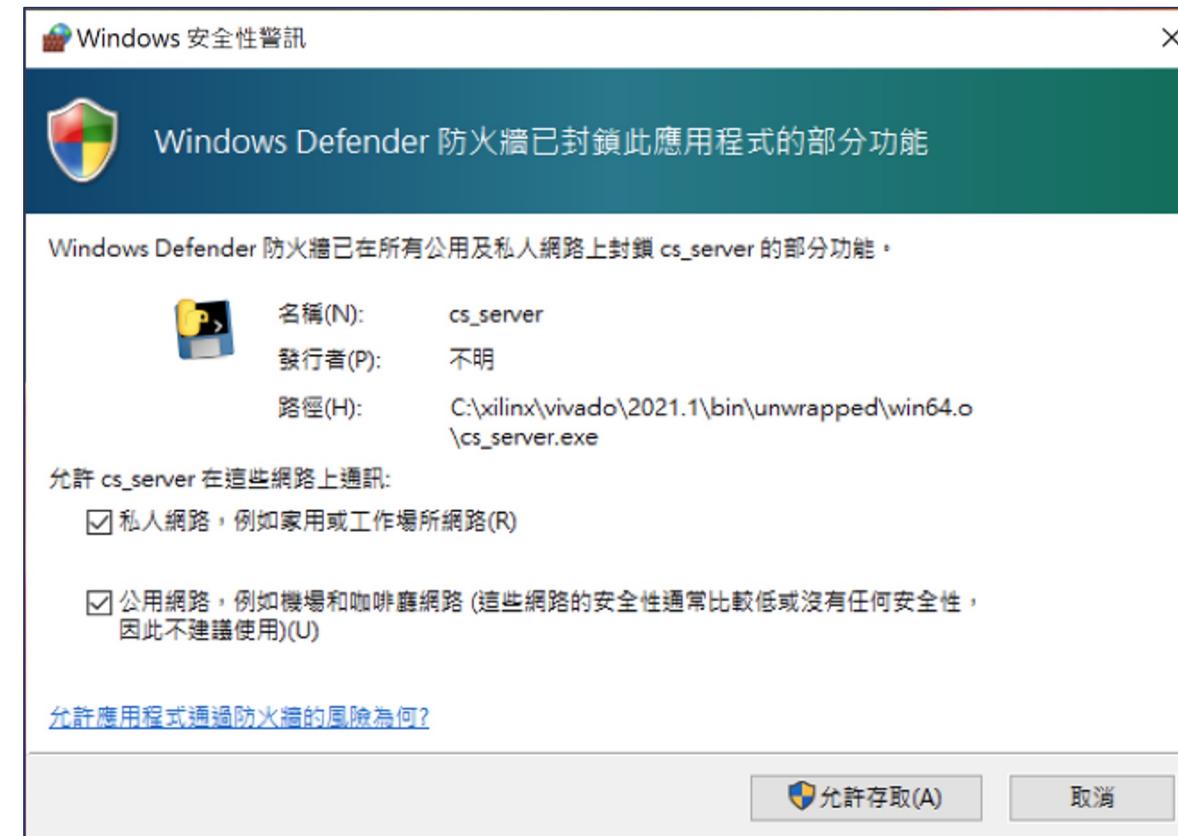
Open Target and Auto Connect (2/2)





Firewall Setting

- 允许存取 for `cs_server.exe` when connecting FPGA board





If FPGA Board Cannot be Connected...(1/2)

(裝置管理員)

- Check the **Device Manager** under the Control Panel of Windows
 - There should be a **Digilent USB Device** when you plug in the FPGA board



List of correct drivers





If FPGA Board Cannot be Connected...(2/2)

- ◆ If the list of drivers does not match the picture on the previous slide, **uninstall** them and **plug in the board again**, to automatically **reinstall** the correct driver.



- If still not working, reinstall the driver manually

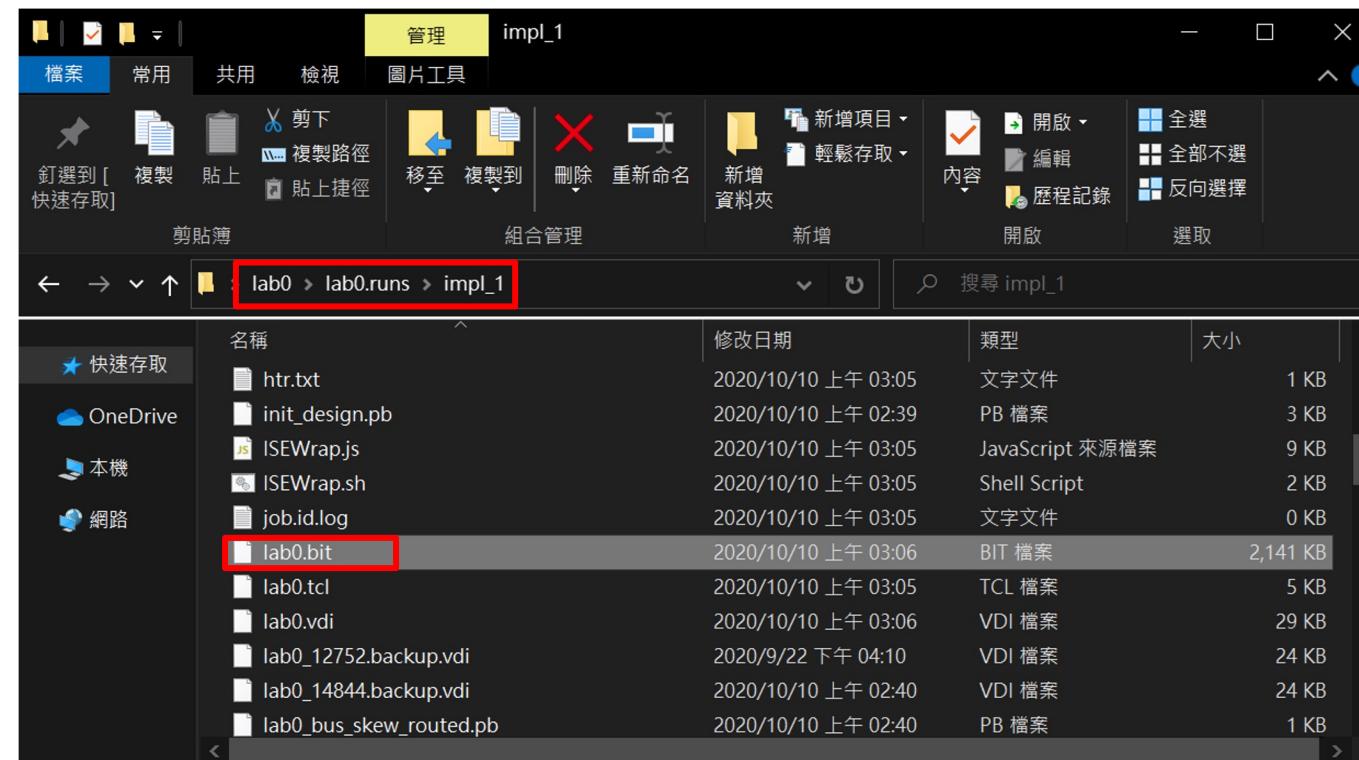
- ◆ Execute the command as administrator:

```
Xilinx\Vivado\2019.2\data\xicom\cable_drivers\nt64\install_drivers.cmd
```



If FPGA Board Still Cannot be Connected...(1/2)

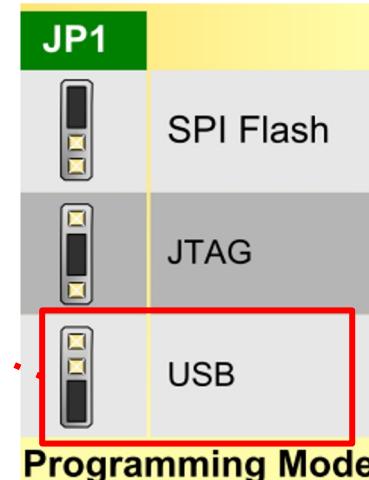
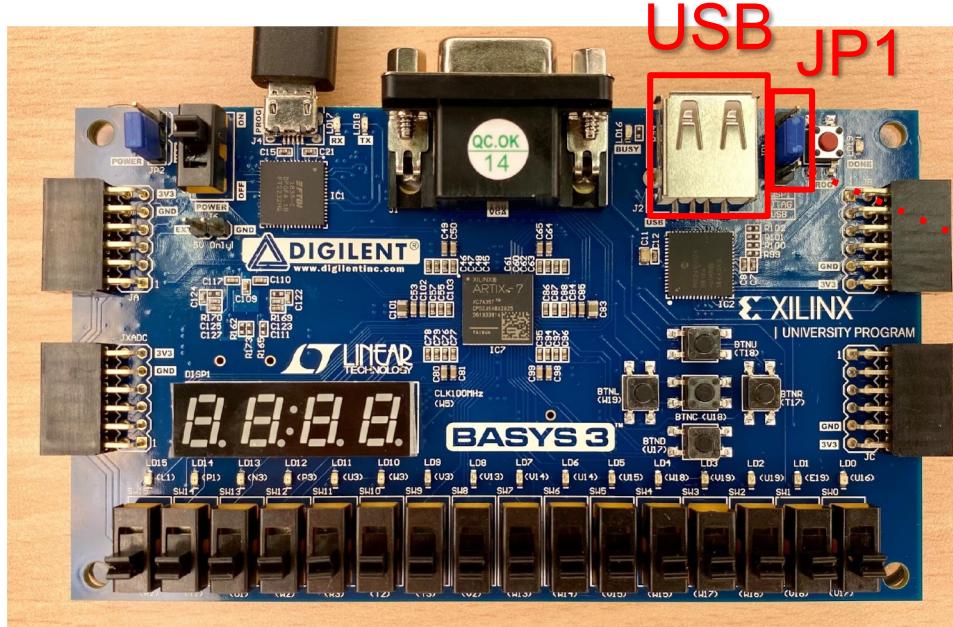
- Store the bitstream file **[top module name].bit** to the **USB drive**
 - ◆ Located in subfolder “[project name]\[project name].runs\impl_1”
 - ◆ Copy the bitstream file to the external USB drive





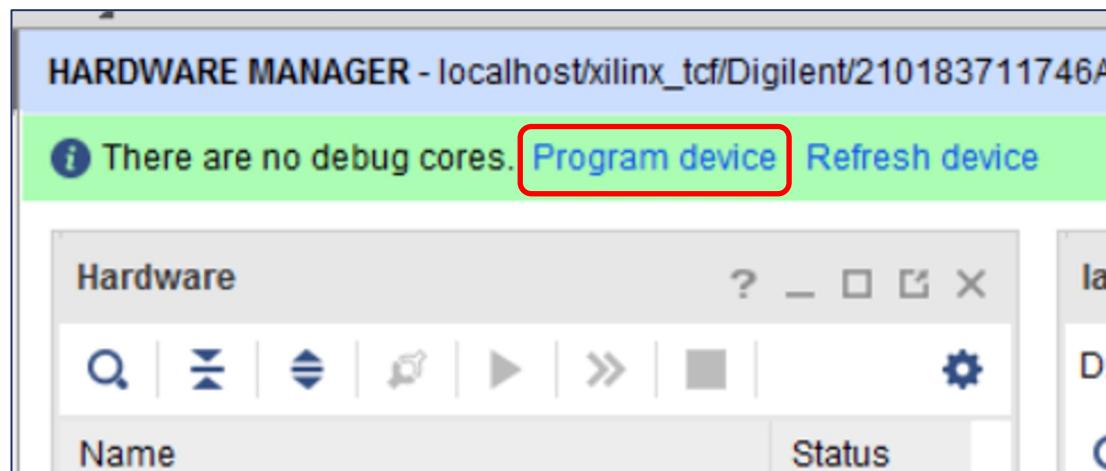
If FPGA Board Still Cannot be Connected...(2/2)

- Switch the jumper **JP1** to **USB** programming mode
- Plug the USB drive into the **USB connector** on the FPGA board
- Power on and wait for the programming
 - ◆ Skip the following two slides and jump to page 47

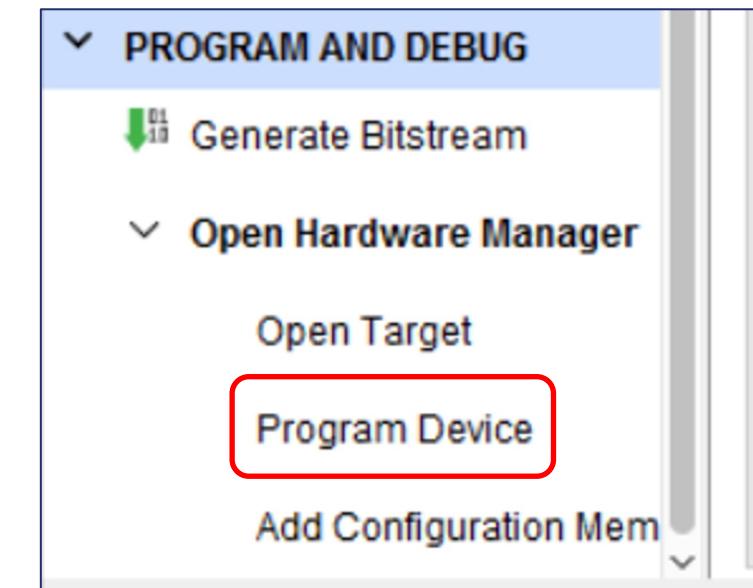




Program Device (1/3)

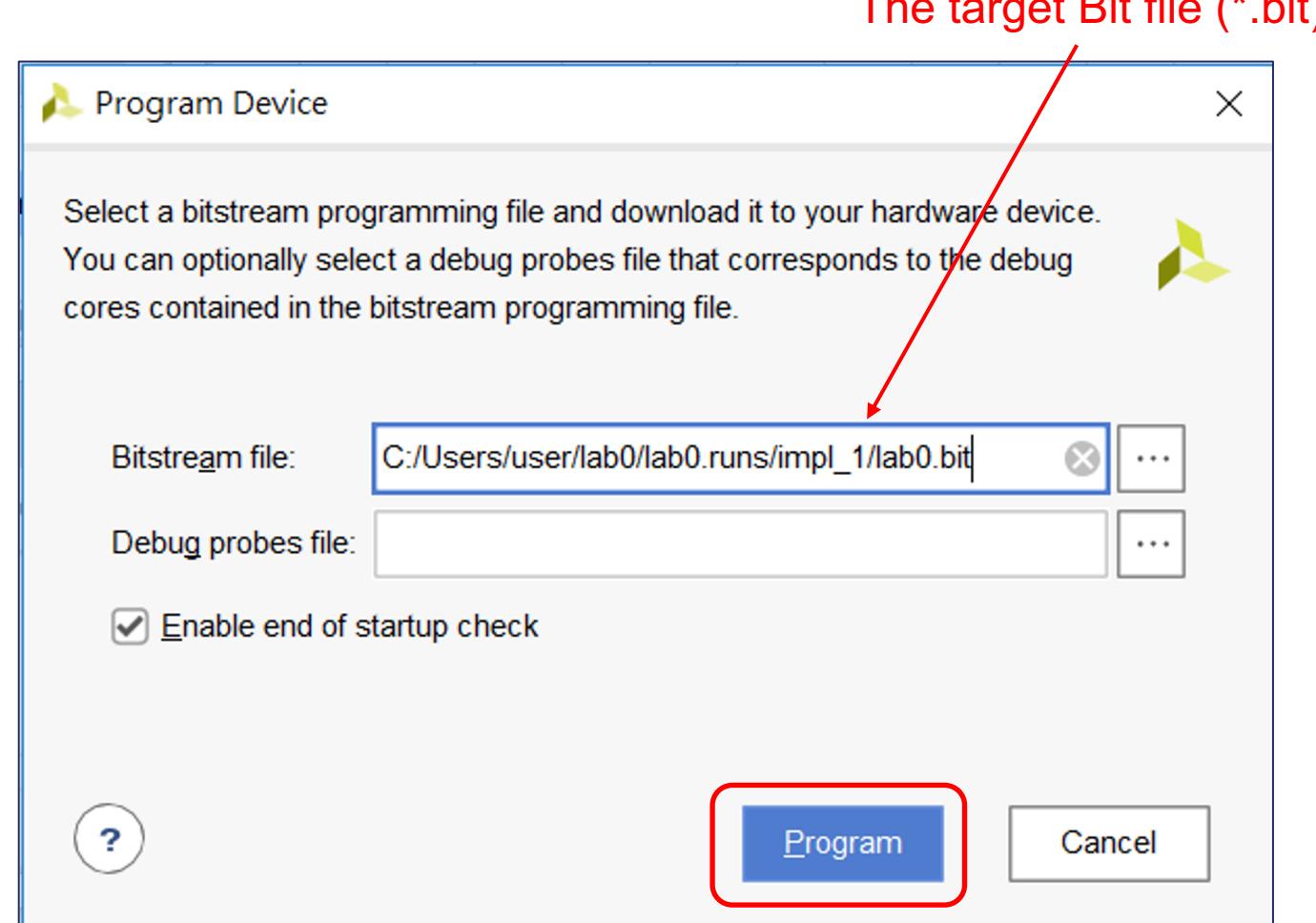


Or





Program Device (2/3)

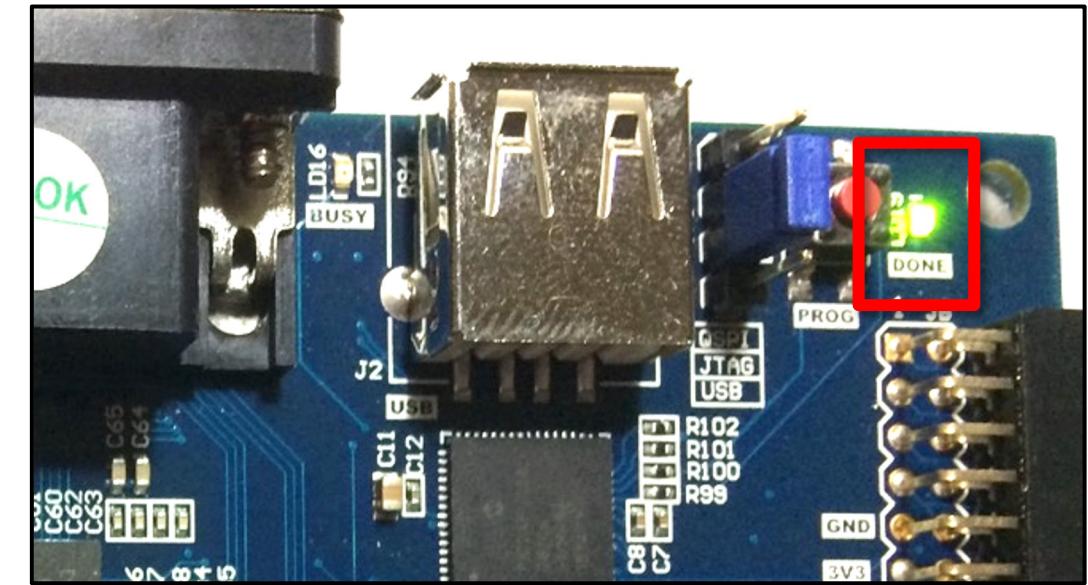
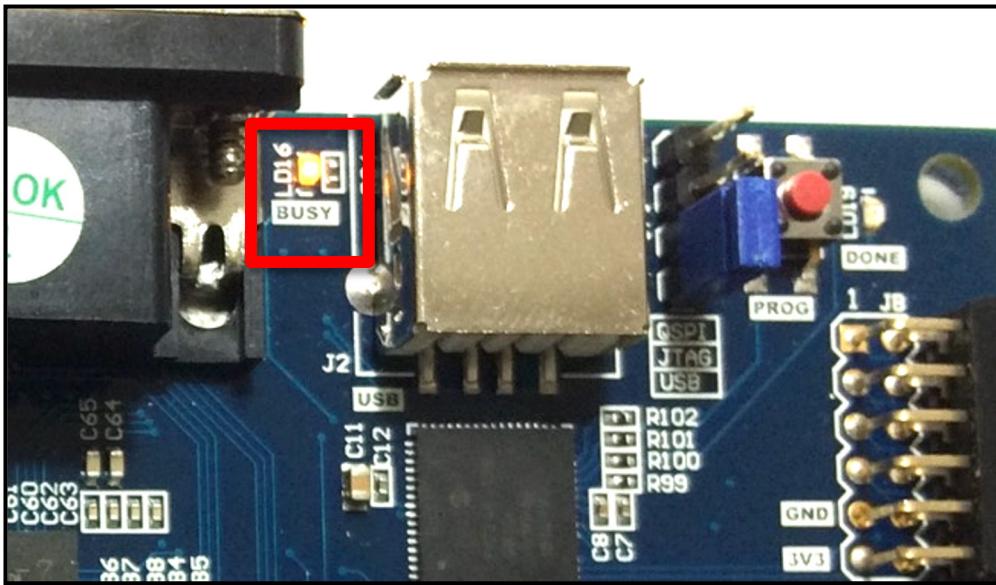




Program Device (3/3)

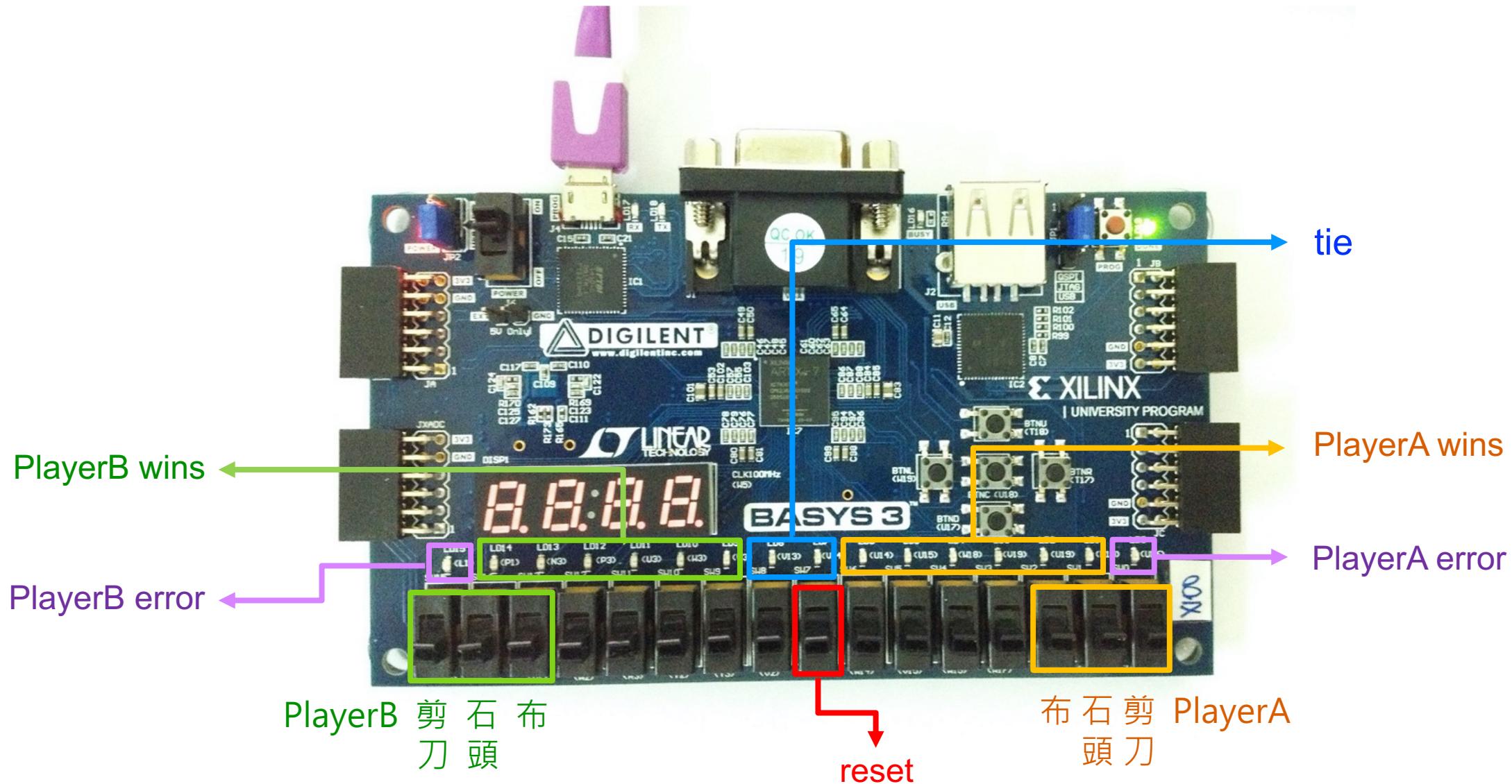
- Wait for programming done

BUSY (yellow) → **DONE (green)**





Rock-Paper-Scissors Game Demo



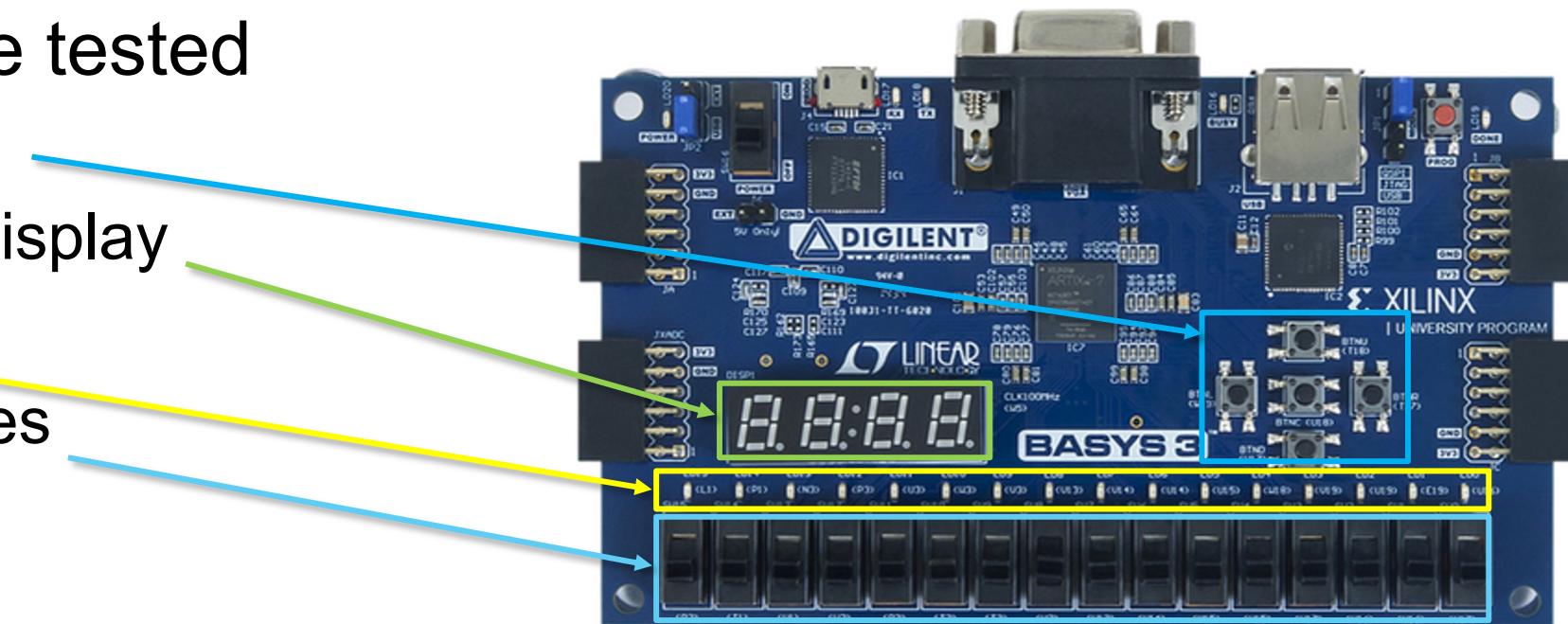


Test-Your-Own-FPGA Demo

- Bit file test.bit is provided for you to test the Basys 3 FPGA board

- The IOs to be tested

- ◆ Pushbuttons
- ◆ 7-segment display
- ◆ LEDs
- ◆ Slide switches



- Program FPGA device with the bit file: see pages 45-47



How to Test

- Or refer to the demo clip:

<https://drive.google.com/file/d/1H9oaKr-OAQiZvuG260TASVvABEnsrcof/view?usp=sharing>

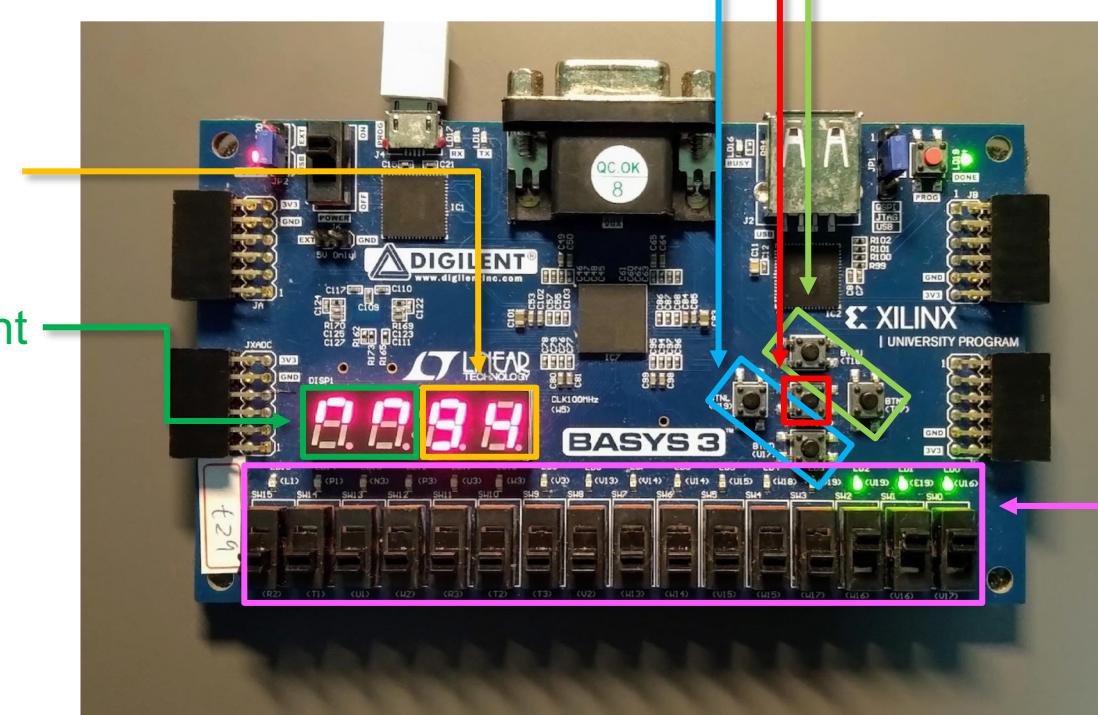
The right two digits of 7-segment display show the counting value between 0 to 99.

The left two digits of 7-segment display indicate the counting direction.

Counting up:



Counting down:



btnC (button C) resets the counter to 0 and its direction to up.

btnU and btnR change the counter's direction to up.

btnD and btnL change the counter's direction to down.

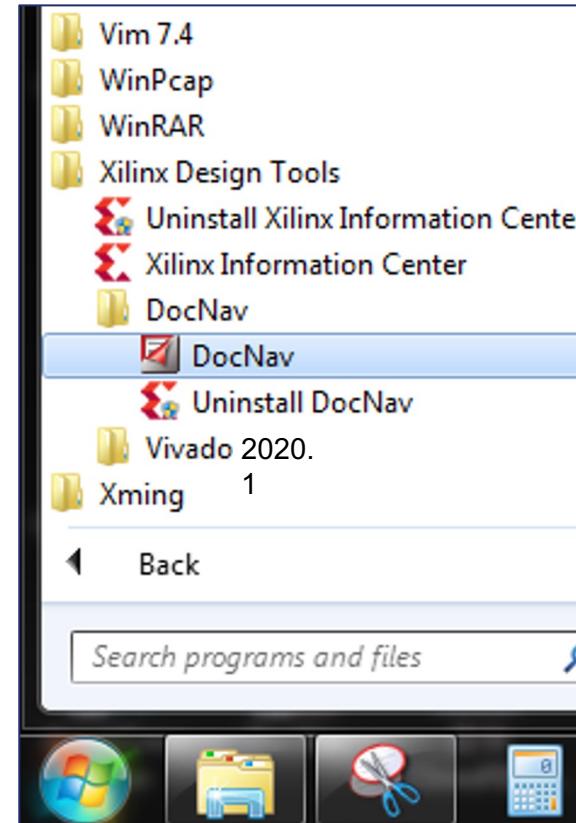
LEDs will turn on when you switch up the corresponding slide switch.



References

- All in DocNav

- ◆ E.g., ug937-vivado-design-suite-simulation-tutorial.pdf





Basys 3 FPGA Board Reference Manual

- PDF version: basys3_rm.pdf

- Web URL:

<https://reference.digilentinc.com/programmable-logic/basys-3/reference-manual>