University of Nevada, Reno

CPE 301-1001 - EMBEDDED SYSTEMS DESIGN
Fall 2019

HOMEWORK No. 03 - DUE before 11:59 PM, September, 18

Description of Purpose

The purpose of this assignment is to teach us how chips work and how to calculate decoder address lines. In addition, we are taught how to calculate address space with the given space of the chip. Overall, this assignment is designed to expand our knowledge on how memory works and how our computer does its calculations.

REMINDER: If you hand in the HW with your statement of purpose on time you will receive full credit for the entire assignment (no matter if right or wrong). The reason for homework is to provide guidance for you while you are studying and learning the course material. Thus, what is really important is that you learn the course material, not that you hand-in perfect homework.

You will submit a pdf file but, there will be no requirement as to format. You may do the HW in pencil, by hand, and scan in the results. You may submit it in any form that is legible in the pdf file. For each HW assignment you must write one or two sentences explaining your understanding of what material (or process) you are trying to learn by answering the question(s). This is the "statement of purpose".

1. The memory units that follow are specified by the number of words times the number of bits per word. How many address lines and input/output data lines are needed in each case?

   (a) 8K X 16 (b) 2G X 8 (c) 16M X 32 (d) 256K X 64

2. Give the number of bytes stored in each memory unit in question 1.

3. Word number 563 decimal in the memory shown in Fig. 7.3 (see Mano-Ch7.pdf) contains the binary equivalent of 1,212 decimal. List the 10-bit address and the 16-bit memory content of the word in binary and hexadecimal.

4. Show the memory cycle timing waveforms for the write and read operations. Assume a CPU clock of 150 MHz and a memory cycle time of 20 ns similar to that shown in Fig. 7.4 (see Mano-Ch7.pdf).

5. Enclose the 4 X 4 RAM of Fig. 7.6 (see Mano-Ch7.pdf) in a block diagram showing all inputs and outputs. Assuming three-state outputs, construct an 8 x 8 memory using four 4 x 4 RAM units.

6. A microprocessor uses RAM chips of 1024 X 1 capacity.
   (a) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?
   (b) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.

7. (a) How many 32K X 8 RAM chips are needed to provide a memory capacity of 256K bytes?
   (b) How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?

(c) Using absolute decoding, how many lines must be decoded for the chip select inputs? Specify the size of the decoder.

8. (a) How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
   (b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?
   (c) How many lines must be decoded for chip select? Specify the size of the decoders.

9. One of the first minicomputers, the PDP-8, had a l2-bit address bus. What was the last address in this computer's memory space? Give the answer in decimal, binary, octal, and hexadecimal.

10. Draw a memory map of a system with a 12-bit address bus, dividing the memory space into 2K blocks. Indicate the hexadecimal address of the first and last address in each block.

11. The 68000 microprocessor has a 24-bit address bus. Into how many 64K blocks can the 68000's memory space be divided?

12. What are the first and last addresses of the 1 Meg block of memory at the top of the 68000's address space?

13. If a 64K(memory space is divided into 8K blocks, what are the beginning and ending addresses of block #3?(Remember, the block starting at address 0 is block #0.)

14. A certain computer has a 4Meg address space. How many bits wide is this computer's address bus?

15. A popular microcontroller is the MCS-51 from Intel Corp. Two versions are the 8751 with an on-chip EPROM and the 8051 with an on-chip mask-programmed ROM. Assume the 8751 sells for $30 in any quantity and the 8051 sells for $3 plus a $10,000 setup fee. (a) How many units are necessary to justify use of an 8051 device?
   (b) What is the savings for projected sales of 3,000 units of the final product if an 805I is used instead of an 8751?

Questions have been adapted from (CPE 201 text) "Digital Design", by Morris Mano and Michael Ciletti, from " Digital Logic and Computer Design ", by Morris Mano, and from “The 68000 Microprocessor” by Scott MacKenzie.