Student ID: b09901142

Name: 呂睿超

RTL Report

Testbench	Pass (Pass/Fail)
Clock Cycle	10.0 (ns)
Total Time	11420 (ns)

Synthesis Report

Testbench	Pass(Pass/Fail)
Clock Cycle	10.0 (ns)
Cell Area	37487.079181 (Please report **Total cell area**)
Total Time	11420.00 (ns)
Area*Time	

APR Report

Testbench	Pass(Pass/Fail)
Clock Cycle	10.0 (ns)
Cell Area	46861.819 (Please report **Total area of Core)**
Total Time	11420.00 (ns)
Area*Time	

How to report area in Innovus?

➔ File > Report > Summary > choose Text only, file name: **summaryReport.rpt**>OK, find **Total area of Core.**

Synthesis No latch

```
Inferred memory devices in process
        in routine IOTDF line 20 in file
                '/home/raid7_2/userb09/b09142/ICD2024/ICD_HW3/02_SYN/IOTDF_syn.v'.
===============================================================================
|     Register Name     |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       busy_reg        | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|       valid_reg       | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
| received_segments_reg | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|    data_buffer_reg    | Flip-flop |  128  |  Y  | N  | Y  | N  | N  | N  | N  |
|      iot_out_reg      | Flip-flop |  128  |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb09/b09142/ICD2024/ICD_HW3/02_SYN/IOTDF.d
Loaded 1 design.
Current design is 'IOTDF'.
```

APR NanoRoute Innovus Result (截圖)