Integrated Circuit Design

Homework #5

Due: 2024/05/21 14:20 (no late submission)

Please follow the steps shown in 20240507_tutorial_icfb.pdf to:

1. Draw the layout of a Gray Cell ($G_{2:1}=G_2+P_2*G_1$) using one INV and two NAND2 gates and run the DRC.
2. Draw its corresponding schematic view and perform LVS. (Use the sizes obtained from the Layout view.)
3. Accomplish PEX and generate the spice file considering the parasitic delay.
4. Run Hspice to check the function of the Gray Cell.

Hint：

G_2	P_2	G_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1

You are asked to:

1. Use the ruler tool to measure and give the area of your layout in the report.
2. Print screens of your results (for report.doc).
3. Convert your report.doc into a PDF file with a filename report_[student_ID].pdf.
4. Provide the PEX spice files (naming rule: gray_[student_ID].pex.sp, gray_[student_ID].pex.sp.pex, gray_[student_ID].pex.sp.GRAY.pxi)
5. Provide the Hspice file. (naming rule: gray_hspice_[student_ID].sp)
6. Include the GDS file of your layout. (naming rule: gray_layout_[student_ID].gds)
7. Put the files in Step 3~6 in a folder named HW5 _[student_ID] and have it compressed into a zip file HW5 _[student_ID].zip

[penalty of wrong formats: - 10 points]

Make sure that all the results are correct.

Note that the area of your DRC-clean layout will affect the final score of your homework, too. (The smaller, the better.)

Basic score (correct simulation) 85 points

Ranking score (out of all ICD students):

Ranking	Points
Top 5	+15
6~10	+12
11~20	+9
21~30	+6
31~40	+3
41~	+0

Example of submission:

HW5_bxxxxxxxx.zip

HW5_bxxxxxxxx

|--- report_bxxxxxxxx.pdf

|--- gray_bxxxxxxxx.pex.sp

|--- gray_bxxxxxxxx.pex.sp.pex

|--- gray_bxxxxxxxx.pex.sp.GRAY.pxi

|--- gray_hspice_bxxxxxxxx.sp

|--- gray_layout_bxxxxxxxx.gds