

Synthesis Report

Testbench	Pass (Pass/Failed)
Clock Cycle	10.0 (ns)
Cell Area	37487.079181 (Please report Total cell area)
Total Time	11420.00 ns (ns)
Area*Time	

Synthesis No-latch (screenshot)

```
Inferred memory devices in process
  in routine IOTDF line 20 in file
    '/home/raid7_2/userb09/b09142/ICD2024/ICD_HW3/02_SYN/IOTDF_syn.v'
=====
| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |
=====
| busy_reg      | Flip-flop | 1 | N | N | Y | N | N | N | N |
| valid_reg     | Flip-flop | 1 | N | N | Y | N | N | N | N |
| received_segments_reg | Flip-flop | 5 | Y | N | Y | N | N | N | N |
| data_buffer_reg | Flip-flop | 128 | Y | N | Y | N | N | N | N |
| iot_out_reg    | Flip-flop | 128 | Y | N | Y | N | N | N | N |
=====
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb09/b09142/ICD2024/ICD_HW3/02_SYN/IOTDF'.
Loaded 1 design.
Current design is 'IOTDF'.
```

Synthesis slack (screenshot)

```
clock clk (rise edge)          10.00      10.00
clock network delay (ideal)     1.00      11.00
clock uncertainty                -0.10      10.90
iot_out_reg[10]/CK (DFFRXL)     0.00      10.90 r
library setup time              -0.14      10.76
data required time               10.76
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data required time               10.76
data arrival time               -10.73
-----
slack (MET)                      0.03
```