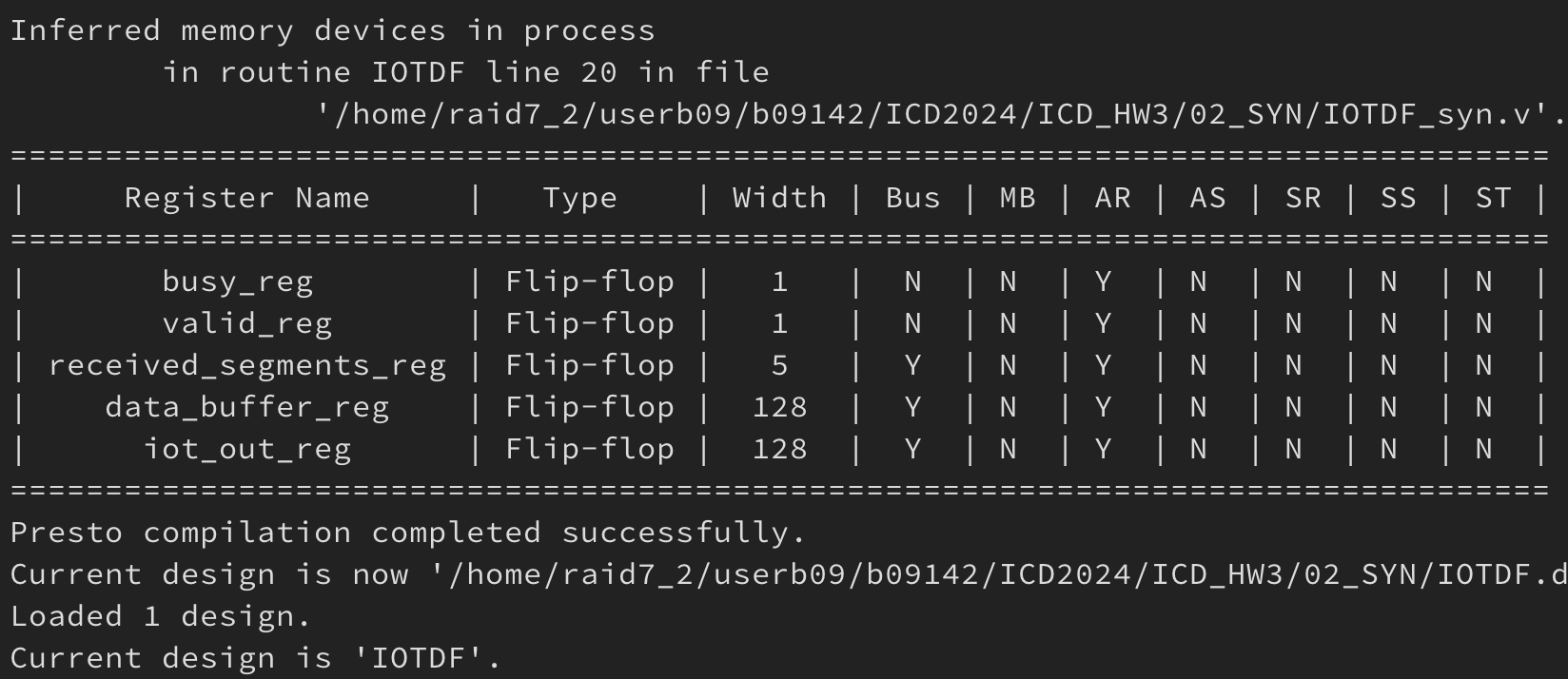
**Synthesis Report**

|  |  |
| --- | --- |
| Testbench | Pass (Pass/Failed) |
| Clock Cycle | 10.0 (ns) |
| Cell Area | 37487.079181 (Please report **Total cell area**) |
| Total Time | 11420.00 ns (ns) |
| Area\*Time |  |

**Synthesis No-latch (screenshot)**



**Synthesis slack (screenshot)**

