Datasheet

MM32SPIN2x

32-Bit Microcontroller based on Arm® Cortex®-M0

Version: 1.21_p

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1 General Introduction

General Introduction

1.1 Introduction

This product incorporates a high performance 32-bit microcontroller with the core of Arm® Cortex®-M0. The highest operating frequency is up to 96MHz, with built-in high-speed memory, a rich set of enhanced I/O ports and peripherals connected to the external bus. This product contains two 12-bit ADCs, five comparators, four operational amplifiers, one 16-bit general-purpose timer, one 32-bit general-purpose timer, three 16-bit basic timers, two 16-bit advanced timers, and standard communication interfaces device: one I2C, two SPI, and two UART interfaces.

The device works between 2.0V to 5.5V range. The regular temperature for the device is -40°C to +85°C and -40°C to +105°C extended temperature range are also available. A comprehensive set of power-saving mode allows the design of low-power applications.

The devices are available in 7 different packages: LQFP64, LQFP48, QFN48, LQFP44, LQFP32,QFN28 and TSSOP20.

The abundant peripherals make this microcontroller suitable for a variety of applications:

- Motor drive and application control
- Healthcare and fitness equipment
- PC gaming peripherals and GPS platform
- Industrial applications: programmable controllers (PLCs), inverters, printers and scanners
- Alarm system, video intercom, heating, ventilation and air conditioning

1.2 Product Characteristics

- Core and system
  - 32-bit Arm® Cortex®-M0 processor as the core
  - Maximum operating frequency is up to 96MHz
  - Single cycle 32-bit hardware multiplier
  - Hardware divider (32bit)
  - Hardware prescribing (32bit)
- Memory
  - 128K bytes of Flash memory
  - 12K bytes of SRAM

  - Boot loader support Chip Flash and ISP (In-System Programming)
- Clock, reset and power management
  - 2.0V to 5.5V application supply
  - Power-on/Power-down reset (POR/PDR), Programmable voltage detector (PVD)
  - External 2 ~ 24MHz high speed crystal oscillator
  - Embedded factory-tuned 48MHz high speed oscillator
- Low-power
  - Sleep, Stop and Standby modes
- Two 12-bit ADCs and 1μS of conversion time (up to 16 channels)
  - Conversion range: 0 to V_{DDA}
  - Support sampling time and resolution configuration
  - On-chip temperature sensor
  - On-chip voltage sensor
- Five comparators
- Four operational amplifiers
- One 5-channel DMA controller
  - Supported peripherals: Timer, UART, I2C, SPI and ADC
- Up to 56 fast I/Os:
  - All I/O ports can be mapped to 16 external interrupts
  - All ports are capable of inputting and outputting 5V signals

Annotation: V_{DD}=5V

- Debug mode
  - Serial wire debug (SWD)
- Ten timers
  - Two 16-bit 4-channel advanced control timer providing 4-channel PWM output, with dead time generation and emergency stop functions
  - One 16-bit timer and one 32-bit timer providing up to 4 input captures/output compares, usable for IR control decoding
  - Two 16-bit timers providing one input capture/output compare and one OCN with functions of dead zone generation, emergency stop and modulator gate circuit for IR control
  - One 16-bit timer providing one input capture/output compare
  - Two watchdog timers (independent and window type)
  - One SysTick timer: 24bit downcounter
- Up to 5 communication interfaces
  - Two UART interfaces
  - One I2C interface
  - Two SPI interfaces
- 96-bit unique ID (UID)
- Packages LQFP64, LQFP48,QFN48, LQFP44, LQFP32, QFN28 and TSSOP20

For more information about the complete product, refer to Section 2.2 of the data sheet. The relevant information about the Cortex®-M0, please refer to Cortex®-M0 technical reference manual.

2 Specification

Specification

2.1 Device contrast

Table 1. Device features and peripheral configurations: M32SPIN27x

Peripheral \ Device		MM32SPIN27PS	MM32SPIN27PF	MM32SPIN27NF	MM32SPIN27PQ	MM32SPIN27PT	MM32SPIN27NU	MM32SPIN27TW
Flash memory-K bytes		128						
SRAM-K bytes		12						
OPA		4			3	2	1	1
Timers	General-purpose (16 bit)	4	4	4	4	4	4	4
	General-purpose (32 bit)	1	1	1	1	1	1	1
	Advanced	2	2	2	2	2	2	2
Communication interfaces	UART	2	2	2	2	2	2	2
	I2C	1	1	1	1	1	1	1
	SPI	2	2	2	2	1	1	1
GPIOs		56	40	40	36	25	25	15
12-bit ADC	Number	2	2	2	2	2	2	2
	Channel	16	16	16	14	11	11	10
DIV		1						
Comparator		5			4	2	2	2
CPU frequency		96 MHz						
Operating voltage		2.0V ~ 5.5V						
Package		LQFP64	LQFP48	QFN48	LQFP44	LQFP32	QFN28	TSSOP20

Table 2. Device features and peripheral configurations: MM32SPIN25x

Peripheral \ Device	MM32SPIN25PF	MM32SPIN25NF	MM32SPIN25PT	MM32SPIN25TW
Flash memory-K bytes	32			
SRAM-K bytes	8			
OPA	4	4	2	1

Peripheral \ Device		MM32SPIN25PF	MM32SPIN25NF	MM32SPIN25PT	MM32SPIN25TW
Timers	General-purpose (16 bit)	4	4	4	4
	General-purpose (32 bit)	1	1	1	1
	Advanced	2	2	2	2
Communication interfaces	UART	2	2	2	2
	I2C	1	1	1	1
	SPI	2	2	1	1
GPIOs		40	40	25	15
12-bit ADC	Number	2	2	2	2
	Channel	16	16	11	10
DIV		1			
Comparator		5		2	
CPU frequency		96 MHz			
Operating voltage		2.0V ~ 5.5V			
Package		LQFP48	QFN48	LQFP32	TSSOP20

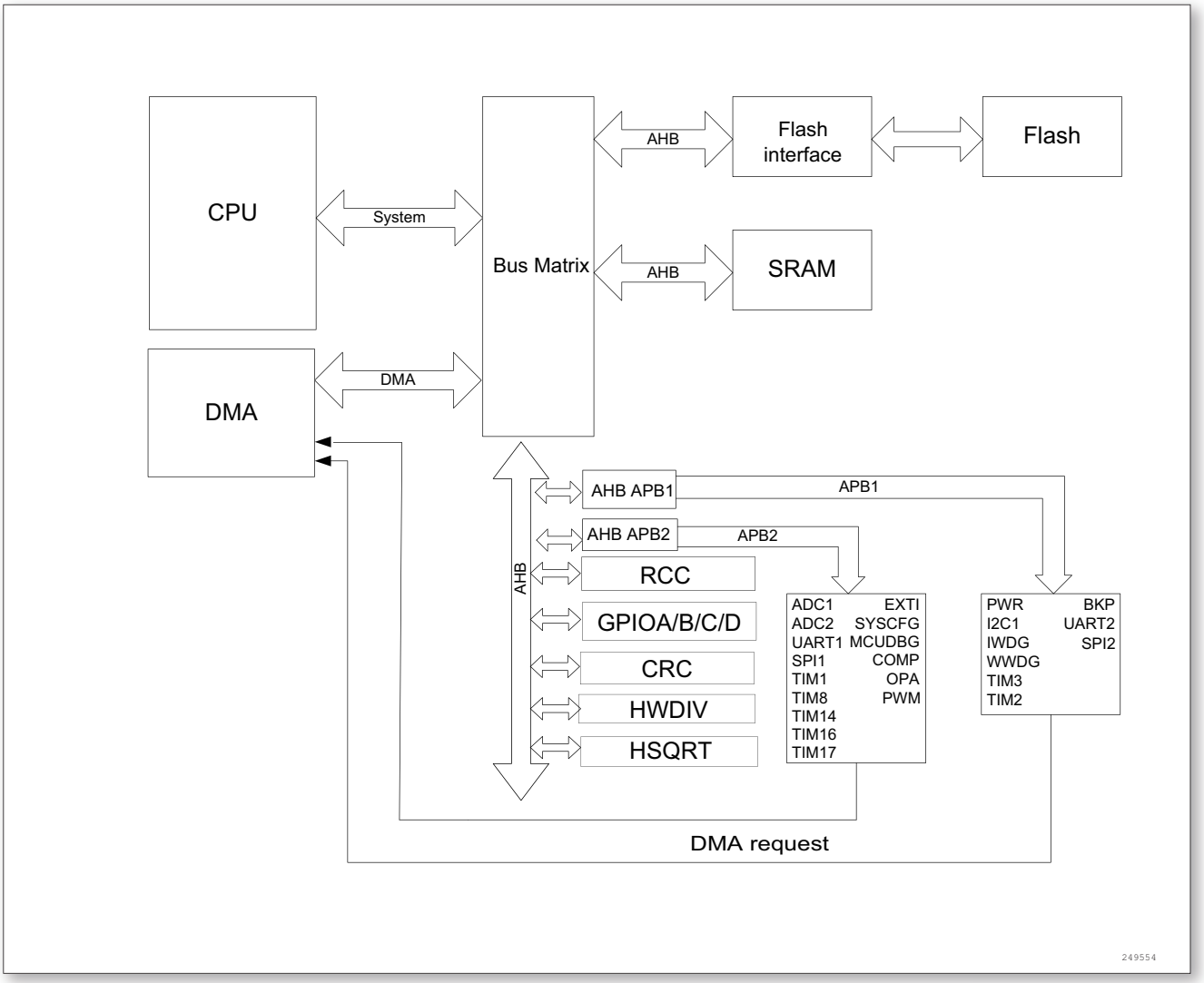

Figure 1. Block diagram

2.2 Summary

2.2.1 Arm® Cortex®-M0 core with embedded flash memory and SRAM

The ARM® Cortex®-M0 processor is configurable and has multilevel pipeline 32-bit reduced instruction set processor, and characterized by high performance and low power consumption.

2.2.2 Embedded flash memory

The embedded flash memory is up to 128K bytes, usable for storing programs and data.

2.2.3 SRAM

The embedded SRAM is up to 12K bytes

2.2.4 Nested vectored interrupt controller (NVIC)

This product embeds a nested vectored interrupt controller, which can handle multiple maskable interrupting channels (excluding 16 Cortex™-M0 interrupt lines) with 16 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry address directly enters into the core
- Tightly coupled NVIC interfaces
- Allows early processing of interrupts
- Handles higher-priority interrupts that arrive late
- Supports tail-chaining of interrupts
- Automatically saves the processor state
- Offers automatic recovery when the interrupt returns with no instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.2.5 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of multiple edge detectors used to generate interrupt/event requests. Each interrupt line can be independently configured to select the trigger event (rising edge, falling edge or both) and can be masked independently. A pending register maintains the status of all interrupt requests. The EXTI can detect a signal with a pulse width shorter than the internal AHB clock period. All GPIOs can be connected to the 16 external interrupt lines.

2.2.6 Clocks and startup

System clock selection is performed on startup, however the internal 48 MHz oscillator with 6 division is selected as default CPU clock on reset. Then an external 2 ~ 24 MHz clock with failure monitoring function can be selected. If an external clock failure is detected, the clock will be isolated. The system automatically switches back to the internal oscillator. If an interrupt is enabled, the software can receive the corresponding interrupt. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example when an indirectly used external oscillator fails).

Multiple prescalers are used to configure AHB frequency, high-speed APB (APB2 and APB1) domain. The maximum frequency of AHB and high-speed APB is 96MHz. Please refer to the clock drive diagram in figure 2.

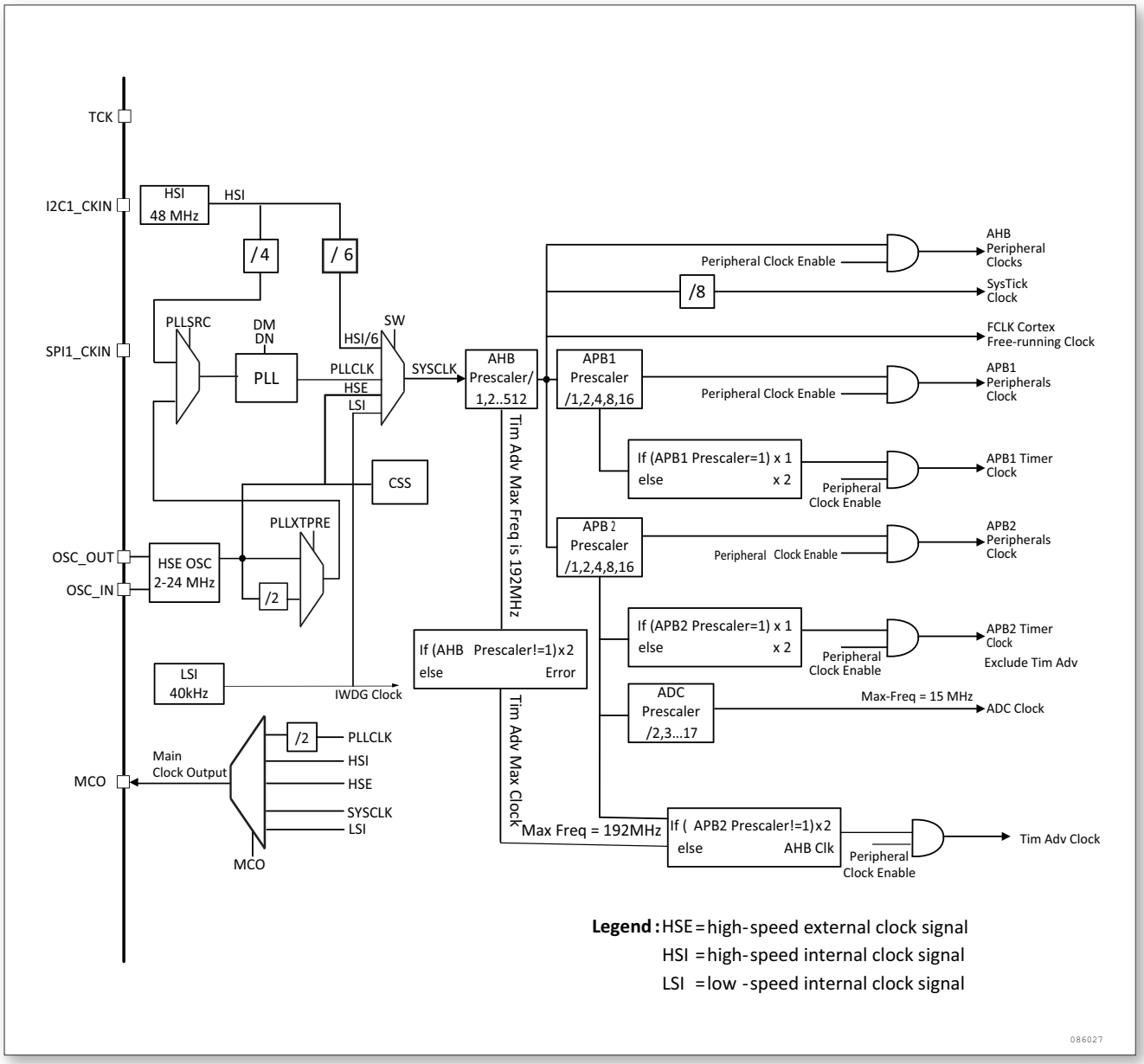

Figure 2. Clock tree

2.2.7 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options：

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using UART1.

2.2.8 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: external power supply for I/Os and the internal regulator through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0V ~ 5.5V: external analog power supply for ADC, reset blocks, oscillators and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.

2.2.9 Power supply monitor

This product has integrated power-on reset (POR)/power-down reset (PDR) circuit. The circuit remains in the working state and ensures proper operation above a threshold of 2.0V. When V_{DD} is below a specified threshold ($V_{POR/PDR}$), the device will be placed in the reset state, without the need for an external reset circuit.

Additionally, the device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, an interrupt can be generated. The interrupt handler will send a warning message or switch the microcontroller to the safe mode. The PVD function should be enabled by a program.

2.2.10 Voltage regulator

The voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.11 Low-power modes

The product supports low-power mode to achieve the best compromise between low power consumption, short startup time and multiple wakeup events.

Table 3. Low power mode list

Mode	Entry	Wakeup	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator
Sleep (SLEEP NOW or SLEEP ON EXIT)	WFI (Wait for Interrupt)	Any interrupt	CPU clock off, no influence on other clock and ADC clock	N/A	On
	WFE (Wait for Event)	Wakeup event			
Stop	PDDS bit SLEEPDEEP bit WFI or WFE	Any arbitrary interrupt (set in the external interrupt register)	All 1.5V area clocks are off	PLL, HSI and HSE oscillator off	On
Standby	PDDS bit SLEEPDEEP bit WFI or WFE	WKUP pin rising edge, NRST pin external reset, IWDG reset			Off

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

The Stop mode minimizes the power consumption while retaining the content of SRAM and registers. The HSI oscillator and HSE crystal oscillator are also shut down in the Stop mode. The microcontroller can be woken up from the Stop mode by any of the EXTI signals. The EXTI signal can be a wakeup signal from one of the 16 external I/O ports and the output of the PVD.

Standby mode

The Standby mode can minimize the power consumption of the system. In the Standby mode, the voltage regulator turns off when the CPU is in the deep sleep mode. The entire 1.5V power supply domain is disconnected. HSI and HSE oscillators are also turned off. They can be woken up by the rising edge of WKUP pin, external reset of NRST pin and IWDG reset. They also can be woken up by the watchdog timer without reset. The contents of SRAM and registers will be lost. Only the backup register and standby circuit provide power.

2.2.12 Direct memory access controller (DMA)

The flexible 5-way universal DMA can manage memory to memory, peripheral to memory and memory to peripheral transfers. The DMA controller supports the management of the ring buffer, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, with support for software trigger on each channel. The length, the source address and the destination address of the transfer can be set separately by the software.

The DMA can be used with major peripherals: UART, I2C, SPI, ADC and general-purpose, basic, advanced control timer TIMx.

2.2.13 Backup register (BKP)

The backup registers are twenty 16-bit registers used to store user application data. They are also not reset when the system is woken up in standby mode, or when the system is reset or power is reset.

2.2.14 Timers and watchdogs

The product includes two advanced timers, two general-purpose timers, three basic timers, two watchdog timers and one SysTick timer.

The following table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/-compare channels	Complem-entary outputs
Advanced control	TIM1 /TIM8	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
Basic	TIM14	16-bit	Up	integer from 1 to 65536	Yes	1	No
	TIM16 / TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	Yes

Advanced-control timer (TIM1 / TIM8)

The advanced-control timer is composed of one 16-bit counter, four capture/compare channels and one three-phase complementary PWM generator. It has complementary PWM output with dead time insertion and can be used as a complete general-purpose timer. Four independent channels can be used for the following:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a 16-bit general-purpose timer, it has the same features as the TIM2 timer. If configured as the 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these output.

Many features are shared with those of the general-purpose timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

Two synchronizable general-purpose timers (TIM2, TIM3) are built into the product. This timer has one 16/32bit auto-load up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and one pulse mode output.

General-purpose timers 32-bit

The timer has one 32-bit auto-reload up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and one-pulse mode output.

General-purpose timers 16-bit

The general-purpose timer has one 16-bit auto-load up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and one pulse mode output.

The general-purpose timers can work together with the advanced control timer via the Timer Link feature for synchronization or event chaining. Their counters can be frozen in the debug mode. Any of the general-purpose timer can be used to produce PWM output. Each timer has independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1～ 4 Hall sensors. Each timer can produce PWM output, or be seen as a simple time reference.

Basic timer

TIM14

This timer contains one 16-bit auto-load upcounter and one 16-bit prescaler. It has one single channel for input capture/output compare, PWM or one pulse mode output. Its counter can be frozen in the debug mode.

TIM16/TIM17

Each timer contains one 16-bit auto-load upcounter and one 16-bit prescaler. They each have one single channel for input capture/output compare, PWM or single pulse mode output. They have complementary output with functions of dead time generation and independent DMA request generation. In the debug mode, the counters can be frozen.

Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter. It is clocked from an independent 40 KHz internal oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the

option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog has one 7-bit downcounter that can be set to run freely. It can be used as a watchdog to reset the entire system in the event of a problem. It is driven by the master clock, providing the early warning of an interrupt. In the debug mode, the counter can be frozen.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.15 Universal asynchronous receiver/transmitter (UART)

The UART interface provides the hardware m anagement of CTS and RTS signals. It also supports LIN master-slave capability and it is compatible with ISO7816 smart card mode. The supported lengths of output data from UART interface can be 5 bits, 6 bits, 7 bits, 8 bits and 9 bits, which are all configurable.

All UART interfaces can be served by the DMA controller.

2.2.16 I2C bus

I2C bus interface can operate in the multi-master mode or slave mode and it supports the standard mode and the fast mode.

The I2C interface supports 7bit or 10bit addressing.

2.2.17 Serial peripheral interface (SPI)

The SPI interface can be configured to 1 ~32 bits per frame in the slave or master mode. The maximum rate is 24M for master mode and 12M for slave mode.

All SPI interfaces can be served by the DMA controller.

2.2.18 General-purpose inputs/outputs (GPIO)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), an input (with or without pull-up/pull-down), or alternate peripheral function. Most GPIO pins are shared with digital or analog alternate peripherals.

If required, the peripheral function of the I/O pins can be locked following a specific sequence in order to avoid spurious writing to the I/O registers.

2.2.19 Analog-to-digital converter (ADC)

The product is embedded with two 12-bit analog-to-digital converters (ADC) which has up to 16 external channels and is available for single-shot, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs.

All ADC can be served by the DMA controller.

The analog watchdog function allows to monitor one or all selected channels precisely. An interrupt will occur when the monitored signal exceeds a preset threshold.

Events generated by general-purpose timers (TIMx) and the advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can synchronize the ADC conversion with the clock.

2.2.20 Hardware division

The hardware division unit consists of four 32-bit data registers, which are dividend, divisor, quotient and remainder, and can be done with signed or unsigned 32-bit division. The hardware division control register USIGN can choose whether to have signed division or unsigned division.

Each time the divisor register is written, the division operation is automatically triggered. After the operation is completed, the result is written to the quotient and remainder registers. If the reader register, remainder register, or status register is read before the end, the read operation is suspended until the end of the operation.

If the divisor is zero, an overflow interrupt flag will be generated.

2.2.21 Hardware square unit

The hardware square unit supports 32-bit root number operations.

2.2.22 PWM controller

The PWM control module controls the PWM waveform output by the advanced timer TIM1 to generate a six-step square wave drive motor. The module supports Auto Phase Mask, Current Compensation and Current Protection.

2.2.23 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel to convert the sensor output to a digital value.

2.2.24 Serial wire debug port (SW-DP)

Two-wire serial debug port (SW-DP) is embedded in the ARM.

An Arm SW-DP allows to be connected to a single-chip microcomputer through serial wire debugging tools.

2.2.25 Comparator (COMP)

Three single-channel comparators and two four-channel comparators are embedded in the product, including:

- Wake-up events from low-power mode triggered by an analog signal
- Adjust the analog signal
- Cycle-by-cycle current control loop when combined with the PWM output from a timer
- Support five independent comparators
- Rail-to-rail comparators
- Each comparator has an optional threshold
  - Reusable I/O pins
  - Internal comparison voltage CRV selects the voltage divider value of AVDD or internal reference voltage
- Programmable hysteresis
- Programmable speed/consumption
- Support filtering function of the comparison results
- Two comparators can be combined and used in one window comparator
- The output terminal can be redirected to an I/O port or multiple timer input terminals to trigger the following events:
  - Capture events
  - OCref_clr events (cycle-by-cycle current control)
  - Brake event to shut off PWM rapidly
- Supports filtering of comparison results
- COMP1 and COMP2 comparators can be combined in a window comparator
- COMP1/2/3 has only one positive input and one inverted input
- COMP4/5 has four positive phase inputs and four inverted inputs with polling:
  - Polling function for constant cycle switching
  - Control polling channel 1/2/3 or 1/2
  - Optional fixed inverted input
- Each comparator generates an interrupt and supports wake-up of the CPU from sleep and shutdown modes (via the EXTI controller)

2.2.26 Operational amplifier

Four op-amps are embedded, and each op-amp input and output is connected to an I/O. The shared I/O allows connection to ADC and comparators.

- Rail-to-rail input/output

- Output is connected to I/O

3 Pin Definition

Pin Definition

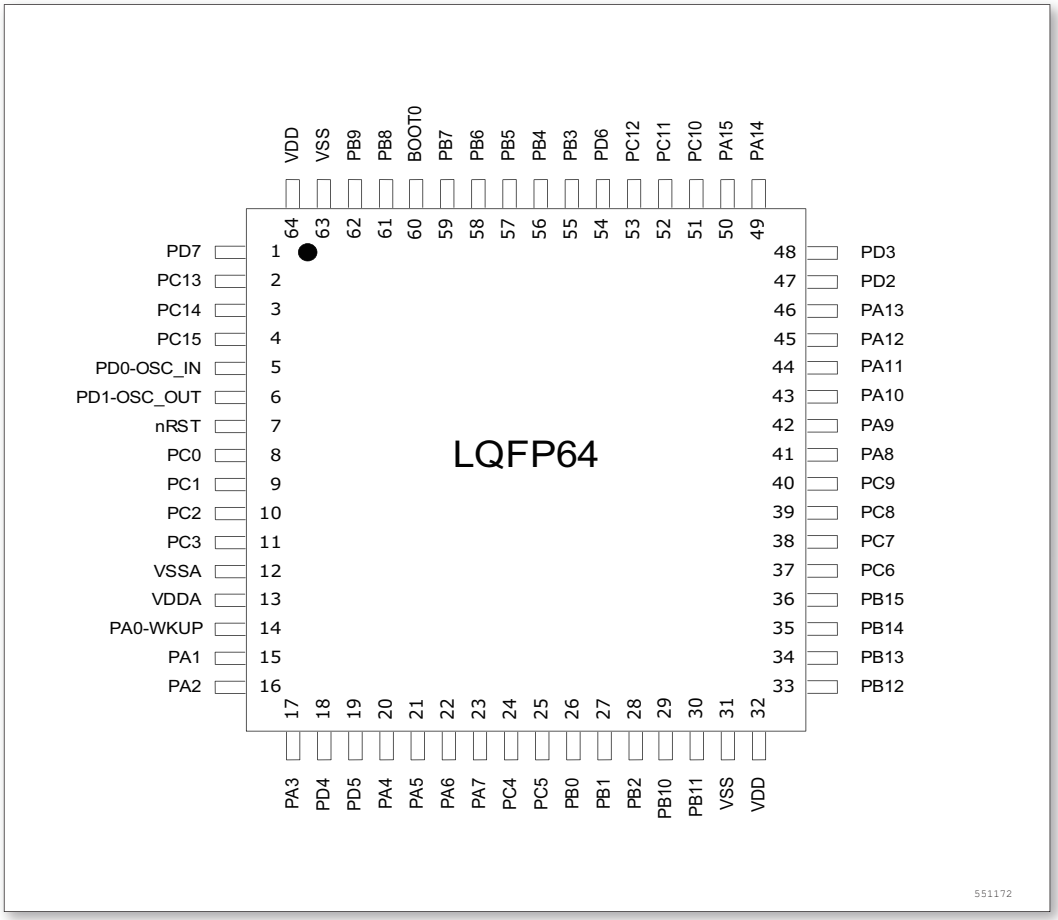

Figure 3. LQFP64 pin assignment

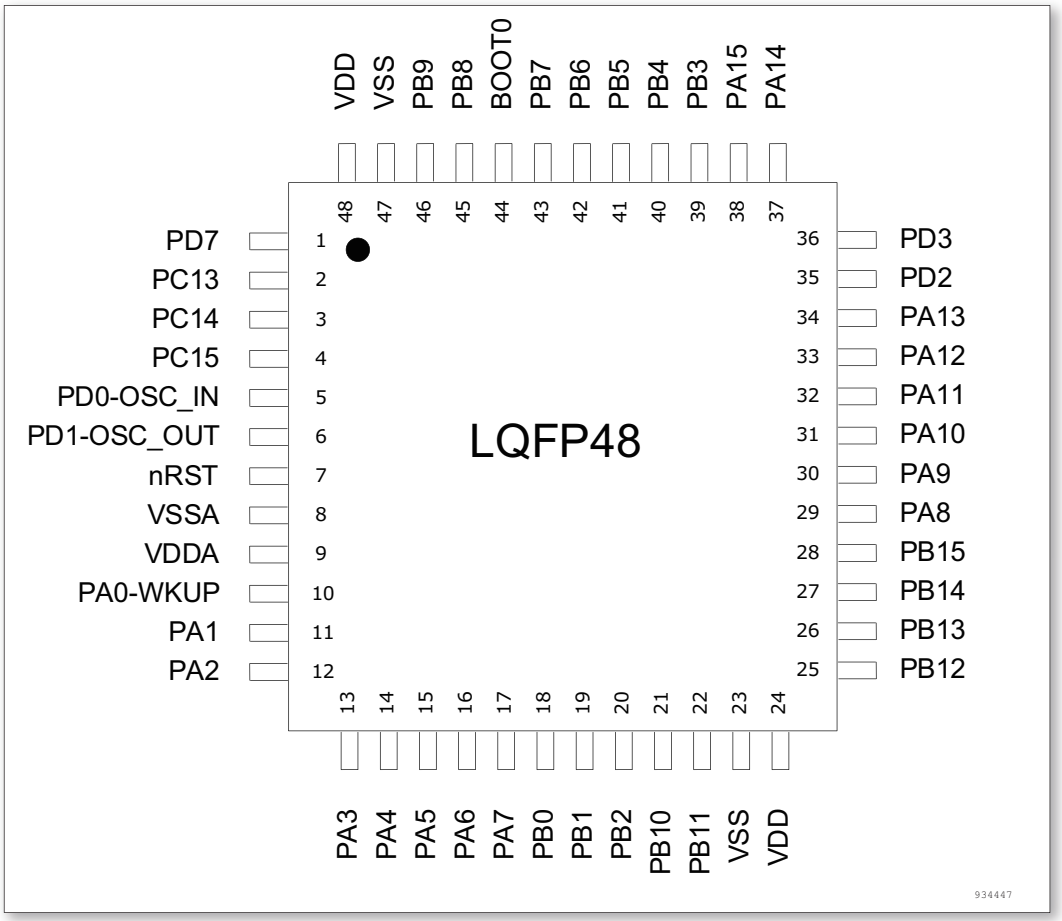

Figure 4. LQFP48 pin assignment

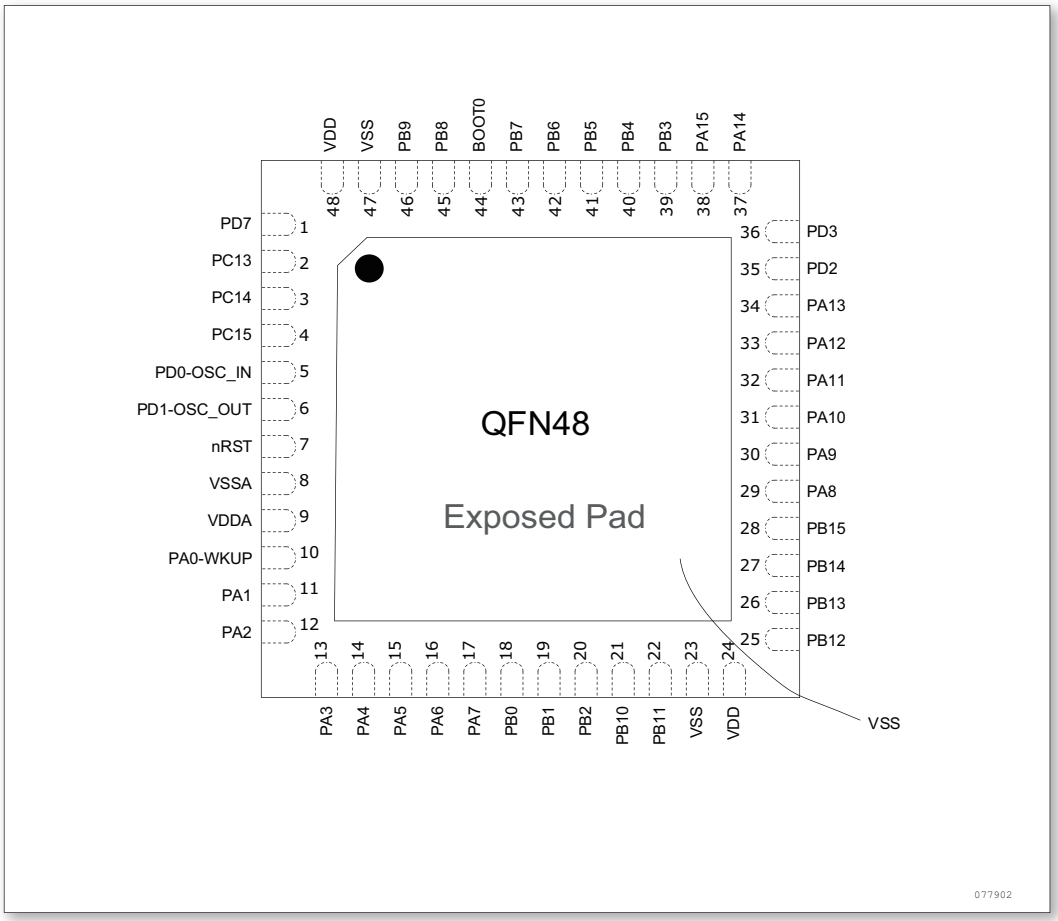

Figure 5. QFN48 pin assignment

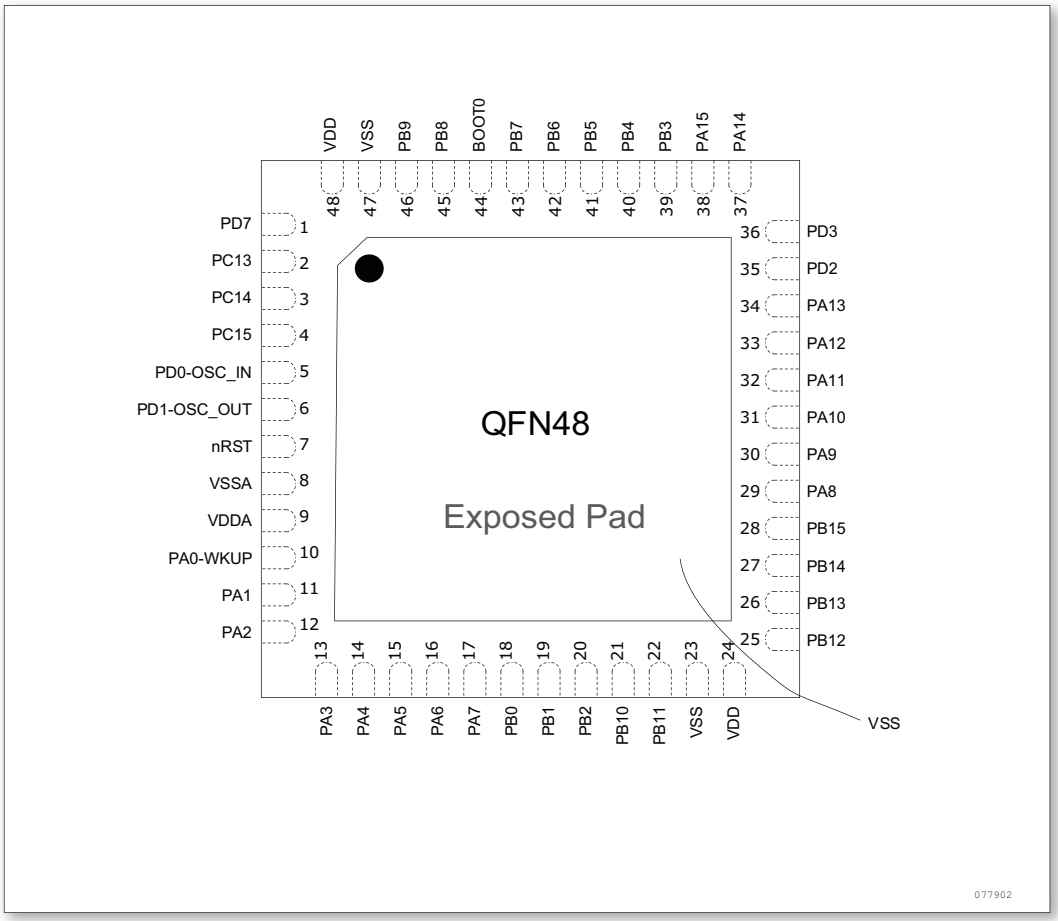

Figure 6. LQFP44 pin assignment

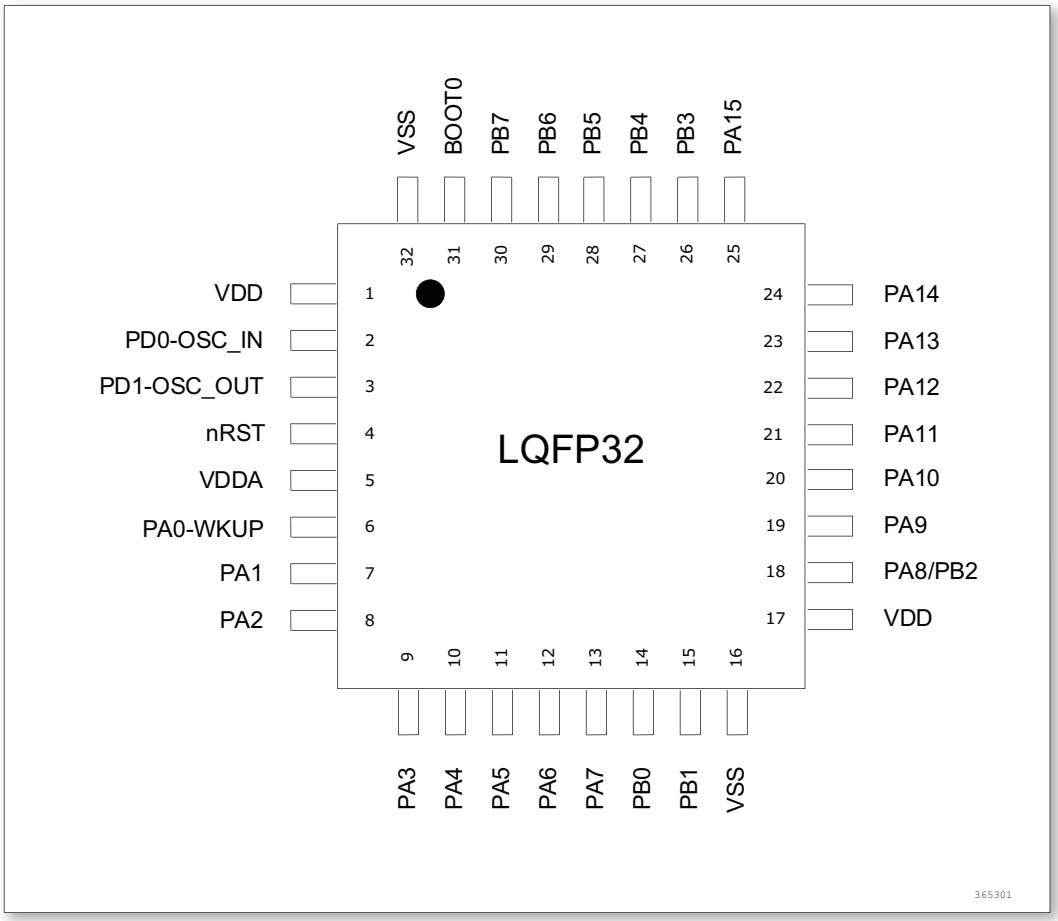

Figure 7. LQFP32 pin assignment

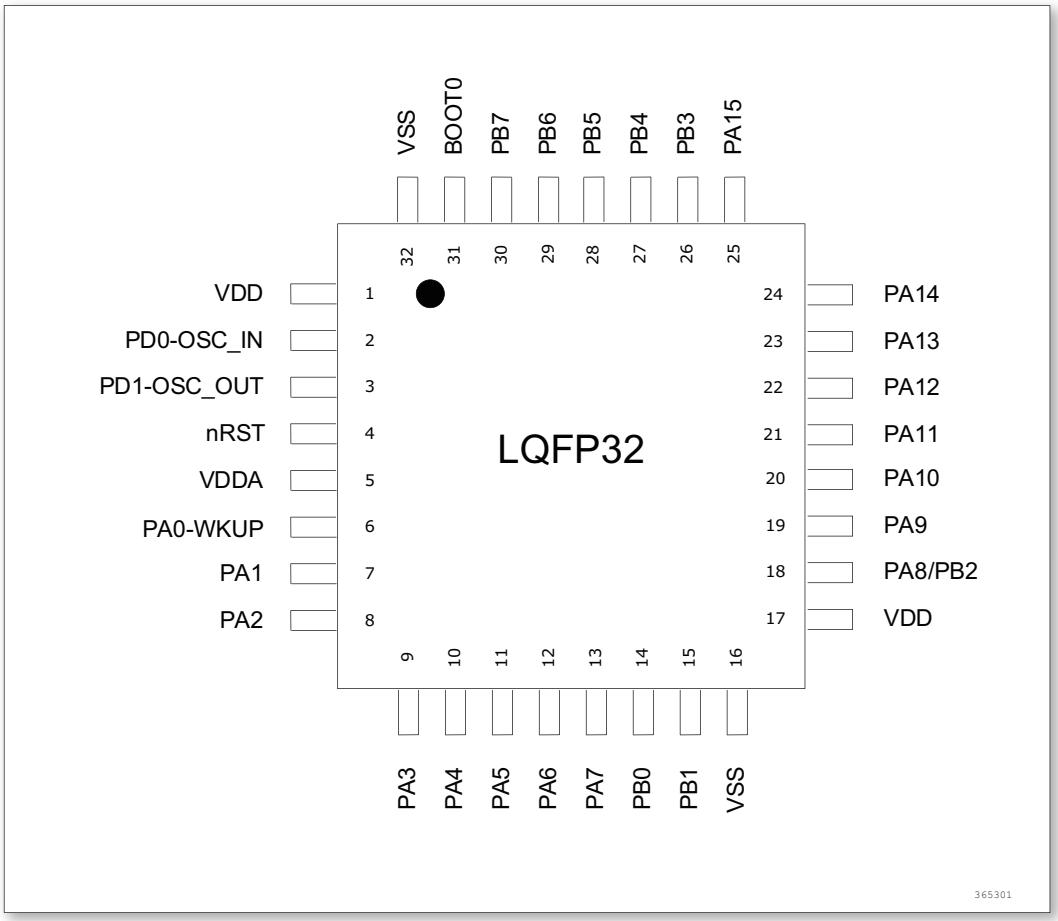

Figure 8. QFN28 pin assignment

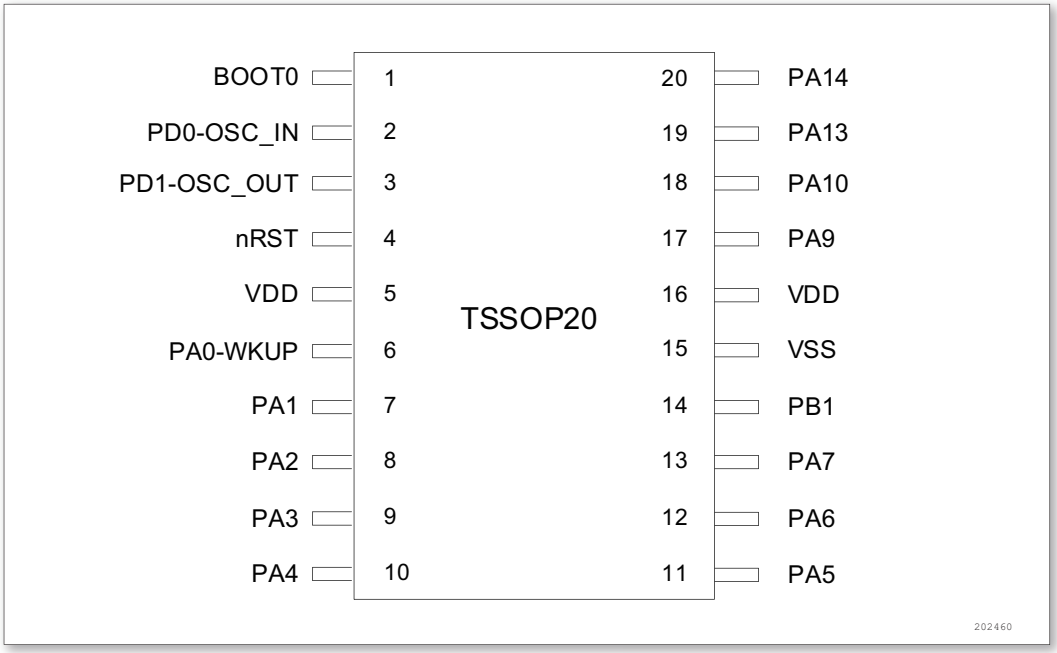

Figure 9. TSSOP20 pin assignment

Table 5. Pin definition

Pin code							Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	QFN 48	LQFP 44	LQFP 32	QFN 28	TSSOP 20						
1	1	1	1	-	-	-	PD7	I/O	FT	PD7	TIM3_CH1 TIM17_CH1	COMP2_INP
2	2	2	2	-	-	-	PC13	I/O	FT	PC13	TIM2_CH1 _ETR	COMP2_INM
3	3	3	3	-	-	-	PC14	I/O	FT	PC14	TIM2_CH2	COMP3_INP
4	4	4	4	-	1	-	PC15 OSC_IN(3)	I/O	FT	PC15	TIM2_CH3	COMP3_INM
5	5	5	5	2	-	2	PD0 OSC_IN(4)	I/O	FT	PD0	TIM1_CH1N I2C1_SDA UART1_TX SPI1_MOSI COMP2_OUT	-
6	6	6	6	3	2	3	PD1 OSC_OUT	I/O	FT	PD1	TIM1_BKIN I2C1_SCL UART1_RX SPI1_MISO SPI1_SCK COMP3_OUT	-
7	7	7	7	4	3	4	nRST	I/O	FT	Reset	-	-
8	-	-	-	-	-	-	PC0	I/O	FT	PC0	TIM8_CH1	-
9	-	-	-	-	-	-	PC1	I/O	FT	PC1	TIM8_CH1N TIM8_CH2	-
10	-	-	-	-	-	-	PC2	I/O	FT	PC2	SPI2_MISO TIM8_CH2 TIM8_CH3	-
11	-	-	-	-	-	-	PC3	I/O	FT	PC3	SPI2_MOSI TIM8_CH2N TIM8_CH1N	-
12	8	8	8	16	-	15	VSSA	S	-	VSSA	-	-
13	9	9	9	5	5	5	VDDA	S	-	VDDA	-	-

Pin code							Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	QFN 48	LQFP 44	LQFP 32	QFN 28	TSSOP 20						
14	10	10	10	6	6	6	PA0 WKUP	I/O	TC	PA0	UART2_CTS TIM2_CH1_ETR TIM14_CH1 COMP4_OUT	ADC1_VIN[0]
15	11	11	11	7	7	7	PA1	I/O	TC	PA1	UART2_RTS TIM2_CH2 TIM1_CH2	ADC1_VIN[1]
16	12	12	12	8	8	8	PA2	I/O	TC	PA2	UART2_TX TIM2_CH3 TIM1_CH2N COMP5_OUT	ADC1_VIN[2]
17	13	13	13	9	9	9	PA3	I/O	TC	PA3	UART2_RX TIM2_CH4 TIM1_CH3	ADC1_VIN[3]
18	-	-	-	-	-	-	PD4	I/O	FT	PD4	SPI1_MISO SPI1_MOSI TIM8_CH3 TIM8_CH2N COMP1_OUT	-
19	-	-	-	-	-	-	PD5	I/O	FT	PD5	SPI1_MOSI SPI1_MISO TIM8_CH3N COMP2_OUT	-
20	14	14	14	10	10	10	PA4	I/O	TC	PA4	SPI1_NSS SPI1_SCK TIM1_CH3N TIM14_CH1	OP1_INP ADC2_VIN[4] ADC1_VIN[4]
21	15	15	15	11	11	11	PA5	I/O	TC	PA5	SPI1_SCK SPI1_NSS TIM2_CH1_ETR	OP1_INM ADC2_VIN[5] ADC1_VIN[5]

Pin code							Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	QFN 48	LQFP 44	LQFP 32	QFN 28	TSSOP 20						
22	16	16	16	12	12	12	PA6	I/O	TC	PA6	SPI1_MISO TIM3_CH1 TIM1_BKIN TIM8_BKIN TIM16_CH1 COMP4_OUT	COMP4_INP3 COMP5_INP3 OP1_OUT ADC2_VIN[6] ADC1_VIN[6]
23	17	17	17	13	13	13	PA7	I/O	TC	PA7	SPI1_MOSI TIM3_CH2 TIM1_CH1N TIM8_CH1N TIM14_CH1 TIM17_CH1 COMP5_OUT	ADC2_VIN[7] ADC1_VIN[7]
24	-	-	-	-	-	-	PC4	I/O	FT	PC4	UART2_TX TIM3_CH1 SPI1_MOSI	-
25	-	-	-	-	-	-	PC5	I/O	FT	PC5	UART2_RX TIM3_CH2 SPI1_MISO	-
26	18	18	18	14	14	-	PB0	I/O	TC	PB0	TIM3_CH3 TIM1_CH2N TIM8_CH2N	OP2_INP ADC2_VIN[8] ADC1_VIN[8]
27	19	19	19	15	15	14	PB1	I/O	TC	PB1	TIM14_CH1 TIM3_CH4 TIM1_CH3N TIM8_CH3N TIM2_CH3	OP2_INM ADC2_VIN[9] ADC1_VIN[9]
28	20	20	20	18	-	-	PB2	I/O	TC	PB2	CSM_CH1_ TXRX	COMP4_INP2 COMP5_INP2 OP2_OUT ADC2_VIN[10] ADC1_VIN[10]

Pin code							Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	QFN 48	LQFP 44	LQFP 32	QFN 28	TSSOP 20						
29	21	21	21	-	-	-	PB10	I/O	TC	PB10	I2C1_SCL TIM2_CH3 CSM_CH2_ TXRX SPI2_SCK	COMP4_INP1 COMP5_INP1 OP3_OUT ADC2_VIN[11] ADC1_VIN[11]
30	22	22	22	-	-	-	PB11	I/O	FT	PB11	I2C1_SDA TIM2_CH4	OP3_INM
31	23	23	23	16	4	15	VSS	S	-	VSS	-	-
32	24	24	24	17	5	16	VDD	S	-	VDD	-	-
33	25	25	25	-	-	-	PB12	I/O	TC	PB12	SPI2_NSS SPI2_SCK TIM1_BKIN SPI2_MOSI SPI2_MISO	OP3_INP COMP4_INM0 COMP5_INM0
34	26	26	26	-	-	-	PB13	I/O	TC	PB13	SPI2_SCK SPI2_MISO TIM1_CH1N SPI2_NSS SPI2_MOSI I2C1_SCL TIM17_CH1	ADC2_VIN[3]
35	27	27	-	-	-	-	PB14	I/O	TC	PB14	SPI2_MISO SPI2_MOSI TIM1_CH2N SPI2_SCK SPI2_NSS I2C1_SDA	ADC2_VIN[2]
36	28	28	-	-	-	-	PB15	I/O	TC	PB15	SPI2_MOSI SPI2_NSS TIM1_CH3N SPI2_MISO SPI2_SCK	ADC2_VIN[1] OP4_INP
37	-	-	-	-	-	-	PC6	I/O	FT	PC6	TIM3_CH1 TIM8_CH1 TIM3_CH3 SPI1_NSS	-

Pin code							Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	QFN 48	LQFP 44	LQFP 32	QFN 28	TSSOP 20						
38	-	-	-	-	-	-	PC7	I/O	FT	PC7	TIM3_CH2 TIM8_CH2 TIM2_CH1_ETR SPI1_SCK	-
39	-	-	-	-	-	-	PC8	I/O	FT	PC8	TIM3_CH3 TIM8_CH3 TIM2_CH2	-
40	-	-	-	-	-	-	PC9	I/O	FT	PC9	TIM3_CH4 TIM8_CH4 TIM2_CH3	-
41	29	29	27	18	16	-	PA8	I/O	TC	PA8	MCO TIM1_CH1	OP4_INM COMP4_INM1 COMP5_INM1
42	30	30	28	19	-	17	PA9	I/O	TC	PA9	UART1_TX TIM1_CH2 UART1_RX I2C1_SCL MCO	OP4_OUT
43	31	31	29	20	17	18	PA10	I/O	TC	PA10	TIM17_BKIN UART1_RX TIM1_CH3 UART1_TX I2C1_SDA TIM16_CH1	ADC2_VIN[0]
44	32	32	30	21	18	-	PA11	I/O	TC	PA11	UART1_CTS TIM1_CH4 TIM1_CH3 TIM2_CH1_ETR I2C1_SCL TIM1_BKIN COMP4_OUT	COMP5_INP0

Pin code							Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	QFN 48	LQFP 44	LQFP 32	QFN 28	TSSOP 20						
45	33	33	31	22	19	-	PA12	I/O	TC	PA12	UART1_RTS TIM1_ETR TIM1_CH3N TIM2_CH2 I2C1_SDA TIM8_BKIN COMP5_OUT	COMP5_INM2
46	34	34	32	23	20	19	PA13	I/O	FT	PA13	SWDIO COMP2_OUT	-
47	35	35	-	-	-	-	PD2	I/O	TC	PD2	I2C1_SCL SPI1_NSS	COMP4_INM2
48	36	36	-	-	-	-	PD3	I/O	TC	PD3	I2C1_SDA SPI1_SCK SPI1_MISO	COMP4_INP0
49	37	37	33	24	21	20	PA14	I/O	FT	PA14	SWDCLK UART2_TX COMP1_OUT	-
50	38	38	34	25	22	-	PA15	I/O	FT	PA15	SPI1_NSS UART2_RX TIM2_CH1_ETR SPI2_SCK SPI2_MOSI SPI2_MISO TIM1_CH1N TIM1_CH3N	-
51	-	-	-	-	-	-	PC10	I/O	FT	PC10	UART1_TX SPI2_MISO SPI2_SCK SPI2_NSS SPI2_MOSI COMP5_OUT	-
52	-	-	-	-	-	-	PC11	I/O	FT	PC11	UART1_RX SPI2_MOSI SPI2_NSS SPI2_SCK SPI2_MISO	-

Pin code							Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	QFN 48	LQFP 44	LQFP 32	QFN 28	TSSOP 20						
53	-	-	-	-	-	-	PC12	I/O	FT	PC12	UART1_TX SPI2_SCK SPI2_MISO SPI2_MOSI SPI2_NSS	-
54	-	-	-	-	-	-	PD6	I/O	FT	PD6	TIM3_ETR TIM1_CH3N TIM1_CH1 TIM1_CH1N COMP3_OUT	-
55	39	39	35	26	23	-	PB3	I/O	FT	PB3	SPI1_SCK TIM2_CH2 TIM1_CH2N TIM1_CH3	-
56	40	40	36	27	24	-	PB4	I/O	FT	PB4	SPI1_MISO TIM3_CH1 TIM17_BKIN TIM1_CH3N TIM1_CH2N	-
57	41	41	37	28	25	-	PB5	I/O	FT	PB5	SPI1_MOSI TIM3_CH2 TIM16_BKIN TIM1_CH1 TIM1_CH2	-
58	42	42	38	29	26	-	PB6	I/O	FT	PB6	UART1_TX I2C1_SCL TIM16_CH1N TIM1_CH2 TIM1_CH1N	-
59	43	43	39	30	27	-	PB7	I/O	FT	PB7	UART1_RX I2C1_SDA TIM17_CH1N TIM1_CH3 TIM1_CH1	-
60	44	44	40	31	-	1	BOOT0	I	-	BOOT0	-	-

Pin code							Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	QFN 48	LQFP 44	LQFP 32	QFN 28	TSSOP 20						
61	45	45	41	-	28	-	PB8	I/O	FT	PB8	UART1_RX I2C1_SCL TIM16_CH1 TIM1_CH1 TIM3_CH2	COMP1_INP
62	46	46	42	-	-	-	PB9	I/O	FT	PB9	UART1_TX I2C1_SDA TIM17_CH1 SPI2_NSS TIM3_CH3	COMP1_INM
63	47	47	43	32	-	-	VSS	S	-	VSS	-	-
64	48	48	44	1	-	-	VDD	S	-	VDD	-	-

1. I = Input, O = Output，S = Power Supply, HiZ = High Resistance
2. FT: 5V tolerant and input signal should be between V_{DD} and 5V
   TC: Standard IO, input signal does not exceed V_{DD} voltage.
3. Applicable to QFN28 package type only
4. Applicable to LQFP64, LQFP48, QFN48, LQFP44, LQFP32 and TSSOP20 package types only

Table 6. PA port alternate function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1_ETR	-	-	-	TIM14_CH1	COMP4_OUT
PA1	-	UART2_RTS	TIM2_CH2	TIM1_CH2	-	-	-	-
PA2	-	UART2_TX	TIM2_CH3	TIM1_CH2N	-	-	-	COMP5_OUT
PA3	-	UART2_RX	TIM2_CH4	TIM1_CH3	-	-	-	-
PA4	SPI1_NSS	SPI1_SCK	-	TIM1_CH3N	TIM14_CH1	-	-	-
PA5	SPI1_SCK	SPI1_NSS	TIM2_CH1_ETR	-	-	-	-	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	TIM8_BKIN	-	TIM16_CH1	-	COMP4_OUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	TIM8_CH1N	TIM14_CH1	TIM17_CH1	-	COMP5_OUT
PA8	MCO	-	TIM1_CH1	-	-	-	-	-
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	-	TIM16_CH1	-
PA11	-	UART1_CTS	TIM1_CH4	TIM1_CH3	TIM2_CH1_ETR	I2C1_SCL	TIM1_BKIN	COMP4_OUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA12	-	UART1_RTS	TIM1_ETR	TIM1_CH3N	TIM2_CH2	I2C1_SDA	TIM8_BKIN	COMP5_OUT
PA13	SWDIO	-	-	-	-	-	-	COMP2_OUT
PA14	SWDCLK	UART2_TX	-	-	-	-	-	COMP1_OUT
PA15	SPI1_NSS	UART2_RX	TIM2_CH1_ETR	SPI2_SCK	SPI2_MOSI	SPI2_MISO	TIM1_CH1N	TIM1_CH3N

Table 7. PB port alternate function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	TIM8_CH2N	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM8_CH3N	TIM2_CH3	-	-	-
PB2	-	-	-	CSM_CH1_TXRX	-	-	-	-
PB3	SPI1_SCK	-	TIM2_CH2	-	-	-	TIM1_CH2N	TIM1_CH3
PB4	SPI1_MISO	TIM3_CH1	-	-	-	TIM17_BKIN	TIM1_CH3N	TIM1_CH2N
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	-	-	-	TIM1_CH1	TIM1_CH2
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-	TIM1_CH2	TIM1_CH1N
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	TIM1_CH3	TIM1_CH1
PB8	UART1_RX	I2C1_SCL	TIM16_CH1	TIM1_CH1	-	-	TIM3_CH2	-
PB9	UART1_TX	I2C1_SDA	TIM17_CH1	-	-	SPI2_NSS	TIM3_CH3	-
PB10	-	I2C1_SCL	TIM2_CH3	CSM_CH2_TXRX	-	SPI2_SCK	-	-
PB11	-	I2C1_SDA	TIM2_CH4	-	-	-	-	-
PB12	SPI2_NSS	SPI2_SCK	TIM1_BKIN	SPI2_MOSI	SPI2_MISO	-	-	-
PB13	SPI2_SCK	SPI2_MISO	TIM1_CH1N	SPI2_NSS	SPI2_MOSI	I2C1_SCL	TIM17_CH1	-
PB14	SPI2_MISO	SPI2_MOSI	TIM1_CH2N	SPI2_SCK	SPI2_NSS	I2C1_SDA	-	-
PB15	SPI2_MOSI	SPI2_NSS	TIM1_CH3N	SPI2_MISO	SPI2_SCK	-	-	-

Table 8. PC port alternate function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	-	-	-	-	-	TIM8_CH1	-
PC1	-	-	-	-	-	TIM8_CH1N	TIM8_CH2	-
PC2	-	SPI2_MISO	-	-	-	TIM8_CH2	TIM8_CH3	-
PC3	-	SPI2_MOSI	-	-	-	TIM8_CH2N	TIM8_CH1N	-
PC4	-	-	-	UART2_TX	-	TIM3_CH1	SPI1_MOSI	-
PC5	-	-	-	UART2_RX	-	TIM3_CH2	SPI1_MISO	-
PC6	-	TIM3_CH1	-	TIM8_CH1	-	TIM3_CH3	SPI1_NSS	-
PC7	-	TIM3_CH2	-	TIM8_CH2	-	TIM2_CH1_ETR	SPI1_SCK	-

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC8	-	TIM3_CH3	-	TIM8_CH3	-	TIM2_CH2	-	-
PC9	-	TIM3_CH4	-	TIM8_CH4	-	TIM2_CH3	-	-
PC10	UART1_TX	-	-	SPI2_MISO	SPI2_SCK	SPI2_NSS	SPI2_MOSI	COMP5_OUT
PC11	UART1_RX	-	-	SPI2_MOSI	SPI2_NSS	SPI2_SCK	SPI2_MISO	-
PC12	UART1_TX	-	-	SPI2_SCK	SPI2_MISO	SPI2_MOSI	SPI2_NSS	-
PC13	-	-	-	-	-	-	TIM2_CH1_ETR	-
PC14	-	-	-	-	-	-	TIM2_CH2	-
PC15	-	-	-	-	-	-	TIM2_CH3	-

Table 9. PD port alternate function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	TIM1_CH1N	I2C1_SDA	-	UART1_TX	-	SPI1_MOSI	SPI1_MOSI	COMP2_OUT
PD1	TIM1_BKIN	I2C1_SCL	-	UART1_RX	-	SPI1_MISO	SPI1_SCK	COMP3_OUT
PD2	-	I2C1_SCL	-	-	-	SPI1_NSS	SPI1_NSS	-
PD3	-	I2C1_SDA	-	-	-	SPI1_SCK	SPI1_MISO	-
PD4	SPI1_MISO	SPI1_MOSI	-	-	-	TIM8_CH3	TIM8_CH2N	COMP1_OUT
PD5	SPI1_MOSI	SPI1_MISO	-	-	-	-	TIM8_CH3N	COMP2_OUT
PD6	-	TIM3_ETR	-	TIM1_CH3N	-	TIM1_CH1	TIM1_CH1N	COMP3_OUT
PD7	-	-	-	-	-	TIM3_CH1	TIM17_CH1	-

Table 10. Comparator 1/2/3 input and output port

Port / Comparator	INP	INM	OUT
COMP1	PB8	PB9	PA14/PD4
COMP2	PD7	PC13	PA13/PD0/PD5
COMP3	PC14	PC15	PD1/PD6

Table 11. Comparator 4/5 input and output port

Port / Comparator	INP0	INP1	INP2	INP3	INM0	INM1	INM2	INM3	OUT
COMP4	PD3	PB10	PB2	PA6	PB12	PA8	PD2	CRV	PA0/ PA6/ PA11
COMP5	PA11	PB10	PB2	PA6	PB12	PA8	PA12	CRV	PA2/ PA7/ PA12/ PC10

Table 12. Operational amplifier input and output port

Port / Operational amplifier	INP	INM	OUT
OP1	PA4	PA5	PA6
OP2	PB0	PB1	PB2
OP3	PB12	PB11	PB10
OP4	PB15	PA8	PA9

Annotation: PB2 and PA8 share with one GPIO function:

1. If this GPIO is set as the op-amp output function, PB2 and PA8 need to be set to analog input mode.
2. If this GPIO is disallowed to be used as an op-amp output function or ADC1_CH10/ADC2_CH10 input function, the GPIO can set the corresponding pin multiplexing function of PB2 and PA8 respectively.

4 Memory mapping

Memory mapping

Table 13. Memory mapping

Bus	Addressing range	Size	Peripheral	Notes
Flash	0x0000 0000 0x0001 FFFF	128 KB	Main flash memory, system memory, or SRAM, depends on the configuration of BOOT	
	0x0002 0000 0x07FF FFFF	~128 MB	Reserved	
	0x0800 0000 0x0801 FFFF	128 KB	Main Flash memory	
	0x0802 0000 - 0x1FFD FFFF	~256 MB	Reserved	
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved	
	0x1FFE 0200 - 0x1FFE 0FFF	3 KB	Reserved	
	0x1FFE 1000 - 0x1FFE 1BFF	3 KB	Reserved	
	0x1FFE 1C00 - 0x1FFF F3FF	~256 MB	Reserved	
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800 - 0x1FFF F80F	16 B	Option bytes	
	0x1FFF F810 - 0x1FFF FFFF	~2 KB	Reserved	
SRAM	0x2000 0000 - 0x2000 2FFF	12 KB	SRAM	
	0x2000 3000 - 0x2FFF FFFF	~512 MB	Reserved	
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2	
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3	
	0x4000 0800 - 0x4000 0BFF	8 KB	Reserved	
	0x4000 2800 - 0x4000 2BFF	1 KB	BKP	
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG	
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG	
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved	
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2	
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved	
	0x4000 4400 - 0x4000 47FF	1 KB	UART2	
	0x4000 4800 - 0x4000 4BFF	3 KB	Reserved	
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1	
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved	
	0x4000 5C00 - 0x4000 5FFF	1 KB	Reserved	
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved	

Bus	Addressing range	Size	Peripheral	Notes
APB1	0x4000 6400 - 0x4000 67FF	1 KB	Reserved	
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved	
	0x4000 6C00 - 0x4000 6FFF	1 KB	Reserved	
	0x4000 7000 - 0x4000 73FF	1 KB	PWR	
	0x4000 7400 - 0x4000 FFFF	35 KB	Reserved	
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI	
	0x4001 0800 0x4001 0BFF	1 KB	TIM8	
	0x4001 0C00 0x4001 23FF	6 KB	Reserved	
	0x4001 2400 - 0x4001 27FF	1 KB	ADC1	
	0x4001 2800 - 0x4001 2BFF	1 KB	ADC2	
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1	
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1	
	0x4001 3400 - 0x4001 37FF	1 KB	DBGMCU	
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1	
	0x4001 3C00 - 0x4001 3FFF	1 KB	COMP	
	0x4001 4000 - 0x4001 43FF	1 KB	TIM14	
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16	
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17	
	0x4001 4C00 0x4001 63FF	6 KB	Reserved	
	0x4001 6400 0x4001 67FF	1 KB	PWM	
	0x4001 6800 0x4001 7FFF	6 KB	Reserved	
AHB	0x4002 0000 - 0x4002 03FF	1 KB	DMA	
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved	
	0x4002 1000 - 0x4002 13FF	1 KB	RCC	
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved	
	0x4002 2000 - 0x4002 23FF	1 KB	Flash 接口	
	0x4002 2400 0x4002 0C00	3 KB	Reserved	
	0x4002 3000 0x4002 33FF	1 KB	CRC	
	0x4002 3400 0x4002 FFFF	51 KB	Reserved	
	0x4003 0000 0x4003 03FF	1 KB	HWDIV	
	0x4003 0400 0x4003 07FF	1 KB	HSQRT	
	0x4003 0800 0x47FF FFFF	~127 MB	Reserved	
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA	
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB	
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC	
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD	
	0x4800 1000 - 0x5FFF FFFF	~383 MB	Reserved	

5 Electrical characteristics

Electrical characteristics

5.1 Test condition

All voltages are based on V_{SS} unless otherwise stated.

5.1.1 Minimum and maximum value

Unless otherwise stated, the minimum and maximum value performed at ambient temperature T_A = 25°C and V_{DD} = 3.3V.

5.1.2 Typical value

Unless otherwise stated, typical data is based on T_A = 25°C and V_{DD} = 3.3V. These data are for design guidance only and have not been tested.

5.1.3 Typical curve

Typical curves are for design guidance only and are not tested unless otherwise stated.

5.1.4 Load capacitor

The load conditions when measuring the pin parameters are shown in the figure below.

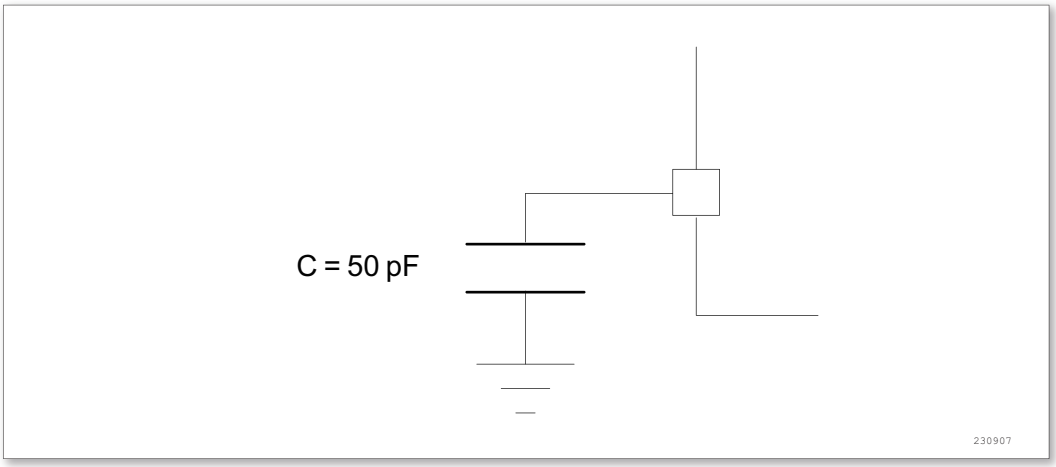

Figure 10. Load condition of the pin

5.1.5 Pin input voltage

The measurement of the input voltage on the pin is shown in the figure below.

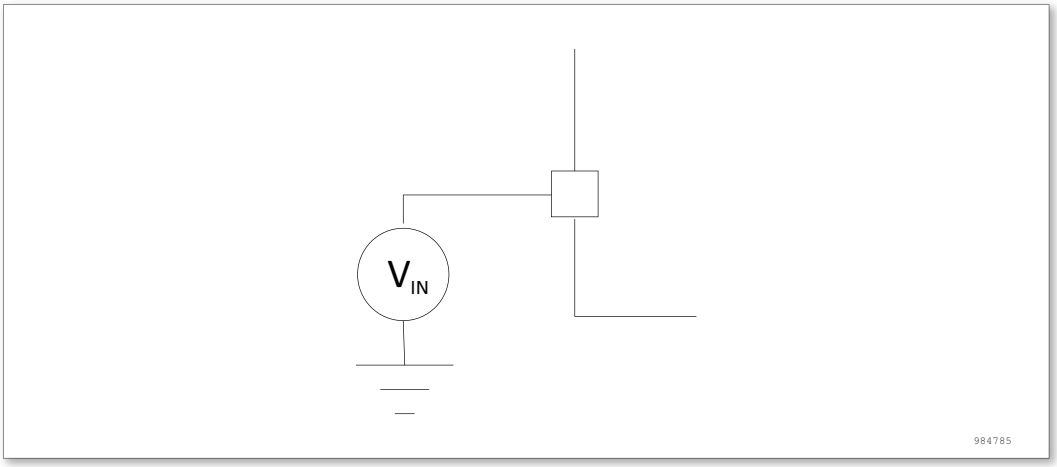

Figure 11. Pin input voltage

5.1.6 Power scheme

The power supply design scheme is shown in the figure below.

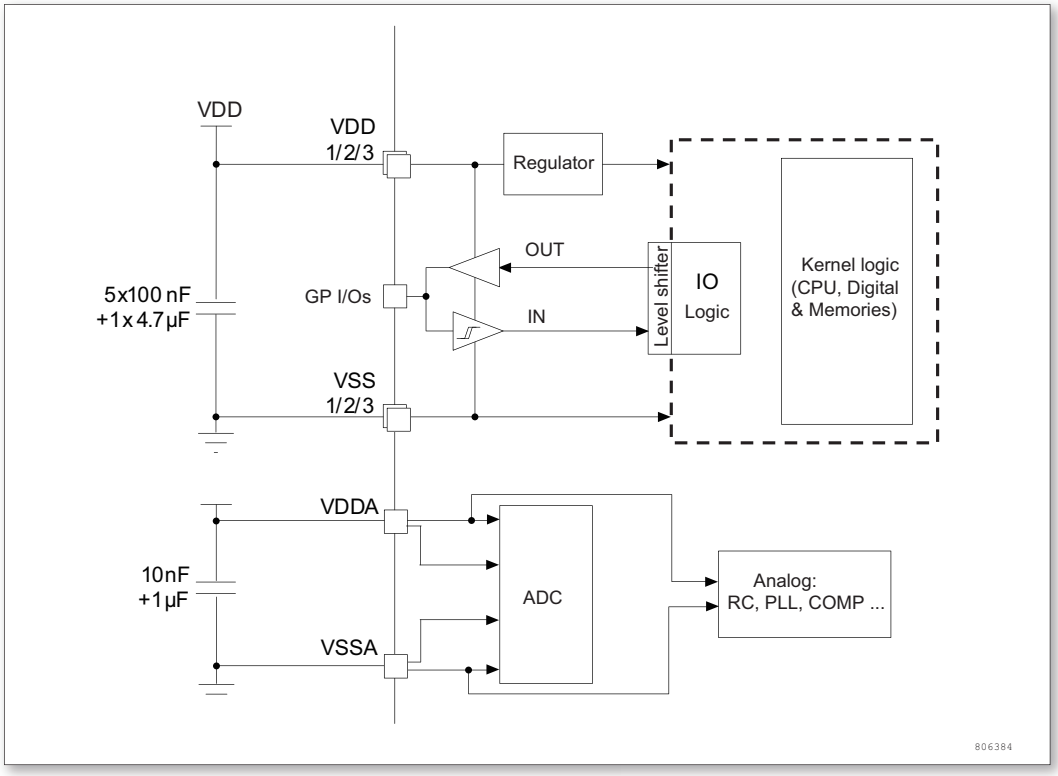

Figure 12. Power scheme

5.1.7 Current consumption measurement

The measurement of the current consumption on the pin is shown in the figure below.

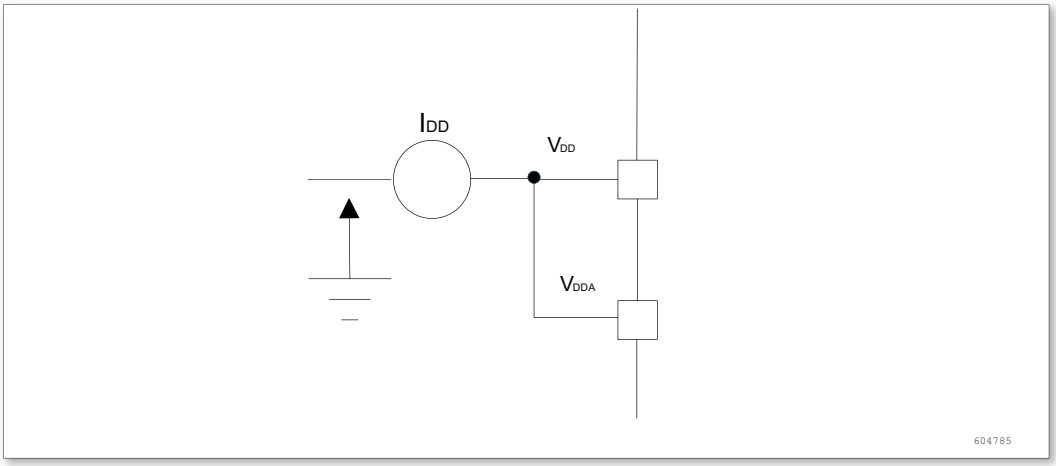

Figure 13. Current consumption measurement scheme

5.2 Absolute maximum rating

If the load applied to the device exceeds the value given in the ”Absolute Group Maximum Ratings” list (Table 14, Table 15), it may result in the device is permanently damaged. This is just to give the maximum load that can be tolerated, and does not mean that the functional operation of the device is correct under these conditions. Long-term operation of the device under maximum conditions can affect device reliability.

Table 14. Voltage characteristics

Symbol	Description	min	max	units
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{SSA})(1)	- 0.3	5.8	V
V_{IN}	Input voltage on the 5Vtolerant pin (2)	V_{SS} - 0.3	5.5	
	Input voltage on other pins (2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert \triangle V_{DDx} \rvert$	voltage difference between different supply pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Voltage difference between different ground pins		50	

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply within the permissible range.
2. V_{IN} maximum must always be respected. For information about the maximum allowed injected current values, please see the table below.

Table 15. Current characteristics

Symbol	Description	Maximum	Units
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (supply current) (1)	120	mA
I_{VSS}	Total current out of V_{SS} wire (outflow current) (1)	120	
I_{IO}	Output sink current on any I/O and control pins	20	
	Output current on any I/O and control pins	-18	
$I_{INJ(PIN)}$ (2)(3)	Injection current on NRST pin	±5	mA
$I_{INJ(PIN)}$ (2)(3)	Injection current on OSC_IN pin of HSE and OSC_IN pin LSE	±5	mA
$I_{INJ(PIN)}$ (2)(3)	Injection current on other pins (4)	±5	mA
$\Sigma I_{INJ(PIN)}$ (6)	Total injection current on all I/O and control pins (5)	±25	mA

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply within the permissible range.
2. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sunk/pulled between two consecutive power pins that refer to LQFP package with dense pins.
3. The reverse injection current can interfere with the analog performance of the device.
4. These I/Os cannot be forward injected, and forward injection does not occur when the input voltage is below the specified maximum.
5. A positive injection current is induced by $V_{IN} > V_{DDA}$ while a negative injection current is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3 Operating conditions

5.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	96	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	
V_{DD}	Standard operating voltage		2.0	5.5	V

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA} (1)	Analog operating voltage (ADC not used)	Must be the same voltage as V_{DD}	2.0	5.5	V
	Analog operating voltage (ADC used)		2.5	5.5	
T_A	Ambient temperature	Maximum power dissipation	-40	85	°C
		Low power dissipation(2)	-40	105	

5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are based on tests under normal operating conditions.

Table 17. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD} (1)	V_{VDD} rise time tr	T_A = 25°C	300	∞	μS/V
	V_{VDD} fall time tr		300	∞	
V_{ft} (3)	Power-down threshold voltage	-	0	-	mV

1. All power-ups need to start at 0V, to ensure that the chip can be powered up reliably.

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 16.

Table 18. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0000 (Rising edge)		1.82		V
		PLS[3：0]=0000 (Falling edge)		1.71		V
		PLS[3：0]=0001 (Rising edge)		2.12		V
		PLS[3：0]=0001 (Falling edge)		2.00		V
		PLS[3：0]=0010 (Rising edge)		2.41		V
		PLS[3：0]=0010 (Falling edge)		2.30		V
		PLS[3：0]=0011 (Rising edge)		2.71		V
		PLS[3：0]=0011 (Falling edge)		2.60		V
		PLS[3：0]=0100 (Rising edge)		3.01		V
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0100 (Falling edge)		2.90		V
		PLS[3：0]=0101 (Rising edge)		3.31		V
		PLS[3：0]=0101 (Falling edge)		3.19		V
		PLS[3：0]=0110 (Rising edge)		3.61		V
		PLS[3：0]=0110 (Falling edge)		3.49		V
		PLS[3：0]=0111 (Rising edge)		3.91		V
		PLS[3：0]=0111 (Falling edge)		3.79		V
		PLS[3：0]=1000 (Rising edge)		4.21		V
		PLS[3：0]=1000 (Falling edge)		4.09		V
		PLS[3：0]=1001 (Rising edge)		4.51		V
		PLS[3：0]=1001 (Falling edge)		4.39		V
		PLS[3：0]=1010 (Rising edge)		4.81		V
		PLS[3：0]=1010 (Falling edge)		4.69		V
$V_{PVDhyst}$(2)	PVD hysteresis			110		mV
$V_{POR/PDR}$	Power on/down reset threshold	Falling edge	1.63(1)	1.66	1.68	V
		Rising edge		1.75		V
V_{PDRhys}(2)	PDR hysteresis			90.9		mV
$T_{RSTTEMPO}$(2)	Reset duration			0.61		ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction.

5.3.4 Supply current characteristics

The current consumption is a function of multiple parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHz is 2 waiting periods, 72 ~ 96 MHz is 3 waiting periods).
- The instruction prefetching function is on. When the peripherals are enabled：$f_{HCLK} = f_{PCLK1}$.

Note：The instruction prefetching function must be set before setting the clock and bus divider.

Table 19. Typical and maximum current consumption in stop and standby modes(2)

Symbol	Parameter	Conditions	Typ(1)	Unit
			T_A=25°C	
I_{DD}	Supply current in Stop mode	Enter the stop mode after reset,V_{DD} = 3.3V, LPDS = 0 (PWR->CR bit 0)	30	μA
		Enter the stop mode after reset,V_{DD} = 3.3V, LPDS = 1 (PWR->CR bit 0)	4.6	
	Supply current in Standby mode	Enter the standby mode after reset,V_{DD} = 3.3V	0.4	

1. Typical values are tested at T_A = 25°C.
2. Data based on characterization results, not tested in production.The IO state is an analog input.

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration, and are connected to a static level —- V_{DD} or V_{SS} (no load).
- All the peripherals are closed, unless otherwise specified.
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHzis 2 waiting periods, 72 ~ 96 MHzis 3 waiting periods).
- The ambient temperature and V_{DD} supply voltage conditions are summarized in Table 16.
- The instruction prefetching function is on. When the peripherals are enabled：$f_{HCLK} = f_{PCLK1} = f_{PCLK2}$.

Note: The instruction prefetch function must be set before the clock is set and the bus is divided.

Table 20. Typical current consumption in Run mode, code executing from flash memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in run mode	External clock(2)	96MHz	26.23	15.2	mA
			72MHz	20.52	12.19	
			48MHz	14.71	9.13	
			36MHz	11.76	7.58	
			24MHz	6.158	1.544	
			8MHz	2.176	0.962	

1. The typical value is tested at T_A = 25°Cand V_{DD} = 3.3V.
2. External clock is 8MHz, when f_{HCLK} > 8MHz enable PLL.

Table 21. Maximum current consumption in sleep mode, code executing from flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(2)	96MHz	30.6	15.7	mA
			72MHz	23.9	12.5	
			48MHz	17	9.08	
			36MHz	13	7.32	
			24MHz	9.51	6.15	
			8MHz	3.51	2.24	

1. The typical value is tested at T_A = 25°Cand V_{DD} = 3.3V.
2. External clock is 8MHz, when f_{HCLK} > 8MHz enable PLL.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 22. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load) .
- All peripherals are disabled except when explicitly mentioned.
- The given value is calculated by measuring the current consumption.
  - With all peripherals clocked OFF
  - With only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions V_{DD} summarized in Table 16.

Table 22. On-chip peripheral current consumption(1)

Peripheral		Typical consumption at 25 °C	Unit	Peripheral		Typical consumption at 25 °C	Unit
APB1	TIM2	0.99	mA	APB2	ADC	1.03	mA
	TIM3	1.00			SPI1	0.99	
	I2C	0.99			UART1	0.52	
APB2	TIM14	1.02		AHB	GPIOA	0.53	
	TIM16	1.02			GPIOB	0.53	
	TIM17	1.02			GPIOC	0.53	
	TIM1	0.99			GPIOD	0.53	

1. f_{HCLK} = 96MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, the prescale coefficient for each device is the default value.

5.3.5 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured using a high-speed external clock source, ambient temperature and power supply voltage meet the conditions of general operating conditions.

Table 23. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		2	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7V_{DD}		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		0.3V_{DD}	V
$t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$	OSC_IN rise time(1)				20	ns
$t_{f(HSE)}$	OSC_IN fall time(1)				20	ns
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	μA

1. Guaranteed by design, not tested in production.

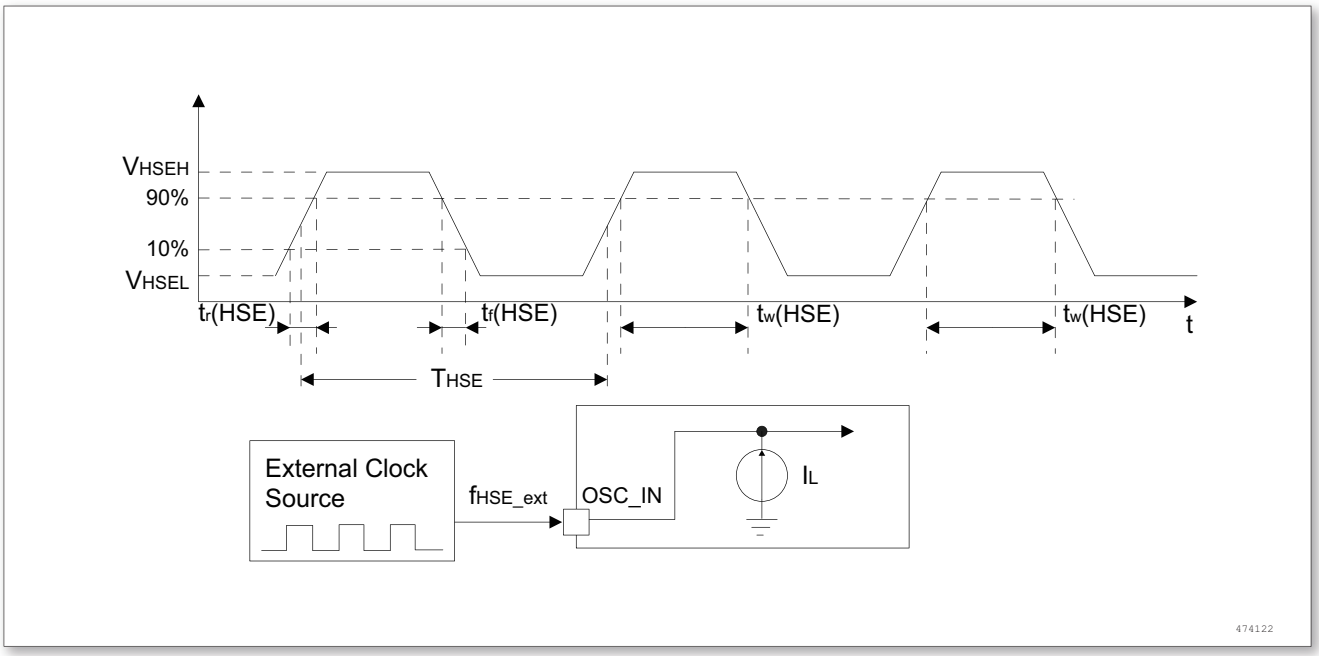

Figure 14. High-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with an 2 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this section are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 24. HSE 2 ~ 24 oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	24	MHz
R_F	Feedback resistor			1000		kΩ
C_{L1} C_{L2}(3)	The proposed load capacitance corresponds to the crystal serial impedance (R_S) (4)	R_S = 30Ω		30		pF
I_2	HSE current consumption	V_{DD} = 3.3V V_{IN} = V_{SS} 30pF load			4.5	mA
g_m	Oscillator transconductance	Startup		8.5		mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized		3		mS

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

2. Drawn from comprehensive evaluation, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF (typical value) range, designed for high-frequency applications. A suitable crystal or resonator should also be carefully selected. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer typically specifies a load capacitance which is the serial combination of C_{L1} and C_{L2}. When choosing C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into account (the combined pin and the PCB board capacitance can be roughly estimated as 10pF).
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time, measured from the moment the software enables HSE to a stable 8MHz oscillation is obtained. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

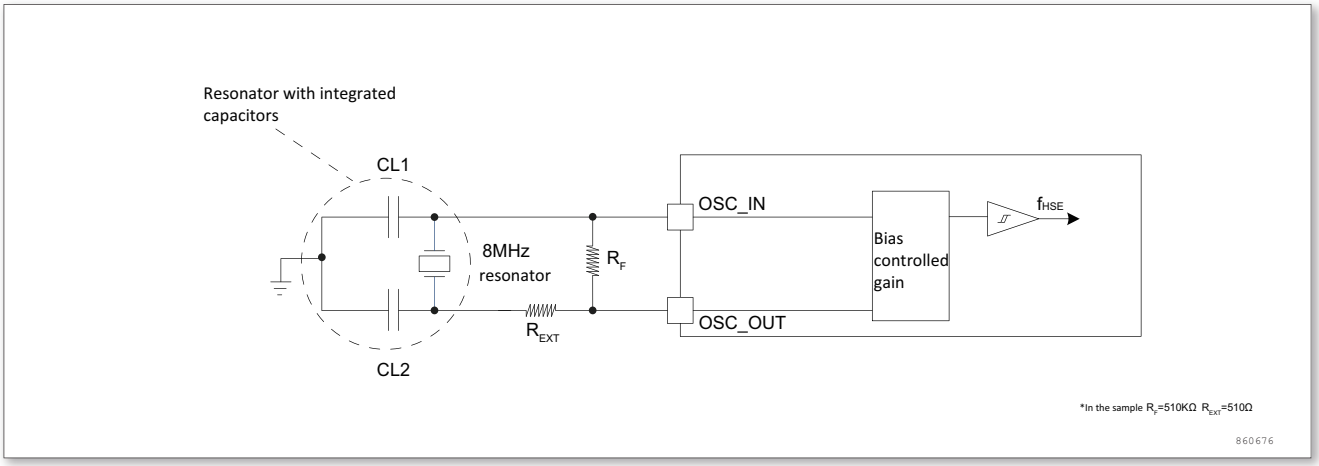

Figure 15. Typical application with an 8 MHz crystal

5.3.6 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 25. HSI oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			48		MHz
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40°C ~ 105°C	-10		7.9	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -20°C ~ 85°C	-7.6		6.6	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 0°C ~ 75°C	-4.6		4.7	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 25°C	-2.5		2.5	%

1. V_{DD} = 3.3V, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 26. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency		31	40	75	KHz
$t_{SU(LSI)}$(2)	LSI oscillator startup time				100	μS
$I_{DD(LSI)}$(3)	LSI oscillator power consumption			1.1	1.7	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, unless otherwise stated
2. Drawn from comprehensive evaluation, not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up times from low power mode

The wake-up times listed in the table below are measured during the wake-up phase of the internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Stop or Standby mode: The clock source is the oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	HSI clock wakeup	4.2	μS
t_{WUSTOP}(1)	Wakeup from Stop mode (Voltage regulator is in run mode)	HSI clock wakeup < 2μS	5	μS
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI clock wakeup < 2μS The regulator wakes up from the off mode < 30μS	510	μS

1. The wake-up time is measured from the start of the wake-up event to the user program to read the first instruction.

5.3.7 PLL characteristics

The parameters listed in the table below are measured using ambient temperature and supply voltage in accordance with the general operating conditions.

Table 28. PLL characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	2		24	MHz
	PLL input clock duty cycle	40		60	%
f_{PLL_OUT}	PLL multiplier output clock	40		200	MHz
t_{LOCK}	PLL lock time			100	μS

1. Guaranteed by design, not tested in production.
2. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.8 Memory characteristics

Flash memory

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	16-bit programming time			6	7.5	μS
t_{ERASE}	Page (1024K bytes) erase time			4	5	mS
t_{ME}	Mass erase time			30	40	mS
I_{DD}	Supply current	Read mode		9		mA
		Write mode			7	mA
		Erase mode			2	mA
V_{prog}	Programming voltage			1.5		V

Table 30. Flash memory endurance and data retention(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NEND	Endurance (Annotation: Erase number of times)		20			K cycle
t_{RET}	Data retention	T_A = 105°C	20			Year
		T_A = 25°C	100			

1. Drawn from comprehensive evaluation, not tested in production.

2. Cycle tests are carried out in the whole temperature range.

5.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports) , the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- EFT：A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in the following table.

Table 31. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transientvoltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pinsto induce a functional disturbance	V_{DD} = 3.3V,T_A=25°C, f_{HCLK}=96MHz.Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore, it is recommended that users apply EMC software optimization and conduct EMC-related prequalification tests.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be

reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

5.3.10 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78A IC latch-up standard.

Table 32. ESD characteristics

Symbol	Parameter	Conditions	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = 25°C, conforming to JESD22-C101	±2000	
I_{LU}	Latch-up current	T_A = 25°C, conforming to JESD78E	±100	mA

5.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 14 are derived from tests. All I/O ports are compatible with CMOS

Table 33. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	2.5V< V_{DD} < 5.5V			0.3*V_{DD}	V
V_{IH}	Input high level voltage	2.5V< V_{DD} < 5.5V	0.7*V_{DD}			V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis(1)	2.5V< V_{DD} < 5.5V		0.1*V_{DD}		V
I_{lkg}	Input leakage current (2)	2.5V< V_{DD} < 5.5V			1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	2.5V< V_{DD} < 5.5V	10		50	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	2.5V< V_{DD} < 5.5V	10		100	kΩ
C_{IO}	I/O pin capacitance	2.5V< V_{DD} < 5.5V			10	pF

1. Schmitt Trigger switching hysteresis voltage level.Data drwan from comprehensive evaluation, not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins.
3. Pull-up and pull-down resistors are MOS.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in section 5.2：

- The sum of the currents obtained from V_{DD} for all I/O ports, plus the maximum operating current that the MCU obtains on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 16. All I/O ports are CMOS compatible.

Table 34. Output voltage characteristics

SPEED[1：0]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)	Output high level voltage		2.60			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)(3)	Output high level voltage		2.40			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			1.40	V
	V_{OH} (2)(3)	Output high level voltage					V
10	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)	Output high level voltage		2.80			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)(3)	Output high level voltage		2.60			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			1.00	V
	V_{OH} (2)(3)	Output high level voltage		1.80			V
01	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)	Output high level voltage		2.80			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)(3)	Output high level voltage		2.80			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			0.80	V
	V_{OH} (2)(3)	Output high level voltage		2.20			V

1. The current absorbed by the chip I_{IO} must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O feet and control pins) must not exceed I_{VSS}.

2. The current output I_{IO} of the chip must always follow the absolute maximum rating given in the table, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.
3. Data drawn from comprehensive evaluation, not tested in production.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in figure 16 and Table 35, respectively.

Unless otherwise stated, the parameters listed in Table 35 are measured using the ambient temperature and supply voltage in accordance with the condition Table 14.

Table 35. I/O AC characteristics (1)

SPEED[1：0]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	tf	Fall time from high level output to low level output	C_L=50pF, V_{DD}=3.3V		7.0		ns
	tr	Rise time from low level output to high level output			11.4		ns
10	tf	Fall time from high level output to low level output			4.9		ns
	tr	Rise time from low level output to high level output			6.5		ns
01	tf	Fall time from high level output to low level output			3.9		ns
	tr	Rise time from low level output to high level output			5.0		ns

1. The speed of the I/O port can be configured via MODEx[1:0]. See the description of the GPIO Port Configuration Register in this chip reference manual.

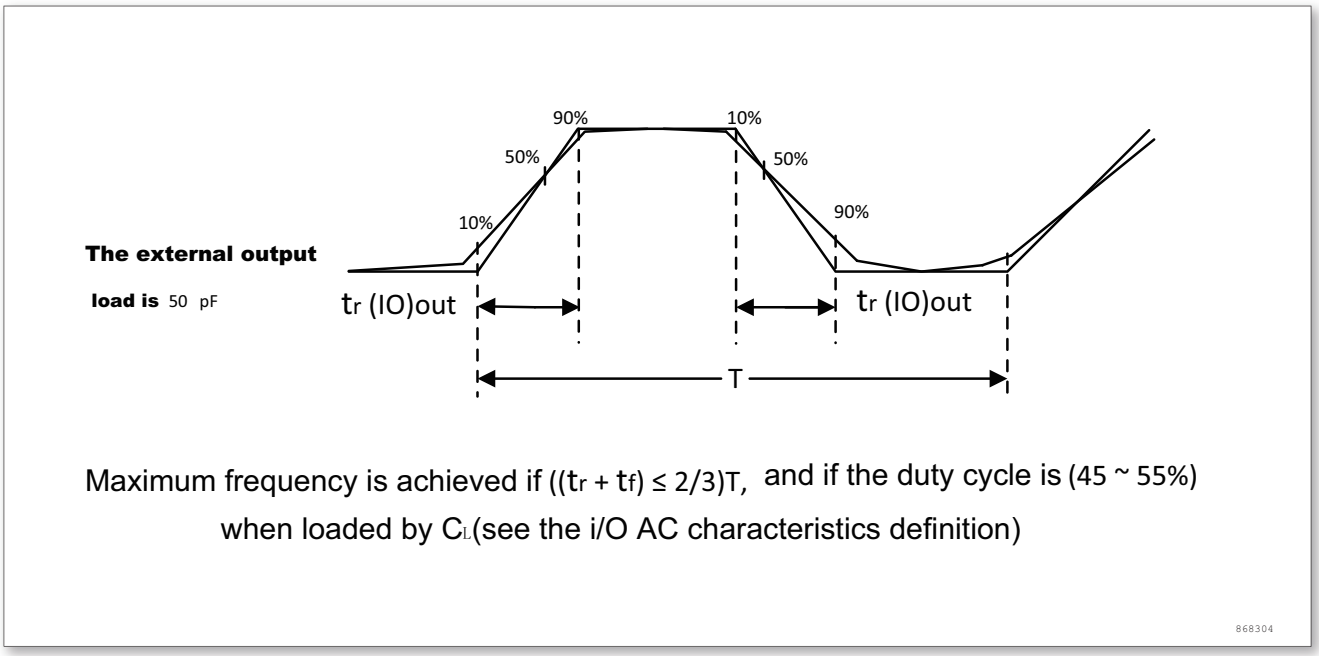

Figure 16. I/O AC characteristics

5.3.12 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 16.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage		-0.3		0.3*V_{DD}	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage		0.7*V_{DD}		V_{DD}	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			0.1*V_{DD}		V
R_{PU}	Weak pull-up equivalent resistor(2)	V_{IN} = V_{SS}	7	19	60	kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse				100	μs
$V_{NF(NRST)}$ (1)	NRST input not filtered pulse		300			μs

1. Guaranteed by design, not tested in production.
2. The pullup resistor is a MOS resistor.

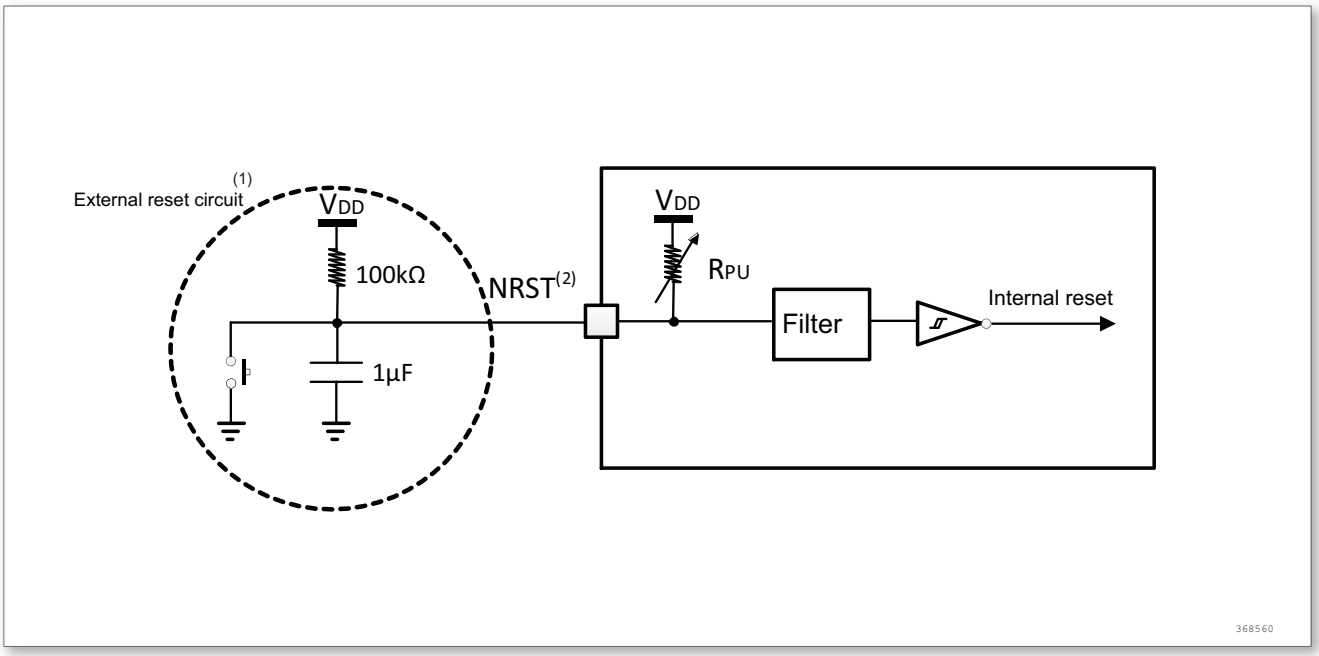

Figure 17. Recommended NRST pin protection

1. The reset network is to prevent parasitic reset.
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 36, otherwise the MCU cannot be reset.

5.3.13 Timer characteristics

The parameters given in the following tables are guaranteed by design.

For details on the characteristics of the I/O multiplexing function pins (output compare, input capture, external clock, PWM output) , see subsubsec 5.3.11.

Table 37. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$ = 96MHz	10.4		nS
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$	MHz
		$f_{TIMxCLK}$ = 96MHz	0	96	
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	16 bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$96MHz	0.0104	682	µS
t_{MAX_COUNT}	The maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$96MHz		44.7	S

1. TIMx is a generic name.

5.3.14 Communication interfaces

I2C interface characteristics

Unless otherwise specified, the parameters given in Table 38 are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in Table 16.

The I2C interface conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not true pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} is closed but still exists.

The I2C I/Os characteristics are listed in Table 38, the alternate function characteristics of I/Os (SDA and SCL) refer to subsubsec 5.3.11.

Table 38. I2C characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock fall time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock rise time	4.0		0.6		μs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SDL)}$	SDA and SCL rise time		1000	2.0+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SDL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		
$t_{w(STO:STA)}$	Time from Stop condition to Start condition	4.7		1.3		
C_b	Capacitive load of each bus		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. In order to span the undefined area of the falling edge of SCL, it must ensure that the SDA signal has a hold time of at least 300nS.

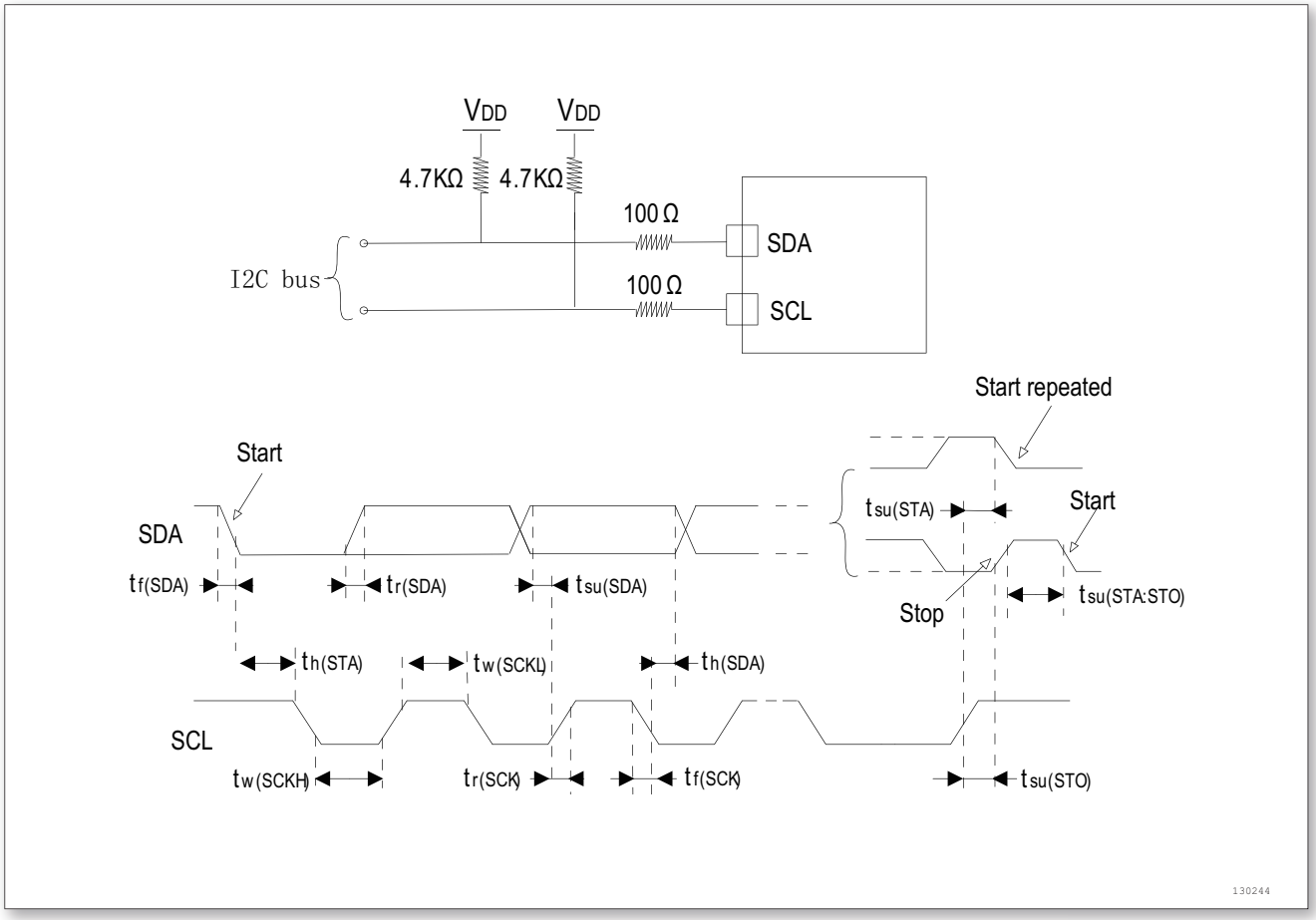

Figure 18. I2C bus AC waveform and measurement circuit(1)

1. Measurement point is set to the CMOS level：0.3V_{DD} and 0.7V_{DD}.

SPI characteristics

Unless otherwise specified, the parameters given in Table 39 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 16.

Refer to subsubsec 5.3.11 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 39. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} 1/$t_{c(SCK)}$	SPI clock frequency	Master mode	0	36	MHz
		Slave mode	0	18	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 30pF		8	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 30pF		8	ns
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	4t_{PCLK}		ns
$t_{h(NSS)}$ (2)	NSS hold time	Slave mode	73		ns
$t_{w(SCKH)}$ (2)	SCK high time	Master mode，f_{PCLK} = 36MHz，prescale coefficient = 4	50	60	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SCKL)}$ (2)	SCK low time	Master mode，f_{PCLK} = 36MHz，prescale coefficient = 4	50	60	ns
$t_{su(SI)}$ (2)	Data input setup time	Slave mode	1		ns
$t_{h(SI)}$ (2)	Data input hold time	Slave mode	3		ns
$t_{a(SO)}$ (2)(3)	Data output access time	Slave mode，f_{PCLK} = 36MHz，prescale coefficient = 4	0	55	ns
		Slave mode，f_{PCLK} = 24MHz		$4t_{PCLK}$	
$t_{dis(SO)}$ (2)(4)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$ (2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$ (2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$ (2)		Master mode (after enable edge)	4		

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

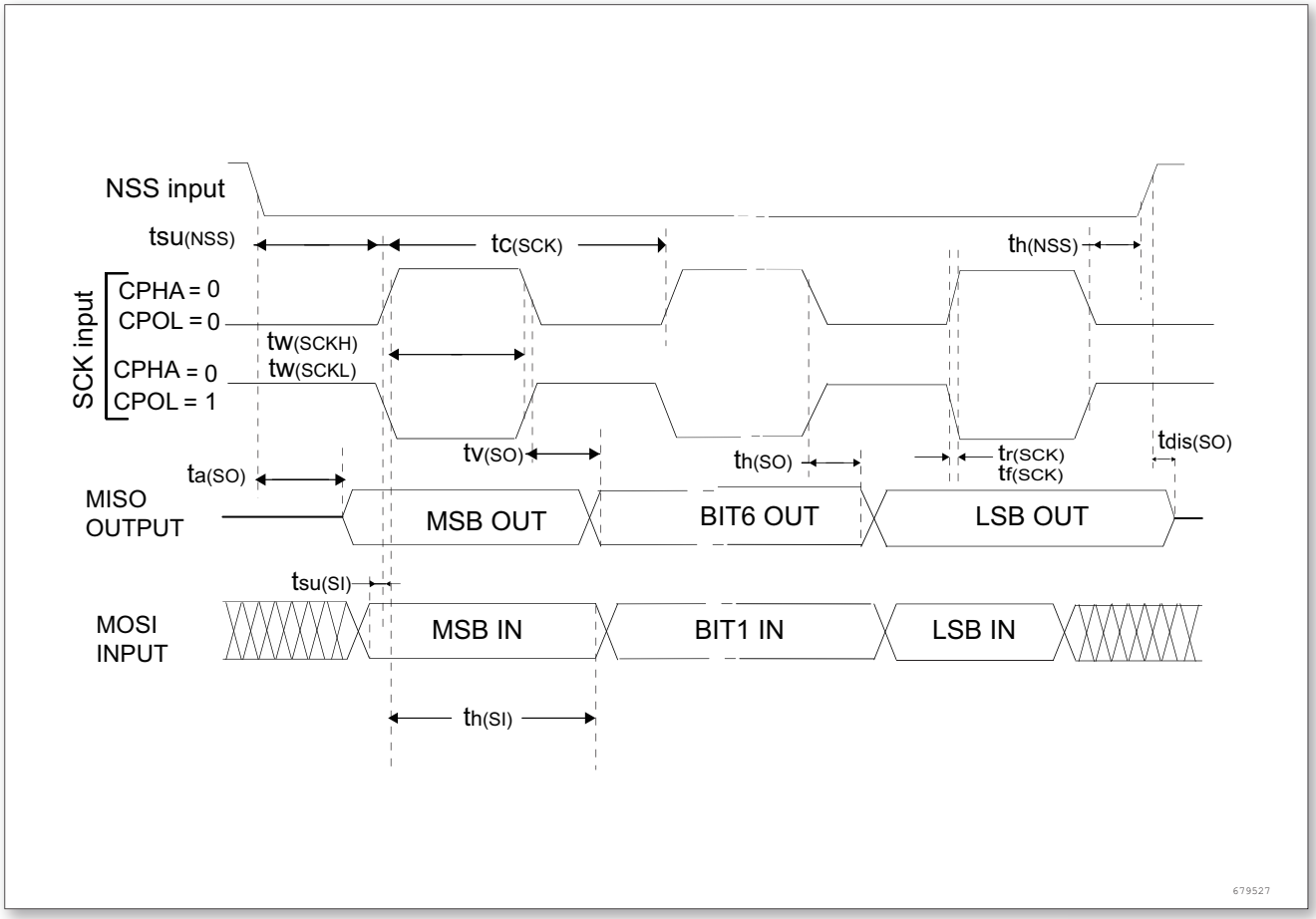

Figure 19. SPI timing diagram-slave mode and CPHA = 0

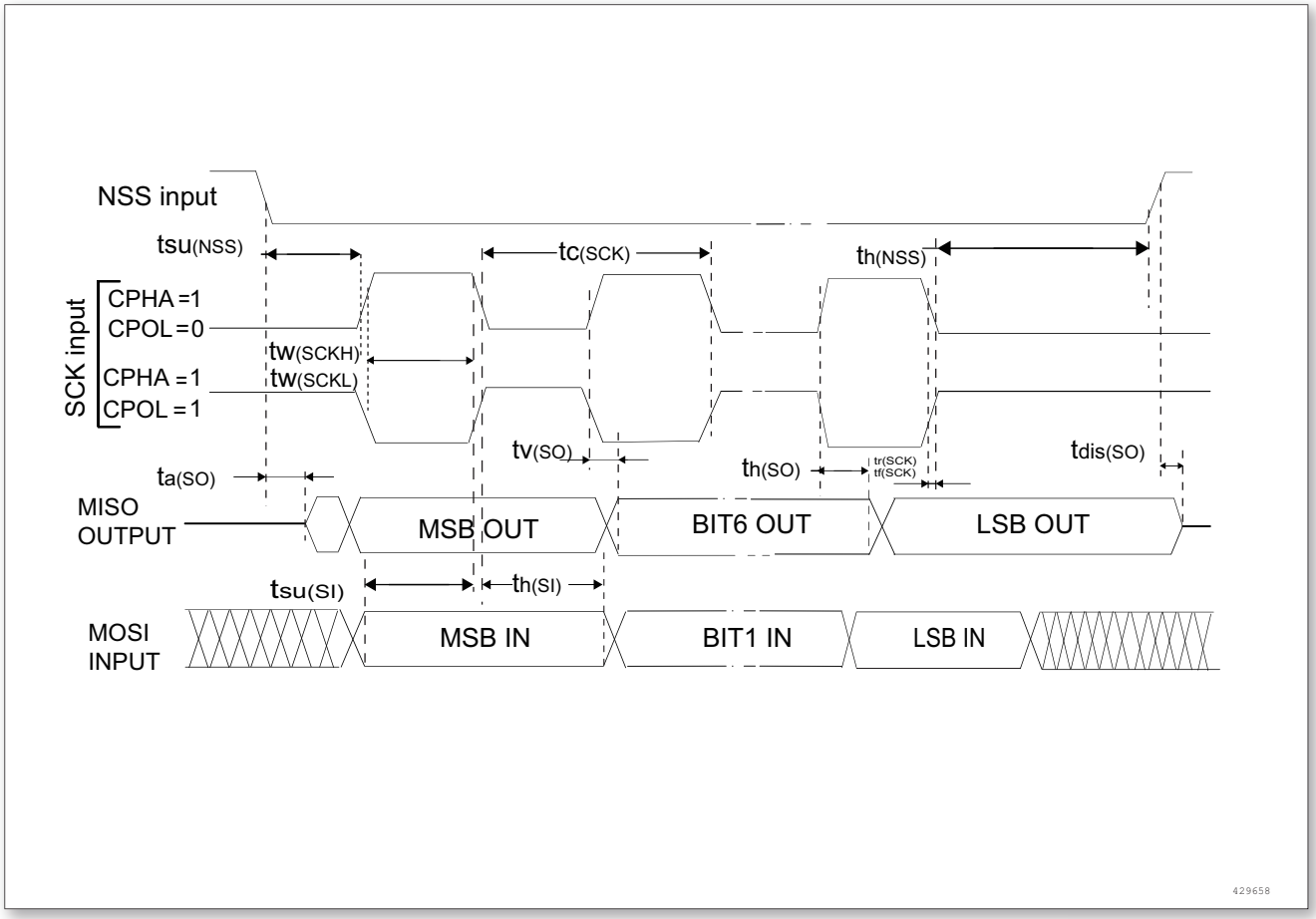

Figure 20. SPI timing diagram-slave mode and CPHA = 1(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

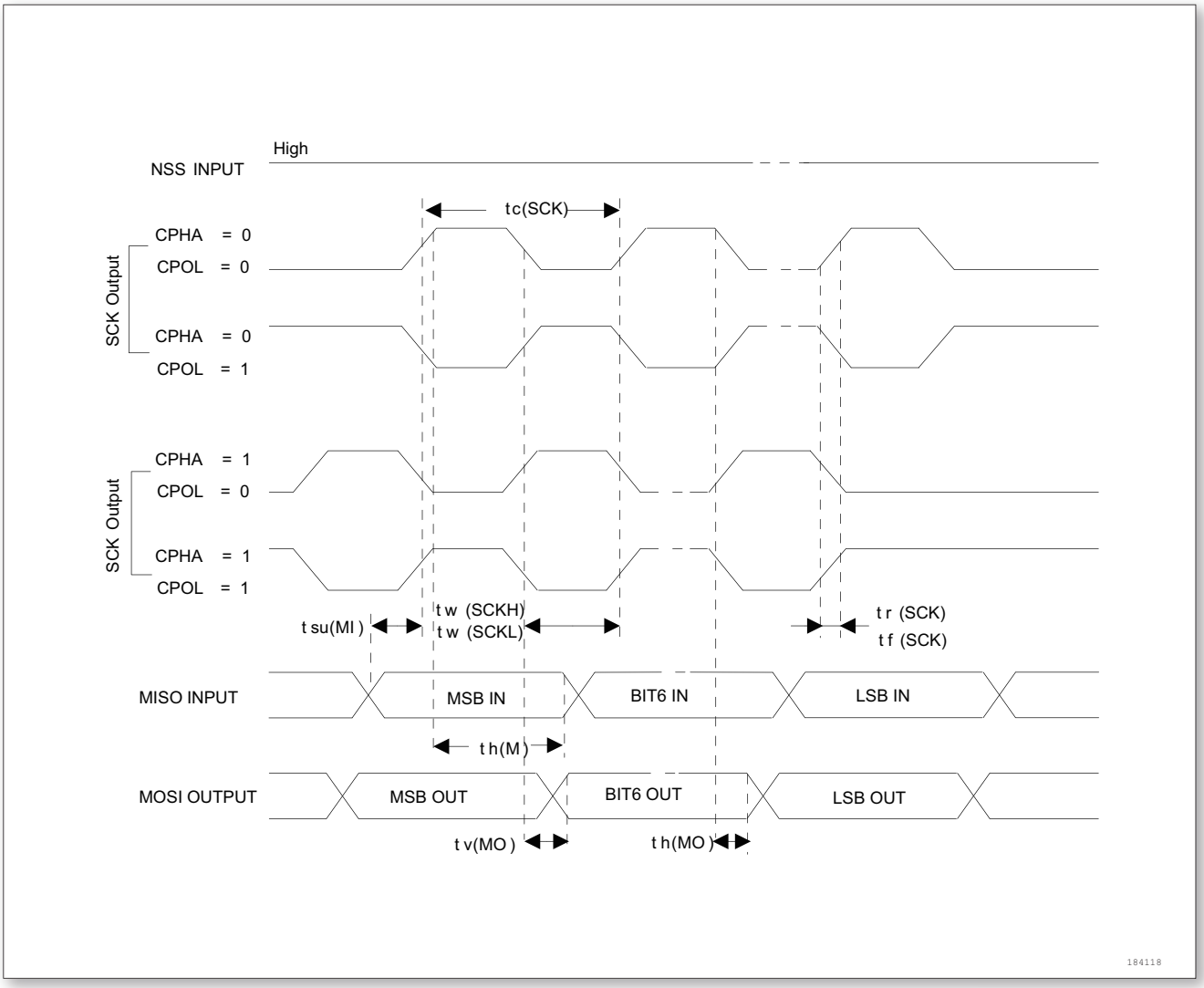

Figure 21. SPI timing diagram-master mode(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.15 12-bit ADC characteristics

Unless otherwise specified, The parameters in the table below are measured using the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions of Table 16.

Note: It is recommended to perform a calibration after each power-up

Table 40. ADC characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{DDA}	Supply voltage		2.5	3.3	5.5	V
V_{REF+}	Positive reference voltage		2.5		V_{DDA}	V

Symbol	Parameter	Conditions	Min	Type	Max	Unit
f_{ADC}	ADC clock frequency				15(1)	MHz
f_S(2)	Sampling rate				1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 15MHz			823	KHz
					1/17	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range(3)		V_{SSA}		V_{DDA}	V
R_{AIN}(2)	External sample and hold capactor		See Formulas 1 and Table 41			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor			10		pF
t_S(2)	Sampling time	f_{ADC} = 15MHz	0.1		16	μs
			1.5		239.5	MHz
t_{STAB}(2)	Stabilization time			1		μs
t_{conv}(2)	Total conversion time (including Sampling time)	f_{ADC} = 15MHz	1		16.9	μs
			15 ~ 253 (sampling t_{S+}) stepwise approximation 13.5			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design. Not tested in production.
3. In this series of products, V_{REF+} is internally connected to V_{DDA}, V_{REF-} is internally connected to V_{SSA}.

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times In(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (namely 12-bit resolution) .

Table 41. Maximum R_{AIN} at f_{ADC} = 15MHz(1)

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.1	1.2
7.5	0.5	30
13.5	0.9	57
28.5	1.9	123
41.5	2.76	180
55.5	3.7	240
71.5	4.77	312
239.5	16.0	1050

1. Guaranteed by design, not tested in production.

Table 42. ADC Accuracy - Limit Test Conditions(1)(2)

Symbol	Parameter	Test Conditions	Type	Max	Unit
ET	Comprehensive error	f_{PCLK2} = 60MHz, f_{ADC} = 15MHz, R_{AIN} < 10KΩ, V_{DDA} = 5V, T_A = 25°C	±10	±14	LSB
EO	Offset error		±4	±10	
EG	Gain error		±6	±8	
ED	Differential linearity error		±2	±4	
EL	Integral linearity error		±4	±6	

1. ADC Accuracy vs Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in subsubsec 5.3.12 does not affect the ADC accuracy.
2. Guaranteed by comprehensive evaluation, not tested in production.

ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.

EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: The deviation between the last ideal transition and the last actual transition.

ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

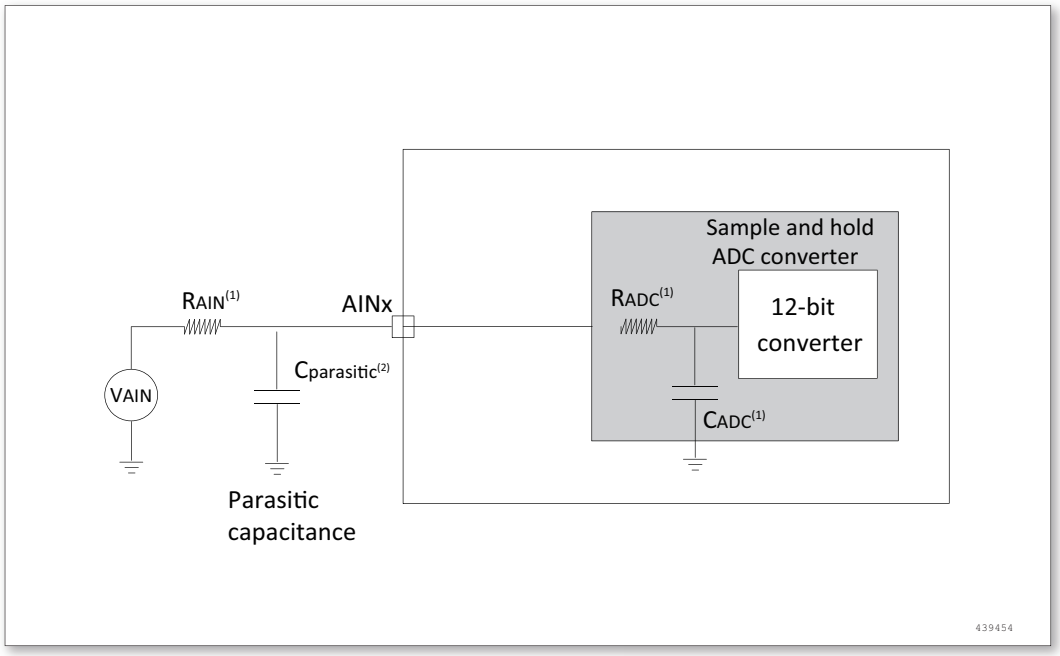

Figure 22. Typical connection diagram using the ADC

1. See Table 42 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly $7pF$) . A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The $10nF$capacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

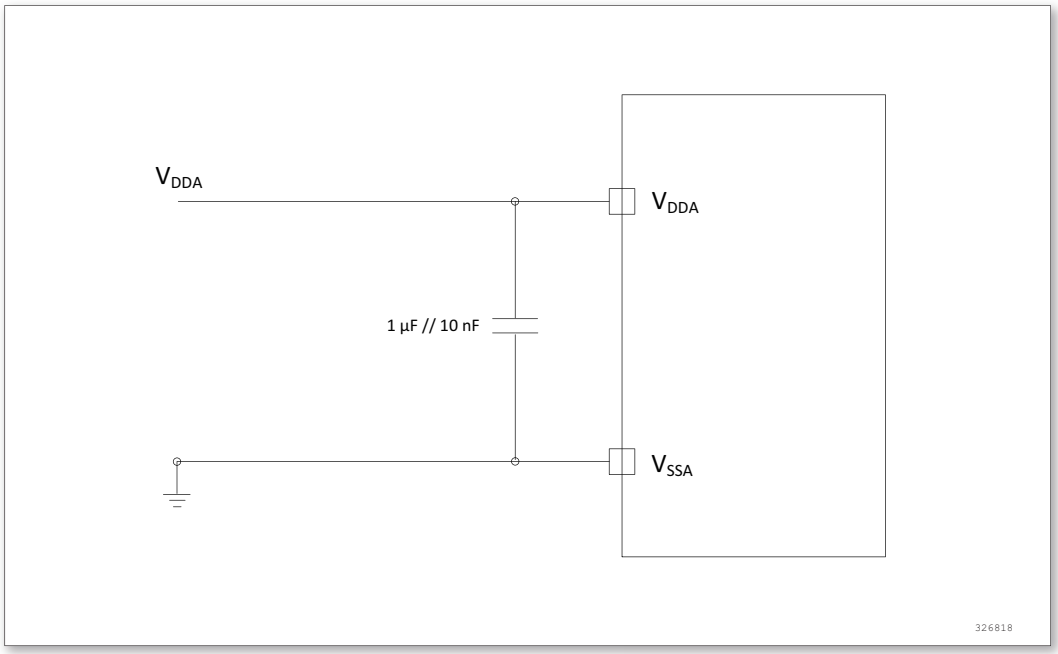

Figure 23. Power supply and reference power supply decoupling circuit

5.3.16 Temperature sensor characteristics

Table 43. Temperature sensor characteristics(3)(4)

Symbol	Parameter	Min	Type	Max	Unit
T_L (1)	V_{SENSE} linearity with respect to temperature		±5		°C
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/°C
V_{25} (1)	Voltage at 25°C	1.433	1.451	1.467	V
t_{start} (2)	Setup time			10	µs
T_{S_temp} (2)	ADC sampling time when reading temperature	10			µs

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by the application through multiple iterations.
4. V_{DD} = 3.3V.

5.3.17 Comparator characteristics

Table 44. Comparator characteristics

Symbol	Parameter	Register configuration	Min	Type	Max	Unit
HYST	Hysteresis	00		0		mV
HYST	Hysteresis	01		15		mV
HYST	Hysteresis	10		30		mV

Symbol	Parameter	Register configuration	Min	Type	Max	Unit
HYST	Hysteresis	11		90		mV
OFFSET	Offset voltage	00	0.091	0.213	0.358	mV
OFFSET	Offset voltage	01	3.23	7.51	12.08	mV
OFFSET	Offset voltage	10	9.79	15	20.8	mV
OFFSET	Offset voltage	11	34.25	47.4	62.22	mV
DELAY(1)	Propagation delay	00		80		nS
DELAY(1)	Propagation delay	01		51		nS
DELAY(1)	Propagation delay	10		26		nS
DELAY(1)	Propagation delay	11		9		nS
I_q(2)	Operating current mean	00		4.5		uA
I_q(2)	Operating current mean	01		4.4		uA
I_q(2)	Operating current mean	10		4.4		uA
I_q(2)	Operating current mean	11		4.4		uA

1. The output flips 50% of the time and the time difference between the input and the flip.
2. Total current consumption, operating current.

5.3.18 Operational amplifier characteristics

Table 45. Operational amplifier characteristics

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{DDA}	Supply voltage		2.5	3.3	5.5	V
CMIR	Common mode input range		0		V_{DDA}	V
VI_{OFFSET}	Input offset voltage			0.6		mV
I_{LOAD}	Drive current				2	mA
IDD_{OPAMP}	Current consumption	No load, static mode		1.05		mA
CMRR	Common mode rejection ratio	@1KHz		80		dB
PSRR	Power supply rejection ratio	@1KHz		76		dB
AV	Open loop gain	C_{LOAD} = 5pF		80		dB
GBW	Bandwidth gain product	C_{LOAD} = 5pF		6		MHz
PM	Phase margin	C_{LOAD} = 5pF		60		
SR	Slew resistance	C_{LOAD} = 5pF		16		V/μs
t_{WAKEUP}	From the off state to the wakeup setup time, 0.1% precision	C_{LOAD} <= 50pF, R_{LOAD} >= 4KΩ, follower structure		2		μs
R_{LOAD}	Resistive load		4			KΩ
C_{LOAD}	Capacitive load				50	pF

Symbol	Parameter	Condition	Min	Type	Max	Unit
VOH_{SAT}	High saturation output voltage	R_{LOAD} = 4KΩ, input V_{DDA}	V_{DDA} - 100			mV
		R_{LOAD} = 20KΩ, input V_{DDA}	V_{DDA} - 20			
VOL_{SAT}	Low saturation output voltage	R_{LOAD} = 4KΩ, input 0V			100	mV
		R_{LOAD} = 20KΩ, input 0V			20	
EN	Equivalent input voltage noise	@1KHz,output resistance load 4K Ω		80		$\frac{nV}{\sqrt{Hz}}$
		@10KHz,output resistance load 4K Ω		30		

1. Design assurance, the product has not been tested.
2. The load current also limits the saturated output voltage.

6 Package information

Package information

6.1 Package LQFP64

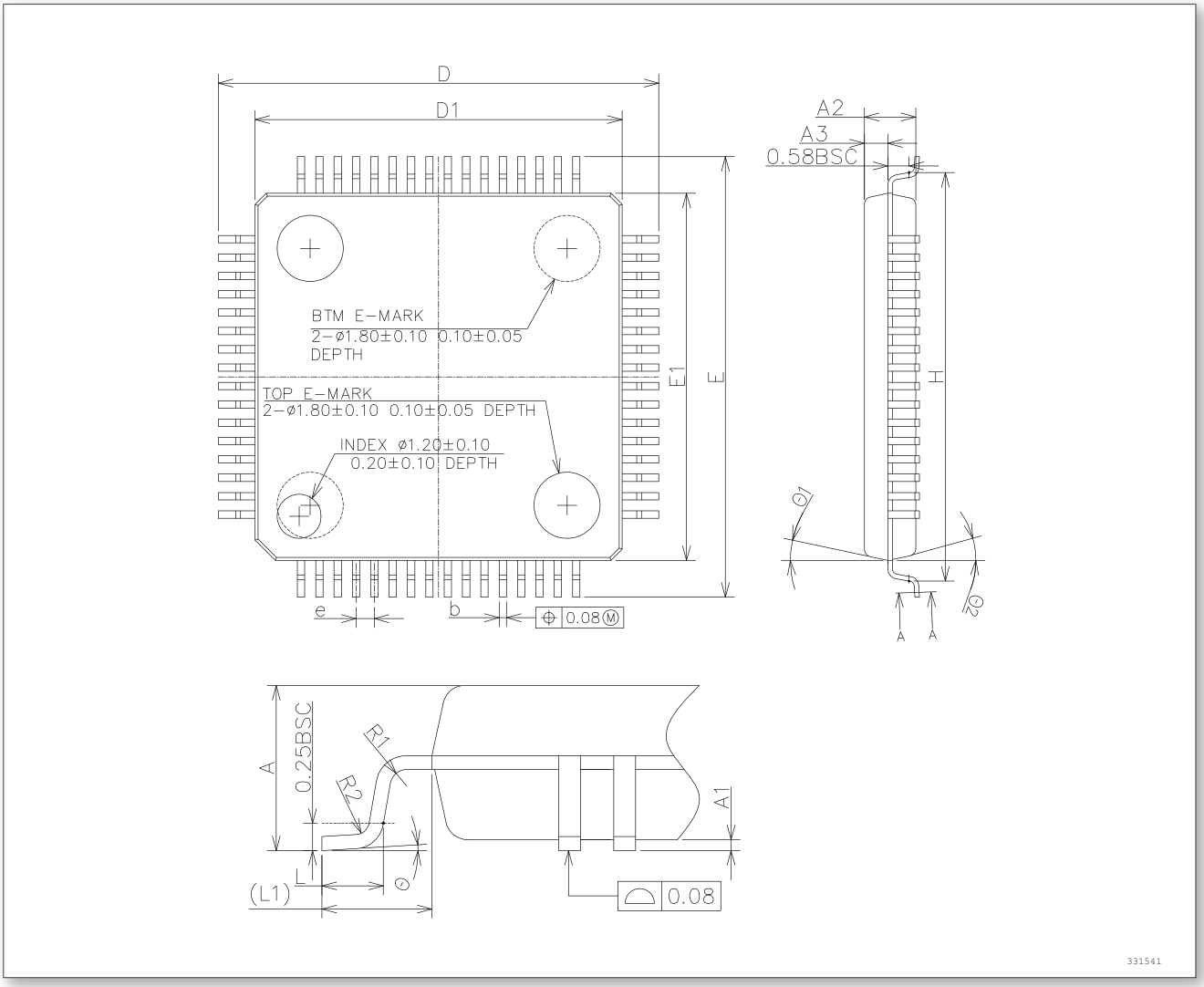

Figure 24. LQFP64, 64-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 46. LQFP64 size description

Label	MM		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0 °	3.5 °	7 °
θ1	11 °	12 °	13 °
θ2	11 °	12 °	13 °

6.2 Package LQFP48

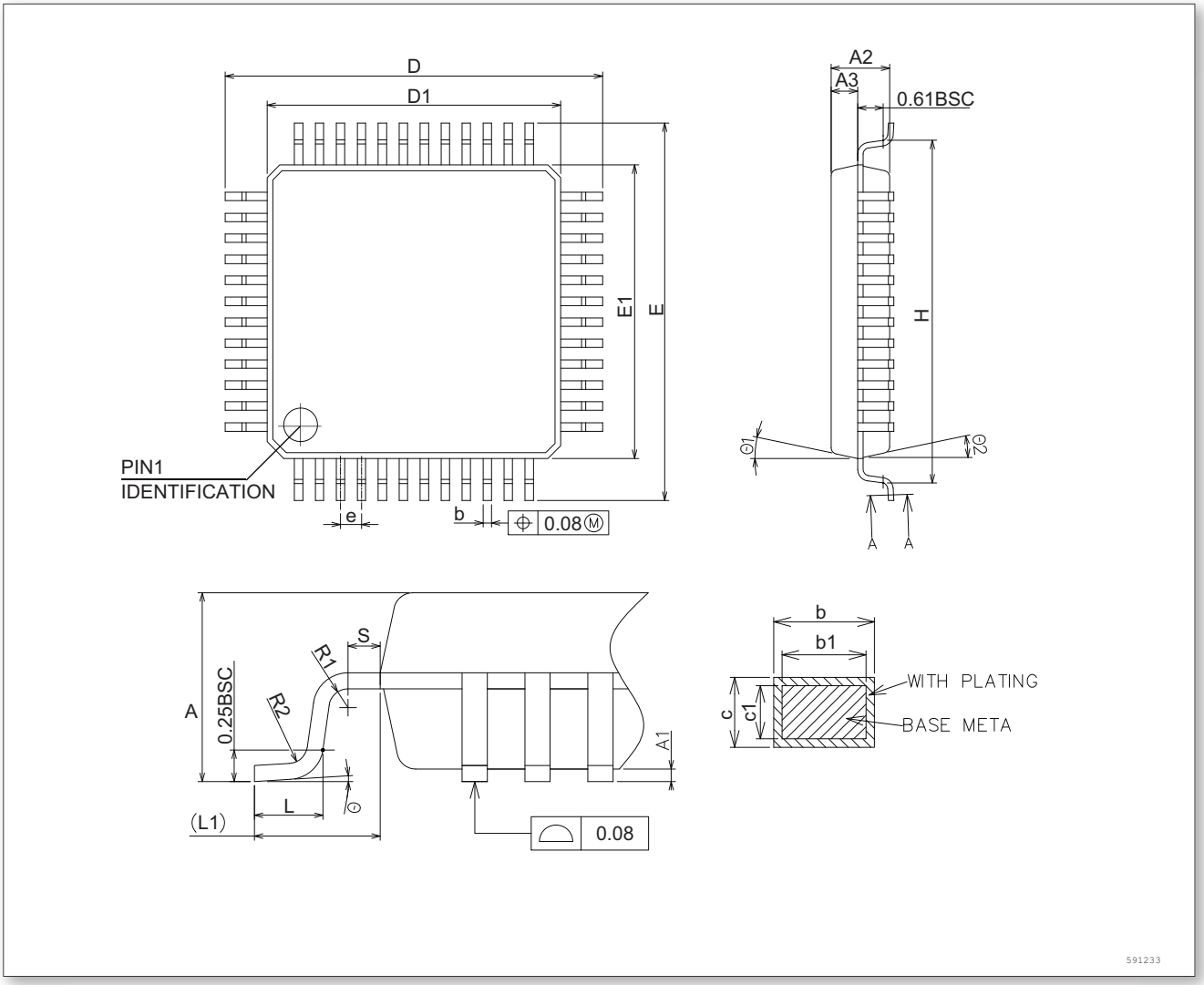

Figure 25. LQFP48, 48-pin low-profile quad square flat package

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 47. LQFP48 size description

Label	MM		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137

Label	MM		
	Min	Typ	Max
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	-	0.70
L1	1.00REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0 °	3.5 °	7 °
θ 1	11 °	12 °	13 °
θ 2	11 °	12 °	13 °

6.3 Package QFN48

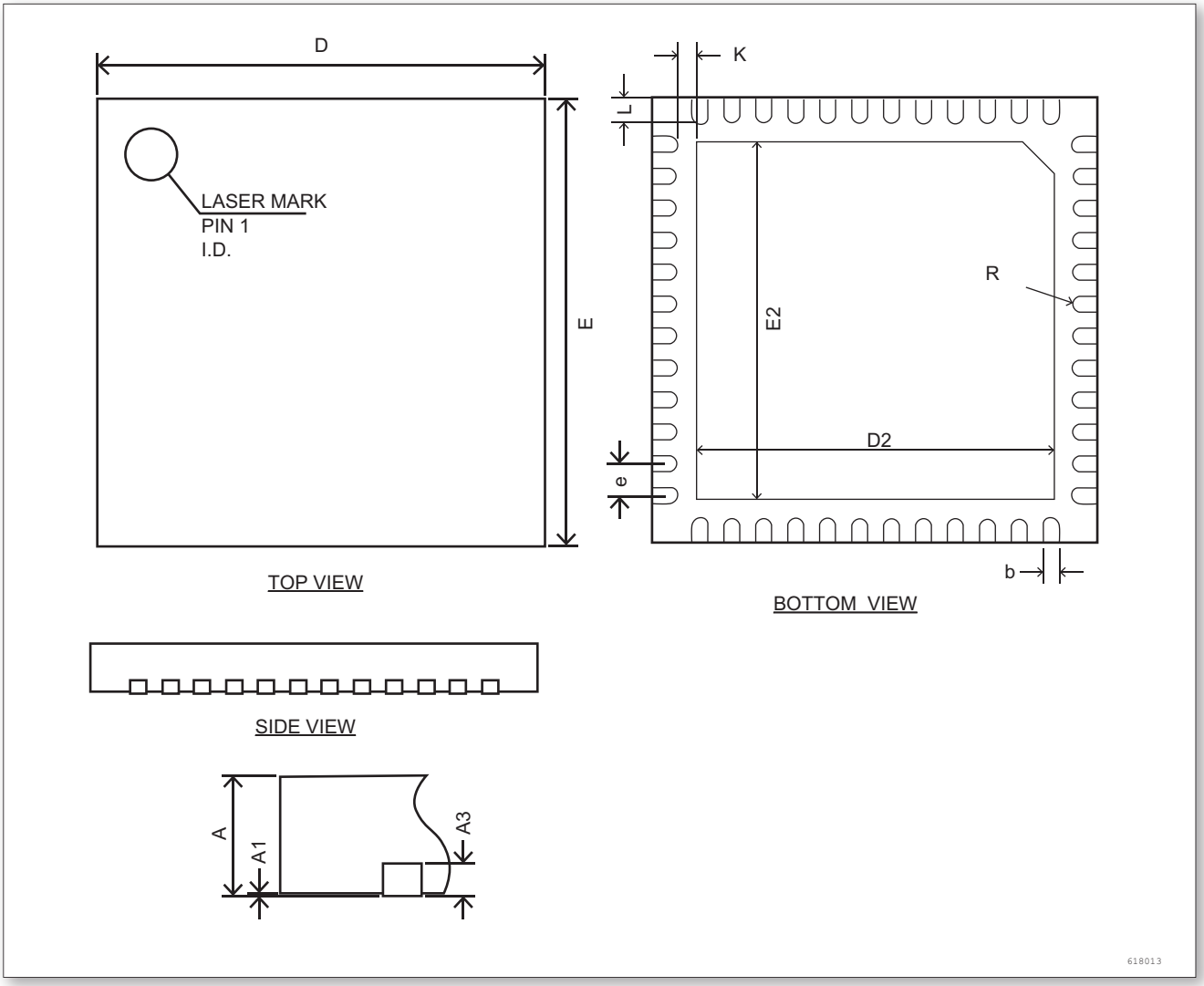

Figure 26. QFN48, 48-pin quad flat no-leads package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 48. QFN48 size description

Label	MM		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.45	5.60	5.75
E2	5.45	5.60	5.75

Label	MM		
	Min	Typ	Max
e	0.40	0.50	0.60
K	0.20	-	-
L	0.35	0.40	0.45
R	0.09	-	-
N	Number of pins = 48		

6.4 Package LQFP44

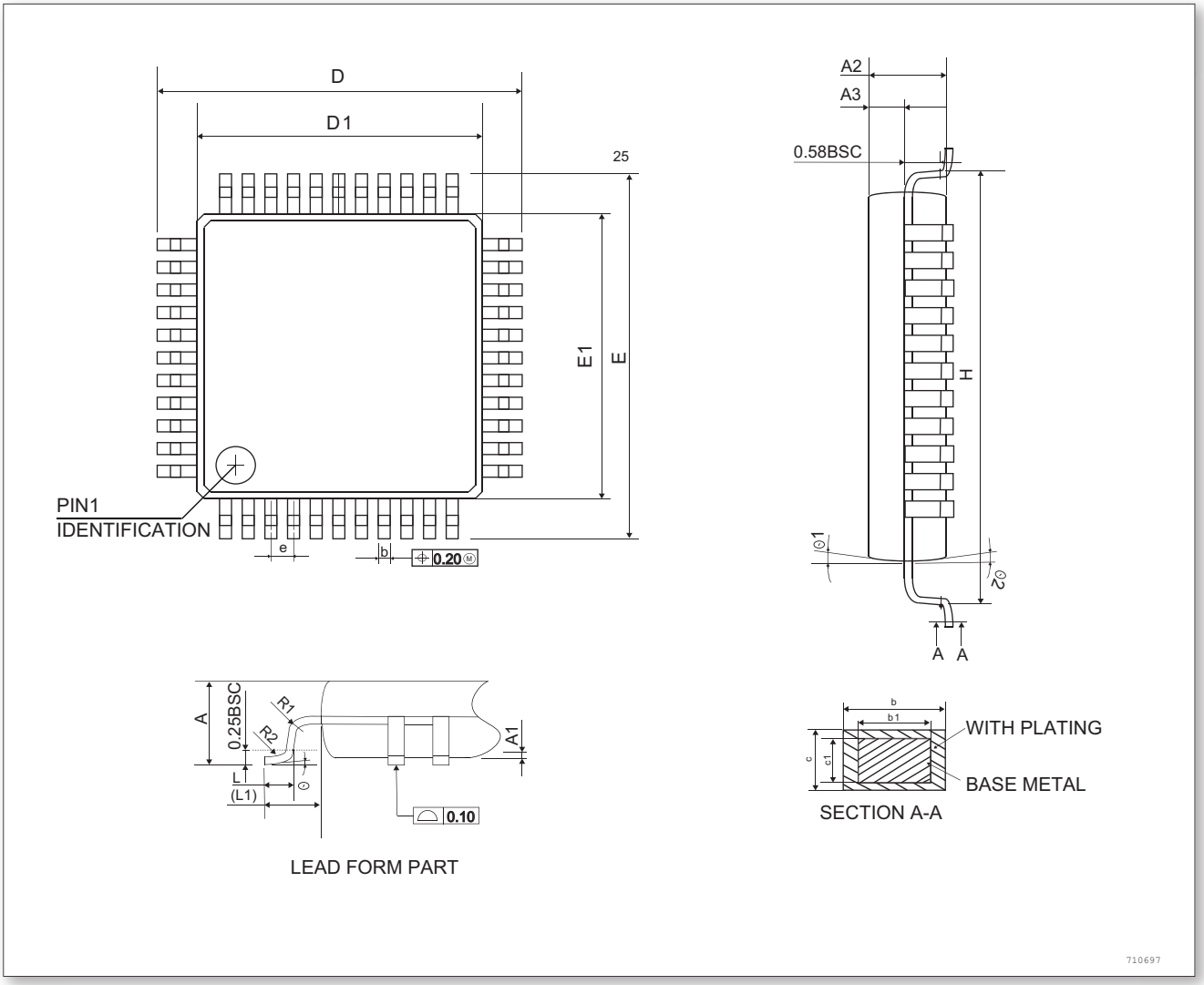

Figure 27. LQFP44, 44-pin low-profile quad square flat package

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 49. LQFP44 size description

Label	MM		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.42
b1	0.32	0.35	0.38
c	0.13	-	0.18
c1	0.117	0.127	0.137

Label	MM		
	Min	Typ	Max
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.70	0.80	0.90
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0 °	3.5 °	7 °
θ1	11 °	12 °	13 °
θ2	11 °	12 °	13 °

6.5 Package LQFP32

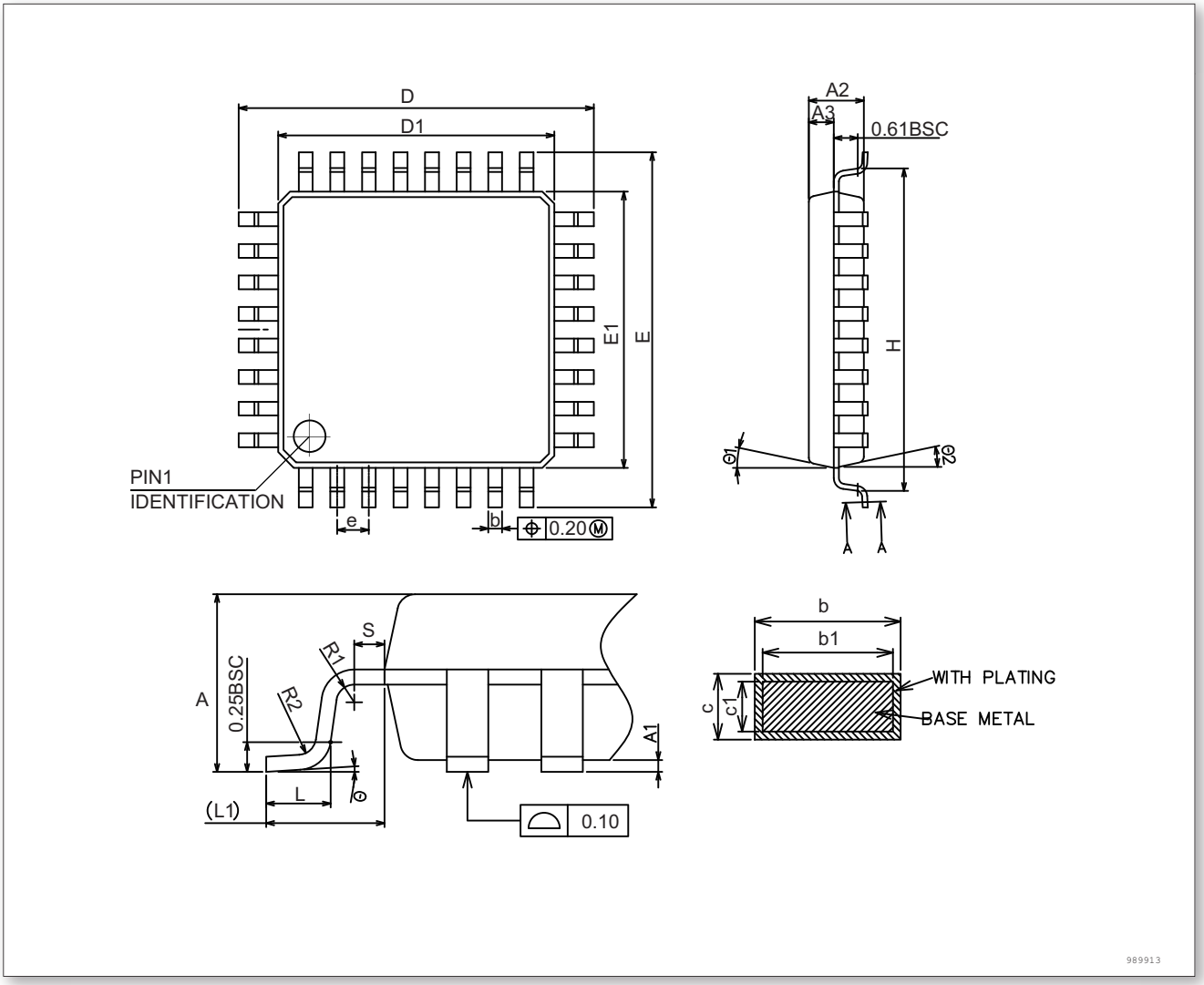

Figure 28. LQFP32, 32-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 50. LQFP32 size description

Label	MM		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.42
b1	0.32	0.35	0.38
c	0.13	-	0.18
c1	0.117	0.127	0.137

Label	MM		
	Min	Typ	Max
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50	-	0.70
L1	1.00REF		
R1	0.08		
R2	0.08		0.20
S	0.20		
θ	0 °	3.5 °	7 °
θ1	11 °	12 °	13 °
θ2	11 °	12 °	13 °

6.6 Package QFN28

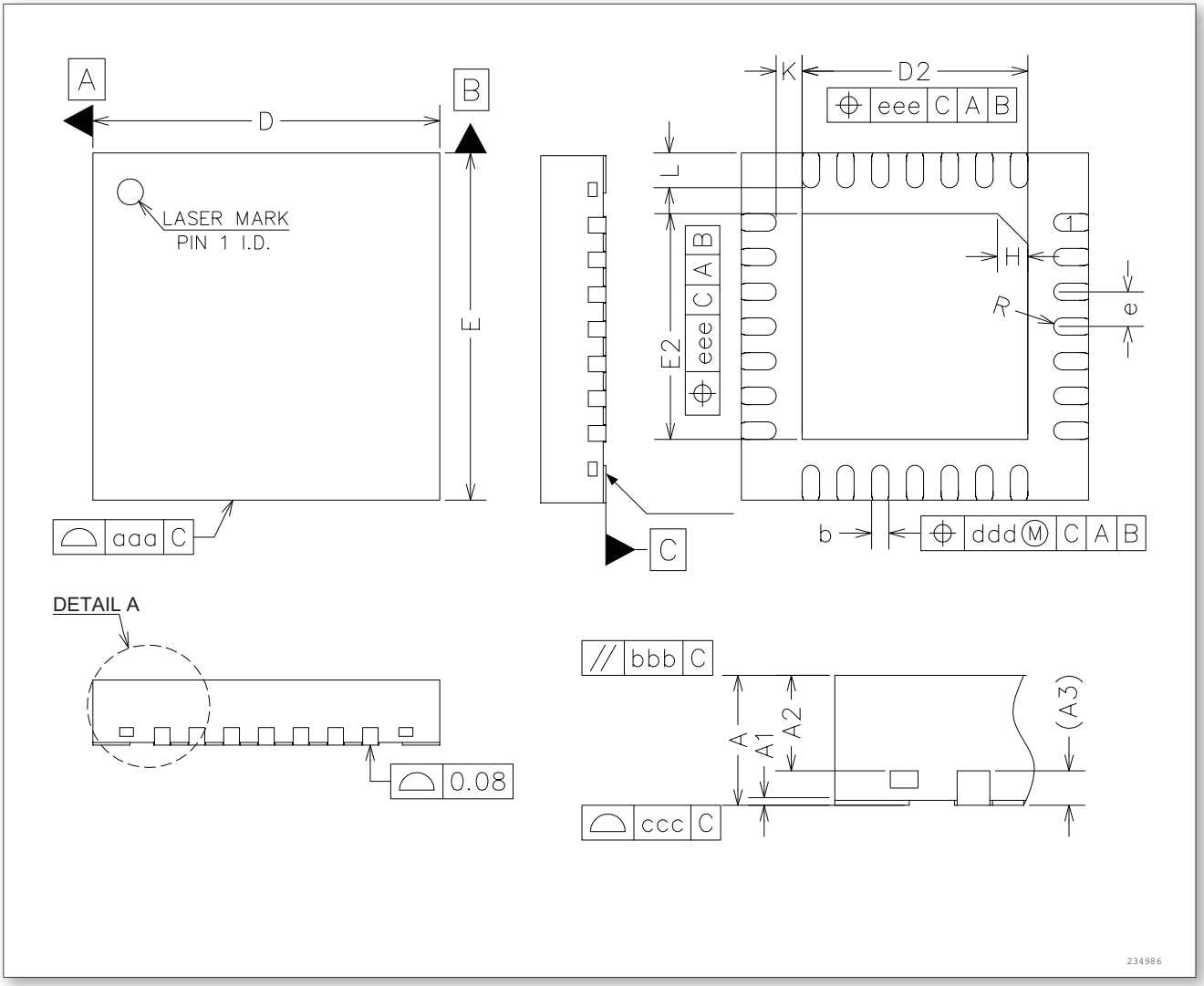

Figure 29. QFN28, 28-pin quad flat no-leads package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 51. QFN28 size description

Label	MM		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70

Label	MM		
	Min	Typ	Max
E2	2.50	2.60	2.70
e		0.40	
H		0.35REF	
k		0.30REF	
L	0.30	0.40	0.45
R	0.075		
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	
N		Number of pins = 28	

6.7 Package TSSOP20

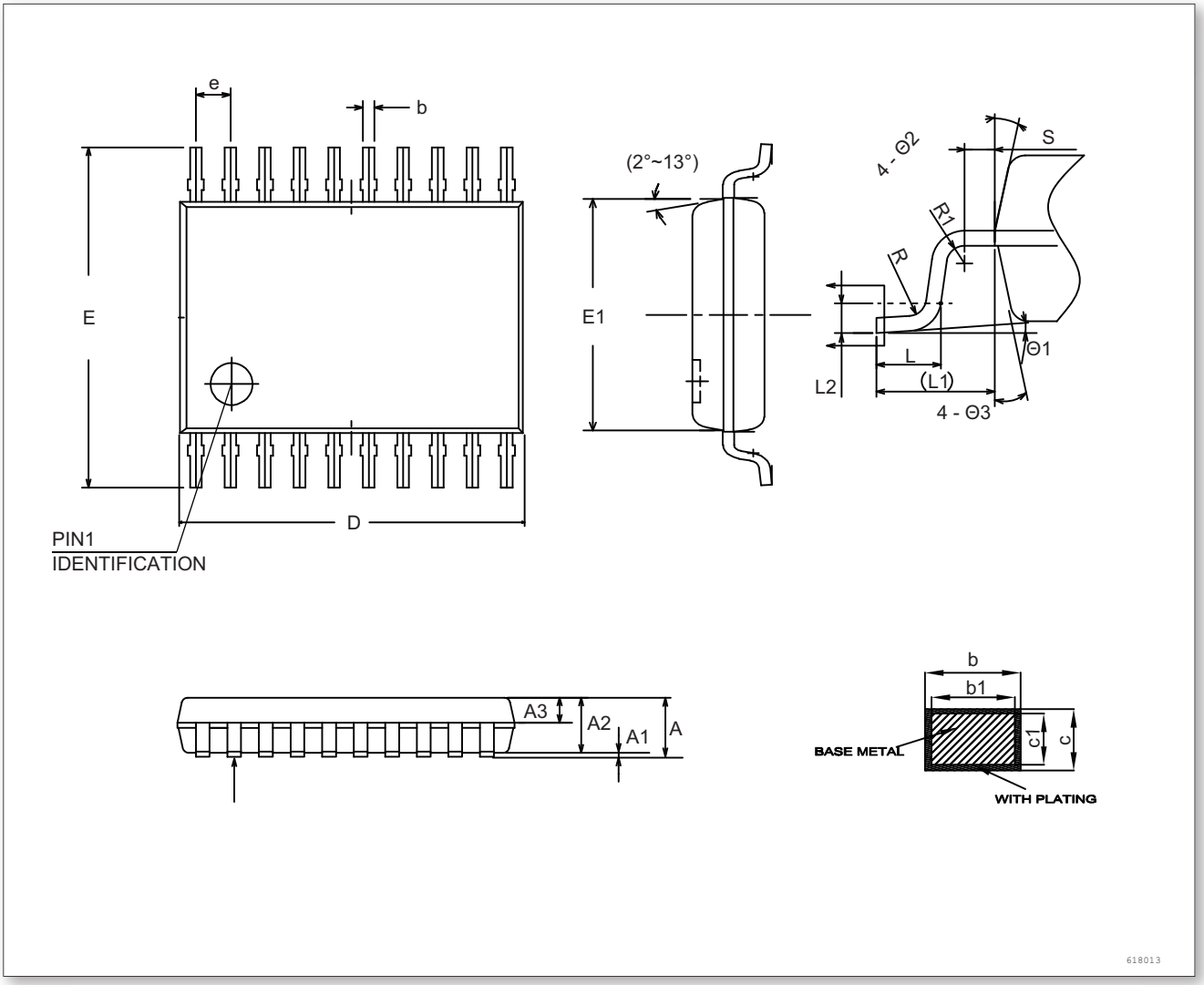

Figure 30. TSSOP20, 20-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 52. TSSOP20 size description

Label	MM		
	Min	Typ	Max
A	1.0	-	1.10
A1	0.05	-	0.15
A2	-	-	0.95
A3	0.39	-	0.40
b	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	-	0.15
D	6.40	6.45	6.50

Label	MM		
	Min	Typ	Max
E	6.25	6.40	6.55
E1	-	4.35	4.40
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L2	0.25BSC		
L1	1.0REF		
R	0.09	-	-
θ1	0 °	-	8 °

7 Ordering information

Ordering information

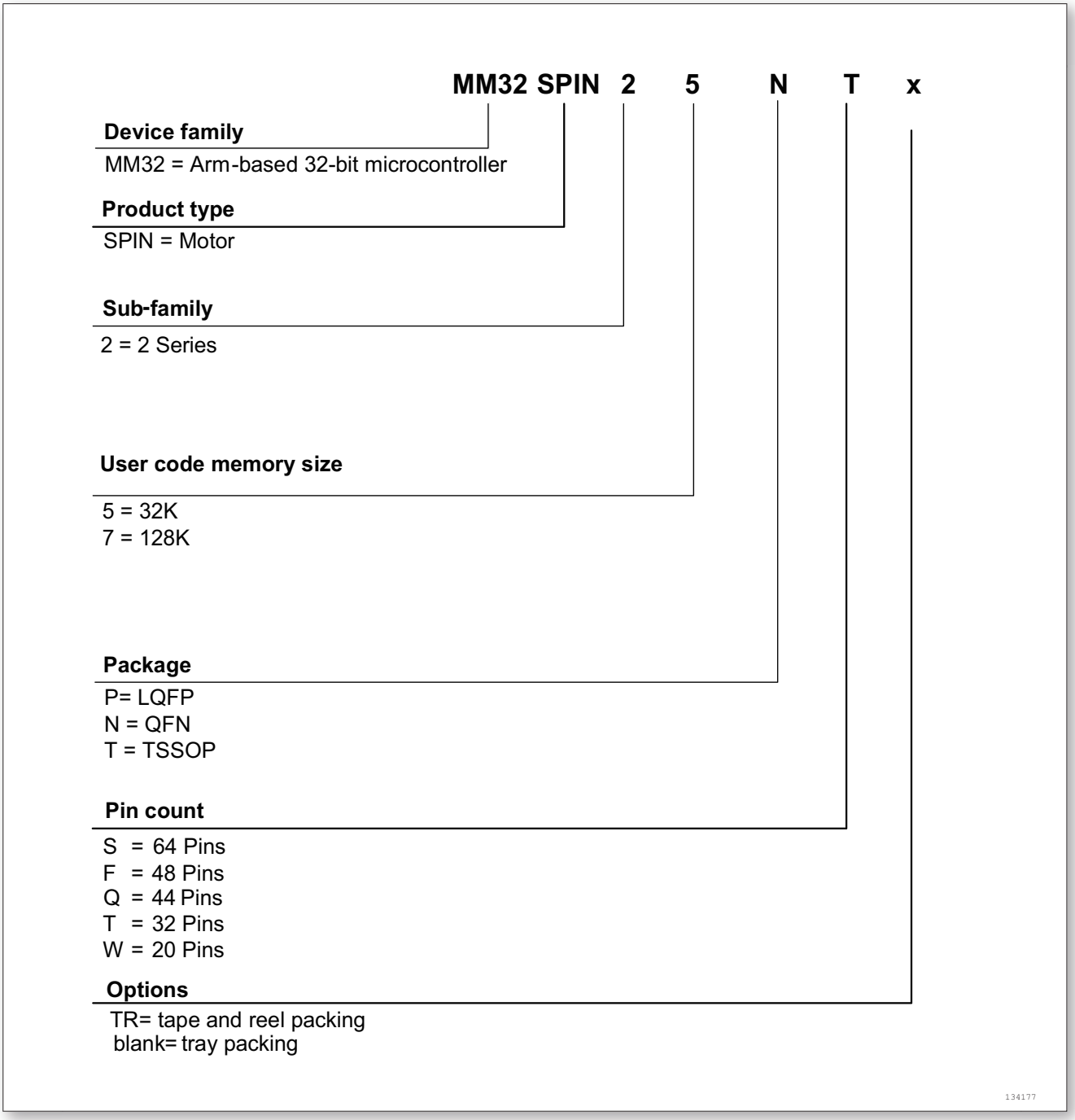

Figure 31. Ordering information scheme

8 Revision history

Revision history

Table 53. Revision history

Date	Version	Changes
2022/06/14	Rev1.21	Add annotation in table 17 and 0.1uF capacitance in NRST figure is changed into 1uF.
2022/05/30	Rev1.20	Add SPIN27TW in table 1, update IO parameters.
2022/01/20	Rev1.19	Modify the maximum value of voltage characteristics.
2021/05/19	Rev1.18	Modify electrical parameters.
2020/08/14	Rev1.17	Modify clock tree.
2020/08/14	Rev1.16	Modify clock tree.
2020/04/08	Rev1.15	Modify high-speed internal oscillator characteristic parameters.
2020/04/04	Rev1.14	Add LQFP44 package.
2019/04/02	Rev1.13	Modify pin definition.
2019/03/11	Rev1.12	Modify package parameters.
2019/01/07	Rev1.11	Modify ADC voltage parameters.
2018/12/11	Rev1.10	Modify package descriptions.
2018/11/13	Rev1.09	Modify parameters.
2018/11/12	Rev1.08	Modify descriptions.
2018/10/22	Rev1.07	Modify device contrast table.
2018/10/19	Rev1.06	Modify electrical characteristics.
2018/10/11	Rev1.05	Modify electrical parameters.
2018/09/14	Rev1.04	Modify electrical parameters.
2018/09/10	Rev1.03	Modify pin definition.
2018/08/06	Rev1.02	Add and modify product descriptions.
2018/08/01	Rev1.01	Modify header and footer.
2018/06/15	Rev1.00	Initial release.