1 Overview

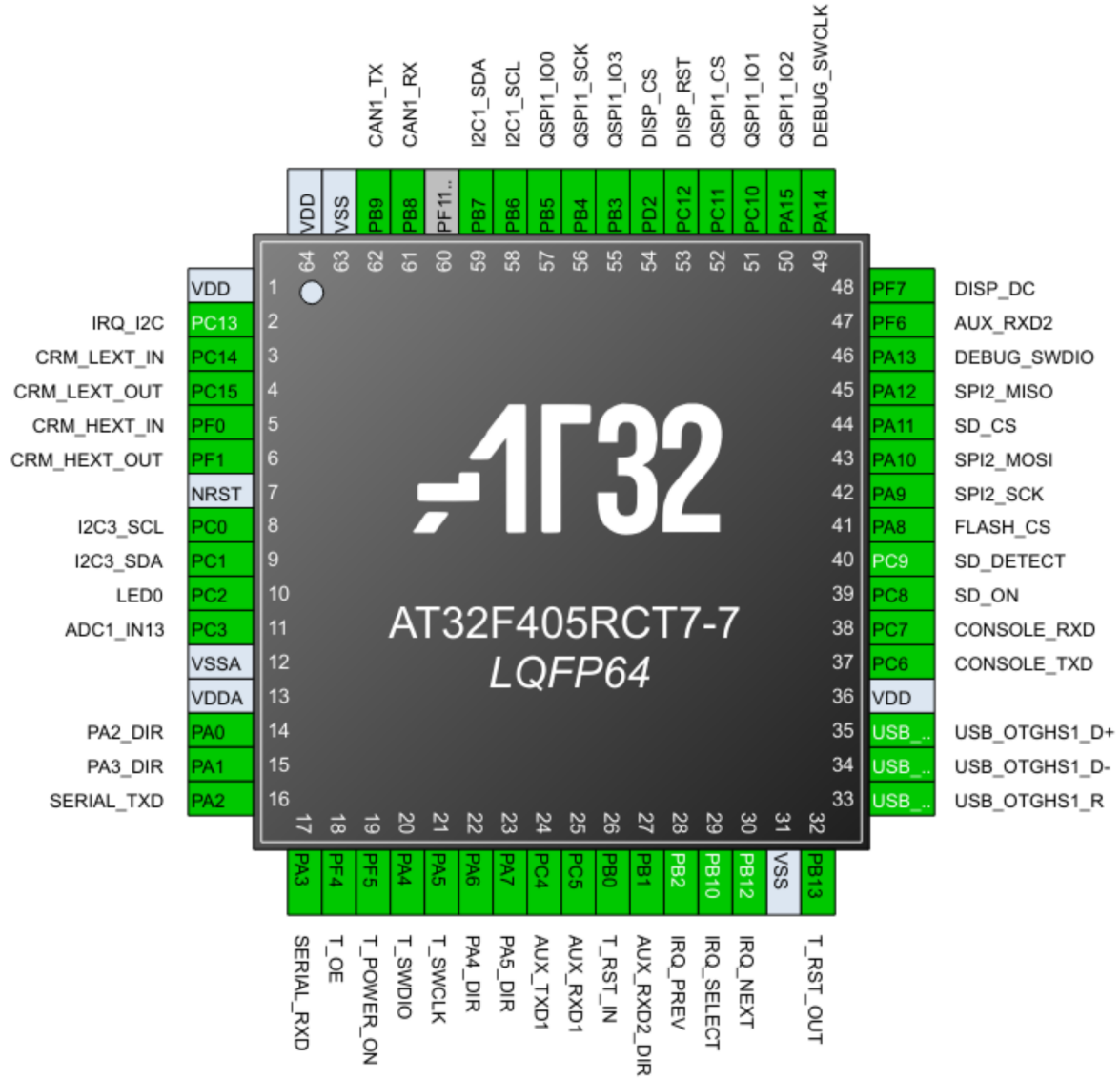
1.1 Project

Project Name	arm_can_tool_WorkBench
Generated with	AT32 WorkBench V1.2.0
Date	2025-08-25

1.2 MCU Information

Product Line	Mainstream
Device Series	AT32F405
Device	AT32F405RCT7-7
Core	M4F
Frequency	216MHz
Package	LQFP64
Flash	256KB
SRAM	102KB

2 Pinout Configuration



3 Pins Configuration

Pin Number	Pin Name	Pin Type	GPIO Structure	Signal Name	Label
1	VDD	S	-	-	
2	PC13	I/O	FT	EXINT13	IRQ_I2C
3	PC14	I/O	TC	CRM_LEXT_IN	
4	PC15	I/O	TC	CRM_LEXT_OUT	
5	PF0	I/O	TC	CRM_HEXT_IN	
6	PF1	I/O	TC	CRM_HEXT_OUT	
7	NRST	I/O	R	-	
8	PC0	I/O	FTa	I2C3_SCL	
9	PC1	I/O	FTa	I2C3_SDA	
10	PC2	I/O	FTa	GPIO_Output	LED0
11	PC3	I/O	FTa	ADC1_IN13	
12	VSSA	S	-	-	
13	VDDA	S	-	-	
14	PA0	I/O	FTa	GPIO_Output	PA2_DIR
15	PA1	I/O	FTa	GPIO_Output	PA3_DIR
16	PA2	I/O	FTa	USART2_TX	SERIAL_TXD
17	PA3	I/O	FTa	USART2_RX	SERIAL_RXD
18	PF4	I/O	FT	GPIO_Output	T_OE
19	PF5	I/O	FT	GPIO_Output	T_POWER_ON
20	PA4	I/O	FTa	GPIO_Output	T_SWDIO
21	PA5	I/O	FTa	GPIO_Output	T_SWCLK
22	PA6	I/O	FTa	GPIO_Output	PA4_DIR
23	PA7	I/O	FTa	GPIO_Output	PA5_DIR
24	PC4	I/O	FTa	USART3_TX	AUX_TXD1
25	PC5	I/O	FTa	USART3_RX	AUX_RXD1
26	PB0	I/O	FTa	GPIO_Input	T_RST_IN
27	PB1	I/O	FTa	GPIO_Output	AUX_RXD2_DIR
28	PB2	I/O	FT	EXINT2	IRQ_PREV
29	PB10	I/O	FTf	EXINT10	IRQ_SELECT
30	PB12	I/O	FT	EXINT12	IRQ_NEXT
31	VSS	S	-	-	
32	PB13	I/O	FT	GPIO_Output	T_RST_OUT
33	USB_OTGHS1_R	-	-	USB_OTGHS1_R	
34	USB_OTGHS1_D-	-	-	USB_OTGHS1_D-	
35	USB_OTGHS1_D+	-	-	USB_OTGHS1_D+	

36	VDD	S	-	-	
37	PC6	I/O	FT	USART6_TX	CONSOLE_TXD
38	PC7	I/O	FT	USART6_RX	CONSOLE_RXD
39	PC8	I/O	FT	GPIO_Output	SD_ON
40	PC9	I/O	FT	EXINT9	SD_DETECT
41	PA8	I/O	FT	GPIO_Output	FLASH_CS
42	PA9	I/O	FT	SPI2_SCK	
43	PA10	I/O	FT	SPI2_MOSI	
44	PA11	I/O	TC	GPIO_Output	SD_CS
45	PA12	I/O	TC	SPI2_MISO	
46	PA13	I/O	FT	DEBUG_SWDIO	
47	PF6	I/O	FT	UART7_RX	AUX_RXD2
48	PF7	I/O	FT	GPIO_Output	DISP_DC
49	PA14	I/O	FT	DEBUG_SWCLK	
50	PA15	I/O	FT	QSPI1_IO2	
51	PC10	I/O	FT	QSPI1_IO1	
52	PC11	I/O	FT	QSPI1_CS	
53	PC12	I/O	FT	GPIO_Output	DISP_RST
54	PD2	I/O	FT	GPIO_Output	DISP_CS
55	PB3	I/O	FTf	QSPI1_IO3	
56	PB4	I/O	FT	QSPI1_SCK	
57	PB5	I/O	FT	QSPI1_IO0	
58	PB6	I/O	FT	I2C1_SCL	
59	PB7	I/O	FT	I2C1_SDA	
61	PB8	I/O	FT	CAN1_RX	
62	PB9	I/O	FTf	CAN1_TX	
63	VSS	S	-	-	
64	VDD	S	-	-	

(1) I = input, O = output, S = supply.

(2) TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog function, FTf = 5 Vtolerant GPIO with 20 mA sink current capability, R = bidirectional reset pin with embedded weak pull-up resistor, B = dedicated BOOT0 pin with embedded weak pull-down resistor. Of those, FTa pin has 5 V-tolerant characteristics when configured as input floating, input pull-up, or input pull-down mode. However, it cannot be 5 V-tolerant when analog mode. In this case, its input level should not be higher than VDD + 0.3 V.

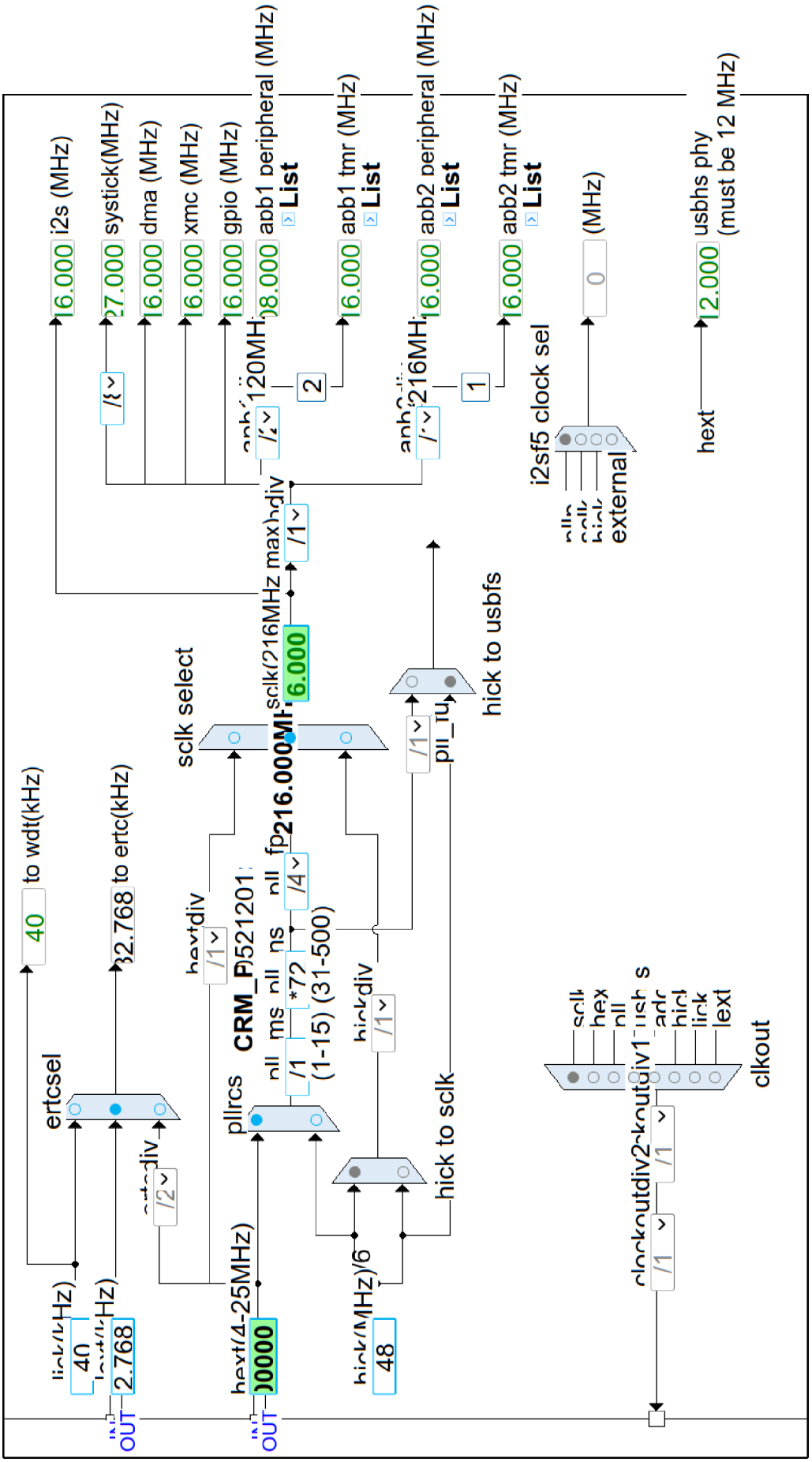
(3) EVENTOUT feature is available on any GPIO.

(4) These are dedicated to OTGHS, not sharing with GPIO or other multiplexed functions.

(5) After reset, PA13/PA14 are configured as multiplexed SWDIO/SWCLK while the internal pull-up resistor on the SWDIO pin and the internal pull-down resistor of the SWCLK pin are ON.

(6) After reset, PF11 is in input pull-down state by default, which can be configured to other states with software.

4 Clock Tree Configuration



5 Software Project

5.1 Project Settings

Name	Value
Project Name	arm_can_tool_WorkBench
Project Folder	/home/koen/src/rt-thread/bsp/at32/arm_can_tool/AT32_Work_Bench
Toolchain/IDE	
Firmware Package Name and Version	AT32F402_405_Firmware_Library_V2.1.1
Minimum Heap Size	0x200
Minimum Stack Size	0x400

6 Peripherals and Middlewares Configuration

6.1 ADC1

IN13: Enable
Temperature sensor Channel: Enable
VINTRV Channel: Enable

6.1.1 Parameter Setting

ADCs Common Settings:

Mode	Independent mode
Clock frequency division	8
Clock (0-28 MHz)	27 MHz

ADC Settings:

Data Alignment	Right alignment
Sequence Mode	Disable

ADC Ordinary Conversion Settings:

Enable Ordinary Conversions	Enable
Repeat Mode	Disable
Ordinary Partitioned Mode	Disable
Ordinary Trigger Source	software(OCSWTRG) control bit as trigger source
Number Of Ordinary Sequence (1-16)	1
Sequence 1 Channel	Channel VINTRV
Sequence 1 Sampling Time	1.5 Cycles
Sequence 1 Sampling Rate	1.929

ADC Preempted Conversion Settings:

Enable Preempted Conversions	Disable

Oversampling:

Ordinary oversampling enable	Disable

Voltage Monitoring:

Enable Voltage Monitoring	Disable

A/D Calibration:

A/D Calibration	Enable

6.2 CAN1

Activated: Enable

6.2.1 Parameter Setting

BaudRate Settings:

Baud Rate (5-1000)	500 KBits/s
Sample point (50-90)	87.5 %
BaudRate Deviation Tolerance	Disable

BaudRate Configuration Result	Result 1
Baud rate division (1-4095)	27
Bit time segment 1 (BSEG1)	6 time quantum
Bit time segment 2 (BSEG2)	1 time quantum
Resynchronization adjust width	1 time quantum

Basic Parameters:

CAN Mode	Communication mode
Time triggered communication mode	Disable
Automatic exit bus-off	Enable
Automatic exit doze mode	Enable
Prohibit retransmission when sending fails	Disable
Message discarding rule select when overflow	The previous message is discarded
Multiple message transmit sequence rule	The smallest identifier is first transmitted

Filter 0 Configuration:

Enable Filter 0	Disable

Filter 1 Configuration:

Enable Filter 1	Disable

Filter 2 Configuration:

Enable Filter 2	Disable

Filter 3 Configuration:

Enable Filter 3	Disable

Filter 4 Configuration:

Enable Filter 4	Disable

Filter 5 Configuration:

Enable Filter 5	Disable

Filter 6 Configuration:

Enable Filter 6	Disable

Filter 7 Configuration:

Enable Filter 7	Disable

Filter 8 Configuration:

Enable Filter 8	Disable

Filter 9 Configuration:

Enable Filter 9	Disable

Filter 10 Configuration:

Enable Filter 10	Disable

Filter 11 Configuration:

Enable Filter 11	Disable

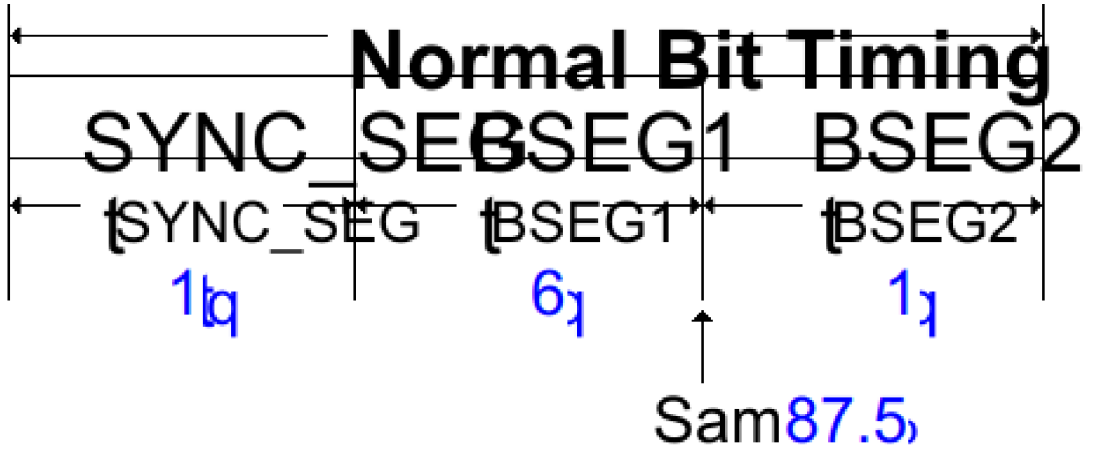
Filter 12 Configuration:

Enable Filter 12	Disable

Filter 13 Configuration:

Enable Filter 13	Disable

6.2.2 Sequence Diagram



6.3 CRC

Activated: Enable

6.3.1 Parameter Setting

Basic Parameters:

Init Value For CRC computation (0x0-0xFFFFFFFF)	0xFFFFFFFF
CRC Polynomial Length	32-bit
CRC Polynomial Value (0x0-0xFFFFFFFF)	0x04C11DB7

Advanced Parameters:

Input Data Reverse Mode	None Reverse
Output Data Reverse Mode	None Reverse

6.4 CRM

High speed external crystal (HEXT): Crystal/Ceramic Resonator
Low speed external crystal (LEXT): Crystal/Ceramic Resonator

6.5 DEBUG

SWD: Enable

6.6 ERTC

Activate Clock Source: Enable

6.6.1 Parameter Setting

General:

Hour Format	Hourformat 24
Predivider A value (0-127)	127
Predivider B value (0-32767)	255

6.7 EXINT

EXINT2: Enable
EXINT9: Enable
EXINT10: Enable
EXINT12: Enable
EXINT13: Enable

6.7.1 Parameter Setting

EXINT2:

Interrupt/Event	Interrupt
Trigger Polarity	Rising Edge

EXINT9:

Interrupt/Event	Interrupt
Trigger Polarity	Rising Edge

EXINT10:

Interrupt/Event	Interrupt
Trigger Polarity	Rising Edge

EXINT12:

Interrupt/Event	Interrupt
Trigger Polarity	Rising Edge

EXINT13:

Interrupt/Event	Interrupt
Trigger Polarity	Rising Edge

6.8 I2C1

I2C: I2C

6.8.1 Parameter Setting

Clock Features:

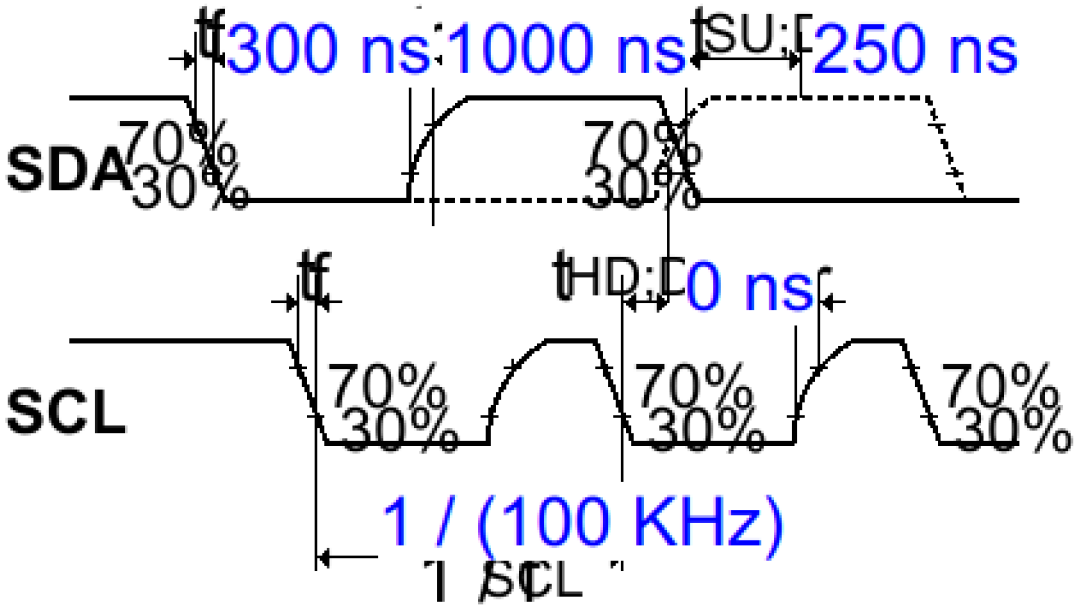
I2C Speed Mode (tSU)	Standard Mode
I2C Clock Speed (fSCL) (KHz) (1-100)	100
Digital Filter (0-15)	0
Rise Time (tr) (ns) (0-1000)	1000
Fall Time (tf) (ns) (0-300)	300
Timing Configuration Value	0x90F02F2F

Slave Features:

Clock Stretch Mode	Enable

Address mode	7-bit
Dual Address mode	Disable
Own address 1 (0x0-0x7F)	0x0
General Call address detection	Disable

6.8.2 Sequence Diagram



6.9 I2C3

I2C: I2C

6.9.1 Parameter Setting

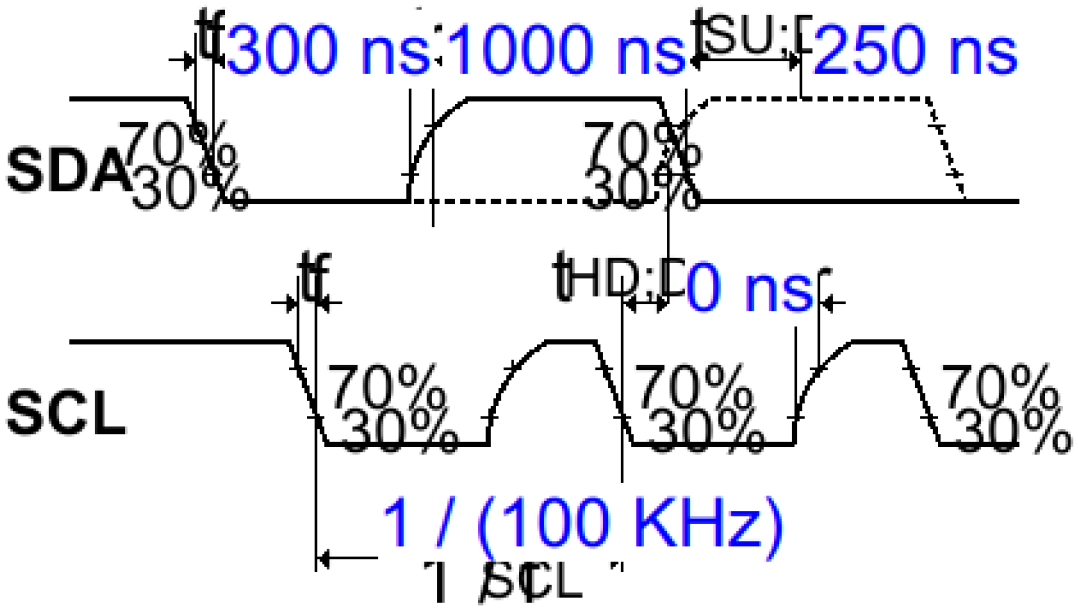
Clock Features:

I2C Speed Mode (tSU)	Standard Mode
I2C Clock Speed (fSCL) (KHz) (1-100)	100
Digital Filter (0-15)	0
Rise Time (tr) (ns) (0-1000)	1000
Fall Time (tf) (ns) (0-300)	300
Timing Configuration Value	0x90F02F2F

Slave Features:

Clock Stretch Mode	Enable
Address mode	7-bit
Dual Address mode	Disable
Own address 1 (0x0-0x7F)	0x0
General Call address detection	Disable

6.9.2 Sequence Diagram



6.10 QSPI1

Activated: Enable

6.10.1 Parameter Setting

Clock Parameters:

Clock frequency division	8
Clock frequency (0-108 MHz)	27 MHz
SCK mode	Mode 0

Basic Parameters:

XIP/CMD port switch selection	XIP Port
Busy offset config	Offset 0 bit
DMA RX threshold	FIFO threshold 8 words
DMA TX threshold	FIFO threshold 8 words
XIP cache enable	Enable
Encryption enable	Disable

6.11 SPI2

Mode: Full-Duplex Master

6.11.1 Parameter Setting

Basic Parameters:

Interface protocol	Motorola Mode
Frame bit num	8 Bits

First Bit	MSB First

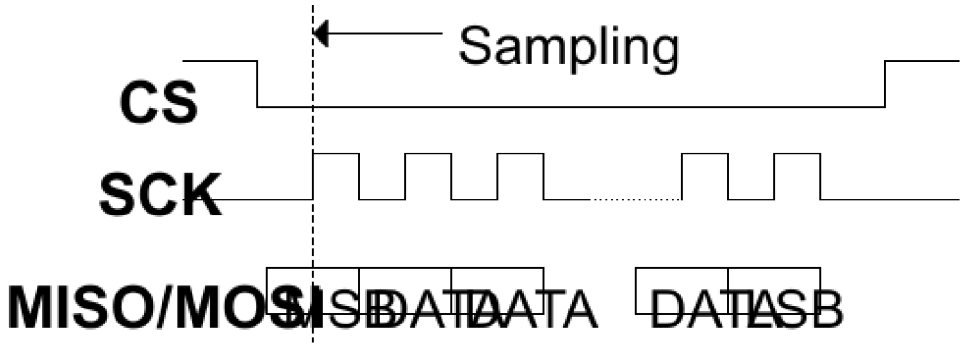
Clock Parameters:

Clock frequency division	3
Clock frequency (0-36 MHz)	36 MHz
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disable
CS Signal Type	Software

6.11.2 Sequence Diagram



6.12 SYSTEM

Delay Timebase Source: SysTick

6.12.1 Parameter Setting

Timebase Parameters:

Delay Mode	Polling

6.13 TMR1

Activated: Enable

6.13.1 Parameter Setting

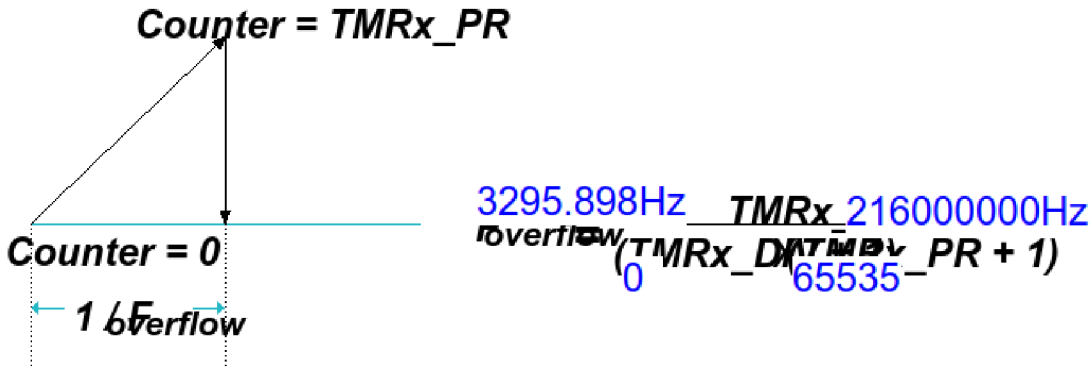
Counter Settings:

Divider value (16 bits value) (0-65535)	0
Counter Direction	Up
Period Value (16 bits value) (0-65535)	65535
Clock divider	No Divider
Repetition of period value (16 bits value) (0-65535)	0
Period buffer enable	Disable
Overflow Event	From counter/ovfswtr/sub-timer

Primary mode settings:

Synchronize with sub-timer	Disable
Primary TMR output selection	Reset

6.13.2 Sequence Diagram



6.14 TMR11

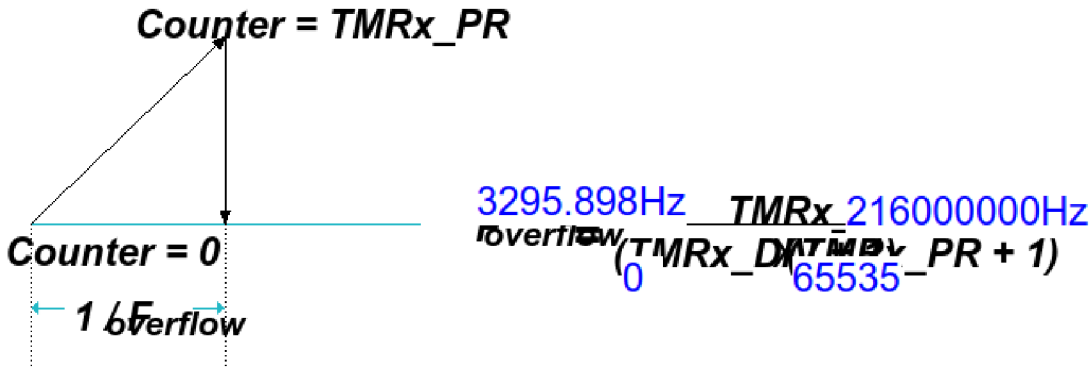
Activated: Enable

6.14.1 Parameter Setting

Counter Settings:

Divider value (16 bits value) (0-65535)	0
Counter Direction	Up
Period Value (16 bits value) (0-65535)	65535
Clock divider	No Divider
Repetition of period value (8 bits value) (0-255)	0
Period buffer enable	Disable
Overflow Event	From counter/ovfswtr/sub-timer

6.14.2 Sequence Diagram



6.15 USART2

Mode: Asynchronous

6.15.1 Parameter Setting

Basic Parameters:

Baud Rate (1647-6750000)	115200 Bits/s
Real Baud Rate	115139 Bits/s
Data bit num	8 Bits (including Parity)
Parity selection	None
STOP bit num	1

Advanced Parameters:

Data Direction	Receive and Transmit

Advanced Features:

TX polarity reverse	Disable
RX polarity reverse	Disable
TX and RX Pins Swapping	Disable
DT register polarity reverse	Disable
MSB transmit first	Disable

6.16 USART3

Mode: Asynchronous

6.16.1 Parameter Setting

Basic Parameters:

Baud Rate (1647-6750000)	115200 Bits/s
Real Baud Rate	115139 Bits/s
Data bit num	8 Bits (including Parity)
Parity selection	None
STOP bit num	1

Advanced Parameters:

Data Direction	Receive and Transmit

Advanced Features:

TX polarity reverse	Disable
RX polarity reverse	Disable
TX and RX Pins Swapping	Disable
DT register polarity reverse	Disable
MSB transmit first	Disable

6.17 USART6

Mode: Asynchronous

6.17.1 Parameter Setting

Basic Parameters:

Baud Rate (3295-13500000)	115200 Bits/s
Real Baud Rate	115200 Bits/s

Data bit num	8 Bits (including Parity)
Parity selection	None
STOP bit num	1

Advanced Parameters:

Data Direction	Receive and Transmit

Advanced Features:

TX polarity reverse	Disable
RX polarity reverse	Disable
TX and RX Pins Swapping	Disable
DT register polarity reverse	Disable
MSB transmit first	Disable

6.18 UART7

Mode: Asynchronous Receive Only

6.18.1 Parameter Setting

Basic Parameters:

Baud Rate (1647-6750000)	115200 Bits/s
Real Baud Rate	115139 Bits/s
Data bit num	8 Bits (including Parity)
Parity selection	None
STOP bit num	1

Advanced Parameters:

Data Direction	Receive Only

Advanced Features:

RX polarity reverse	Disable
TX and RX Pins Swapping	Disable
DT register polarity reverse	Disable
MSB transmit first	Disable

6.19 USB_OTGHS1

Mode: Device Only

6.20 USB_DEVICE

OTGHS1 Device Class: Winusb

6.20.2 HS Device Descriptor

HS Device Descriptor config:

USB VID (0x0-0xFFFF)	0x2E3C

USB PID (0x0-0xFFFF)	0x5780
Manufacturer string	Artery
Product string	AT32 WinUSB
Configuration string	WinUSB Config
Interface string	WinUSB Interface

HS Endpoint FIFO Size config:

Receive FIFO Size(word) (0-1024)	256
IN Endpoint 0 Transmit FIFO Size(word) (0-1024)	64
IN Endpoint 1 Transmit FIFO Size(word) (0-1024)	256
IN Endpoint 2 Transmit FIFO Size(word) (0-1024)	20
IN Endpoint 3 Transmit FIFO Size(word) (0-1024)	0
IN Endpoint 4 Transmit FIFO Size(word) (0-1024)	0
IN Endpoint 5 Transmit FIFO Size(word) (0-1024)	0
IN Endpoint 6 Transmit FIFO Size(word) (0-1024)	0
IN Endpoint 7 Transmit FIFO Size(word) (0-1024)	0

7 System Configuration

7.1 GPIO Configuration

IP	Pin Name	Signal	Output level	GPIO type	Pull type	GPIO mode	Driver capability	Label
ADC1	PC3	ADC1_IN13	n/a	n/a	Pull-none	Analog mode	n/a	
CAN1	PB8	CAN1_RX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PB9	CAN1_TX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
CRM	PC14	CRM_LEXT_IN	n/a	n/a	n/a	n/a	n/a	
	PC15	CRM_LEXT_OUT	n/a	n/a	n/a	n/a	n/a	
	PF0	CRM_HEXT_IN	n/a	n/a	n/a	n/a	n/a	
	PF1	CRM_HEXT_OUT	n/a	n/a	n/a	n/a	n/a	
DEBUG	PA13	DEBUG_SWDIO	n/a	n/a	n/a	n/a	n/a	
	PA14	DEBUG_SWCLK	n/a	n/a	n/a	n/a	n/a	
EXINT	PC13	EXINT13	n/a	n/a	Pull-none	Input mode	n/a	IRQ_I2C
	PB2	EXINT2	n/a	n/a	Pull-none	Input mode	n/a	IRQ_PREV
	PB10	EXINT10	n/a	n/a	Pull-none	Input mode	n/a	IRQ_SELECT
	PB12	EXINT12	n/a	n/a	Pull-none	Input mode	n/a	IRQ_NEXT
	PC9	EXINT9	n/a	n/a	Pull-none	Input mode	n/a	SD_DETECT
I2C1	PB6	I2C1_SCL	n/a	Open Drain	Pull-none	Mux function mode	Moderate	
	PB7	I2C1_SDA	n/a	Open Drain	Pull-none	Mux function mode	Moderate	
I2C3	PC0	I2C3_SCL	n/a	Open Drain	Pull-none	Mux function mode	Moderate	
	PC1	I2C3_SDA	n/a	Open Drain	Pull-none	Mux function mode	Moderate	
QSPI1	PA15	QSPI1_IO2	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PC10	QSPI1_IO1	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PC11	QSPI1_CS	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PB3	QSPI1_IO3	n/a	Push Pull	Pull-none	Mux function mode	Moderate	

QSPI1	PB4	QSPI1_SCK	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PB5	QSPI1_IO0	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
SPI2	PA9	SPI2_SCK	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PA10	SPI2_MOSI	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PA12	SPI2_MISO	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
USART2	PA2	USART2_TX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	SERIAL_TXD
	PA3	USART2_RX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	SERIAL_RXD
USART3	PC4	USART3_TX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	AUX_TXD1
	PC5	USART3_RX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	AUX_RXD1
USART6	PC6	USART6_TX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	CONSOLE_TXD
	PC7	USART6_RX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	CONSOLE_RXD
UART7	PF6	UART7_RX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	AUX_RXD2
USB_OTGHS1	USB_OTGHS1_R	USB_OTGHS1_R	n/a	n/a	n/a	n/a	n/a	
	USB_OTGHS1_D-	USB_OTGHS1_D-	n/a	n/a	n/a	n/a	n/a	
	USB_OTGHS1_D+	USB_OTGHS1_D+	n/a	n/a	n/a	n/a	n/a	
GPIO	PC2	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	LED0
	PA0	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	PA2_DIR
	PA1	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	PA3_DIR
	PF4	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	T_OE
	PF5	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	T_POWER_ON
	PA4	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	T_SWDIO
	PA5	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	T_SWCLK
	PA6	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	PA4_DIR
	PA7	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	PA5_DIR

GPIO	PB0	GPIO_Input	n/a	n/a	Pull-none	Input mode	n/a	T_RST_IN
	PB1	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	AUX_RXD2_DIR
	PB13	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	T_RST_OUT
	PC8	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	SD_ON
	PA8	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	FLASH_CS
	PA11	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	SD_CS
	PF7	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	DISP_DC
	PC12	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	DISP_RST
	PD2	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	DISP_CS

7.2 DMA Configuration

DMA Request	Channel	Direction	Priority
SPI2_RX	DMA1 Channel 3	Peripheral To Memory	Low
SPI2_TX	DMA1 Channel 4	Memory To Peripheral	Low
I2C1_RX	DMA2 Channel 3	Peripheral To Memory	Low
I2C1_TX	DMA2 Channel 4	Memory To Peripheral	Low
I2C3_RX	DMA2 Channel 5	Peripheral To Memory	Low
I2C3_TX	DMA2 Channel 6	Memory To Peripheral	Low
USART2_RX	DMA1 Channel 1	Peripheral To Memory	Low
USART2_TX	DMA1 Channel 2	Memory To Peripheral	Low
USART3_RX	DMA2 Channel 1	Peripheral To Memory	Low
USART3_TX	DMA2 Channel 2	Memory To Peripheral	Low
USART6_RX	DMA1 Channel 5	Peripheral To Memory	Low
USART6_TX	DMA1 Channel 6	Memory To Peripheral	Low
UART7_RX	DMA1 Channel 7	Peripheral To Memory	Low

SPI2_RX: DMA1 Channel 3 DMA request Settings:

Mode: Normal

Peripheral Increment: Peripheral Inc Disable

Memory Increment: Memory Inc Enable

Peripheral Data Alignment: Byte

Memory Data Alignment: Byte

Enable synchronization: Disable

SPI2_TX: DMA1 Channel 4 DMA request Settings:

Mode: Normal

Peripheral Increment: Peripheral Inc Disable

Memory Increment: Memory Inc Enable

Peripheral Data Alignment: Byte

Memory Data Alignment: Byte

Enable synchronization: Disable

I2C1_RX: DMA2 Channel 3 DMA request Settings:

Mode: Normal

Peripheral Increment: Peripheral Inc Disable

Memory Increment: Memory Inc Enable

Peripheral Data Alignment: Byte

Memory Data Alignment: Byte

Enable synchronization: Disable

I2C1_TX: DMA2 Channel 4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable
Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

I2C3_RX: DMA2 Channel 5 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable
Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

I2C3_TX: DMA2 Channel 6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable
Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

USART2_RX: DMA1 Channel 1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable
Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

USART2_TX: DMA1 Channel 2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable
Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

USART3_RX: DMA2 Channel 1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable

Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

USART3_TX: DMA2 Channel 2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable
Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

USART6_RX: DMA1 Channel 5 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable
Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

USART6_TX: DMA1 Channel 6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable
Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

UART7_RX: DMA1 Channel 7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Peripheral Inc Disable
Memory Increment:	Memory Inc Enable
Peripheral Data Alignment:	Byte
Memory Data Alignment:	Byte
Enable synchronization:	Disable

7.3 NVIC Configuration

NVIC Interrupt Table	Enabled	Preemption Priority	Sub Priority
Reset_IRQ	true	0	0
NonMaskableInt_IRQ	true	0	0
HardFault_IRQ	true	0	0
MemoryManagement_IRQ	true	0	0
BusFault_IRQ	true	0	0
UsageFault_IRQ	true	0	0
SVCall_IRQ	true	0	0
DebugMonitor_IRQ	true	0	0
PendSV_IRQ	true	0	0
SysTick_IRQ	true	15	0
OTGHS_IRQ	true	0	0
WWDT_IRQ	Unused		
PVM_IRQ	Unused		
TAMP_STAMP_IRQ	Unused		
ERTC_WKUP_IRQ	Unused		
FLASH_IRQ	Unused		
CRM_IRQ	Unused		
EXINT0_IRQ	Unused		
EXINT1_IRQ	Unused		
EXINT2_IRQ	Unused		
EXINT3_IRQ	Unused		
EXINT4_IRQ	Unused		
DMA1_Channel1_IRQ	Unused		
DMA1_Channel2_IRQ	Unused		
DMA1_Channel3_IRQ	Unused		
DMA1_Channel4_IRQ	Unused		
DMA1_Channel5_IRQ	Unused		
DMA1_Channel6_IRQ	Unused		
DMA1_Channel7_IRQ	Unused		
ADC1_IRQ	Unused		
CAN1_TX_IRQ	Unused		
CAN1_RX0_IRQ	Unused		
CAN1_RX1_IRQ	Unused		
CAN1_SE_IRQ	Unused		

EXINT9_5_IRQ	Unused
TMR1_BRK_TMR9_IRQ	Unused
TMR1_OVF_TMR10_IRQ	Unused
TMR1_TRG_HALL_TMR11_IRQ	Unused
TMR1_CH_IRQ	Unused
TMR2_GLOBAL_IRQ	Unused
TMR3_GLOBAL_IRQ	Unused
TMR4_GLOBAL_IRQ	Unused
I2C1_EVT_IRQ	Unused
I2C1_ERR_IRQ	Unused
I2C2_EVT_IRQ	Unused
I2C2_ERR_IRQ	Unused
SPI1_IRQ	Unused
SPI2_IRQ	Unused
USART1_IRQ	Unused
USART2_IRQ	Unused
USART3_IRQ	Unused
EXINT15_10_IRQ	Unused
ERTCAlarm_IRQ	Unused
OTGFS1_WKUP_IRQ	Unused
TMR13_GLOBAL_IRQ	Unused
TMR14_GLOBAL_IRQ	Unused
SPI3_IRQ	Unused
USART4_IRQ	Unused
USART5_IRQ	Unused
TMR6_GLOBAL_IRQ	Unused
TMR7_GLOBAL_IRQ	Unused
DMA2_Channel1_IRQ	Unused
DMA2_Channel2_IRQ	Unused
DMA2_Channel3_IRQ	Unused
DMA2_Channel4_IRQ	Unused
DMA2_Channel5_IRQ	Unused
OTGFS1_IRQ	Unused
DMA2_Channel6_IRQ	Unused
DMA2_Channel7_IRQ	Unused
USART6_IRQ	Unused
I2C3_EVT_IRQ	Unused

I2C3_ERR_IRQ	Unused
OTGHS_EP1_OUT_IRQ	Unused
OTGHS_EP1_IN_IRQ	Unused
OTGHS_WKUP_IRQ	Unused
FPU_IRQ	Unused
UART7_IRQ	Unused
UART8_IRQ	Unused
I2SF5_IRQ	Unused
QSPI1_IRQ	Unused
DMAMUX_IRQ	Unused
ACC_IRQ	Unused

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