1 Overview

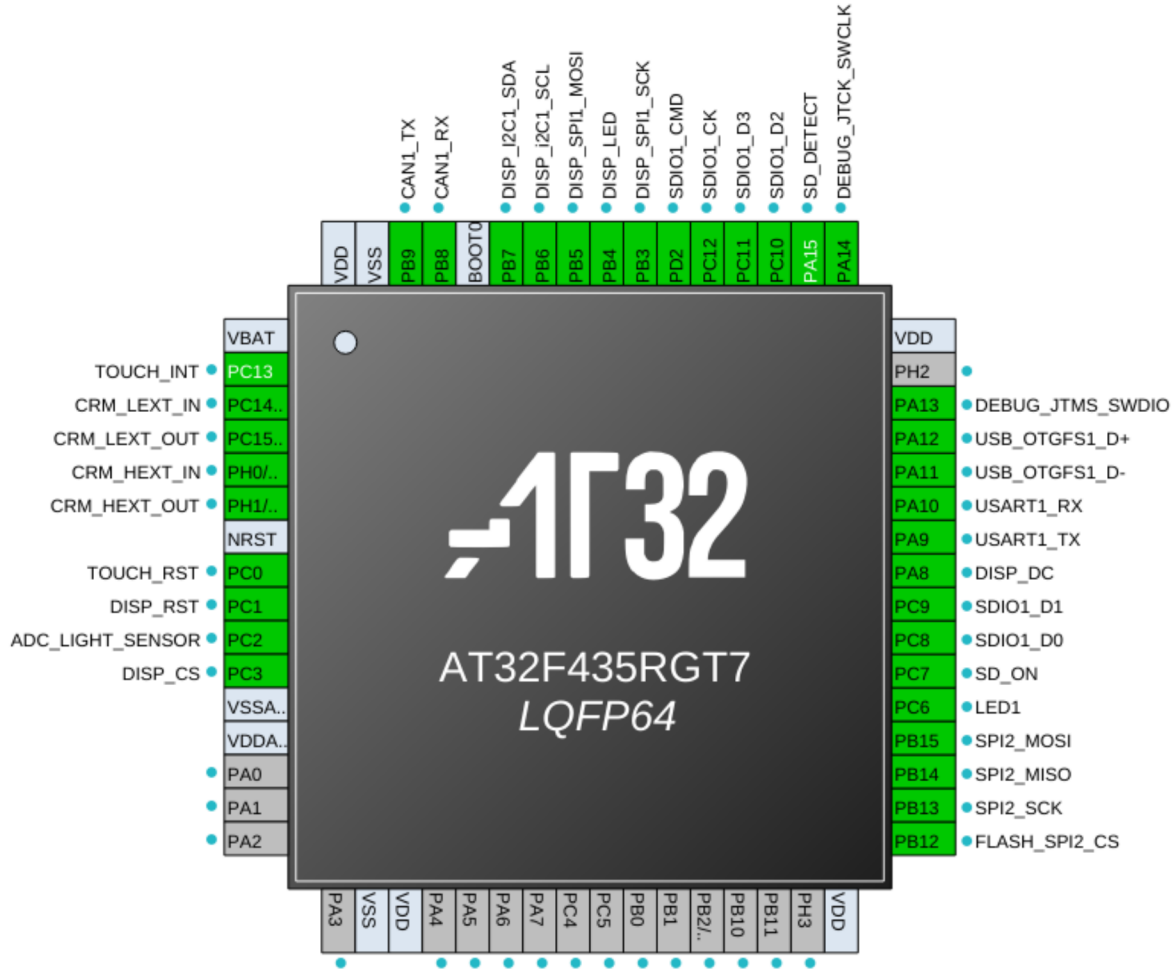
1.1 Project

Project Name	AT32F435RGT7_WorkBench
Generated with	AT32 WorkBench V1.1.2
Date	2024-11-04

1.2 MCU Information

Product Line	High performance
Device Series	AT32F435
Device	AT32F435RGT7
Core	M4F
Frequency	288MHz
Package	LQFP64
Flash	1024KB
SRAM	Default: 384KB Max: 512KB

2 Pinout Configuration



3 Pins Configuration

Pin Number	Pin Name	Pin Type	GPIO Structure	Signal Name	Label
1	VBAT	S	-	-	
2	PC13	I/O	FT	EXINT13	TOUCH_INT
3	PC14/LEXT_IN	I/O	TC	CRM_LEXT_IN	
4	PC15/LEXT_OUT	I/O	TC	CRM_LEXT_OUT	
5	PH0/HEXT_IN	I/O	TC	CRM_HEXT_IN	
6	PH1/HEXT_OUT	I/O	TC	CRM_HEXT_OUT	
7	NRST	I/O	R	-	
8	PC0	I/O	FTa	GPIO_Output	
9	PC1	I/O	FTa	GPIO_Output	
10	PC2	I/O	FTa	ADC1_IN12	
11	PC3	I/O	FTa	GPIO_Output	
12	VSSA/VREF-	S	-	-	
13	VDDA/VREF+	S	-	-	
18	VSS	S	-	-	
19	VDD	S	-	-	
32	VDD	S	-	-	
33	PB12	I/O	FT	GPIO_Output	
34	PB13	I/O	FT	SPI2_SCK	
35	PB14	I/O	TC	SPI2_MISO	
36	PB15	I/O	TC	SPI2_MOSI	
37	PC6	I/O	FT	GPIO_Output	
38	PC7	I/O	FT	GPIO_Output	
39	PC8	I/O	FT	SDIO1_D0	
40	PC9	I/O	FT	SDIO1_D1	
41	PA8	I/O	FT	GPIO_Output	
42	PA9	I/O	FT	USART1_TX	
43	PA10	I/O	FT	USART1_RX	
44	PA11	I/O	TC	USB_OTGFS1_D-	
45	PA12	I/O	TC	USB_OTGFS1_D+	
46	PA13	I/O	FT	DEBUG_JTMS_SWDIO	
48	VDD	S	-	-	
49	PA14	I/O	FT	DEBUG_JTCK_SWCLK	
50	PA15	I/O	FT	EXINT15	SD_DETECT
51	PC10	I/O	FT	SDIO1_D2	
52	PC11	I/O	FT	SDIO1_D3	

53	PC12	I/O	FT	SDIO1_CK	
54	PD2	I/O	FT	SDIO1_CMD	
55	PB3	I/O	FTf	SPI1_SCK	
56	PB4	I/O	FT	TMR3_CH1	
57	PB5	I/O	FT	SPI1_MOSI	
58	PB6	I/O	FT	I2C1_SCL	
59	PB7	I/O	FT	I2C1_SDA	
60	BOOT0	I	B	-	
61	PB8	I/O	FT	CAN1_RX	
62	PB9	I/O	FTf	CAN1_TX	
63	VSS	S	-	-	
64	VDD	S	-	-	

(1) I = input, O = output, S = supply.

(2) TC TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog functionalities, FTf = 5 V-tolerant GPIO with 20 mA sink current capability, R = bidirectional reset pin with embedded weak pull-up resistor, B = dedicated BOOT0 pin with embedded weak pull-down resistor. Among them, FTa pin has 5 V-tolerant characteristics when configured as input floating, input pull-up, or input pull-down mode. However, it cannot be 5 V-tolerant when configured as analog mode. Meanwhile, its input level should not higher than VDD + 0.3 V.

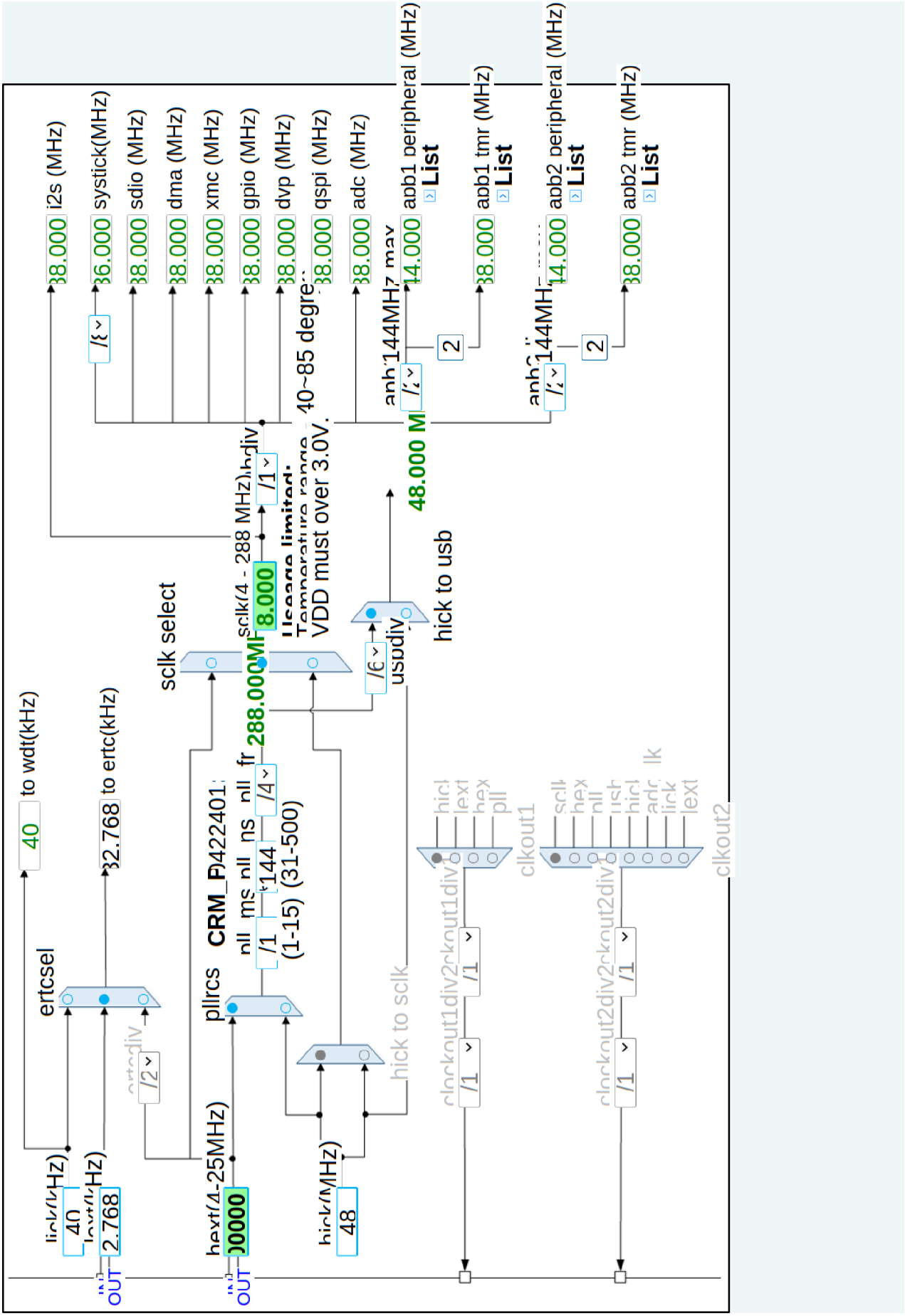
(3) Function availability depends on the chosen device. Every GPIO can function as EVENTOUT.

(4) PC13, PC14, and PC15 are supplied through the power switch. Since the switch only drives a limited amount of current (3 mA), the use of these three GPIOs as output mode is limited not to be used as a current source (e.g. to drive an LED).

(5) Main function after the first battery powered domain power-up. Later on, it depends on the contents of the battery powered registers even after reset (because these registers are not reset by the main reset). For details on how to manage these GPIOs, refer to the battery powered domain and register description sections in the AT32F435/437 reference manual.

(6) PA0, PA1, PC0, PC1, PC2, and PC3 are ADC fast channels; others are slow channels.

4 Clock Tree Configuration



5 Software Project

5.1 Project Settings

Name	Value
Project Name	AT32F435RGT7_WorkBench
Project Folder	/home/koen/dta/at32f435-board
Toolchain/IDE	AT32_IDE
Firmware Package Name and Version	AT32F435_437_Firmware_Library_V2.2.0
Minimum Heap Size	0x200
Minimum Stack Size	0x400

6 Peripherals and Middlewares Configuration

6.1 ADC-Common

Activated: Enable

6.1.1 Parameter Setting

ADCs Common Settings:

Master Slave mode	Non-combined mode
Clock frequency division	4
Clock (0-80 MHz)	72 MHz

6.2 ADC1

IN12: Enable

6.2.1 Parameter Setting

ADCs Common Settings:

Master Slave mode	Non-combined mode

ADC Settings:

Data Alignment	Right alignment
Sequence Mode	Disable
Resolution select	12 bit

ADC Ordinary Conversion Settings:

Enable Ordinary Conversions	Disable

ADC Preempted Conversion Settings:

Enable Preempted Conversions	Disable

A/D Calibration:

A/D Calibration	Enable

6.3 CAN1

Activated: Enable

6.3.1 Parameter Setting

BaudRate Settings:

Baud Rate (5-1000)	500 KBits/s
Sample point (50-90)	87.5 %
BaudRate Deviation Tolerance	Disable
BaudRate Configuration Result	Result 1
Baud rate division (1-4095)	36

Bit time segment 1 (BSEG1)	6 time quantum
Bit time segment 2 (BSEG2)	1 time quantum
Resynchronization adjust width	1 time quantum

Basic Parameters:

CAN Mode	Communication mode
Time triggered communication mode	Disable
Automatic exit bus-off	Enable
Automatic exit doze mode	Enable
Prohibit retransmission when sending fails	Disable
Message discarding rule select when overflow	The previous message is discarded
Multiple message transmit sequence rule	The smallest identifier is first transmitted

Filter 0 Configuration:

Enable Filter 0	Enable
FIFO select	FIFO0
Identifier Type Select	Standard identifier
Filter Mode Configuration	Identifier Mask Mode
Frame Type	Data/Remote frame
ID1 (11bit) (0x0-0x7FF)	0x0
Mask1 (11bit) (0x0-0x7FF)	0x0
ID2 (11bit) (0x0-0x7FF)	0x0
Mask2 (11bit) (0x0-0x7FF)	0x0

Filter 1 Configuration:

Enable Filter 1	Disable

Filter 2 Configuration:

Enable Filter 2	Disable

Filter 3 Configuration:

Enable Filter 3	Disable

Filter 4 Configuration:

Enable Filter 4	Disable

Filter 5 Configuration:

Enable Filter 5	Disable

Filter 6 Configuration:

Enable Filter 6	Disable

Filter 7 Configuration:

Enable Filter 7	Disable

Filter 8 Configuration:

Enable Filter 8	Disable

Filter 9 Configuration:

Enable Filter 9	Disable

Filter 10 Configuration:

Enable Filter 10	Disable

Filter 11 Configuration:

Enable Filter 11	Disable

Filter 12 Configuration:

Enable Filter 12	Disable

Filter 13 Configuration:

Enable Filter 13	Disable

Filter 14 Configuration:

Enable Filter 14	Disable

Filter 15 Configuration:

Enable Filter 15	Disable

Filter 16 Configuration:

Enable Filter 16	Disable

Filter 17 Configuration:

Enable Filter 17	Disable

Filter 18 Configuration:

Enable Filter 18	Disable

Filter 19 Configuration:

Enable Filter 19	Disable

Filter 20 Configuration:

Enable Filter 20	Disable

Filter 21 Configuration:

Enable Filter 21	Disable

Filter 22 Configuration:

Enable Filter 22	Disable

Filter 23 Configuration:

Enable Filter 23	Disable

Filter 24 Configuration:

Enable Filter 24	Disable

Filter 25 Configuration:

Enable Filter 25	Disable

Filter 26 Configuration:

Enable Filter 26	Disable

Filter 27 Configuration:

Enable Filter 27	Disable

6.4 CRM

High speed external crystal (HEXT): Crystal/Ceramic Resonator
Low speed external crystal (LEXT): Crystal/Ceramic Resonator

6.5 DEBUG

Debug interface: SWD

6.6 EXINT

EXINT13: Enable
EXINT15: Enable

6.6.1 Parameter Setting

EXINT13:

Interrupt/Event	Interrupt
Trigger Polarity	Rising Edge

EXINT15:

Interrupt/Event	Interrupt
Trigger Polarity	Rising Edge

6.7 I2C1

I2C: I2C

6.7.1 Parameter Setting

Clock Features:

I2C Speed Mode (tSU)	Standard Mode
I2C Clock Speed (fSCL) (KHz) (1-100)	100
Digital Filter (0-15)	0
Rise Time (tr) (ns) (0-1000)	1000
Fall Time (tf) (ns) (0-300)	300
Timing Configuration Value	0xC0F03030

Slave Features:

Clock Stretch Mode	Enable
Address mode	7-bit
Dual Address mode	Disable

Own address 1 (0x0-0x7F)	0x0
General Call address detection	Disable

6.8 SDIO1

Mode: SD Card 4bit bus width

6.8.1 Parameter Setting

Basic Parameters:

Clock division (0-1023)	0
Clock frequency	144 MHz
SDIO_CK edge selection	SDIO_CK generated on the rising edge
Power saving mode enable	Disable
Hardware flow control enable	Disable
Clock divider bypass	Disable

6.9 SPI1

Mode: Transmit Only Master

6.9.1 Parameter Setting

Basic Parameters:

Interface protocol	Motorola Mode
Frame bit num	8 Bits
First Bit	MSB First

Clock Parameters:

Clock frequency division	4
Clock frequency (0-36 MHz)	36 MHz
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disable
CS Signal Type	Software

6.10 SPI2

Mode: Full-Duplex Master

6.10.1 Parameter Setting

Basic Parameters:

Interface protocol	Motorola Mode
Frame bit num	8 Bits

First Bit	MSB First

Clock Parameters:

Clock frequency division	4
Clock frequency (0-36 MHz)	36 MHz
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disable
CS Signal Type	Software

6.11 SYSTEM

Timebase Source: SysTick

6.11.1 Parameter Setting

Timebase Parameters:

Delay Mode	Polling

6.12 TMR3

Activated: Enable
Channel1 mode: Output_CH1

6.12.1 Parameter Setting

Counter Settings:

Divider value (16 bits value) (0-65535)	0
Counter Direction	Up
Period Value (16 bits value) (0-65535)	65535
Clock divider	Divided by 2
Period buffer enable	Enable
Overflow Event	From counter/ovfswtr/sub-timer

Primary mode settings:

Synchronize with sub-timer	Disable
Primary TMR output selection	Reset

Output Channel 1:

Mode	PWM mode A
Channel data (16 bits value) (0-65535)	0
Channel output buffer	Enable
Immediately Mode	Disable
CH Polarity	High

6.13 USART1

Mode: Asynchronous

6.13.1 Parameter Setting

Basic Parameters:

Baud Rate (2197-9000000)	115200 Bits/s
Real Baud Rate	115200 Bits/s
Data bit num	8 Bits (including Parity)
Parity selection	None
STOP bit num	1

Advanced Parameters:

Data Direction	Receive and Transmit
TX and RX Pins Swapping	Disable

6.14 USB_OTGFS1

Mode: Device Only

7 System Configuration

7.1 GPIO Configuration

IP	Pin Name	Signal	Output level	GPIO type	Pull type	GPIO mode	Driver capability	Label
ADC1	PC2	ADC1_IN12	n/a	n/a	Pull-none	Analog mode	n/a	ADC_LIGHT_SENSOR
CAN1	PB8	CAN1_RX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PB9	CAN1_TX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
CRM	PC14/ LEXT_IN	CRM_LEXT_IN	n/a	n/a	n/a	n/a	n/a	
	PC15/ LEXT_OUT	CRM_LEXT_OUT	n/a	n/a	n/a	n/a	n/a	
	PH0/ HEXT_IN	CRM_HEXT_IN	n/a	n/a	n/a	n/a	n/a	
	PH1/ HEXT_OUT	CRM_HEXT_OUT	n/a	n/a	n/a	n/a	n/a	
DEBUG	PA13	DEBUG_JTMS_SWDIO	n/a	n/a	n/a	n/a	n/a	
	PA14	DEBUG_JTCK_SWCLK	n/a	n/a	n/a	n/a	n/a	
EXINT	PC13	EXINT13	n/a	n/a	Pull-none	Input mode	n/a	TOUCH_INT
	PA15	EXINT15	n/a	n/a	Pull-none	Input mode	n/a	SD_DETECT
I2C1	PB6	I2C1_SCL	n/a	Open Drain	Pull-none	Mux function mode	Moderate	DISP_i2C1_SCL
	PB7	I2C1_SDA	n/a	Open Drain	Pull-none	Mux function mode	Moderate	DISP_I2C1_SDA
SDIO1	PC8	SDIO1_D0	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PC9	SDIO1_D1	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PC10	SDIO1_D2	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PC11	SDIO1_D3	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PC12	SDIO1_CK	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PD2	SDIO1_CMD	n/a	Push Pull	Pull-none	Mux function mode	Moderate	

SPI1	PB3	SPI1_SCK	n/a	Push Pull	Pull-none	Mux function mode	Moderate	DISP_SPI1_SCK
	PB5	SPI1_MOSI	n/a	Push Pull	Pull-none	Mux function mode	Moderate	DISP_SPI1_MOSI
SPI2	PB13	SPI2_SCK	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PB14	SPI2_MISO	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PB15	SPI2_MOSI	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
TMR3	PB4	TMR3_CH1	n/a	Push Pull	Pull-none	Mux function mode	Moderate	DISP_LED
USART1	PA9	USART1_TX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PA10	USART1_RX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
USB_OTGFS1	PA11	USB_OTGFS1_D-	n/a	n/a	n/a	n/a	n/a	
	PA12	USB_OTGFS1_D+	n/a	n/a	n/a	n/a	n/a	
GPIO	PC0	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	TOUCH_RST
	PC1	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	DISP_RST
	PC3	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	DISP_CS
	PB12	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	FLASH_SPI2_CS
	PC6	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	LED1
	PC7	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	SD_ON
	PA8	GPIO_Output	Output level low	Push Pull	Pull-none	Output mode	Moderate	DISP_DC

7.2 DMA Configuration

Nothing configuration in DMA Service.

7.3 EDMA Configuration

Nothing configuration in EDMA Service.

7.4 NVIC Configuration

NVIC Interrupt Table	Enabled	Preemption Priority	Sub Priority
Reset_IRQ	true	0	0
NonMaskableInt_IRQ	true	0	0
HardFault_IRQ	true	0	0
MemoryManagement_IRQ	true	0	0
BusFault_IRQ	true	0	0
UsageFault_IRQ	true	0	0
SVCall_IRQ	true	0	0
DebugMonitor_IRQ	true	0	0
PendSV_IRQ	true	0	0
SysTick_IRQ	true	15	0
WWDT_IRQ	Unused		
PVM_IRQ	Unused		
TAMP_STAMP_IRQ	Unused		
ERTC_WKUP_IRQ	Unused		
FLASH_IRQ	Unused		
CRM_IRQ	Unused		
EXINT0_IRQ	Unused		
EXINT1_IRQ	Unused		
EXINT2_IRQ	Unused		
EXINT3_IRQ	Unused		
EXINT4_IRQ	Unused		
EDMA_Stream1_IRQ	Unused		
EDMA_Stream2_IRQ	Unused		
EDMA_Stream3_IRQ	Unused		
EDMA_Stream4_IRQ	Unused		
EDMA_Stream5_IRQ	Unused		
EDMA_Stream6_IRQ	Unused		
EDMA_Stream7_IRQ	Unused		
ADC1_2_3_IRQ	Unused		
CAN1_TX_IRQ	Unused		
CAN1_RX0_IRQ	Unused		
CAN1_RX1_IRQ	Unused		
CAN1_SE_IRQ	Unused		
EXINT9_5_IRQ	Unused		

TMR1_BRK_TMR9_IRQ	Unused
TMR1_OVF_TMR10_IRQ	Unused
TMR1_TRG_HALL_TMR11_IRQ	Unused
TMR1_CH_IRQ	Unused
TMR2_GLOBAL_IRQ	Unused
TMR3_GLOBAL_IRQ	Unused
TMR4_GLOBAL_IRQ	Unused
I2C1_EVT_IRQ	Unused
I2C1_ERR_IRQ	Unused
I2C2_EVT_IRQ	Unused
I2C2_ERR_IRQ	Unused
SPI1_IRQ	Unused
SPI2_I2S2EXT_IRQ	Unused
USART1_IRQ	Unused
USART2_IRQ	Unused
USART3_IRQ	Unused
EXINT15_10_IRQ	Unused
ERTCAlarm_IRQ	Unused
OTGFS1_WKUP_IRQ	Unused
TMR8_BRK_TMR12_IRQ	Unused
TMR8_OVF_TMR13_IRQ	Unused
TMR8_TRG_HALL_TMR14_IRQ	Unused
TMR8_CH_IRQ	Unused
EDMA_Stream8_IRQ	Unused
XMC_IRQ	Unused
SDIO1_IRQ	Unused
TMR5_GLOBAL_IRQ	Unused
SPI3_I2S3EXT_IRQ	Unused
UART4_IRQ	Unused
UART5_IRQ	Unused
TMR6_DAC_GLOBAL_IRQ	Unused
TMR7_GLOBAL_IRQ	Unused
DMA1_Channel1_IRQ	Unused
DMA1_Channel2_IRQ	Unused
DMA1_Channel3_IRQ	Unused
DMA1_Channel4_IRQ	Unused
DMA1_Channel5_IRQ	Unused

EMAC_IRQ	Unused
EMAC_WKUP_IRQ	Unused
CAN2_TX_IRQ	Unused
CAN2_RX0_IRQ	Unused
CAN2_RX1_IRQ	Unused
CAN2_SE_IRQ	Unused
OTGFS1_IRQ	Unused
DMA1_Channel6_IRQ	Unused
DMA1_Channel7_IRQ	Unused
USART6_IRQ	Unused
I2C3_EVT_IRQ	Unused
I2C3_ERR_IRQ	Unused
OTGFS2_WKUP_IRQ	Unused
OTGFS2_IRQ	Unused
DVP_IRQ	Unused
FPU_IRQ	Unused
UART7_IRQ	Unused
UART8_IRQ	Unused
SPI4_IRQ	Unused
QSPI2_IRQ	Unused
QSPI1_IRQ	Unused
DMAMUX_IRQ	Unused
SDIO2_IRQ	Unused
ACC_IRQ	Unused
TMR20_BRK_IRQ	Unused
TMR20_OVF_IRQ	Unused
TMR20_TRG_HALL_IRQ	Unused
TMR20_CH_IRQ	Unused
DMA2_Channel1_IRQ	Unused
DMA2_Channel2_IRQ	Unused
DMA2_Channel3_IRQ	Unused
DMA2_Channel4_IRQ	Unused
DMA2_Channel5_IRQ	Unused
DMA2_Channel6_IRQ	Unused
DMA2_Channel7_IRQ	Unused

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