

Ambient Light Sensor

ALS-AK610P-DF Specification

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公司名: 深圳市工采网络科技有限公司

地址: 广东省深圳市南山区高新南一道中国科技开发院3号楼16层

电话: +86-0755-83279017-8007 传真: +86-0755-83279017-8007



Description

The ALS-AK610 provides ambient light sensing (ALS) detection. The ALS approximates human eye response to light intensity under a difference of lighting conditions and through a difference of attenuation materials. ALS-AK610 can detect the wide range illumination from the dark up to under direct sun light. It also support program hardware interrupt with interrupt with hysteresis to respond to events.

Features

- I²C interface (Fast Speed Mode at 400kHz/s)
- Dedicated Interrupt Pin
- Supply Voltage Range from 1.7V to 3.6V
- Operating Temperature Range from-40°C to +85°C
- Ambient Light Photo Sensor
 - Close to human eyes responsibility
 - Up to 16-bit Digital Output (0~65535)
 - Programmable Dynamic Range Ratio = 1:4:16:64:256
 - Linear Output Code for Dynamic Range Selection
 - Eliminate 50 / 60 Hz Filter by Programmable Integrated Time
 - · Fluorescent light flicker immunity
- Package level trimming by software.

Application

- Cell Phone and LCD display backlight control
- Notebook/Monitor Security
- Automatic Menu Pop
- Digital Camera light meter



1. Function Block Diagram VDD ALS PGA ADC Circuit ► INT Low Dropout 10 Interface Regulator **ASIC** SCL Oscillator Temperature SDA Circuit **GND**

2. I/O Pins Configuration

Pin	I/O Type	Pin Name	Description	
1	VDD	VDD	Power Supply Voltage	
2	0	INT	Interrupt pin	
3	I	SCL	I2C serial clock line	
4	I/O	SDA	I2C serial data line	
5	GND	Ground	GND	

Note: INT is an open drain Circuit; it can be removed bonding wire in different package type.

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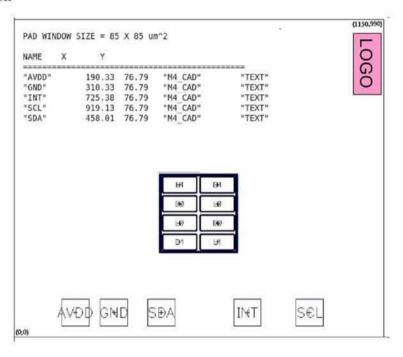
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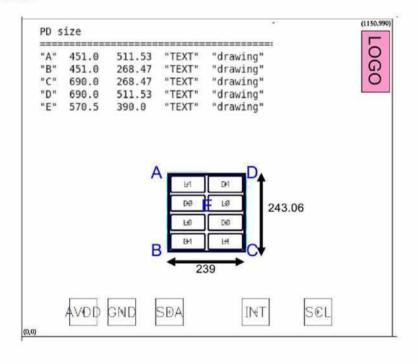


3. Die Information

PAD Location



· Photo Diode Location



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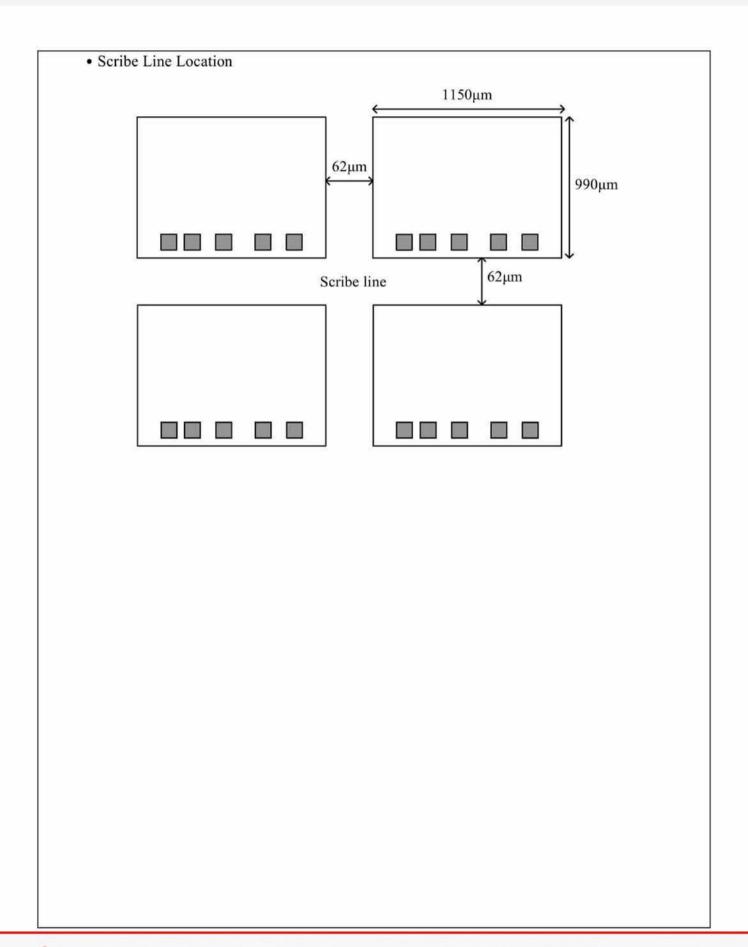
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Specification

Absolute Maximum Ratings*

Parameter	Symbol	Value	Unit	
Supply Voltage	VDD	4.5	V	
I ² C Bus Pin Voltage	SCL, SDA, INT	-0.2 to 4.5	V	
I ² C Bus Pin Current	SCL, SDA, INT	10	mA	
Operating Temperature	Торе	-40 to +85	°C	
Storage Temperature	Tstg	-45 to +100	°C	
ESD Rating	Human Body Model	2	KV	

^{*}Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

Recommended Operation Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage Note1,2	V_{DD}	1.7		3.6	V	
I ² C Bus Pin Voltage Note3	V_{Bus}		V_{DD}		V	$V_{Bus} = V_{DD}$
Operating Temperature	Tope	-40		+85	°C	
I ² C Bus Input High Voltage Note3	VIH_SCL,	VDD			V	
1-C Bus input High Voltage	V_{IH_SDA}	*0.7			v	
I'C D. J. J. V. L. Note3	VIL_SCL,			VDD	v	
I ² C Bus Input Low Voltage Note3	V_{IL_SDA}			*0.3	V	
SDA Output I au Valtaga	V	0		0.4	V	3mA sinking current
SDA Output Low Voltage	V_{OL_SDA}	0		0.6	V	6mA sinking current
INT Output Low Voltage	V _{OL INT}	0		0.4	V	3mA sinking current

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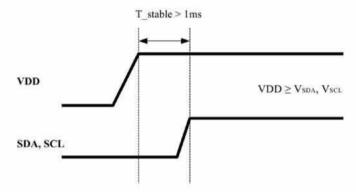
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Notes:

- The power supply need to make sure the VDD slew rate at least 0.5V/ms. ALS-AK610 have power on reset function. When VDD drops below 1.4V under room temp, the IC will be reset automatically. Then power back up at the requirement slew rate, and write registers to the desired values.
- 2. The IC power supply sequence is shown in below:



3. The specs are defined under VDD=3.3V, T=25°C



3.1 Electrical & Optical Specifications

Unless otherwise specified, the following specifications apply over the operating ambient temperature $T=25^{\circ}C$, VDD=3.3V, and measure the output current by white light LED.

Electrical Characteristics	Symbol	MIN	TYP	MAX	Notes	Unit
	I_{DD1}		220	1	Ev=0, conv=80ms	μΑ
	I_{DD2}		40		Ev=0, conv=600ms	
Active Supply Current	I _{DD3}		8		Ev=0, conv=4000ms Note3	μА
	I_{PD1}		2.5		Sleep mode,Ev=0, I ² C inactive	μА
	I_{PD2}		1.5		Sleep mode, Ev=0, Brown out disable	μА
Device Boot Time	T_{boot}		20		Note3	ms

Notes:

- 1. CLSCONV=1, INTE TIME=64, no wait time
- 2. CLSCONV=1, INTE_TIME=64, WUNIT=1T(8ms), WSTEP=64
- 3.CLSCONV=1, INTE_TIME=64, WUNIT=8T(64ms), WSTEP=62
- 4. The Device Boot Time (Tboot) is the delay time that the host can send the first I2C command after the VDD ready.

Waiting Characteristics	Symbol	MIN	TYP	MAX	Notes	Unit
Wait time unit	UNIT		8			ms
Wait time unit select	WUNIT	1		8		WUNIT
Wait time number	WSTEP	1		64		WUNIT

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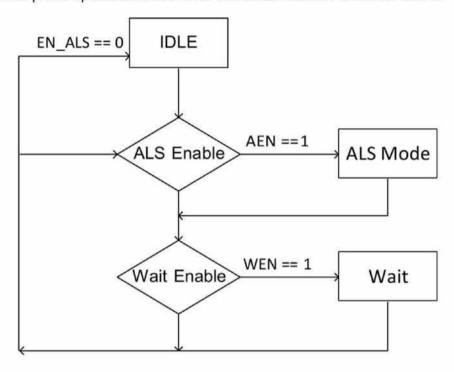
ALS Characteristics	Symbol	MIN	TYP	MAX	Notes	Unit
			4			-
Sensing Gain, relative to x1 setting	AGAIN		16			
Sensing Gam, relative to X1 setting	AGAIN		64			
			256			
ALS ADC integration time step size			1.17			ms
ALS ADC number of integration unit	CLSCONV	1		16		Unit
ALS ADC number of integration steps	INTE_TIME	ī		64		Step
Full scale ADC counts per step				1023		coun
Full scale ADC counts value				65535		coun
Dark Count (White LED, Ev=0)	ALS_L		0	5	AGAIN=256 ATIME=64	coun
ALS ADC count value (White LED, Ev=100Lux)	ALS_L		256		AGAIN= 8 ATIME= 64	coun



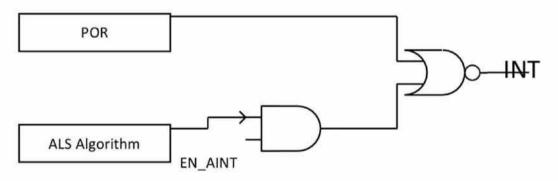
4. Operation

4.1 State Machine

There is one prime operation mode ALS. The state machine is shown below:



4.2 Interrupt



4.2.1 ALS Interrupt Algorithm

Correlative register:

TheALS Interrupt (INT ALS, register 0x02, bit0).

The ALS Persistence (PRS ALS, register 0x0B, bit0 to bit3),

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The ALS Data (Y channel data, register 0x20 to 0x21),

The ALS Low Threshold (ALS THRES L, register 0x0C to 0x0D),

The ALS High Threshold (ALS THRES H, register 0x0E to 0x0F).

INT ALStriggered condition:

- 1. Rule of active interrupt: DATA > ALS THRES H or DATA < ALS THRES L.
- If the <u>DATA</u> meets the rule, the <u>interrupt</u> count increasesone.
 If the <u>DATA</u> fails in the rule, the interrupt count will be clear.
- When the <u>interrupt</u> count equal to <u>PRS ALS setting</u>, <u>INT ALS</u> will be triggered and reset the interrupt counter.
- If <u>PRS ALS</u> is set to zero, <u>threshold</u> will be ignored and <u>DATA</u> will meets the active interrupt rule forcibly.

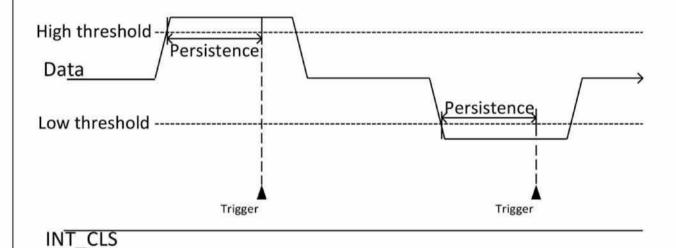


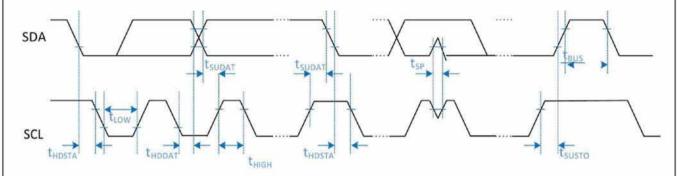
Fig.



5. I²C Interface

5.1 Communication Interface Timing Characteristics

This section will describe the protocol of the I²C bus. For more details and timing diagrams please refer to the I²C specification.



Powermetow (#)	Cumbal	Fast	mode	1144
Parameter (*)	Symbol	Min	Max	Unit
SCL clock frequency	fscL	100	400	kHz
Bus free time between STOP condition and START condition	t _{BUS}	1.3	*	μs
LOW period of the SCL clock	tLOW	1.3	·	μs
HIGH period of the SCL clock	t HIGH	0.6	3==0)	μs
Hold time (repeated) START condition	t HDSTA	0.6	s = -	μs
Set-up time (repeated) START condition	tsusta	0.6	-	μs
Set-up time for STOP condition	t susto	0.6	-	μs
Data hold time	t HDDAT	50		ns
Data set-up time	tsudat	100	-	ns
Pulse width of spikes which must be suppressed by the input filter	tsp	0	50	ns
Rise time of both SDA and SCL signals		20 x VDD/5.5	300	ns
Fall time of both SDA and SCL signals		20 x VDD/5.5	300	ns

^(*) Specified by design and characterization; not production tested.

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^(**) All specifications are at V_{Bus} = 3.3V, T_{ope} =25°C, unless otherwise noted.



5.21 ² C Protocol
5.2.1 I ² C Write
S Slave Addr W A Reg Addr A Data 8 Bit A P
7 Bit W A 8 Bit A 8 Bit A F
5.2.2 I ² CBlock Write
S Slave Addr W A Reg Addr A Data A Data A P
7 Bit W A 8 Bit A 8 Bit A 8 Bit A
5.2.3 I ² CRead
J.Z.J TORCAG
S Slave Addr W A Reg Addr A S Slave Addr R A Data N P
7 Bit W A 8 Bit A 3 7 Bit A 8 Bit N P
5.2.4 I ² CBlock Read
5.2.4 I ² CBlock Read
Slave Addr M A Reg Addr A S Slave Addr D A Data A
S Slave Addr W A Reg Addr A S Slave Addr R A Data 8 Bit A
Slave Addr M A Reg Addr A S Slave Addr D A Data A
S Slave Addr W A Reg Addr A S Slave Addr R A Bit A A Data 8 Bit N P
S Slave Addr W A Reg Addr A S Slave Addr R A Data 8 Bit A
S Slave Addr N A Reg Addr A S Slave Addr R A Bit A A Data 8 Bit N P Master to Slave S Start Condition, 1 Bit
S Slave Addr W A Reg Addr A S Slave Addr R A Bit A A Data 8 Bit N P
S Slave Addr N A Reg Addr A S Slave Addr R A Bit A A Data 8 Bit N P Master to Slave S Start Condition, 1 Bit
S Slave Addr 7 Bit W A Reg Addr 8 Bit A S Slave Addr 7 Bit R A Data 8 Bit A Master to Slave S Start Condition, 1 Bit Slave to Master P Stop Condition, 1 Bit
S Slave Addr W A Reg Addr A S Slave Addr R A Bit A A Data 8 Bit N P Master to Slave S Start Condition, 1 Bit Slave to Master P Stop Condition, 1 Bit W Write, Set 0 for write, 1 Bit
S Slave Addr 7 Bit W A Reg Addr 8 Bit A S Slave Addr 7 Bit R A Data 8 Bit A A Data 8 Bit N P Master to Slave S Start Condition, 1 Bit Slave to Master W Write, Set 0 for write, 1 Bit R Read, Set 1 for read, 1 Bit

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5.2.5 I2CSlave Address and R/W bit

This address is seven bits long followed by an eighth bit which is a datadirection bit (R/W). A '0' indicates a transmission (WRITE), a '1' indicates a request for data (READ). The slave address of this device is 0x38.

5.2.6 I²CBus Clear

In the unlikely event where the clock (SCL) is stuck LOW, the preferential procedure is to reset the bus using the HW reset signal if your I2C devices have HW reset inputs. If the I2C devices do not have HW reset inputs, cycle power to the devices to activate themandatory Internal Power-On Reset (POR) circuit.

If the data line (SDA) is stuck LOW, the master should send nine clock pulses. The device that held the bus LOW should release it sometime within those nine clocks.

5.2.7 I²CGeneral Call Software Reset

Following a General Call, (0000 0000), sending 0000 0110 (06h) as the second byte causes software reset. This feature is optional and not all devices will respond to this command. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address.

Precautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

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6. Register

6.1 Register Set

The ALS-AK610 is operated over the I2C bus with registers that contain configuration, status, and result information. All registers are 8 bits long. Table X lists these registers

Address	Name	Туре	Default value	Description
0x00	SYSM_CTRL	RW	0x00	ALS/PS/CALIB operation mode control, waiting m control, SW reset
0x01	INT_CTRL	R/W	0x01	Interrupt pin control, interrupt persist control
0x02	INT_FLAG	R/W	0x00	Interrupt flag, error flag, power on reset(POR) flag
0x03	WAIT_TIME	R/W	0x00	Waiting time setting
0x04	ALS_GAIN	R/W	0x00	ALS analog gain setting
0x05	ALS_TIME	R/W	0x03	ALS integrated time setting
0x0B	PERSISTENCE	R/W	0x01	ALS persistence setting
0x0C	ALS_THRES_LL	R/W	0x00	ALS low interrupt threshold - LSB
0x0D	ALS_THRES_LH	R/W	0x00	ALS low interrupt threshold - MSB
0x0E	ALS_THRES_HL	R/W	0xFF	ALS high interrupt threshold - LSB
0x0F	ALS_THRES_HH	R/W	0xFF	ALS high interrupt threshold - MSB
0x17	DATA_STAT	R/W	0x00	Data status
0x1E	ALS_DATA_L	R	0x00	ALS channel output data - LSB
0x1F	ALS_DATA_H	R	0x00	ALS channel output data - MSB
0xBC	PROD_ID_L	R	0x11	Product ID - LSB
0xBD	PROD_ID_H	R	0x10	Product ID - MSB
0xBE	MARK_ID	R	0x00	Mark ID
0xBF	REV_ID	R	0x00	Revision ID

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6.2 SYSM_CTRL

0x00	SYSM_C	SYSM_CTRL, System Control (Default = 0x00)								
BIT	7	7 6 5 4 3 2 1 0								
R/W	SWRST	EN_ WAIT	EN_ FRST	0	0	0	EN_ ONCE	EN_ ALS		

SWRST: Software reset. Reset all register to default value.

0: (Default)

1: Reset will be triggered.

EN_WAIT: Waiting time will be inserted between two measurements.

0: Disable waiting function. (Default)

1: Enable waiting function.

EN_FRST:

0: Enable (Brown out Reset circuit enable). (Default)

1: Disable (Brown out Reset circuit disable).

EN ONCE: Enables ALS function once.

0: Disable ALS function. (Default)

1: Enable ALS function.

EN ALS: Enables ALS function.

0: Disable ALS function. (Default)

1: Enable ALS function.



6.3 INT CTRL

0x01	Interrupt F	Pin Control	(Default =	0x01)				
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	ALS_ SYNC	0	0	0	EN_ AINT

ALS SYNC: Measurement is pended when ALS interrupt is triggered. Until clear the interrupt then start the next measurement.

0: Disable pending ALS function.(Default)

1: Enable pending ALS function.

EN AINT: The ALS interrupt (INT_ALS) flag can trigger the INT pin to low.

0: Disable INT_ALS effect INT pin.

1: Enable INT_ALS effect INT pin. (Default)

6.4 INT FLAG

0x02	INT_FLAC	INT_FLAG, System Control (Default = 0x00)									
BIT	7	6	5	4	3	2	1	0			
R/W	INT_ POR	DATA_ FLAG	0	0	0	0	0	INT_ALS			

INT POR: Power-On-Reset Interrupt flag trigger the INT pin when the flag sets to one. Write zero to clear the flag.

1: This bit will be set to one when it satisfy one of the following conditions:

- Power On
- VDD < 1.4V
- **SWRST**

DATA FLAG: It shows if any data is invalid after completion of each conversion cycle. This bit is read-only.

0: Data valid.

1: Data invalid.

INT ALS: ALS Interrupt flag. It correlation with CH0/1 data and ALS high/low threshold. Write zero to clear the flag.

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0: ALS interrupt not triggered or be cleared.

1: ALS interrupt triggered.

6.5 WAIT_TIME

0x03	WAIT_TIME, waiting time (Default = 0x00)									
BIT	7	6	6 5 4 3 2 1 0							
R/W	WTIME	_UNIT	WTIME_STEP							

WTIME UNIT: This register controls the waiting time unit of waiting state which is inserted between any two measurements. It is 8 ms per time unit.

0x0: 1 time unit. (Default)

0x1: 2 time units. 0x2: 4 time units. 0x3: 8 time units.

WTIME STEP: This register controls the time step of waiting state. It is increase one WTIME_UNIT per step.

0x00: 1 WTIME_UNIT. (Default)

0x01: 2 WTIME_UNIT.

.....

0x3f: 64 WTIME_UNIT.

Total wating time = WTIME STEP WTIME STEP x WTIME UNIT

6.6 ALS_GAIN

0x04	ALS_GAIN	ALS_GAIN, ALS analog gain (Default = 0x01)								
BIT	7	7 6 5 4 3 2 1 0								
R/W	PD_SEL	0	0			PGA_ALS				

PD SEL: PD gain select.

0x00: x1 (Default)

0x01: x2

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PGA ALS: ALS sensing gain.

0x01: x1 (Default)

0x02: x4 0x04: x16 0x08: x64

0x10: x256

6.7 ALS TIME

0x05	ALS_TIME	E, ALS inte	grated time	(Default =	0x03)				
BIT	7	7 6 5 4 3 2 1 0							
R/W		ALSC	ONV		0	0	INT_	TIME	

 $\underline{\mathsf{ALSCONV}}$: This register controls the conversion time of AD converter at ALS mode ($\mathsf{T}_{\mathsf{ALS}}$), and the resolution of output dat.

0x00: The maximum count of output data is 1023, TALS = 1 INT_TIME (Default)

0x01: The maximum count of output data is 2047, TALS = 2 INT_TIME

......

0xff: The maximum count of output data is 16384, TALS = 16 INT_TIME

INT TIME: This register controls the integrated time.

0x0: 1 INT_TIME (T) = 1.171 ms.

 $0x1: 1 INT_TIME (4T) = 4.683 ms.$

 $0x2: 1 INT_TIME (16T) = 18.731 ms.$

0x3: 1 INT_TIME (64T) = 74.923 ms. (Default)

The conversion time of ALS function (T_{ALS}) is decided by ALSCONV and INT_TIME.

T_{ALS}= INT TIME x (ALSCONV + 1) (ms)

EX:

Setting INT_TIME= 0x01 (4T UNIT) and ALSCONV = 0x01

The maximum count of output data is minimum of

[1024 x [INT_TIME * (ALSCONV+1)] - 1 , 65535]

= [1024 x [4 * (1+1)] - 1, 65535].



6.8 PERSISTENCE

0x0B	PERSISTENCE, ALS persistence setting (Default = 0x01)								
BIT	7	7 6 5 4 3 2 1 0							
R/W	0	0	0	INT_ SRC		PRS	_ALS		

INT SRC: This register sets to select the ALS data for the ALS Interrupt algorithm.

0x00: Select ALS DATA. (Default)

0x01: Select COMP_DATA.

PRS ALS: This register sets the numbers of similar consecutive ALS interrupt events before the interrupt pin is triggered.

0x0: Every ALS conversion is done.

0x1: 1 ALS interrupt event is asserted. (Default)

.......

0xf: 15 consecutive ALS interrupt events are asserted.

6.9 ALS_THRES_L

0x0C 0x0D	ALS_THRES_L, ALS low interrupt threshold (Default = 0x0000)														
BIT	7	7 6 5 4 3 2 1 0													
R/W		ALS_THRE_LL													
R/W				ALS_TH	HRE_LH			ALS_THRE_LH							

This register sets the lower threshold value of ALS interrupt. The interrupt algorithm compares the selected ALS data and ALS threshold value.

ALS THRE LL: ALS lower interrupt threshold value, LSB. (Reg. 0x0C) ALS THRE LH: ALS lower interrupt threshold value, MSB. (Reg. 0x0D)

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6.10 ALS_THRES_H

0x0E 0x0F	ALS_THRES_H, ALS high interrupt threshold (Default = 0xFFFF)									
BIT	7	7 6 5 4 3 2 1 0								
R/W		ALS_THRE_HL								
R/W			ALS_THRE_HH							

This register sets the high threshold value of ALS interrupt. The interrupt algorithm compares the selected ALS data and ALS threshold value.

ALS THRE HL: ALS high interrupt threshold value, LSB. (Reg. 0x0E)
ALS THRE HH: ALS high interrupt threshold value, MSB. (Reg. 0x0F)

6.11 DATA STAT

0x17	DATA_STAT_0, Data status								
BIT	7	6	5	4	3	2	1	0	
R	DATA_ REDY	0	0	0	0	0	SAT_ ALS	SAT_ COMP	

This register indicates the ALS data status.

The data ready flag will set to one when the data register is updated. After read the data register, the data ready flag will clear to zero.

If the ALS data is outside of measurable range, the corresponding saturation flag will set to one. That means the data is invalid.

6.12 ALS_DATA

0x1E 0x1F	ALS_DAT	A, ALS cha	annel outpu	t data.					
BIT	7	7 6 5 4 3 2 1 0							
R		ALS_DATA_L							
R		ALS DATA H							

The result of ALS sensor is written into ALS_DATA when ALS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has being accessed until the high byte data has be read.

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电话: +86-0755-83279017-8007 传真: +86-0755-83279017-8007 邮箱: sa



6.13 Register Table

Address (HEX)	Register Name	Bit	Command	Function/Description
		7	SWRST	0x0 : Disable software reset. (Default) 0x1 : Enable software reset.
		6	EN_WAIT	0x0 : Disable wait state. (Default) 0x1 : Enable wait state.
0x00 (R/W)	System control (Default : 0x00)	5	EN_FRST	0x0 : Enable FRST. (Default) 0x1 : Disable FRST.
(1011)	(2000)	1	EN_ONCE	0x0 : Disable ALS_ONE_SHOT function. (Default) 0x1 : Enable ALS_ONE_SHOT function.
		0	EN_ALS	0x0 : Disable ALS function. (Default) 0x1 : Enable ALS function.
0x01	Interrupt control	4	ALS_SYNC	0x0 : ALS suspend mode disable. (Default) 0x1 : ALS suspend mode enable.
(R/W)	(Default : 0x01)	0	EN_CINT	0x0 : ALS interrupt disable, 0x1 : ALS interrupt enable. (Default)
	7	INT_POR	POR flag. Write 0 clear flag.	
0x02 (R/W)	Interrupt flag (Default : 0x00)	6	SAT_FLAG (Read only)	0x0 : output data valid 0x1 : output data invalid
		0	INT_ALS	ALS interrupt flag. Write 0 clear flag.
0x03 (R/W)	Waiting time (Default : 0x00)	7:6	WTIME_UNIT	Wtime unit 0x0: 1T (Default) 0x1: 2T 0x2: 4T 0x3: 8T
		5:0	WTIME_STEP	0x00: 1 WTIME_UNIT (Default) 0x01: 2 WTIME_UNIT 0x3F: 64 WTIME_UNIT
0x04 (R/W)	ALS gain (Default : 0x01)	7	PD_SELT	0x0 : x1 (Default) 0x1 : x2

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0x17 (R/W)	Data status	7	Data Ready	Data Ready flag (every conversion time update , Read clear) 0x0 : Data complete 0x1 : Data not complete
0x0F (R/W)	(Default : 0xFFFF)	7:0	ALS_THRE_HH	ALS upper threshold high byte
0x0E (R/W)	ALS upper threshold	7:0	ALS_THRE_HL	ALS upper threshold low byte
0x0D (R/W)	(Default : 0x0000)	7:0	ALS_THRE_LH	ALS lower threshold high byte
0x0C (R/W)	ALS lower threshold	7:0	ALS_THRE_LL	ALS lower threshold low byte
0x0B Persistence setting (Default : 0x01)		3:0	PRS_ALS	INT_ALS triggered after 0x0: every conversion time 0x1: 1 conversion time (Default) 0xF: 15 conversion times
0x0R	W) (Default : 0x03)	4	INT_SRC	INT data source select 0x00 : Comp data 0x01 : ALS data
0x05 (R/W)		1:0	INTE_TIME	Integrated time 0x0: 1T 0x1: 4T 0x2: 16T 0x3: 64T (Default) 1T = 1.171 ms
		7:4	ALSCONV	0x00 : 1 time unit (Default) 0x01 : 2 time unit 0x0F : 16 time unit
		4:0	PGA_ALS	0x01 : x1 (Default) 0x02 : x4 0x04 : x16 0x08 : x64 0x10 : x256

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电话: +86-0755-83279017-8007

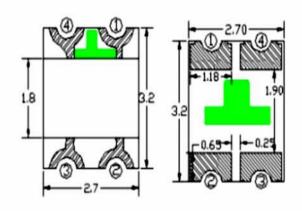
传真: +86-0755-83279017-8007

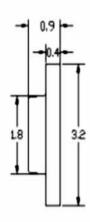


		1	SAT_ALS	ALS data error flag 0x0 : valid data 0x1 : invalid data
		0	SAT_COMP	COMPCH data error flag 0x0 : valid data 0x1 : invalid data
0x1E (R)	ALS data	7:0	ALS_DATA_L	ALS data, low byte
0x1F (R)	ALS data	7:0	ALS_DATA_H	ALS data, high byte
0xBC (R)	Product ID	7:0		Product ID lower byte, Default value is 0x11
0xBD (R)	(Default : 0x1011)	7:0		Product ID higher byte, Default value is 0x10
0xBE (R)	Mark ID (Default : 0x00)	3:0		
0xBF (R)	Revision ID (Default : 0x00)	3:0		



Package Outlines (Unit: mm)





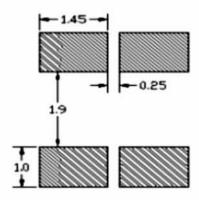
- 1、VDD
- 2, SDA
- 3、SCL
 - 4、VSS

unitimm toli+/-0.2mm

Notes:

- 1. All dimensions are in millimeter, tolerance is +/- 0.2mm unless otherwise noted.
- 2. Specifications are subject to change without notice.

Recommended PCB Layout (Unit: mm)



Notes:

- 1. All dimensions are in millimeters.
- 2. The tolerances unless mentioned is ±0.1mm.

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