

Multi-Gigabit Complex Sub-Nyquist Sampling SDR for 60 GHz

Master Thesis at the Telecommunications Circuits Lab, EPFL

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1. September 2014

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Introduction

- Mobile communication systems became ubiquitous
- Essential importance that network throughput increases logarithmically
- Higher spectral efficiency (channel allocation, MIMO etc.) is possible
- Use new frequency bands
- 60 GHz ISM band, which defines 1.76 GHz wide channels
- Possibility for big antenna arrays on small surface
- High free space path loss allows reusage of channel
- New Applications: lossless, uncompressed HD video streams, high density cell networks (5G)

Goal

- Analyze different receiver designs
- Implement a versatile simulation and test setup to analyze designs
- Measure channel characteristics like delay spread, phase noise etc.
- Make a demo setup to show that high data rates using high QAM modulation are possible
- Find performance limiting impairments for 60 GHz communication systems

Receiver Designs

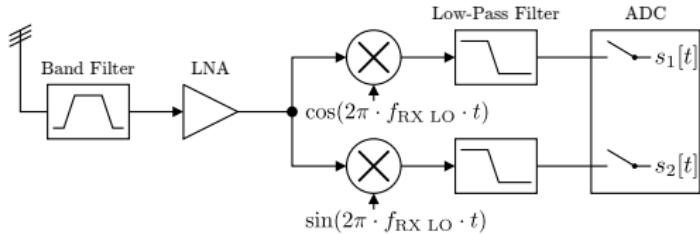
Goal

- Digitize the channel of interest with as high as possible dynamic range
- Suppress influence of other channels

Challenge

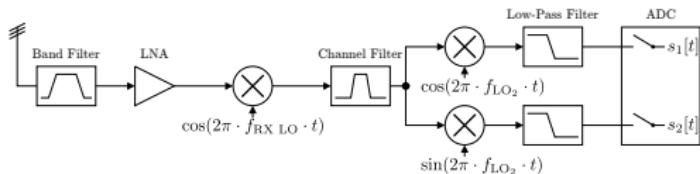
- Channel width is as high as the available ADC sampling speeds - \downarrow Oversampling is not easily possible
- Channel width can be bigger of IF frequency (1.8 GHz wide channel on IF center frequency of 1 GHz)
- Many component restrictions exist

Direction Conversion / High IF Receiver



Direction Conversion

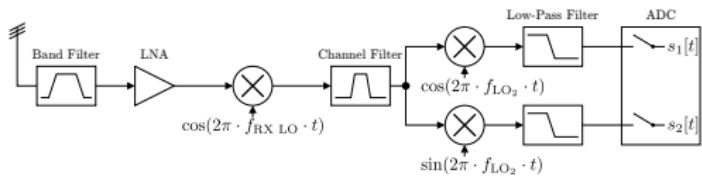
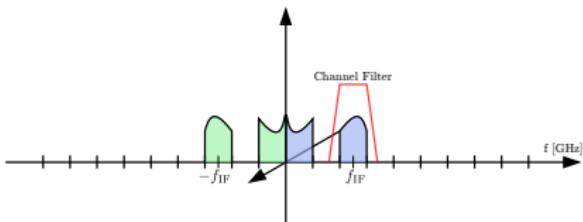
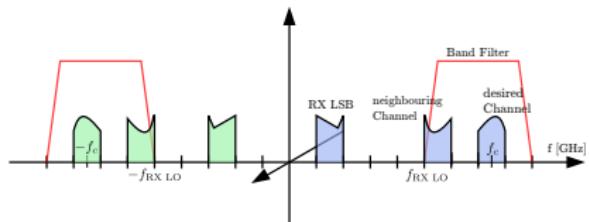
- Most popular RX Architecture for SDRs
- 60 GHz RF frontend does not go below 1 GHz



High IF Receiver

- Second mixer must run at 5 GHz
- DC-Block blocks part of signal

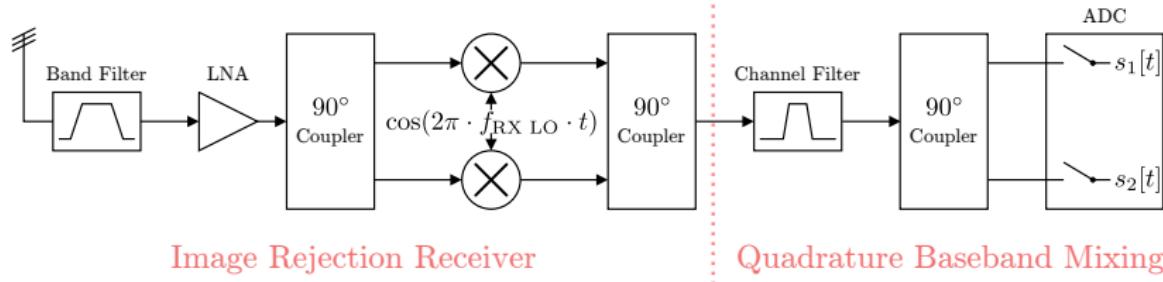
Direction Conversion / High IF Receiver



High IF Receiver

- Second mixer must run at 5 GHz
- DC-Block blocks part of signal

Quadrature Intermediate Frequency Sub-Nyquist Sampling Receiver

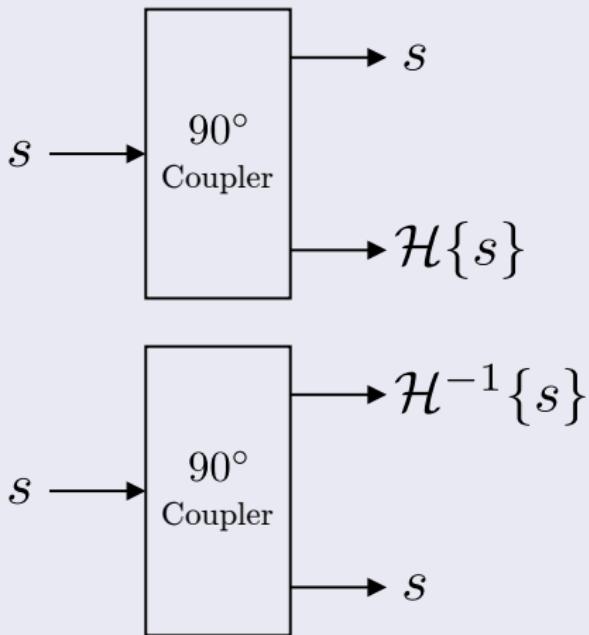


XXX

- Uses only one mixer stage
- Higher analog than digital bandwidth of ADC allows for Sub-Nyquist Sampling
- Channel-dependent, Frequency selectivity leads to non linear error

90° Coupler / Hilbert Transform

Time Domain



Frequency Domain

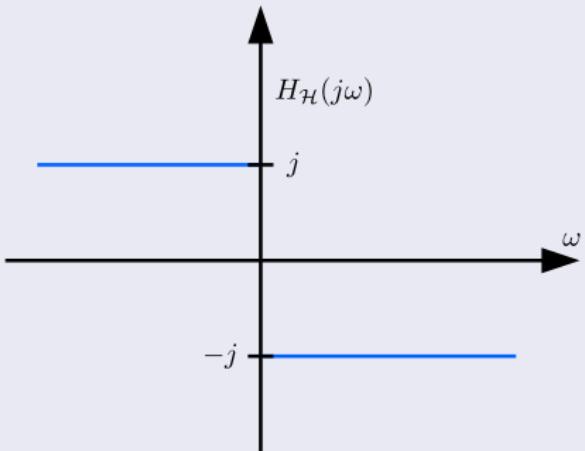


Image Rejection using 90° Couplers

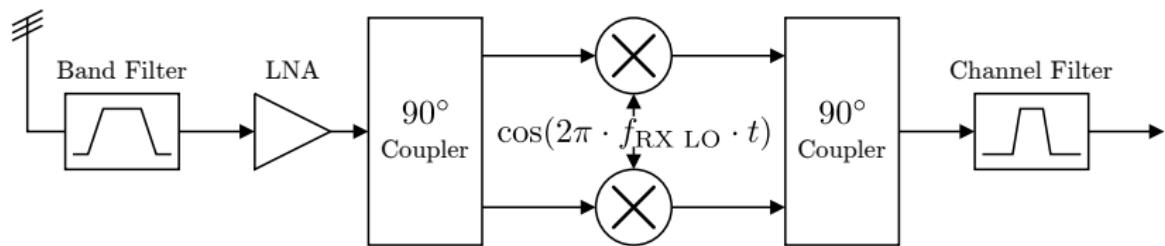
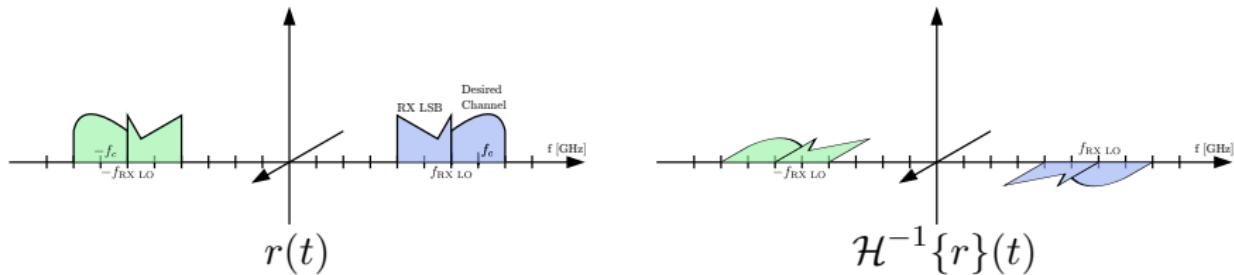


Image Rejection using 90° Couplers

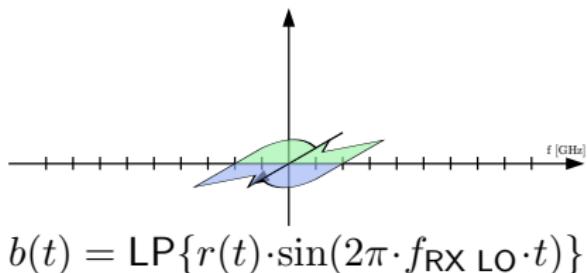
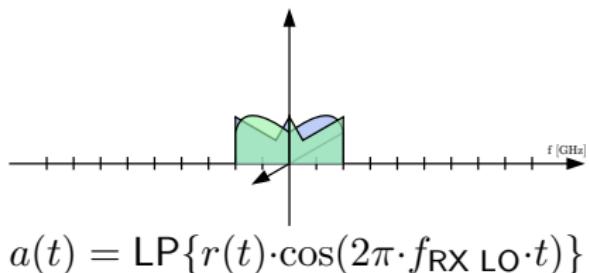
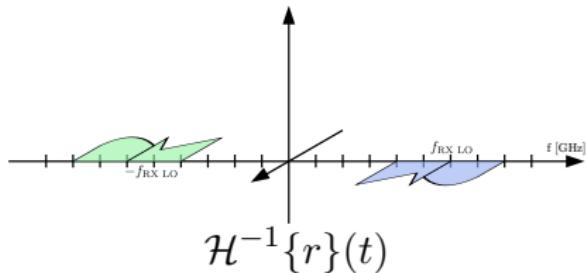
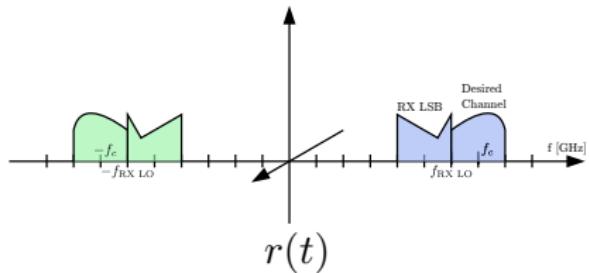
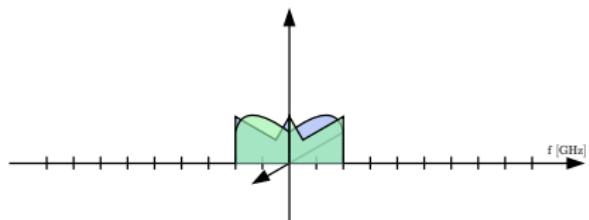
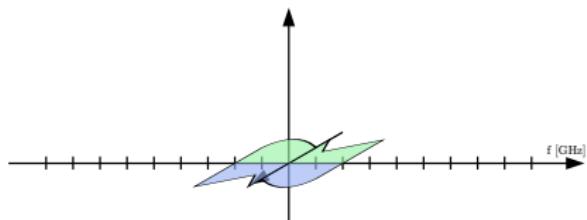


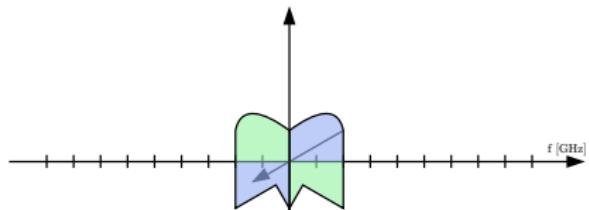
Image Rejection using 90° Couplers



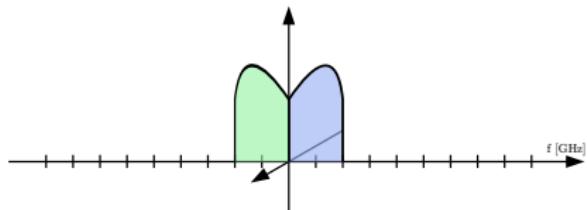
$$a(t) = \text{LP}\{r(t) \cdot \cos(2\pi \cdot f_{\text{RX LO}} \cdot t)\}$$



$$b(t) = \text{LP}\{r(t) \cdot \sin(2\pi \cdot f_{\text{RX LO}} \cdot t)\}$$

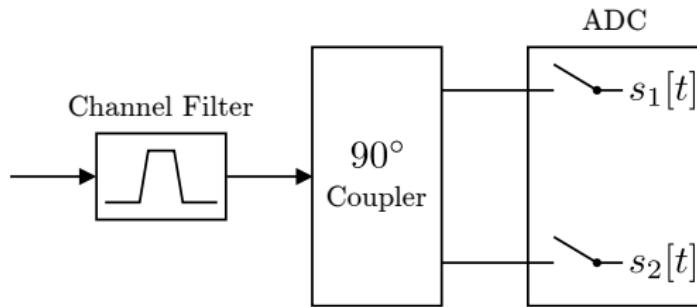
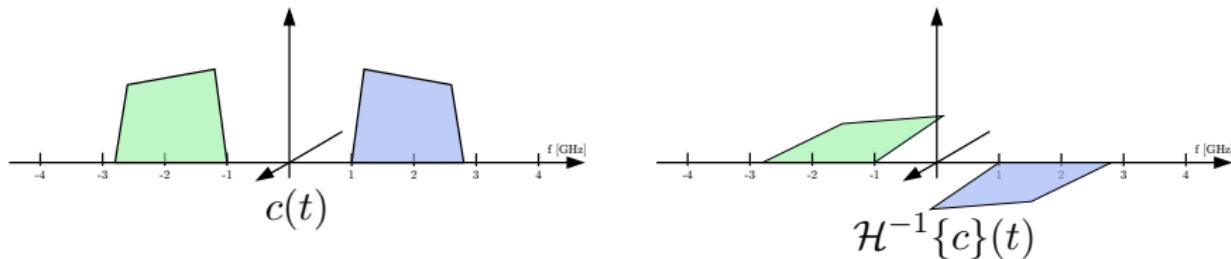


$$\mathcal{H}^{-1}\{b\}(t)$$

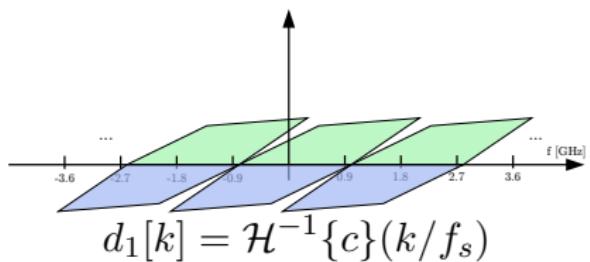
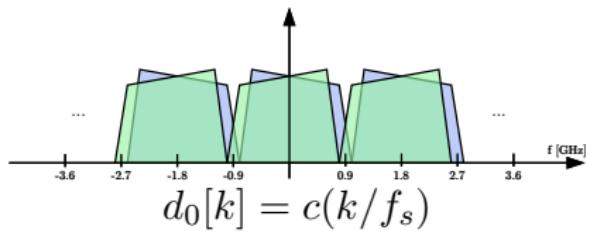
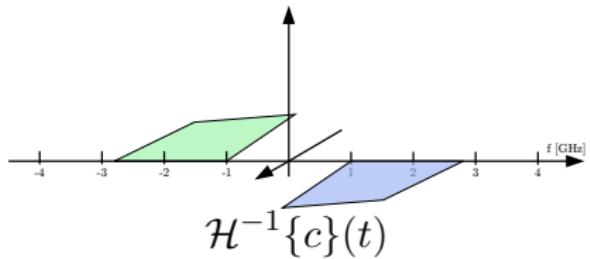
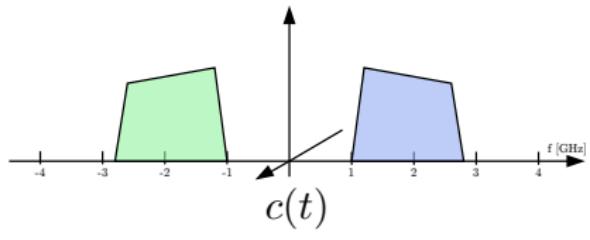


$$c(t) = a(t) + \mathcal{H}^{-1}\{b\}(t)$$

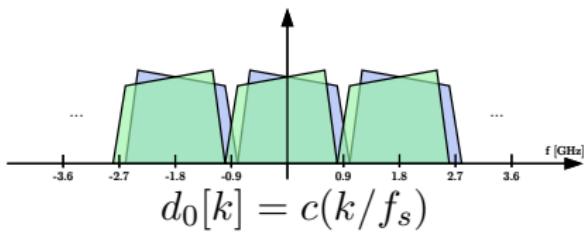
Quadrature Intermediate Frequency Sub-Nyquist Sampling



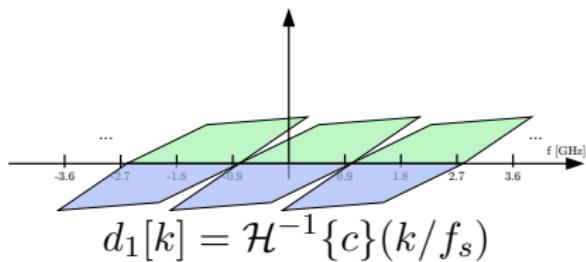
Quadrature Intermediate Frequency Sub-Nyquist Sampling



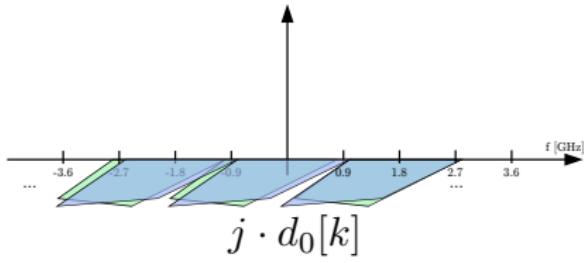
Quadrature Intermediate Frequency Sub-Nyquist Sampling



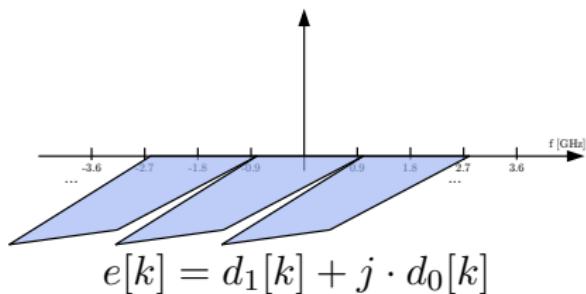
$$d_0[k] = c(k/f_s)$$



$$d_1[k] = \mathcal{H}^{-1}\{c\}(k/f_s)$$

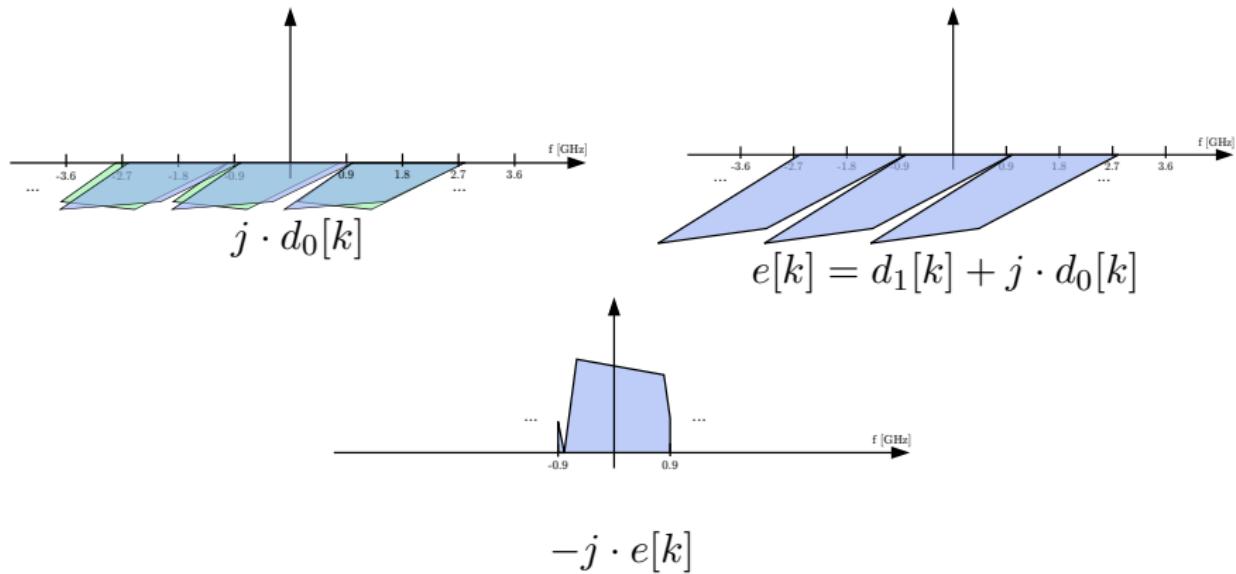


$$j \cdot d_0[k]$$



$$e[k] = d_1[k] + j \cdot d_0[k]$$

Quadrature Intermediate Frequency Sub-Nyquist Sampling



Tasks

- Acquire Data from ADC
- Store Data in real-time
- Provide download to PC

TODO: add pic of FPGA board

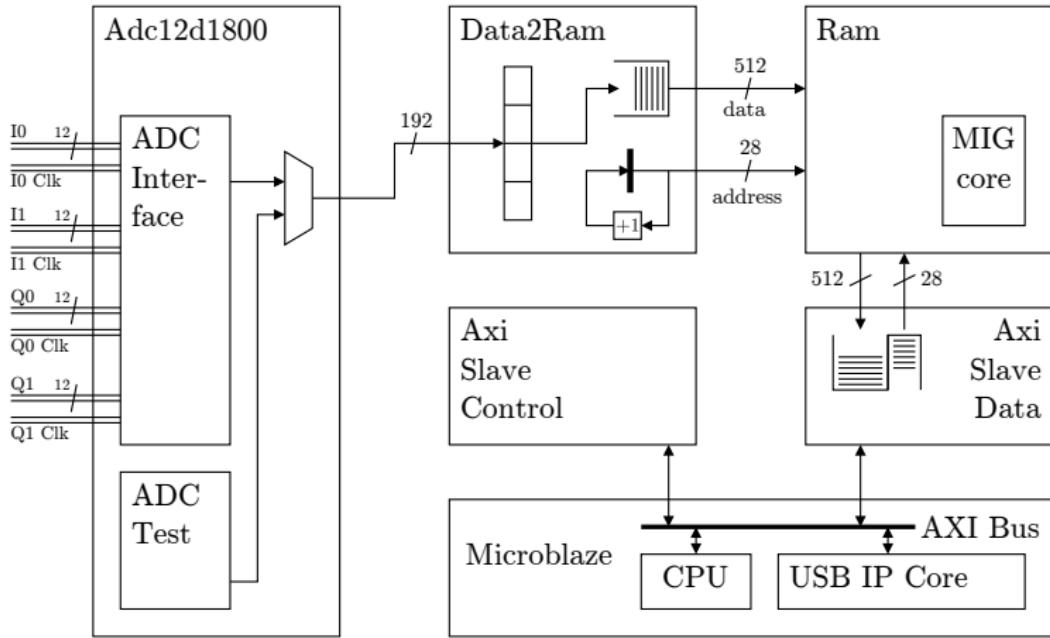
Data Storage Speed

- ADC delivers one 12-bit channel at 3.6 GHz or two 12-bit channels at 1.8 GHz → 5.4 GB/s.
- DDR3 Ram 64 bits at 500 MHz DDR → 8 GB/s.
(P&R difficult at 800 MHz)

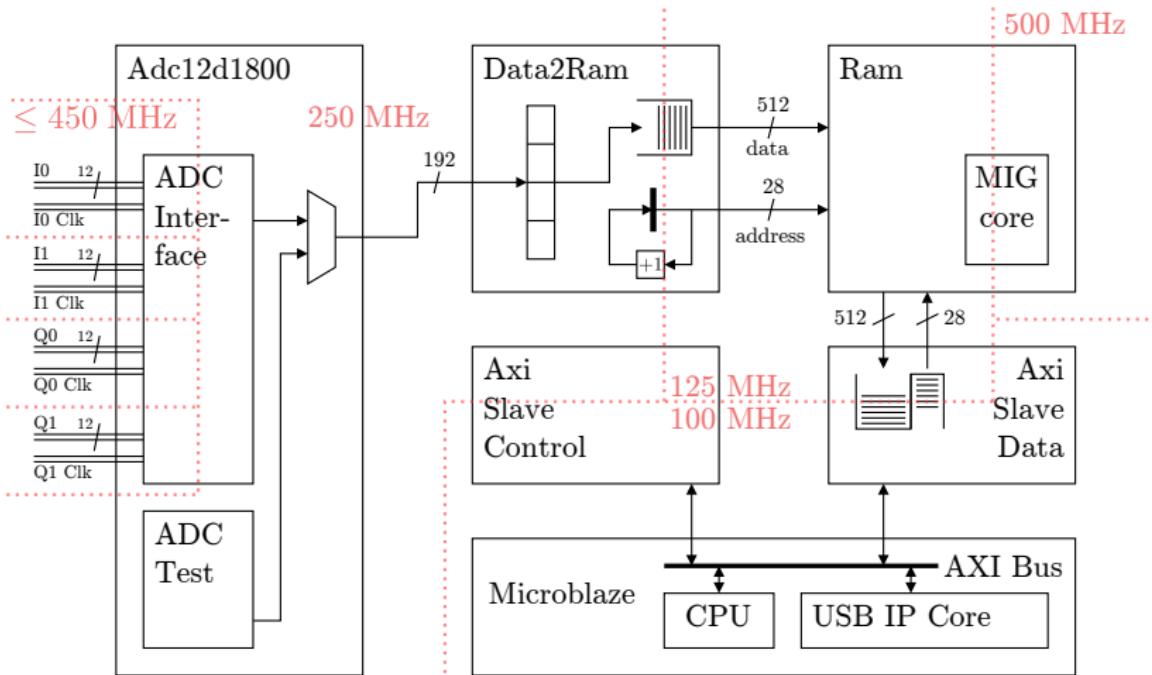
Download Speed

- USB-to-UART bridge is limited to 1Mbit/s
- Download of 1 GiB takes approx. 18 minutes
- USB 2.0 can go up to

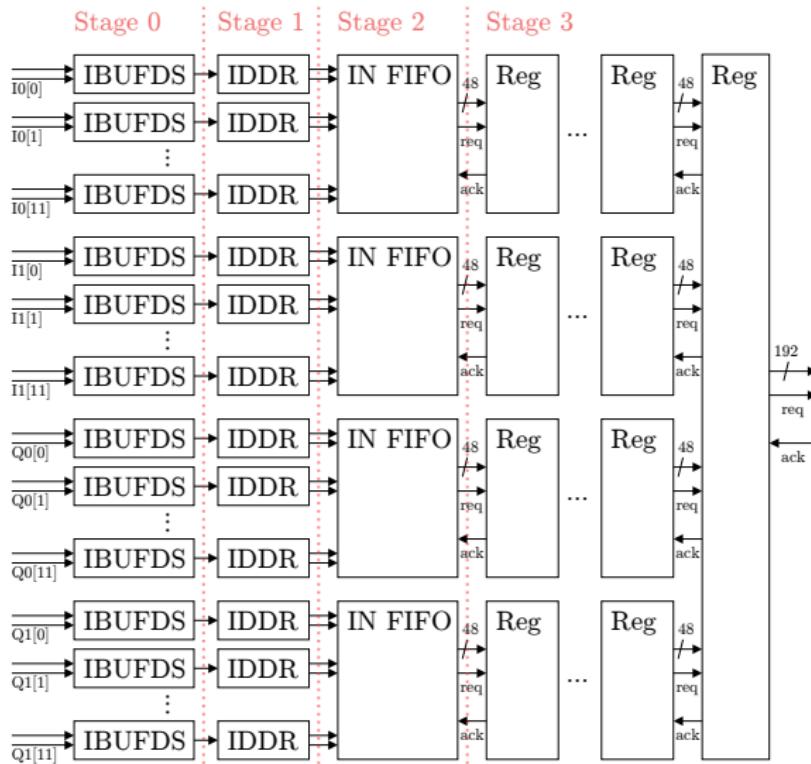
FPGA - Architecture



FPGA - Architecture



FPGA - ADC Interface



Stage 0

LVDS to single ended

Stage 1

Double to Single Data Rate

Stage 2

Clock boundary 450 MHz to 250 MHz

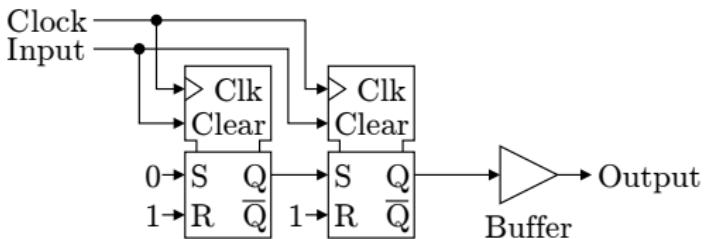
Stage 3

Centralization and Reordering

FPGA - Reset Distribution

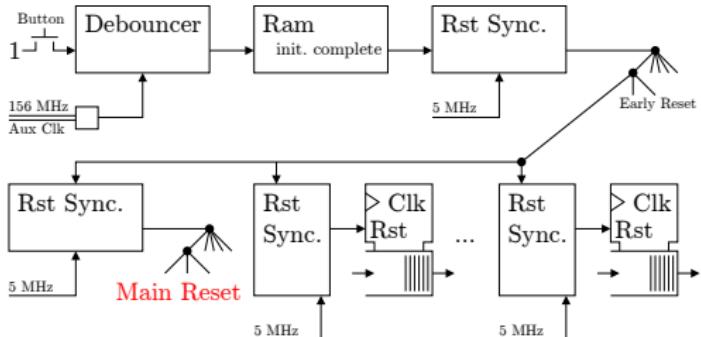
Challenge

Release asynchronous reset accross multiple clock domains in same cycle on whole FPGA die

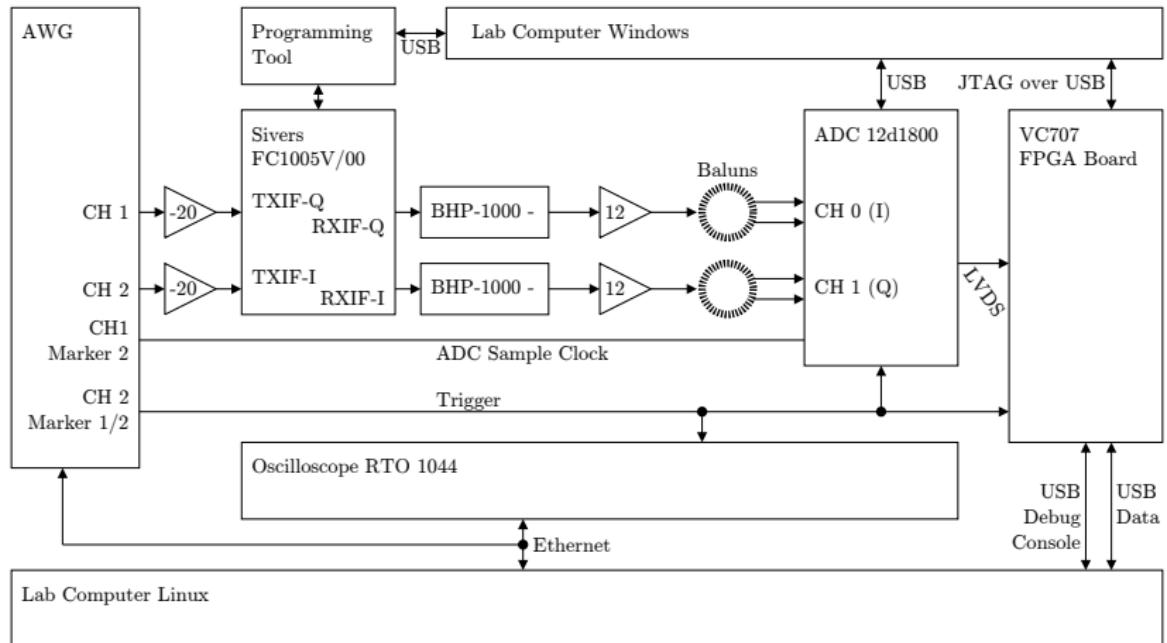


Solution

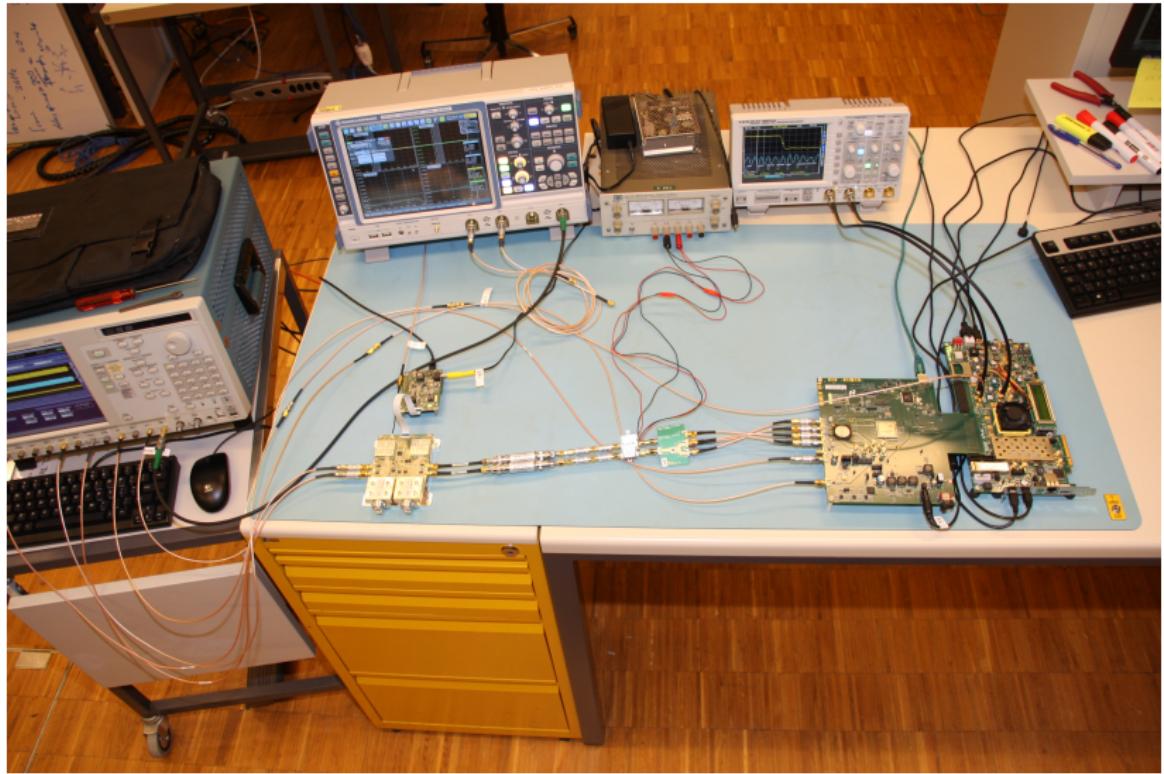
- Reset Synchronizers
- Global 5 MHz reset distribution clock
- Two global reset trees



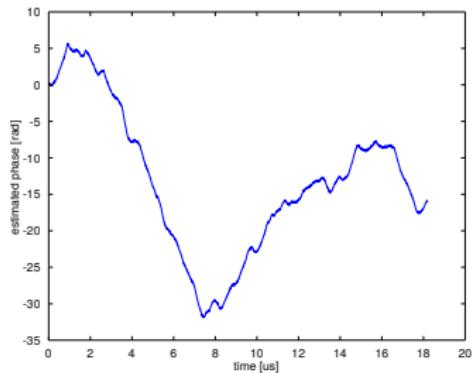
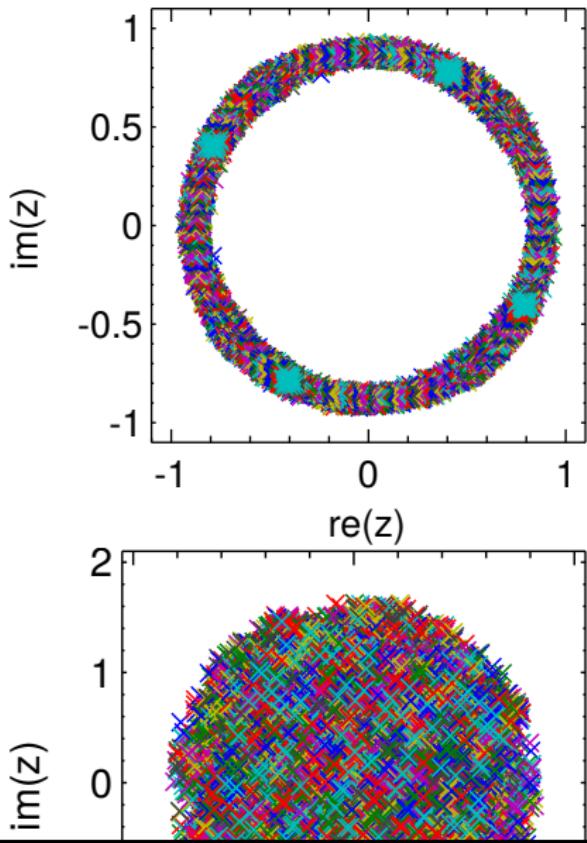
Test-Setup Block Diagram



Test-Setup Picture



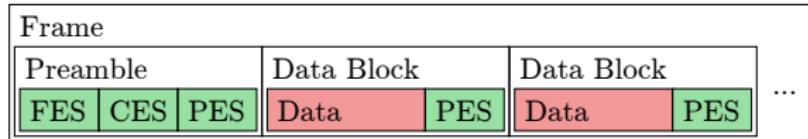
Phase Noise, First Results at 450 MS / s



Time Comparison

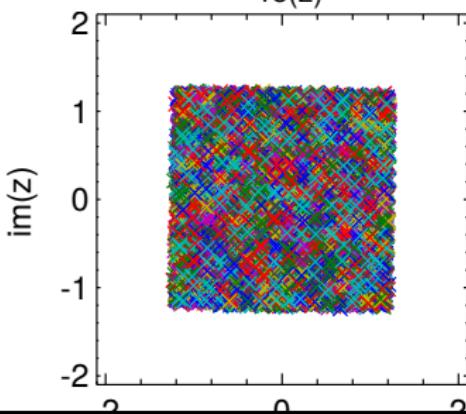
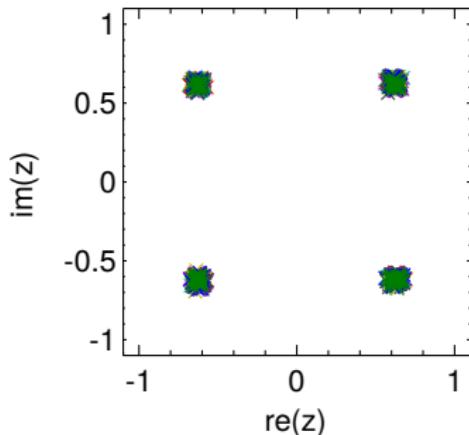
@1.8 GS/s 1800 symbols per 1 μ s
CIFS 2 μ s

Frame Structure



Modulation of Data Fiel	QAM-4	QAM-256
Modulation of Estimation Fields	BPSK	
Length of FES field	256 symbols	
Length of CES field	1152 symbols	
Length of PES field	32 symbols	
Length of Data Block	147 symbols	
Length of Data Field	115 symbols	
Length of Data Field	230 bits	920 bits

Result at Symbol Rate of 450 MS / s



Error Vector Magnitude

	EVM_D
channel correction	1.52
+ phase noise	-23.88
+ phase	-30.29

Raw Data Speed

QAM-4: $0.838 \frac{\text{GiBit}}{\text{s}}$

QAM-256: $3.353 \frac{\text{GiBit}}{\text{s}}$

Summary

Conclusion

- Multi-Gigabit Throughput is possible
- Sub-Nyquist Sampling works well

Outlook

- Framework can be used for further simulations
- FPGA is ready to be extended