

US 20240235498A9

(19) United States

(12) Patent Application Publication GU

(10) Pub. No.: US 2024/0235498 A9

(48) **Pub. Date: Jul. 11, 2024 CORRECTED PUBLICATION**

(54) BIAS CIRCUIT AND POWER AMPLIFIER

(71) Applicant: Shanghai WUQI Microelectronics

Co., Ltd., Shanghai (CN)

(72) Inventor: Qiang GU, Shanghai (CN)

(73) Assignee: Shanghai WUQI Microelectronics Co., Ltd., Shanghai (CN)

(21) Appl. No.: 18/109,876

(22) Filed: Feb. 15, 2023

Prior Publication Data

- (15) Correction of US 2024/0136985 A1 Apr. 25, 2024 See (30) Foreign Application Priority Data.
- (65) US 2024/0136985 A1 Apr. 25, 2024
- (30) Foreign Application Priority Data

Oct. 25, 2022 (CN) 2022113128826

Publication Classification

(51) Int. Cl. *H03F 3/213* (2006.01) *H03F 3/45* (2006.01)

(52) **U.S. CI.** CPC *H03F 3/213* (2013.01); *H03F 3/45179* (2013.01); *H03F 2200/21* (2013.01)

(57) ABSTRACT

Bias circuits for CMOS power amplifiers are provided. The bias circuit includes a feedback module, a first bias module, and a second bias module. The feedback module has a first input connected to a output common mode voltage, a second input connected to a reference voltage, and an output connected to gates of main amplification transistors in a first differential amplification module; based on a difference between the output common mode voltage and the reference voltage, the feedback module adjusts gate voltages of main amplification transistors until the output common mode voltage is equal to the reference voltage; the first bias module provides bias voltages for the first differential amplification module; the second bias module provides bias voltages for a second differential amplification module. The present disclosure adopts direct negative feedback and cascoded current mirrors, which realize accurate DC gate bias and accurate control of the output common mode voltage.

