



US 20240213290A1

(19) **United States**

(12) **Patent Application Publication**
KAMATANI et al.

(10) **Pub. No.: US 2024/0213290 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **SEMICONDUCTOR CHIP, METHOD FOR
MANUFACTURING THE SAME, AND
ELECTRONIC DEVICE**

Publication Classification

(51) **Int. Cl.**

H01L 27/146 (2006.01)

H01L 21/02 (2006.01)

(52) **U.S. Cl.**

CPC .. H01L 27/14645 (2013.01); **H01L 21/02422**

(2013.01); **H01L 27/1462** (2013.01); **H01L**

27/14627 (2013.01); **H01L 27/14689**

(2013.01)

(71) Applicant: **SONY SEMICONDUCTOR
SOLUTIONS CORPORATION,**
KANAGAWA (JP)

(72) Inventors: **RYOSUKE KAMATANI,**
KANAGAWA (JP); **TOMIYUKI**
YUKAWA, KANAGAWA (JP);
ATSUSHI YAMAMOTO,
KANAGAWA (JP)

(21) Appl. No.: **18/558,198**

(22) PCT Filed: **Feb. 4, 2022**

(86) PCT No.: **PCT/JP2022/004382**

§ 371 (c)(1),

(2) Date: **Oct. 31, 2023**

(30) **Foreign Application Priority Data**

May 17, 2021 (JP) 2021-083153

(57)

ABSTRACT

The present technology relates to a semiconductor chip, a method for manufacturing the same, and an electronic device that can improve reliability and durability. The semiconductor chip includes a solid-state imaging element such as a complementary metal oxide semiconductor (CMOS) image sensor (CIS), a glass substrate provided on the solid-state imaging element, and a lens formed on the glass substrate. The glass substrate has a groove having a depth of L1-L2 around a region where the lens is formed. The present technology can be applied, for example, to a semiconductor chip or the like that is a wafer level chip size package (WCSP) having a solid-state imaging element such as a CIS.

