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(54) **BIDIRECTIONAL I/O CIRCUIT AND INTEGRATED CIRCUIT INCLUDING BIDIRECTIONAL I/O CIRCUIT**

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(57) **ABSTRACT**

A bidirectional I/O circuit includes an output post driver configured to control an output signal of a bidirectional pad during a normal mode, a floating N-well network configured to apply a VDD-level bias to the output post driver based on an input signal of the bidirectional pad during a power down mode, and a post driver control circuit configured to set an input voltage level of the output post driver to a VDD level during the power down mode to prevent a leakage current path from being formed through the output post driver. A parasitic diode is formed between the drain of the first PMOS transistor and an N-well of the first PMOS transistor. The N-well of the first PMOS transistor is connected to the floating N-well network, and the source and the N-well of the first PMOS transistor are not physically connected to each other.