



US 20240213242A1

(19) **United States**

(12) **Patent Application Publication**
WEI

(10) **Pub. No.: US 2024/0213242 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **INTEGRATED CIRCUIT AND LOW
DROP-OUT LINEAR REGULATOR CIRCUIT**

(52) **U.S. Cl.**

CPC *H01L 27/0886* (2013.01); *H01L 23/4824*
(2013.01); *H01L 23/485* (2013.01); *H01L*
27/0207 (2013.01); *H01L 29/4238* (2013.01)

(71) Applicant: **Realtek Semiconductor Corporation,**
Hsinchu (TW)

(72) Inventor: **Tzu-Chieh WEI,** Hsinchu (TW)

(21) Appl. No.: **18/329,589**

(22) Filed: **Jun. 6, 2023**

(30) **Foreign Application Priority Data**

Dec. 26, 2022 (TW) 111150011

Publication Classification

(51) **Int. Cl.**

H01L 27/088 (2006.01)
H01L 23/482 (2006.01)
H01L 23/485 (2006.01)
H01L 27/02 (2006.01)
H01L 29/423 (2006.01)

(57)

ABSTRACT

An integrated circuit is provided and includes multiple first conductive segments, multiple second conductive segments, multiple third conductive segments, multiple fourth conductive segments, a first conductive line, and a second conductive line. The plurality of first conductive segments and the third conductive segments are arranged between multiple first gates, and the second conductive segments and the fourth conductive segments are arranged between multiple second gates. The first conductive line transmits a drain/source signal and is coupled to the first conductive segments and the second conductive segments. The second conductive line transmits a source/drain signal and is coupled to the third conductive segments and the fourth conductive segments. The plurality of third conductive segments and the fourth conductive segments are mirrored symmetrically with respect to the second conductive line in a plan view.

40

