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(54) **THREE-DIMENSIONAL SEMICONDUCTOR DEVICE HAVING A SUPPORT PATTERN IN CONTACT WITH A SIDE SURFACE OF A CONTACT PLUG**

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(57) **ABSTRACT**

The semiconductor device includes a substrate having a cell area and a via area; a transistor and a logic interconnection disposed over the substrate; a lower insulating layer covering the transistor and the logic interconnection; a lower conductive layer on the lower insulating layer in the cell area; a support pattern disposed on the lower insulating layer in the via area; a lower via plug having a side surface in contact with the support pattern and a bottom surface in contact with the logic interconnection; a word line stack disposed on the lower conductive layer in the cell area; an dielectric layer stack disposed on the support pattern in the via area; a vertical channel pillar penetrating the word line stack to be connected to the lower conductive layer; and an upper via plug penetrating the dielectric layer stack to be vertically aligned with the lower via plug.