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(54) **SEMICONDUCTOR MEMORY DEVICE**

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**ABSTRACT**

Disclosed is a semiconductor memory device including a peripheral gate structure on a substrate, bitlines disposed on the peripheral gate structure and extending in a first direction, a protruding insulating pattern including channel trenches, extending in a second direction intersecting the first direction, channel structures disposed on the bitlines in the channel trenches and including a metal oxide, first wordlines disposed on the channel structures and extending in the second direction, second wordlines disposed on the channel structures, extending in the second direction, and spaced apart from the first wordlines in the first direction, landing pads disposed on the channel structures and connected to the channel structures, pad separation patterns disposed on the protruding insulating pattern and separating the landing pads, first passage patterns connected to the protruding insulating pattern through pad separation patterns and formed of an oxide-based insulating material, and data storage patterns disposed on the landing pads.

