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(19) **United States**(12) **Patent Application Publication****Goyal et al.**(10) **Pub. No.: US 2024/0213978 A1**(43) **Pub. Date: Jun. 27, 2024**(54) **CIRCUIT TO REDUCE GATE INDUCED DRAIN LEAKAGE**(52) **U.S. Cl.**CPC **H03K 17/161** (2013.01)(71) Applicant: **NXP B.V.**, Eindhoven (NL)

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ABSTRACT(72) Inventors: **Saurabh Goyal**, Sonipat (IN); **Krishna Thakur**, GautumBudh Nagar (IN)

A bootstrap switch circuit includes a transistor-based switch controlled by a first gate signal and a leakage protection transistor controlled by a second gate signal configured to reduce gate induced drain leakage in the transistor-based switch. A first gate driver is included that produces a first gate signal at its output so that the first gate signal turns on the transistor-based switch during a sampling mode and turns off the transistor-based switch during a hold mode. A second gate driver is included that produces a second gate signal at its output and to receive the output signal of the bootstrap switch circuit so that the second gate signal turns on the leakage protection transistor during the sampling mode and turns off the leakage protection transistor during the hold mode and the second gate signal is based upon the output signal of the bootstrap switch circuit.

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