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(54) **TESTABLE TIME-TO-DIGITAL CONVERTER**

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(57) **ABSTRACT**

A delay selector includes a first multiplexer, a first inverter, a second multiplexer, and a second inverter. The first multiplexer has a first input coupled to an input of the delay selector. The first inverter is coupled between the input of the delay selector and a second input of the first multiplexer. The second multiplexer has a first input coupled to an output of the first multiplexer. The second inverter is coupled between the output of the first multiplexer and a second input of the second multiplexer.