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(54) **DATA RETENTION CIRCUIT AND METHOD**

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(57) **ABSTRACT**

A circuit includes first and second power nodes having differing first and second voltage levels, and a reference node having a reference voltage level. A master latch outputs a first data bit based on a received data bit; a slave latch includes a first inverter that outputs a second data bit based on the first data bit and a second inverter that outputs an output data bit based on a selected one of the first data bit or a third data bit; a level shifter outputs the third data bit based on a fourth data bit; and a retention latch outputs the fourth data bit based on the second data bit. The first and second inverters and the level shifter are coupled between the first power node and the reference node, and the retention latch includes a plurality of transistors coupled between the second power node and the reference node.