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PARK et al.(10) **Pub. No.: US 2023/0403855 A1**(43) **Pub. Date: Dec. 14, 2023**(54) **VERTICAL SEMICONDUCTOR DEVICE AND
METHOD FOR FABRICATING THE
VERTICAL SEMICONDUCTOR DEVICE****Publication Classification**(51) **Int. Cl.****H10B 43/27** (2006.01)**H01L 23/535** (2006.01)**H01L 23/532** (2006.01)**H01L 21/285** (2006.01)**H01L 21/768** (2006.01)**H10B 41/27** (2006.01)(52) **U.S. Cl.****CPC** **H10B 43/27** (2023.02); **H01L 23/535**(2013.01); **H01L 23/53271** (2013.01); **H01L****21/28525** (2013.01); **H01L 21/76823**(2013.01); **H01L 21/76834** (2013.01); **H01L****21/76895** (2013.01); **H01L 21/76805**(2013.01); **H10B 41/27** (2023.02)(71) Applicant: **SK hynix Inc.**, Icheon-si Gyeonggi-do
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(KR)(21) Appl. No.: **18/446,827**(22) Filed: **Aug. 9, 2023****Related U.S. Application Data**(63) Continuation of application No. 17/567,423, filed on
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(57)

ABSTRACT

A vertical semiconductor device includes: a lower structure;
a multi-layer stack structure including a source layer formed
over the lower structure and gate electrodes formed over the
source layer; a vertical structure penetrating the multi-layer
stack structure and including a channel layer insulated from
the source layer; a vertical source line spaced apart from the
vertical structure to penetrate the multi-layer stack structure
and contacting the source layer; and a horizontal source
channel contact suitable for coupling the source layer and
the channel layer and including a first conductive layer and
a second conductive layer that include different dopants.

