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(54) INTERNAL NODE JUMPER FOR MEMORY BIT CELLS

(71) Applicant: **Intel Corporation**, Santa Clara, CA (US)

(72) Inventors: **Smita SHRIDHARAN**, Beaverton, OR (US); **Zheng GUO**, Portland, OR (US); **Eric A. KARL**, Portland, OR (US); **George SHCHUPAK**, Zviya (IL); **Tali KOSINOVSKY**, Haifa (IL)

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(57) **ABSTRACT**

Memory bit cells having internal node jumpers are described. In an example, an integrated circuit structure includes a memory bit cell on a substrate. The memory bit cell includes first and second gate lines parallel along a second direction of the substrate. The first and second gate lines have a first pitch along a first direction of the substrate, the first direction perpendicular to the second direction. First, second and third interconnect lines are over the first and second gate lines. The first, second and third interconnect lines are parallel along the second direction of the substrate. The first, second and third interconnect lines have a second pitch along the first direction, where the second pitch is less than the first pitch. One of the first, second and third interconnect lines is an internal node jumper for the memory bit cell.