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(19) **United States**(12) **Patent Application Publication****Rueda et al.**(10) **Pub. No.: US 2023/0231034 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **LDMOS TRANSISTOR WITH IMPLANT
ALIGNMENT SPACERS****H01L 29/40** (2006.01)**H01L 29/78** (2006.01)(71) Applicant: **NXP USA, INC.**, AUSTIN, TX (US)(52) **U.S. Cl.****CPC** **H01L 29/66689** (2013.01); **H01L 29/086**
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ABSTRACT(21) Appl. No.: **18/190,452**(22) Filed: **Mar. 27, 2023****Related U.S. Application Data**(62) Division of application No. 17/316,091, filed on May
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A Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistor with implant alignment spacers includes a gate stack comprising a first nitride layer. The first nitride layer is formed on a silicon layer. The gate stack is separated from a substrate by a first oxide layer. The gate stack includes a polysilicon layer formed from the silicon layer, and a second oxide layer is formed on a sidewall of the polysilicon layer. A drain region of the LDMOS transistor is implanted with a first implant aligned to a first edge formed by the second oxide layer. A second nitride layer conformingly covers the second oxide layer. A nitride etch-stop layer conformingly covers the second nitride layer.

