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(54) **SEMICONDUCTOR MEMORY DEVICE**

(71) Applicant: SAMSUNG ELECTRONICS CO., LTD., Suwon-si (KR)

(72) Inventors: **Hosun JUNG**, Hwaseong-si (KR);

Minwu KIM, Hwaseong-si (KR); Jungwoo SONG, Hwaseong-si (KR); Wonchul LEE, Seongnam-si (KR)

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(57)**ABSTRACT**

A semiconductor memory device includes a substrate including memory cell, peripheral, and intermediate regions; a device isolation pattern; a partitioning pattern; bit lines extending in a first direction to a boundary between the intermediate and peripheral regions; storage node contacts on the memory cell region and filling a lower portion of a space between bit lines; landing pads on the storage node contacts; dummy storage node contacts on the intermediate region and filling a lower portion of a space between bit lines; dummy landing pads on the dummy storage node contacts; and a dam structure on the intermediate region, extending in the first direction, and having a bar shape, wherein the dummy landing pads are spaced apart from an edge of the dam structure in a second direction, and the dummy storage node contacts are in contact with the partitioning pattern.

