



US 20240215220A1

(19) **United States**

(12) **Patent Application Publication**
Fulford et al.

(10) **Pub. No.: US 2024/0215220 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **INTEGRATED NANOSHEET MEMORY
ELEMENTS, DEVICES AND METHODS**

(71) Applicant: **Tokyo Electron Limited**, Tokyo (JP)

(72) Inventors: **H. Jim Fulford**, Marianna, FL (US);
Mark I. Gardner, Cedar Creek, TX
(US)

(21) Appl. No.: **18/509,560**

(22) Filed: **Nov. 15, 2023**

Related U.S. Application Data

(60) Provisional application No. 63/434,389, filed on Dec.
21, 2022.

Publication Classification

(51) **Int. Cl.**
H10B 12/00 (2006.01)

(52) **U.S. Cl.**
CPC **H10B 12/30** (2023.02); **H10B 12/03**
(2023.02); **H10B 12/05** (2023.02)

(57) **ABSTRACT**

A memory element and method of formation is disclosed that includes a transistor integrated with a capacitor through a common nanosheet. The transistor includes a channel, a source region, a drain region and a gate component on at least one side of the channel between the source region and drain region. The channel is formed in a first portion of a nanosheet. The capacitor has a first capacitor component and second capacitor component separated by an insulator. The first capacitor component is provided in a second portion of the nanosheet.

