



US 20240179925A1

(19) **United States**

(12) **Patent Application Publication**  
**SUNG et al.**

(10) **Pub. No.: US 2024/0179925 A1**

(43) **Pub. Date: May 30, 2024**

(54) **SEMICONDUCTOR PACKAGE**

(71) Applicant: **Samsung Electronics Co., Ltd.**,  
Suwon-si (KR)

(72) Inventors: **Jaekyu SUNG**, Suwon-si (KR);  
**Joonghyun BAEK**, Suwon-si (KR);  
**Cheolwoo LEE**, Suwon-si (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.**,  
Suwon-si (KR)

(21) Appl. No.: **18/453,611**

(22) Filed: **Aug. 22, 2023**

(30) **Foreign Application Priority Data**

Nov. 25, 2022 (KR) ..... 10-2022-0160588

**Publication Classification**

(51) **Int. Cl.**  
**H10B 80/00** (2006.01)  
**H01L 23/00** (2006.01)  
**H01L 25/18** (2006.01)

(52) **U.S. Cl.**

CPC ..... **H10B 80/00** (2023.02); **H01L 24/06**  
(2013.01); **H01L 24/48** (2013.01); **H01L 24/49**  
(2013.01); **H01L 25/18** (2013.01); **H01L**  
**23/3128** (2013.01); **H01L 2224/06135**  
(2013.01); **H01L 2224/48091** (2013.01); **H01L**  
**2224/48106** (2013.01); **H01L 2224/48145**  
(2013.01); **H01L 2224/48227** (2013.01); **H01L**  
**2224/4903** (2013.01); **H01L 2224/49175**  
(2013.01)

(57)

**ABSTRACT**

A semiconductor package may include a substrate; at least one controller chip on the substrate; at least one chip structure on the substrate, the at least one chip structure including a buffer chip, an upper chip stack on the buffer chip, and a lower chip stack below the buffer chip; an upper wire electrically connecting the upper chip stack, the buffer chip, and the at least one controller chip; a lower wire electrically connecting the lower chip stack and the at least one controller chip; a connection wire electrically connecting the at least one controller chip to the substrate; and connection bumps below the substrate, the connection bumps being electrically connected to the at least one controller chip and the at least one chip structure.

