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(54) **SEMICONDUCTOR DEVICE INCLUDING MEMORY ELEMENTS**

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(57) **ABSTRACT**

In a semiconductor device including pillar-shaped Players standing erect on Player substrates, a random access memory cell includes a first gate insulating layer and a first gate conductor layer surrounding a lower P layer, a second gate insulating layer surrounding a first Player, a second gate conductor layer, and N^+ layers at either end of the first Player, a metal oxide semiconductor transistor includes a third gate insulating layer surrounding a second P layer, a third gate conductor layer, and N^+ layers at either end of the second Player, a read only memory cell includes a memory layer surrounding a third Player, a fourth gate conductor layer, and N^+ layers at either end of the third Player, and bottom portion positions of the first to third Players are substantially aligned with a single horizontal line.