



US 20240215218A1

(19) **United States**(12) **Patent Application Publication**
LI et al.(10) **Pub. No.: US 2024/0215218 A1**(43) **Pub. Date: Jun. 27, 2024**(54) **SEMICONDUCTOR STRUCTURE AND
FORMING METHOD THEREOF****Publication Classification**(51) **Int. Cl.**
H10B 12/00 (2006.01)(52) **U.S. Cl.**
CPC **H10B 12/0387** (2023.02); **H10B 12/056**
(2023.02); **H10B 12/36** (2023.02); **H10B**
12/373 (2023.02)(71) Applicant: **HeFeChip Corporation Limited,**
HONG KONG (CN)(72) Inventors: **Liang LI**, SINGAPORE (SG); **Chunyu**
WONG, Clifton Park, NY (US); **John**
H. ZHANG, Altamont, NY (US);
Yanzun LI, Lagrangeville, NY (US);
Huang LIU, Mechanicville, NY (US);
Yuan Lung LIN, Zhubei City (TW);
Haijiang YUAN, Shanghai (CN);
Chung-Chiang LIN, Qonglin (TW)(57) **ABSTRACT**

A semiconductor structure and a method of forming it are disclosed by the present application. Deep trench capacitors are formed in a substrate, and fin contacts formed by upper portions of inner electrodes in the deep trench capacitors are connected to fins on a surface of the substrate. At least one of word lines formed on the substrate pass over and are separated by a word line isolation layer from the inner electrodes. The word line isolation layer covers portions of the inner electrodes between a buried oxide layer and the fin contacts, while the fins are exposed therefrom.

(21) Appl. No.: **18/088,944**(22) Filed: **Dec. 27, 2022**