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(54) **LOW OVERHEAD TRANSITION ENCODING CODES**

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(57)

ABSTRACT

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A processing circuit configured to: receive original data; partition the original data into a plurality of original q-bit words; assemble a data packet including N original q-bit words from the plurality of original q-bit words; identify a first encoder value and a second encoder value that are absent from the values of the N original q-bit words; encode the N original q-bit words based on a one-to-one mapping from q-bit original values to q-bit encoded values based on the first encoder value and the second encoder value to generate N encoded q-bit payload words, the N encoded q-bit payload words being free of words that are all-zeroes and free of words that are all-ones; generate a key representing the first encoder value and the second encoder value; and transmit the key and the N encoded q-bit payload words.

