



US 20220385303A1

(19) **United States**

(12) **Patent Application Publication**  
**AVRAHAM et al.**

(10) **Pub. No.: US 2022/0385303 A1**

(43) **Pub. Date: Dec. 1, 2022**

(54) **MULTI-RATE ECC PARITY FOR FAST SLC READ**

(52) **U.S. Cl.**

CPC ..... *H03M 13/098* (2013.01); *H03M 13/118* (2013.01); *H03M 13/1105* (2013.01); *G06F 11/1068* (2013.01)

(71) Applicant: **Western Digital Technologies, Inc.**,  
San Jose, CA (US)

(72) Inventors: **Dudy David AVRAHAM**, Even Yehuda (IL); **Ran ZAMIR**, Ramat Gan (IL); **Eran SHARON**, Rishon Lezion (IL)

(21) Appl. No.: **17/331,346**

(22) Filed: **May 26, 2021**

**Publication Classification**

(51) **Int. Cl.**

*H03M 13/09* (2006.01)

*H03M 13/11* (2006.01)

*G06F 11/10* (2006.01)

(57) **ABSTRACT**

A data storage device includes a memory device and a controller coupled to the memory device. The controller is configured to create a dual parity matrix. The dual parity matrix includes a full parity form that includes a payload, a first parity portion, and a second parity portion and a reduced parity form that includes the payload and the first parity portion. The second parity portion is 0. The controller is further configured to create an incremental parity construction matrix. The incremental parity construction matrix includes two arrays. A first array includes a first payload portion, a first, first parity portion, and a first, second parity portion and a second array includes a second payload portion, a second, first parity portion, and a second, second parity portion. The incremental parity construction matrix is arranged in either a block triangular construction or a block diagonal construction.

