US 20240215263A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0215263 A1**

BARRAUD et al. (43) **Pub. Date: Jun. 27, 2024**

(54) **MEMORY DEVICE COMPRISING LARGE CONTACT SURFACES BETWEEN THE CONDUCTION CHANNEL AND THE CONTACT REGIONS**

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(21) Appl. No.: **18/393,200**

(22) Filed: **Dec. 21, 2023**

(30) **Foreign Application Priority Data**

Dec. 22, 2022 (FR) 22 14257

Publication Classification

(51) **Int. Cl.**
H10B 63/00 (2006.01)

(52) **U.S. Cl.**
CPC ***H10B 63/30*** (2023.02); ***H10B 63/80*** (2023.02)

(57) **ABSTRACT**

A memory device (**100**) comprising at least one memory stack (**158**) electrically connected in series with a selection transistor, comprising:

- a semiconductor layer (**120**) first areas (**122**) of which are superimposed and form a channel;
- an electrostatic control gate (**110**) and a gate dielectric layer (**112**) such that parts of the gate dielectric layer are each arranged between a part (**106**, **108**) of the gate and one of the first areas;
- dielectric spacers (**114**) arranged against sidewalls of the gate;
- contact regions (**116**, **118**) electrically coupled to the first areas via second areas (**124**) of the semiconductor layer extending between the contact regions and the spacers, one of the contact regions (**118**) comprising the memory stack;
- and wherein the second areas form a continuous layer with the first areas.