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MEMORY DEVICE****Publication Classification**(51) **Int. Cl.****H10B 51/30** (2006.01)**G11C 11/22** (2006.01)**H01L 27/12** (2006.01)(52) **U.S. Cl.**CPC **H10B 51/30** (2023.02); **H01L 27/1211**
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(57)

ABSTRACT

Various embodiments of the present disclosure are directed towards a method of forming a ferroelectric memory device. In the method, a pair of source/drain regions is formed in a substrate. A gate dielectric and a gate electrode are formed over the substrate and between the pair of source/drain regions. A polarization switching structure is formed directly on a top surface of the gate electrode. By arranging the polarization switching structure directly on the gate electrode, smaller pad size can be realized, and more flexible area ratio tuning can be achieved compared to arranging the polarization switching structure under the gate electrode with the aligned sidewall and same lateral dimensions. In addition, since the process of forming gate electrode can endure higher annealing temperatures, such that quality of the ferroelectric structure is better controlled.

