

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0213177 A1 Park

Jun. 27, 2024 (43) **Pub. Date:**

(54) FABRICATION METHOD OF SEMICONDUCTOR PACKAGE

(71) Applicant: SAMSUNG ELECTRONICS CO., LTD., Suwon-si (KR)

Inventor: Young-Woo Park, Cheonan-si (KR)

(21) Appl. No.: 18/429,039

(22) Filed: Jan. 31, 2024

Related U.S. Application Data

(60) Division of application No. 17/117,547, filed on Dec. 10, 2020, now Pat. No. 11,923,319, which is a continuation of application No. 16/224,556, filed on Dec. 18, 2018, now Pat. No. 10,943,872.

(30)Foreign Application Priority Data

Jun. 26, 2018 (KR) 10-2018-0073589

Publication Classification

(51)	Int. Cl.	
	H01L 23/552	(2006.01)
	H01L 21/48	(2006.01)
	H01L 21/56	(2006.01)
	H01L 23/00	(2006.01)
	H01L 23/053	(2006.01)

H01L 23/31	(2006.01)
H01L 23/498	(2006.01)
H01L 25/00	(2006.01)
H01L 25/065	(2006.01)
H01L 25/10	(2006.01)

(52) U.S. Cl. CPC H01L 23/552 (2013.01); H01L 21/4817 (2013.01); H01L 21/4853 (2013.01); H01L 21/565 (2013.01); H01L 23/053 (2013.01); H01L 23/3128 (2013.01); H01L 23/49838 (2013.01); H01L 24/48 (2013.01); H01L 25/0657 (2013.01); H01L 25/105 (2013.01); H01L 25/50 (2013.01); H01L 2224/48157 (2013.01); H01L 2225/06506 (2013.01); H01L 2225/0651 (2013.01); H01L 2225/06537 (2013.01); H01L 2225/06562 (2013.01); H01L 2225/06586 (2013.01); H01L 2225/1023 (2013.01); H01L 2225/1058 (2013.01); H01L 2924/3025 (2013.01)

(57)**ABSTRACT**

A method of fabricating a semiconductor package includes mounting at least one semiconductor chip to a package substrate, forming a shielding wall around the at least one semiconductor chip, forming a molded body on the package substrate in a space surrounded by the shielding wall, and forming a shielding cover covering the molding unit and in contact with the shielding wall.

