US 20230232638A1

(19) **United States**

(12) **Patent Application Publication**

Wang et al.

(10) **Pub. No.: US 2023/0232638 A1**

(43) **Pub. Date: Jul. 20, 2023**

(54) **MEMORY ARRAY**

(71) Applicant: **UNITED MICROELECTRONICS CORP.**, Hsin-Chu City (TW)

(72) Inventors: **Hui-Lin Wang**, Taipei City (TW); **Ju-Chun Fan**, Tainan City (TW); **Ching-Hua Hsu**, Kaohsiung City (TW); **Chun-Hao Wang**, Taipei City (TW); **Yi-Yu Lin**, Taichung City (TW); **Dong-Ming Wu**, Taichung City (TW); **Po-Kai Hsu**, Tainan City (TW)

(73) Assignee: **UNITED MICROELECTRONICS CORP.**, Hsin-Chu City (TW)

(21) Appl. No.: **17/673,760**

(22) Filed: **Feb. 16, 2022**

(30) **Foreign Application Priority Data**

Jan. 14, 2022 (CN) 202210041541.3

Publication Classification

(51) **Int. Cl.**

H01L 27/22	(2006.01)
H01L 43/02	(2006.01)
H01L 43/08	(2006.01)
G11C 5/02	(2006.01)
H01L 23/522	(2006.01)
H01L 23/528	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 27/226*** (2013.01); ***H01L 43/02*** (2013.01); ***H01L 43/08*** (2013.01); ***G11C 5/02*** (2013.01); ***H01L 23/5226*** (2013.01); ***H01L 23/5283*** (2013.01)

(57) **ABSTRACT**

Abstract of Disclosure A memory array includes at least one strap region, at least two sub-arrays, a plurality of staggered, dummy magnetic storage elements, and a plurality of bit line structures. The strap region includes a plurality of source line straps and a plurality of word line straps. The two sub-arrays include a plurality of staggered, active magnetic storage elements. The two sub -arrays are separated by the strap region. The staggered, dummy magnetic storage elements are disposed within the strap region. The bit line structures are disposed in the two sub-arrays, and each of the bit line structures is disposed above and directly connected with at least one of the staggered, active magnetic storage elements.