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(54) **EMBEDDED DIE PACKAGING FOR POWER SEMICONDUCTOR DEVICES FOR IMPROVED SOLDER RELIABILITY**

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(57) **ABSTRACT**

A laminated embedded die package for a power semiconductor device, wherein a laminated body comprises a layup of a plurality of electrically conductive layers and dielectric layers. The die may be mounted in thermal contact with a leadframe. Electrical connections between contact areas of the die, external contact pads of the package and internal conductive layers are made by electrically conductive vias or microvias, formed by laser drilling of vias through the dielectric layers, which are then filled with conductive metal. A plurality of unfilled half-vias are arranged around edges of the laminated body adjacent external contact pads. Half-vias are formed by laser or mechanical drilling along scribe lines before singulation of packages. Surface plating of the half-vias comprises a solder wettable material. The half-vias are unfilled to form a wettable flank which allows for lateral wicking of solder during surface mounting, to facilitate optical inspection of solder reliability.