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(54) **INTEGRATED ASSEMBLIES AND METHODS OF FORMING INTEGRATED ASSEMBLIES**

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(57) **ABSTRACT**

Some embodiments include an integrated assembly having a first memory region, a second memory region offset from the first memory region, and an intermediate region between the first and second memory regions. Channel-material-pillars are arranged within the memory regions. Conductive posts are arranged within the intermediate region. A panel extends across the memory regions and the intermediate region. The panel is laterally between a first memory-block-region and a second memory-block-region. Doped-semiconductor-material is within the memory regions and the intermediate region, and is directly adjacent to the panel. The doped-semiconductor-material is at least part of conductive source structures within the memory regions. Insulative rings laterally surround lower regions of the conductive posts and are between the conductive posts and the doped-semiconductor-material. Insulative liners are along upper regions of the conductive posts. Some embodiments include methods of forming integrated assemblies.