US 20230232623A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2023/0232623 A1**

Fan et al. (43) **Pub. Date: Jul. 20, 2023**

(54) **METHOD OF MANUFACTURING NON-VOLATILE MEMORY DEVICE**

(71) Applicant: **IOTMEMORY TECHNOLOGY INC.**, Taipei City (TW)

(72) Inventors: **Der-Tsyr Fan**, Taoyuan City (TW); **I-Hsin Huang**, Taoyuan City (TW); **Chen-Ming Tsai**, Miaoli County (TW); **Yu-Ming Cheng**, Yilan County (TW)

(73) Assignee: **IOTMEMORY TECHNOLOGY INC.**, Taipei City (TW)

(21) Appl. No.: **17/578,414**

(22) Filed: **Jan. 18, 2022**

Publication Classification

(51) **Int. Cl.**
H01L 27/11521 (2006.01)
H01L 27/11519 (2006.01)

(52) **U.S. Cl.**
CPC .. ***H01L 27/11521*** (2013.01); ***H01L 27/11519*** (2013.01)

(57) **ABSTRACT**

A method of manufacturing a non-volatile memory includes the following steps. A stacked structure is formed on a substrate and includes a gate dielectric layer, an assist gate, an insulation layer, and a sacrificial layer stacked in order. A tunneling dielectric layer is formed at one side of the stacked structure. A floating gate is formed on the tunneling dielectric layer. The stacked structure is etched until an uppermost edge of the floating gate is higher than a top surface of the insulation layer. A dielectric material layer is formed to cover sidewalls of the floating gate. The dielectric material layer is etched to form an etched dielectric material layer and expose the uppermost edge of the floating gate. An upper gate structure is formed on the etched dielectric material layer, where a portion of the etched dielectric material layer is disposed between the upper gate structure and the substrate.