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(54) **ERROR-FEEDBACK SAR-ADC**

(71) Applicant: **Nordic Semiconductor ASA**, Trondheim (NO)

(72) Inventors: **Erlend Strandvik**, Trondheim (NO); **Harald Garvik**, Trondheim (NO)

(73) Assignee: **Nordic Semiconductor ASA**, Trondheim (NO)

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(57) **ABSTRACT**

Analog to digital conversion circuitry has an input sampling buffer, which has an input sampling capacitor for sampling an analog signal. The conversion circuitry also has a successive-approximation-register analog to digital converter (SAR-ADC) which converts the sampled analog signal to a digital signal. The input sampling buffer has an amplifier and a gain-control capacitor, and has an amplification configuration and an error-feedback configuration. In the amplification configuration, the input sampling capacitor is coupled to the amplifier and gain-control capacitor, with the gain-control capacitor connected in feedback with the amplifier, for applying gain to the sampled analog signal. In the error-feedback configuration, the gain-control capacitor is decoupled from the input sampling capacitor and receives a residue voltage from the SAR-ADC, such that the level of the analog signal determined in the amplification configuration varies depending on the residue voltage received onto the gain-control capacitor in the error-feedback configuration.