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LEE(10) **Pub. No.: US 2023/0232607 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SEMICONDUCTOR DEVICE STRUCTURE
AND METHOD MAKING THE SAME**(52) **U.S. Cl.**CPC *H10B 12/0387* (2023.02); *H10B 12/373*
(2023.02); *H01L 28/91* (2013.01)(71) Applicant: **ChangXin Memory Technologies, Inc.**,
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ABSTRACT(21) Appl. No.: **17/420,124**(22) PCT Filed: **Dec. 3, 2020**(86) PCT No.: **PCT/CN2020/133567**

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The present disclosure is in the field of semiconductor devices, in particular, to a semiconductor structure and a method of forming the same. The semiconductor structure includes: a substrate with a trench extending in a direction of the substrate; a capacitor fabricated in the trench, the capacitor includes a lower electrode disposed on an inner wall of the trench, a dielectric combination layer disposed on the lower electrode, and an upper electrode disposed on the dielectric combination layer; the dielectric combination layer includes a stacked structure composed of a nitride layer and an oxide layer. The device can increase the capacitance of the capacitor significantly and reduce the occurrence of charge leakage, thereby improving the electrical performance of the semiconductor memory device.

