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(54) **ELIMINATION OF PROBABILITY OF BIT ERRORS IN SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG-TO-DIGITAL CONVERTER (ADC) LOGIC**

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(57) **ABSTRACT**

Systems and methods related to successive approximation register (SAR) analog-to-digital converters (ADCs) are provided. A method for performing successive approximation registers (SAR) analog-to-digital conversion includes comparing, using a comparator, a first digital-to-analog (DAC) output voltage to a sampled analog input voltage to generate a comparison result including a first positive output and a first negative output; and gating, using gating logic circuitry, at least one of the first positive output or the first negative output of the comparator to next logic circuitry, the gating based at least in part on a digital feedback comprising information associated with at least one of an opposite polarity of the first positive output or an opposite polarity of the first negative output.