



US 20220386452A1

(19) **United States**(12) **Patent Application Publication**

Asl et al.

(10) **Pub. No.: US 2022/0386452 A1**(43) **Pub. Date: Dec. 1, 2022**(54) **INTERLACED CROSSTALK CONTROLLED TRACES, VIAS, AND CAPACITORS**(71) Applicant: **Cisco Technology, Inc.**, San Jose, CA (US)(72) Inventors: **Shadi Ebrahimi Asl**, Cary, NC (US); **Stephen Aubrey Searce**, Apex, NC (US); **Quinn Gaumer**, Durham, NC (US); **Linda W. Scott**, Winter Springs, FL (US)(21) Appl. No.: **17/335,591**(22) Filed: **Jun. 1, 2021****Publication Classification**(51) **Int. Cl.**

<b>H05K 1/02</b>	(2006.01)
<b>H05K 1/18</b>	(2006.01)
<b>H05K 1/11</b>	(2006.01)
<b>H05K 3/00</b>	(2006.01)
<b>H05K 3/30</b>	(2006.01)
<b>H05K 3/42</b>	(2006.01)

(52) **U.S. Cl.**

CPC ..... **H05K 1/0218** (2013.01); **H05K 1/181** (2013.01); **H05K 1/0298** (2013.01); **H05K 1/115** (2013.01); **H05K 3/0047** (2013.01); **H05K 3/303** (2013.01); **H05K 3/42** (2013.01); **H05K 2201/10015** (2013.01)

(57)

**ABSTRACT**

A multilayer printed circuit board having a stackup including an upper half of the stackup and a lower half of the stackup, the multilayer printed circuit board having a top exposed surface and a bottom exposed surface, a first trace and via structure, having one portion disposed on the top exposed surface and another portion disposed within the upper half of the stackup, a second trace and via structure, having one portion disposed on the top exposed surface and another portion disposed within the upper half of the stackup, and first electrical components and second electrical components disposed on the top exposed surface of the multilayer printed circuit board and associated, respectively, with the first trace and via structure and the second trace and via structure, wherein the first electrical components are mounted orthogonally with respect to the second electrical components.

