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(54) **TIME INTERLEAVING CIRCUIT HAVING GLITCH MITIGATION**

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(57) **ABSTRACT**

Provided is a time interleaving circuit to mitigate glitches. A first loading stage outputs first data representative of first serialized data. A second loading stage generates second serialized data. The second loading stage receives the first data output by the first loading stage. In response to the first data having a first state, the time interleaving circuit inverts the second serialized data to generate second data representative of the second serialized data. In response to the first data having a second state, the time interleaving circuit outputting the second data without inverting the second serialized data. Exclusive disjunction logic receives the second data and operates on the first data and the second data to generate output data.