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(54) **ULTRA-WIDEBAND ATTENUATOR WITH LOW PHASE VARIATION AND IMPROVED STABILITY WITH RESPECT TO TEMPERATURE VARIATIONS**

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(57) **ABSTRACT**

A method for improving the stability and reducing phase variations of an ultra-wideband attenuator, with respect to temperature variations, comprising the steps of providing an attenuator implemented in π-topology and consisting of a serial path between the input and the output of the attenuator, including a first serial resistor Rs_1 connected to the input, followed by a serial inductor Ls, followed by a second serial resistor Rs_2 connected to the output; a first transistor T_1 bridging between the input and the output, for controlling the impedance of the serial path by a first control input provided to the first transistor T_1; a first parallel path between the input and ground, including a first parallel transistor T_{2a} followed by first parallel resistor Rp_1; a second parallel path between the output and ground, including a second parallel transistor T_{2b} followed by second parallel resistor Rp_2; a second control input commonly provided to first parallel transistor T_{2a} and to the second parallel transistor T_{2b}, for controlling the impedance of the first and second parallel paths; unifying the serial resistors to a common serial resistor Rs and splitting the serial inductor Ls to two serial inductors Ls_1 and Ls_2, such that one serial inductor is connected between the input and a first contract of the common serial resistor Rs and the other serial inductor is connected between the output and the other contact of the common serial resistor Rs; splitting the parallel resistor Rp_1 to two smaller resistors, connecting a first smaller resistor to the input, connecting a second smaller resistor to the first smaller resistor via the first parallel transistor T_{2a} and to ground via a third parallel transistor T_{3a}; splitting the parallel resistor Rp_2 to two smaller resistors, connecting a third smaller resistor to the output, connecting a fourth smaller resistor to the third smaller resistor via the second parallel transistor T_{2b} and to ground via a fourth parallel transistor T_{3b}; connecting a first feedback capacitor Cfb_1 between the common point connecting between the ungrounded port of the second parallel transistor T_{3a} and the first contract of the common serial resistor Rs and connecting a second feedback capacitor Cfb_2 between the common point connecting between the ungrounded port of the fourth parallel transistor T_{3b} and the second contract of the common serial resistor Rs; upon controlling the first and second parallel transistors T_{2a} and T_{2b} by the second control input, simultaneously controlling also the third and the fourth parallel transistors T_{3a} and T_{3b} by the second control input; controlling the first and the second control inputs to obtain a desired attenuation between the input and output of the attenuator.