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(54) **OCTAGONAL INTERCONNECT WIRING FOR ADVANCED LOGIC**

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(57) **ABSTRACT**

A chip is manufactured using a method for forming a back-end-of-line (BEOL) layer on an IC chip surface comprises providing a first layer on top of a substrate layer of the IC chip, the first layer comprising a bottom portion of a metallic fill region having a first width as seen in a vertical cross-section of the IC chip. The method further provides a second layer on top of the first layer. The second layer comprises a middle portion of the metallic fill region having a second width that is wider than the bottom portion of the metallic fill region. The method provides a third layer on top of the second layer. The third layer comprises a top portion of the metallic fill region having a third width as seen in the vertical cross-section of the IC chip that is narrower than the middle portion of the metallic fill region.