



US 20240213355A1

(19) **United States**

(12) **Patent Application Publication**
SASAKI et al.

(10) **Pub. No.: US 2024/0213355 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **SEMICONDUCTOR DEVICE AND METHOD
FOR MANUFACTURING SEMICONDUCTOR
DEVICE**

(52) **U.S. Cl.**
**CPC H01L 29/66462 (2013.01); H01L 29/2003
(2013.01); H01L 29/7786 (2013.01)**

(71) Applicant: **SUMITOMO ELECTRIC DEVICE
INNOVATIONS, INC., Kanagawa (JP)**

(57) **ABSTRACT**

(72) Inventors: **Atsuya SASAKI, Kanagawa (JP);
Yukinori NOSE, Kanagawa (JP)**

(21) Appl. No.: **18/545,295**

(22) Filed: **Dec. 19, 2023**

(30) **Foreign Application Priority Data**

Dec. 26, 2022 (JP) 2022-208886

Publication Classification

(51) **Int. Cl.**
H01L 29/66 (2006.01)
H01L 29/20 (2006.01)
H01L 29/778 (2006.01)

A semiconductor device includes a first nitride semiconductor layer having a first surface, and a first recess formed in the first surface, a second nitride semiconductor layer provided inside the first recess, a first insulating film, covering the first nitride semiconductor layer and the second nitride semiconductor layer, and having a first opening exposing at least a portion of the second nitride semiconductor layer, and an interconnect layer making ohmic contact with the second nitride semiconductor layer through the first opening. The second nitride semiconductor layer has a second surface opposing the interconnect layer. A second recess, continuous with the first opening, is formed in the second surface. The interconnect layer makes direct contact with the second nitride semiconductor layer at an inner surface of the second recess.

