US 20220368345A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2022/0368345 A1

Secareanu (43) Pub. Date: Nov. 17, 2022

(54) **HARDWARE IMPLEMENTABLE DATA COMPRESSION/DECOMPRESSION ALGORITHM**

(71) Applicant: **Radu Mircea Secareanu**, Phoenix, AZ (US)

(72) Inventor: **Radu Mircea Secareanu**, Phoenix, AZ (US)

(21) Appl. No.: **17/398,728**

(22) Filed: **Aug. 10, 2021**

Related U.S. Application Data

(60) Provisional application No. 63/189,247, filed on May 17, 2021.

Publication Classification

(51) **Int. Cl.**

H03M 7/30 (2006.01)

H03M 7/40 (2006.01)

(52) **U.S. Cl.**

CPC ***H03M 7/3064*** (2013.01); ***H03M 7/4031*** (2013.01); ***H03M 7/6005*** (2013.01)

(57) **ABSTRACT**

A hardware implementable lossless data compression decompression algorithm is disclosed, where the input data string is described in term of consecutive groups of alternating same type bits, where one of these groups of same type bits is defined as a preferred group with the other groups having either lower or higher number of same type bits, where the data string is partitioned into variable length processing strings where the variable length is determined by the occurrence of the preferred group or of a determined number of bits consisting of groups of lower number of same type bits, where these variable length processing strings are processed function of the configuration and content of each processing string only, where consecutive processing strings are additionally processed based on their content only, where processing is performed in a loop until a certain target performance is achieved, where processing is done without any data analysis, and where no negative compression gain is achieved for any content of an input string.