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(54) THREE-DIMENSIONAL NAND MEMORY DEVICE AND METHOD OF FORMING THE

- (71) Applicant: Yangtze Memory Technologies Co., Ltd., Wuhan (CN)
- (72) Inventors: Beibei LI, Wuhan Hubei (CN); Wei XU, Wuhan Hubei (CN); Bin YUAN, Wuhan Hubei (CN); ZongLiang HUO, Wuhan Hubei (CN); Lei XUE, Wuhan Hubei (CN)
- (73) Assignee: Yangtze Memory Technologies Co., Ltd., Wuhan (CN)
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(57)ABSTRACT

A semiconductor device includes Number of decks that are stacked up in a Z direction and extend in parallel with an X-Y plane. N is an integer greater than 1. Each deck includes alternating word line layers and insulating layers. The N number of decks includes a first deck and a second deck adjacent to the first deck. A multi-deck gate line slit (GLS) structure extends in an X-Z plane and cuts through the word line layers and the insulating layers of the N number of decks. The multi-deck GLS structure has a first sidewall in the first deck, a second sidewall in the second deck, and a third sidewall at a border between the first deck and the second deck. The third sidewall connects the first sidewall and the second sidewall.



