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(54) CIRCUIT FOR PREVENTING LATCH-UP AND INTEGRATED CIRCUIT

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(57) **ABSTRACT**

Disclosed is an circuit for preventing latch-up, comprising a first transistor, a second transistor of a type opposite to that of the first transistor, and a control circuit, wherein a control terminal of the first transistor receives a first control voltage and a first terminal of the first transistor receives a first supply voltage; a control terminal of the second transistor receives a second control voltage, and is connected to a second terminal of the first transistor; a first terminal of the second transistor is connected to the control terminal of the first transistor, and a second terminal of the second transistor receives a second supply voltage. The control circuit is coupled on a path formed by the first transistor and the second transistor between the first supply voltage and the second supply voltage for disconnecting the path when the first control voltage and/or the second control voltage is out of a predetermined range. The circuit for preventing latch-up provided by the present invention, by introducing the control circuit on the path formed by the first transistor and the second transistor between the first supply voltage and the second supply voltage, can disconnect the path when the first control voltage and/or the second control voltage is out of the predetermined range, so that a latch-up effect is prevented from occurring during power-on phase.