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(54) VERTICAL FIELD EFFECT TRANSISTOR

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DEVICE AND METHOD OF FABRICATION

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(57)ABSTRACT

A method and vertical FET device fabricated in GaN or other suitable material. The device has a selective area implant region comprising an activated impurity configured from a bottom portion of a recessed regions, and substantially free from ion implant damage by using an annealing process. A p-type gate region is configured from the selective area implant region, and each of the recessed regions is characterized by a depth configured to physically separate an n+ type source region and the p-type gate region such that a low reverse leakage gate-source p-n junction is achieved. An extended drain region is configured from a portion of an n-type GaN region underlying the recessed regions. An n+ GaN region is formed by epitaxial growth directly overlying the backside region of the GaN substrate and a backside drain contact region configured from the n+ type GaN region overlying the backside region.

