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(54) **CONTROLLING DUTY CYCLE DISTORTION WITH DIGITAL CIRCUIT**

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(57) **ABSTRACT**

A method controls duty cycle distortion of clock signals. An electronic device obtains an input clock signal having a first frequency and a sampling clock signal having a second frequency that is lower than the first frequency. The sampling clock signal has a random noise distribution. The sampling clock signal is applied to sample high voltage duty cycles and low voltage duty cycles of the input clock signal for a duration of time to obtain a sampling result. The electronic device determines a duty cycle distortion level of the input clock signal in the duration of time based on the sampling result. A duty cycle control signal is generated based on the duty cycle distortion level to control the high voltage duty cycles of the input clock signal.