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(19) **United States**(12) **Patent Application Publication**
CHIU(10) **Pub. No.: US 2024/0244827 A1**(43) **Pub. Date: Jul. 18, 2024**(54) **MEMORY DEVICE HAVING IMPROVED P-N
JUNCTION AND MANUFACTURING
METHOD THEREOF**(52) **U.S. Cl.**CPC **H10B 12/34** (2023.02); **H10B 12/053**
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(57)

ABSTRACT

The present application provides a memory device including a semiconductor substrate having a first surface and defined with an active area under the first surface; a gate structure adjacent to the active area and indented into the semiconductor substrate from the first surface; a doped member extending into the semiconductor substrate and surrounded by the active area; a conductive layer including a first portion extending into the semiconductor substrate from the first surface and a second portion disposed over the doped member and coupled to the first portion; and a first insulating layer disposed adjacent to the first portion of the conductive layer and between the doped member and the active area of the semiconductor substrate, wherein the first portion of the conductive layer is disposed between the gate structure and the doped member. A method of manufacturing the memory device is also disclosed.

