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(54) ELECTRONIC CIRCUIT

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(57) **ABSTRACT**

A spike generation circuit includes a first CMOS inverter connected between a first power supply and a second power supply, an output node of the first CMOS inverter being coupled to a first node that is an intermediate node coupled to an input terminal to which an input signal is input, a switch connected in series with the first CMOS inverter, between the first power supply and the second power supply, a first inverting circuit that outputs an inversion signal of a signal of the first node to a control terminal of the switch, and a delay circuit that delays the signal of the first node, outputs a delayed signal to an input node of the first CMOS inverter, and outputs an isolated output spike signal to an output terminal.