US 20220368317A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0368317 A1**

Samra et al. (43) **Pub. Date: Nov. 17, 2022**

(54) **FLIP FLOP STANDARD CELL**

(71) Applicant: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsinchu (TW)

(72) Inventors: **Nick Samra**, Austin, TX (US); **Stefan Rusu**, Sunnyvale, CA (US); **Ta-Pen Guo**, Taipei City (TW)

(21) Appl. No.: **17/815,983**

(22) Filed: **Jul. 29, 2022**

Related U.S. Application Data

(63) Continuation of application No. 17/201,617, filed on Mar. 15, 2021, now Pat. No. 11,437,982, which is a continuation of application No. 16/428,123, filed on May 31, 2019, now Pat. No. 10,951,201.

(60) Provisional application No. 62/764,735, filed on Aug. 15, 2018.

Publication Classification

(51) **Int. Cl.**

H03K 3/037	(2006.01)
G11C 11/412	(2006.01)
G01R 31/3177	(2006.01)
G01R 31/317	(2006.01)
G11C 11/419	(2006.01)

(52) **U.S. Cl.**

CPC ***H03K 3/0372*** (2013.01); ***G11C 11/412*** (2013.01); ***G01R 31/3177*** (2013.01); ***G01R 31/31713*** (2013.01); ***G11C 11/419*** (2013.01); *G11C 11/418* (2013.01)

(57) **ABSTRACT**

A flip flop standard cell that includes a data input terminal configured to receive a data signal, clock input terminal configured to receive a clock signal, a data output terminal, and a latch. A bit write circuit is configured to receive a bit write signal. The received data signal is latched and provided at the output terminal in response to the bit write signal and the clock signal. A hold circuit is configured to receive a hold signal, and the received data signal is not latched and provided at the data output terminal in response to the hold signal and the clock signal.