US 20220352898A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0352898 A1**

LIU et al. (43) **Pub. Date: Nov. 3, 2022**

(54) **METHOD FOR UP-CONVERTING CLOCK SIGNAL, CLOCK CIRCUIT AND DIGITAL PROCESSING DEVICE**

(71) Applicant: **SHENZHEN MICROBT ELECTRONICS TECHNOLOGY CO., LTD.**, GUANGDONG (CN)

(72) Inventors: **Jianbo LIU**, GUANGDONG (CN); **Weibin MA**, GUANGDONG (CN); **Lihong HUANG**, GUANGDONG (CN); **Zuoxing YANG**, GUANGDONG (CN); **Haifeng GUO**, GUANGDONG (CN)

(21) Appl. No.: **17/621,138**

(22) PCT Filed: **Jun. 22, 2021**

(86) PCT No.: **PCT/CN2021/101449**

§ 371 (c)(1),
(2) Date: **Dec. 20, 2021**

(30) **Foreign Application Priority Data**

Jun. 23, 2020 (CN) 202010582032.2

Publication Classification

(51) **Int. Cl.**

H03L 7/099	(2006.01)
H03L 7/089	(2006.01)
H03L 7/093	(2006.01)

(52) **U.S. Cl.**

CPC ***H03L 7/0992*** (2013.01); ***H03L 7/089*** (2013.01); ***H03L 7/093*** (2013.01)

(57) **ABSTRACT**

The present disclosure relates to a method for up-converting a clock signal, a clock circuit and a digital processing device. More specifically, provided is a method for up-converting a clock signal, comprising: employing a first clock sub-circuit to provide a clock signal having a first frequency to a chip; receiving an instruction to up-convert the clock signal having the first frequency to a clock signal having a second frequency; in response to receiving the instruction, causing a second clock sub-circuit to output the clock signal having the second frequency; and after the second clock sub-circuit outputs the clock signal having the second frequency, employing the second clock sub-circuit to provide the clock signal having the second frequency to the chip in place of the first clock sub-circuit.