US 20230231572A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2023/0231572 A1**

YOON (43) **Pub. Date: Jul. 20, 2023**

(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: **SAMSUNG ELECTRONICS CO., LTD.**, SUWON-SI (KR)

(72) Inventor: **Young Hyun YOON**, Gwangmyeong-si (KR)

(21) Appl. No.: **18/148,604**

(22) Filed: **Dec. 30, 2022**

(30) **Foreign Application Priority Data**

Jan. 19, 2022 (KR) 10-2022-0007881
May 10, 2022 (KR) 10-2022-0057004

Publication Classification

(51) **Int. Cl.**
H03M 3/00 (2006.01)
H03K 19/20 (2006.01)

(52) **U.S. Cl.**
CPC ***H03M 3/502*** (2013.01); ***H03M 3/422*** (2013.01); ***H03M 3/464*** (2013.01); ***H03K 19/20*** (2013.01)

(57) **ABSTRACT**

A semiconductor device such as a sigma delta A/D converter comprises an integrator configured to output first and second output signals, a quantizer configured to generate a first digital signal based on the output signals, first and second switches configured to control application of first and second reference voltages to a first resistor based on respective first and second control signals, and a third switch configured to control connection between the first resistor and a first input terminal of the integrator based on a third control signal. The first through third control signals are generated based on the first digital signal and a second digital signal obtained by delaying the first digital signal. The third switch is turned on when any one of the first and second switches is turned on, and is turned off when both the first and second switches are turned off.