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(54) **METHOD FOR PROGRAMMING AN FPGA**

(71) Applicant: **dSPACE GmbH**, Paderborn (DE)

(72) Inventors: **Heiko KALTE**, Paderborn (DE); **Dominik LUBELEY**, Paderborn (DE)

(73) Assignee: **dSPACE GmbH**, Paderborn (DE)

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(57) **ABSTRACT**

A method for programming an FPGA, wherein a library, which includes elementary operations and a particular latency table for each of the elementary operations of the library is provided. Each latency table indicates the latency of the particular operation for a plurality of clock rates of the FPGA and for a plurality of input bit widths of the particular operation during the execution on the FPGA, depending on the input bit width of the particular operation and the clock rate of the FPGA. A data path indicating a consecutive execution of at least two elementary operations of the library on the FPGA is defined. The latencies given for the particular input bit width of the particular elementary operations of the data path for a plurality of different clock rates in the latency tables are detected and added, then one of the clock rates is selected.