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(54) **ERROR PROTECTION FOR MANAGED MEMORY DEVICES**

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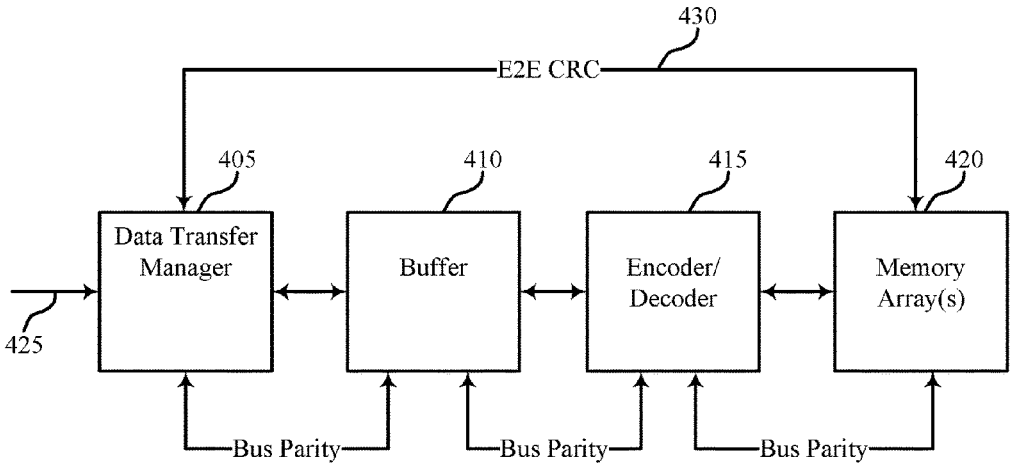
(57) **ABSTRACT**

Methods, systems, and devices for error protection for managed memory devices are described. In some examples, a memory system may receive data units from a host device. The data units may include respective sets of parity bits, and the memory system may perform an error detection operation on the data units. A first controller of the memory system may generate a protocol unit using data (e.g., a subset of data) from the data units. The protocol unit may include a set of parity bits (e.g., a different set of parity bits), and a second controller of the memory system may perform an error detection operation on the protocol unit. The second controller of the memory system may generate a data storage unit using data (e.g., a subset of data) from the protocol unit, and may store the data unit and another set of parity bits to a memory device.



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