



US 20230230995A1

(19) **United States**(12) **Patent Application Publication**
HONG et al.(10) **Pub. No.: US 2023/0230995 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SEMICONDUCTOR DEVICE INCLUDING
THROUGH VIA, SEMICONDUCTOR
PACKAGE, AND METHOD OF
FABRICATING THE SAME****Publication Classification**(51) **Int. Cl.****H01L 27/146** (2006.01)**H01L 21/768** (2006.01)**H01L 23/00** (2006.01)**H01L 23/48** (2006.01)(52) **U.S. Cl.****CPC .. H01L 27/14634** (2013.01); **H01L 27/14636**(2013.01); **H01L 27/14645** (2013.01); **H01L****27/1469** (2013.01); **H01L 21/76898** (2013.01);**H01L 24/08** (2013.01); **H01L 24/80** (2013.01);**H01L 23/481** (2013.01); **H01L 2224/80894**(2013.01); **H01L 2224/08146** (2013.01)(71) Applicant: **Samsung Electronics Co., Ltd.**,
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Suwon-si (KR)(21) Appl. No.: **18/191,218**(22) Filed: **Mar. 28, 2023****Related U.S. Application Data**(63) Continuation of application No. 16/926,924, filed on
Jul. 13, 2020, now Pat. No. 11,626,443, which is a
continuation of application No. 16/233,900, filed on
Dec. 27, 2018, now Pat. No. 10,734,430.**Foreign Application Priority Data**

Jun. 14, 2018 (KR) 10-2018-0068289

(57)

ABSTRACT

A semiconductor device including a first structure including a first conductive pattern, the first conductive pattern exposed on an upper portion of the first structure, a mold layer covering the first conductive pattern, a second structure on the mold layer, and a through via penetrating the second structure and the mold layer, the through via electrically connected to the first conductive pattern, the through via including a first via segment in the second structure and a second via segment in the mold layer, the second via segment connected to the first via segment, an upper portion of the second via segment having a first width and a middle portion of the second via segment having a second width greater than the first width may be provided.

