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(54) **CLOCK SYNTHESIZER**

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(57) **ABSTRACT**

A clock synthesizer is provided. The Clock synthesizer includes a Phase Locked Loop (PLL) configured to generate a clock signal based on a reference signal. A clock buffer is connected to the PLL. The clock buffer stores the clock signal. A Duty Cycle Controller and Phase Interpolator (DCCPI) circuit is connected to the clock buffer. The DCCPI circuit receives the clock signal from the clock buffer, adjusts a duty cycle of the clock signal to substantially equal to 50%, performs phase interpolation on the clock signal, and provides the clock signal as an output after adjusting the duty cycle substantially equal to 50% and performing the phase interpolation.