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(19) **United States**(12) **Patent Application Publication**
Liu et al.(10) **Pub. No.: US 2024/0244845 A1**(43) **Pub. Date: Jul. 18, 2024**(54) **ELECTRONIC DEVICES COMPRISING
REDUCED CHARGE CONFINEMENT
REGIONS IN STORAGE NODES OF
PILLARS AND RELATED METHODS AND
SYSTEMS**(71) Applicant: **Micron Technology, Inc.**, Boise, ID
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Eagle, ID (US)(21) Appl. No.: **18/622,671**(22) Filed: **Mar. 29, 2024****Related U.S. Application Data**(62) Division of application No. 17/092,916, filed on Nov.
9, 2020, now Pat. No. 11,956,954.**Publication Classification**(51) **Int. Cl.***H10B 43/27* (2006.01)*H01L 23/522* (2006.01)*H10B 43/10* (2006.01)*H10B 43/35* (2006.01)*H10B 43/40* (2006.01)(52) **U.S. Cl.**CPC *H10B 43/27* (2023.02); *H01L 23/5226*(2013.01); *H10B 43/10* (2023.02); *H10B**43/35* (2023.02); *H10B 43/40* (2023.02)

(57)

ABSTRACT

An electronic device comprises a stack of alternating dielectric materials and conductive materials, a pillar region extending vertically through the stack, an oxide material within the pillar region and laterally adjacent to the dielectric materials and the conductive materials of the stack, and a storage node laterally adjacent to the oxide material and within the pillar region. A charge confinement region of the storage node is in horizontal alignment with the conductive materials of the stack. A height of the charge confinement region in a vertical direction is less than a height of a respective, laterally adjacent conductive material of the stack in the vertical direction. Related methods and systems are also disclosed.

