

(19) **United States**

(12) **Patent Application Publication**
Billa et al.

(10) **Pub. No.: US 2022/0407476 A1**

(43) **Pub. Date: Dec. 22, 2022**

(54) **DC-BLOCKING AMPLIFIER WITH
ALIASING TONE CANCELLATION CIRCUIT**

(52) **U.S. Cl.**
CPC **H03F 3/005** (2013.01)

(71) Applicant: **MEDIATEK INC.**, Hsin-Chu (TW)

(72) Inventors: **Sujith Kumar Billa**, Hsinchu City (TW); **Sung-Han Wen**, Hsinchu City (TW)

(73) Assignee: **MEDIATEK INC.**, Hsin-Chu (TW)

(21) Appl. No.: **17/751,630**

(22) Filed: **May 23, 2022**

Related U.S. Application Data

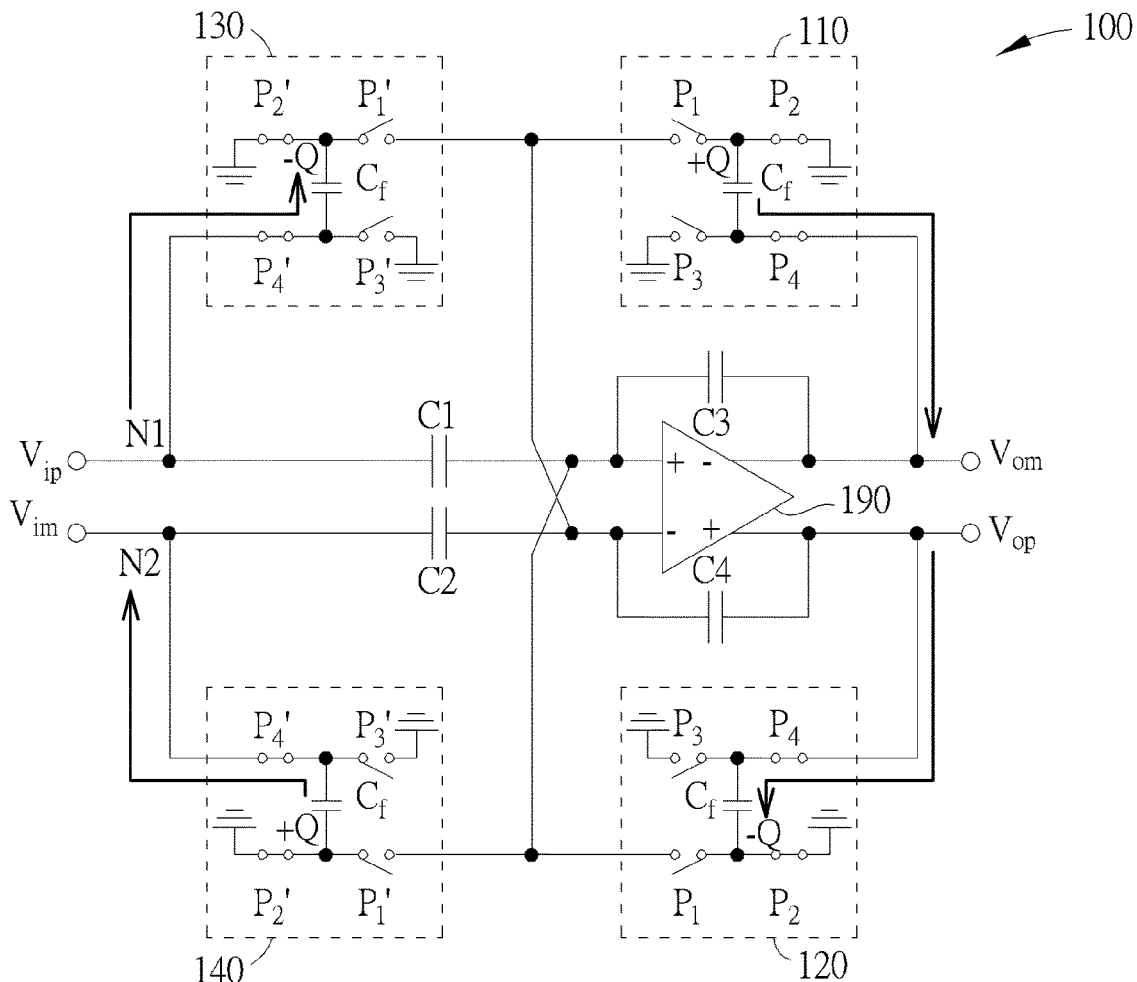
(60) Provisional application No. 63/211,036, filed on Jun. 16, 2021.

Publication Classification

(51) **Int. Cl.**
H03F 3/00 (2006.01)

(57) **ABSTRACT**

The present invention provides an amplifier circuit, wherein the amplifier circuit includes an input terminal, a capacitor, an amplifier, a feedback circuit and an aliasing tone cancellation circuit. The input terminal is configured to receive a first input signal. The capacitor is coupled to the input terminal. The amplifier is configured to receive the input signal through the capacitor to generate an output signal. The feedback circuit is coupled between an input node and an output node of the amplifier, and is configured to generate a feedback signal according to the output signal, wherein the feedback circuit includes a storage block including a switched-capacitor. The aliasing tone cancellation circuit is coupled between the input terminal of the amplifier circuit and the input node of the amplifier, and configured to generate a signal to cancel or reduce an aliasing tone of the feedback signal according to the input signal.



First phase : opposite charges on storage blocks