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(19) **United States**(12) **Patent Application Publication**  
**YI et al.**(10) **Pub. No.: US 2024/0213322 A1**(43) **Pub. Date: Jun. 27, 2024**(54) **FIELD EFFECT TRANSISTOR,  
PREPARATION METHOD THEREOF, AND  
ELECTRONIC CIRCUIT****H01L 21/3213** (2006.01)**H01L 29/20** (2006.01)**H01L 29/66** (2006.01)**H01L 29/778** (2006.01)(71) Applicant: **HUAWEI TECHNOLOGIES CO.,  
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**ABSTRACT**(22) Filed: **Mar. 8, 2024****Related U.S. Application Data**(63) Continuation of application No. PCT/CN2022/  
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This application provides a field effect transistor, a preparation method, and an electronic circuit. During preparation, after a channel layer, a control gate layer, a metal gate layer, a hard mask layer, and a photoresist layer are sequentially formed on a substrate, a first photoresist mask pattern is formed. Dry etching is performed on the hard mask layer, to form a first hard mask pattern. Size shrinkage treatment is performed on the first photoresist mask pattern, to form a second photoresist mask pattern. A part, exposing the first hard mask pattern, of the second photoresist mask pattern forms a step surface. Dry etching is sequentially performed on the first hard mask pattern, the metal gate layer, and the control gate layer. During dry etching, the step surface extends downward and stops on a side wall of a control gate. The step surface may improve electrical leakage from the side wall.

