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(54) **SEMICONDUCTOR CHIP INCLUDING LOW-K DIELECTRIC LAYER**

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(57) **ABSTRACT**

A semiconductor chip includes a device layer on a substrate, the device layer including a plurality of semiconductor devices; a wiring structure and a lower inter-wiring dielectric layer each on the device layer, the lower inter-wiring dielectric layer surrounding the wiring structure and having a lower permittivity than silicon oxide; an upper inter-wiring dielectric layer arranged on the lower inter-wiring dielectric layer; an isolation recess arranged along an edge of the substrate, the isolation recess formed on side surfaces of the lower and upper inter-wiring dielectric layers and having a bottom surface at a level equal to or lower than that of a bottom surface of the lower inter-wiring dielectric layer; and a cover dielectric layer covering the side surfaces of the lower and upper inter-wiring dielectric layers and the bottom surface of the isolation recess.