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(19) **United States**(12) **Patent Application Publication**
JUN et al.(10) **Pub. No.: US 2023/0231015 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **CROSSING MULTI-STACK NANOSHEET
STRUCTURE AND METHOD OF
MANUFACTURING THE SAME**(71) Applicant: **SAMSUNG ELECTRONICS CO.,
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LTD, Suwon-si (KR)**(21) Appl. No.: **18/187,506**(22) Filed: **Mar. 21, 2023****Related U.S. Application Data**(63) Continuation of application No. 17/148,252, filed on
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(57)

ABSTRACT

A semiconductor device includes a substrate; a 1st transistor formed above the substrate, and having a 1st transistor stack including a plurality of 1st channel structures, a 1st gate structure surrounding the 1st channel structures, and 1st and 2nd source/drain regions at both ends of the 1st transistor stack in a 1st channel length direction; and a 2nd transistor formed above the 1st transistor in a vertical direction, and having a 2nd transistor stack including a plurality of 2nd channel structures, a 2nd gate structure surrounding the 2nd channel structures, and 3rd and 4th source/drain regions at both ends of the 2nd transistor stack in a 2nd channel length direction, wherein the 3rd source/drain region does not vertically overlap the 1st source/drain region or the 2nd source/drain region, and the 4th source/drain region does not vertically overlap the 1st source/drain region or the 2nd source/drain region.

