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(54) **METHOD FOR PRODUCING 3D SEMICONDUCTOR DEVICES AND STRUCTURES WITH TRANSISTORS AND MEMORY CELLS**

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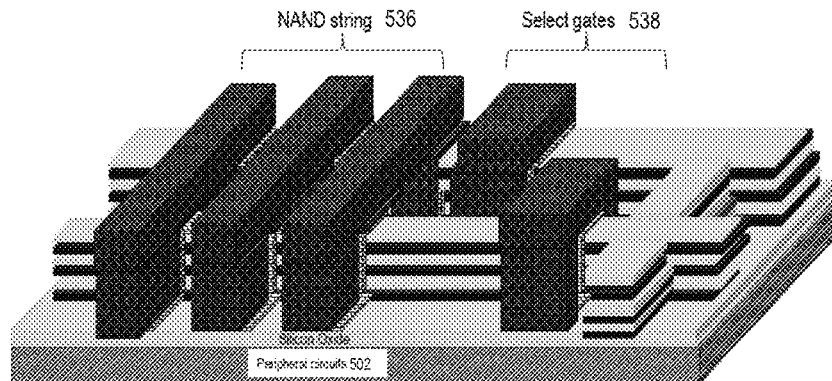
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(57)

ABSTRACT

A method for producing a 3D semiconductor device including: providing a first level, including a single crystal layer; forming memory control circuits in and/or on the first level which include first single crystal transistors and at least two interconnection metal layers; forming at least one second level disposed above the memory control circuits; performing a first etch step into the second level; forming at least one third level on top of the second level; performing additional processing steps to form first memory cells within the second level and second memory cells within the third level, where each of the first memory cells include at least one second transistor including a metal gate, where each of the second memory cells include at least one third transistor; and performing bonding of the first level to the second level, where the bonding includes oxide to oxide bonding.



Symbols

n+ Silicon 528  Gate electrode 524 
Silicon oxide 522  Gate dielectric 526 