



US 20230231039A1

(19) **United States**

(12) **Patent Application Publication**
HUANG

(10) **Pub. No.: US 2023/0231039 A1**

(43) **Pub. Date: Jul. 20, 2023**

(54) **SEMICONDUCTOR STRUCTURE AND
METHOD FOR FABRICATING SAME**

(52) **U.S. Cl.**

CPC *H01L 29/685* (2013.01); *H10B 20/25*
(2023.02); *H01L 27/088* (2013.01); *H01L*
29/401 (2013.01)

(71) Applicant: **CHANGXIN MEMORY
TECHNOLOGIES, INC.**, Hefei (CN)

(72) Inventor: **Jinrong HUANG**, Hefei (CN)

(21) Appl. No.: **18/150,191**

(22) Filed: **Jan. 4, 2023**

(30) **Foreign Application Priority Data**

Jan. 14, 2022 (CN) 202210041574.8

Publication Classification

(51) **Int. Cl.**

H01L 29/68 (2006.01)
H10B 20/25 (2006.01)
H01L 27/088 (2006.01)
H01L 29/40 (2006.01)

(57)

ABSTRACT

Embodiments disclose a semiconductor structure and a method for fabricating the same. The semiconductor structure includes: a substrate, a gate dielectric layer, a first conductive layer, and a conductive plug. The gate dielectric layer is provided on the substrate, and the first conductive layer is provided on the gate dielectric layer. The conductive plug is provided on the gate dielectric layer and covers a side wall of the first conductive layer, where a projection of the conductive plug on the substrate and a projection of the gate dielectric layer on the substrate at least partially overlap. By providing the conductive plug, a breakdown current can break down a region of the gate dielectric layer corresponding to the conductive plug by means of the conductive plug. That is, a breakdown position is adjusted by controlling an overlapping position between the conductive plug and the gate dielectric layer.

