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**RAMIREZ et al.**(10) **Pub. No.: US 2022/0399882 A1**(43) **Pub. Date: Dec. 15, 2022**(54) **LOW POWERED CLOCK DRIVING****Publication Classification**(71) Applicant: **INTERNATIONAL BUSINESS  
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(2013.01); **H03K 2005/00195** (2013.01)(72) Inventors: **DANIEL RAMIREZ,** Rochester, MN  
(US); **SUDIPTO CHAKRABORTY,**  
Plano, TX (US)(57) **ABSTRACT**

A clock driver circuit for low powered clock driving may include: a multiple phase divider; a buffer supplying at least one of multiple phases to the multiple phase divider at a center frequency that is an integer multiple of an input frequency; and wherein the multiple phase divider and the buffer share a same current from a supply rail.

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