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(54) **MATCH-SLAVE LATCH WITH SKEWED CLOCK**

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(57) **ABSTRACT**

Circuits, systems, and methods are described herein for generating master clock signals and slave clock signals for controlling a flip-flop having a master latch and a slave latch. A circuit includes a master latch configured to latch an input data signal and to output a data latch signal based on a master clock signal. The circuit also includes a slave latch coupled to the master latch and configured to generate an output data signal based on a slave latch clock signal and the data latch signal. Additionally, the circuit includes a skewed clock circuit coupled to the master latch and the slave latch. The skewed clock circuit is configured to receive a clock signal and generate the master clock signal and the slave clock signal based on the clock signal. The master clock signal and the slave clock signal are independent clock signals whose timing is skewed relative to one another by the skewed clock circuit.