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Kinyua et al.(10) **Pub. No.: US 2022/0368340 A1**(43) **Pub. Date: Nov. 17, 2022**(54) **ANALOG TO DIGITAL CONVERTER WITH
VCO-BASED AND PIPELINED QUANTIZERS**(52) **U.S. Cl.**CPC *H03M 3/368* (2013.01); *H03M 3/412*
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3/464 (2013.01)(71) Applicant: **Taiwan Semiconductor
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ABSTRACT(73) Assignee: **Taiwan Semiconductor
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Hsinchu (TW)(21) Appl. No.: **17/876,761**(22) Filed: **Jul. 29, 2022****Related U.S. Application Data**(63) Continuation of application No. 17/181,381, filed on
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Mar. 31, 2020, now Pat. No. 10,931,299.**Publication Classification**(51) **Int. Cl.**
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An analog-to-digital converter (“ADC”) includes an input terminal configured to receive an analog input signal. A first ADC circuit is coupled to the input terminal and includes a VCO. The first ADC circuit is configured to output a first digital signal in a frequency domain based on the analog input signal. The first digital signal includes an error component. A first DAC is configured to convert the first digital signal to an analog output signal. A first summation circuit is configured to receive the analog output signal, the analog input signal, and a loop filtered version of the analog input signal and extract the error component, and output a negative of the error component. A second ADC circuit is configured to convert the negative of the error component to a digital error signal. A second summation circuit is configured to receive the first digital signal and the digital error signal, and to output a digital output signal corresponding to the analog input at an output terminal.

