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(54) **SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING THE SAME**

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(57) **ABSTRACT**

A semiconductor package including a package substrate, a bridge structure stacked on the package substrate, a first molding member surrounding a side surface of the bridge structure, a trace pattern extending along an upper surface of the bridge structure and an upper surface of the first molding member, a via pattern penetrating through the first molding member and electrically connecting the package substrate and the trace pattern to each other, and a first semiconductor chip and a second semiconductor chip each stacked on the upper surface of the first molding member and electrically connected to each other by the bridge structure. The first semiconductor chip and the second semiconductor chip are arranged along a first direction parallel to an upper surface of the package substrate and the trace pattern extends in the first direction and is electrically connected to at least one of the first semiconductor chip and the second semiconductor chip.