



US 20230231011A1

(19) **United States**(12) **Patent Application Publication**
Tokuda(10) **Pub. No.: US 2023/0231011 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SEMICONDUCTOR DEVICE INCLUDING
VERTICAL MOSFET AND METHOD OF
MANUFACTURING THE SAME**(71) Applicant: **RENESAS ELECTRONICS
CORPORATION**, Tokyo (JP)(72) Inventor: **Satoru Tokuda**, Tokyo (JP)(21) Appl. No.: **18/189,463**(22) Filed: **Mar. 24, 2023****Related U.S. Application Data**(63) Continuation of application No. 16/782,802, filed on
Feb. 5, 2020.(30) **Foreign Application Priority Data**

Feb. 7, 2019 (JP) 2019-020340

Publication Classification(51) **Int. Cl.**
H01L 29/06 (2006.01)
H01L 29/66 (2006.01)
H01L 29/423 (2006.01)
(52) **U.S. Cl.**
CPC **H01L 29/0634** (2013.01); **H01L 29/66734**
(2013.01); **H01L 29/4238** (2013.01); **H01L**
29/4236 (2013.01)(57) **ABSTRACT**

A semiconductor device that achieves both miniaturization and high breakdown voltage is disclosed. The semiconductor device has a gate electrode G1 formed in a trench TR extending in Y direction and a plurality of column regions PC including column regions PC1 to PC3 formed in a drift region ND. The column regions PC1, PC2 and PC3 are provided in a staggered manner to sandwich the trench TR. An angle $\theta 1$ formed by a line connecting the centers of the column regions PC1 and PC2 and a line connecting the centers of the column regions PC1 and PC3 is 60 degrees or more and 90 degrees or less.

