

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0251549 A1 KO et al.

Jul. 25, 2024 (43) **Pub. Date:**

(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: SAMSUNG ELECTRONICS CO., LTD., Suwon-si (KR)

(72) Inventors: **SANGGYU KO**, Suwon-si (KR); HYUCKCHAI JUNG, Suwon-si (KR); SANG-IL HAN, Suwon-si (KR); JUNGJIN PARK, Suwon-si (KR); SUHYUN KIM, Suwon-si (KR); CHUL LEE, Suwon-si (KR);

> SUNGHO JANG, Suwon-si (KR); HYEONGWON JANG, Suwon-si (KR)

(21) Appl. No.: 18/456,655

(22)Filed: Aug. 28, 2023

(30)Foreign Application Priority Data

Jan. 25, 2023 (KR) 10-2023-0009750

Publication Classification

(51) Int. Cl. H10B 12/00 (2006.01)

U.S. Cl.

CPC H10B 12/50 (2023.02); H10B 12/315 (2023.02); H10B 12/482 (2023.02); H10B 12/485 (2023.02); H10B 12/488 (2023.02)

(57)**ABSTRACT**

A semiconductor device includes a substrate including a peripheral active pattern defined by a device isolation layer, a gate structure on the peripheral active pattern, and a gate spacer covering at least a portion of a side surface of the gate structure. The gate structure includes an insulating pattern structure and a metal pattern structure on the insulating pattern structure. The insulating pattern structure includes a recess having a maximum depth in a first direction parallel to a top surface of the substrate at a first height. The insulating pattern structure includes a first gate insulating pattern and a high-k dielectric layer, which are sequentially stacked on the top surface of the substrate. The gate spacer includes a protrusion inserted in the recess.

