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**KANG et al.**(10) **Pub. No.: US 2022/0352887 A1**(43) **Pub. Date: Nov. 3, 2022**(54) **POWER ON CONTROL CIRCUITS AND  
METHODS OF OPERATING THE SAME**(52) **U.S. Cl.**CPC ..... **H03K 17/6872** (2013.01); **H03K 19/20**  
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**ABSTRACT**(72) Inventors: **Po-Zeng KANG**, Hsinchu (TW);  
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A semiconductor device includes a hysteresis block configured to generate an output voltage at corresponding disabling enabling voltage levels and a core-voltage-gated (CVG) device configured to receive a core voltage, an input terminal of the hysteresis block is coupled to a control node. The CVG device is configured to alter a control voltage at the control node so as to cause the output voltage of the hysteresis block to be generated at the disabling voltage level in response to the core voltage being at or below a first trigger level. Additionally, the CVG device is configured to alter the control voltage at the control node so as to cause the output voltage of the hysteresis block to be generated at the enabling voltage level in response to the core voltage being at or above a second trigger level, the second trigger level being above the first trigger level.

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