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(54) **CLOCK INTERPOLATION SYSTEM FOR EYE-CENTERING**

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(57) **ABSTRACT**

Embodiments herein relate to a clock interpolation system. The system may be configured to identify, at a change in logical state of a recovered clock signal, a logical state of a first signal when the first signal is delayed by a delay value. The system may be further configured to identify, at a change in logical state of a second signal, a logical state of the clock signal when the clock signal is delayed by the delay value. Based on the two identifications, the delay value and/or a timing of the clock signal may be adjusted. Other embodiments may be described and/or claimed.

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