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(54) **RESILIENT STORAGE CIRCUITS**

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(57) **ABSTRACT**

The present disclosure includes an integrated circuit comprising a first pair of complementary transistors configured in series, a second pair of complementary transistors configured in series, and at least one charge extraction transistor having a gate coupled to a first potential, a source coupled to a second potential, and a drain coupled to a data storage node of one of the first or second pairs of complementary transistors. The first potential and second potential bias the at least one charge extraction transistor in a nonconductive state. The drain of the at least one charge extraction transistor is formed in a doped material shared with a drain of a transistor of the first or second pairs of complementary transistors.