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(54) **VERTICAL THIN-FILM TRANSISTOR AND APPLICATION AS BIT-LINE CONNECTOR FOR 3-DIMENSIONAL MEMORY ARRAYS**

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(57) **ABSTRACT**

A memory circuit includes: (i) a semiconductor substrate having a planar surface, the semiconductor substrate having formed therein circuitry for memory operations; (ii) a memory array formed above the planar surface, the memory array having one or more electrodes to memory circuits in the memory array, the conductors each extending along a direction substantially parallel to the planar surface; and (iii) one or more transistors each formed above, alongside or below a corresponding one of the electrodes but above the planar surface of the semiconductor substrate, each transistor (a) having first and second drain/source region and a gate region each formed out of a semiconductor material, wherein the first drain/source region, the second drain/source region or the gate region has formed thereon a metal silicide layer; and (b) selectively connecting the corresponding electrode to the circuitry for memory operations.