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Simsek-Ege(10) **Pub. No.: US 2024/0215221 A1**(43) **Pub. Date: Jun. 27, 2024**(54) **MICROELECTRONIC DEVICES, AND
RELATED MEMORY DEVICES, AND
ELECTRONIC SYSTEMS**(52) **U.S. Cl.**
CPC **H10B 12/30** (2023.02); **H10B 12/03**
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23, 2022.**Publication Classification**(51) **Int. Cl.**
H10B 12/00 (2006.01)(57) **ABSTRACT**

A microelectronic device includes first memory array region and second memory array regions, each comprising vertical stacks of dynamic random access memory (DRAM) cells. A staircase region is between the first memory array region and the second memory array region and comprises a staircase structure comprising a vertical stack of first conductive structures horizontally extending through the staircase region in a first direction, the first conductive structures configured to be in contact with the DRAM cells of the first memory array region and DRAM cells of the second memory array region, and sub-staircase structures individually comprising second conductive structures horizontally extending from the vertical stack of first conductive structures in a second direction. Horizontally neighboring sub-staircase structures are substantially evenly horizontally spaced from one another in the first direction. Related microelectronic devices, memory devices, and electronic systems are also described.

