



(19) **United States**

(12) **Patent Application Publication**
CHENG et al.

(10) **Pub. No.: US 2024/0213110 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **EMBEDDED DIE PACKAGING OF POWER SEMICONDUCTOR DEVICES**
(2013.01); *H01L 23/5226* (2013.01); *H01L 23/5283* (2013.01); *H01L 24/32* (2013.01); *H01L 29/401* (2013.01); *H01L 29/41775* (2013.01); *H01L 2224/32225* (2013.01); *H01L 2924/1033* (2013.01); *H01L 2924/13064* (2013.01)

(71) Applicant: **GaN Systems Inc.**, Kanata (CA)

(72) Inventors: **An-Sheng CHENG**, Hsinchu City (TW); **Stephen COATES**, San Francisco, CA (US)

(21) Appl. No.: **18/085,660**

(57) **ABSTRACT**

(22) Filed: **Dec. 21, 2022**

Publication Classification

(51) **Int. Cl.**
H01L 23/31 (2006.01)
H01L 21/48 (2006.01)
H01L 21/56 (2006.01)
H01L 23/00 (2006.01)
H01L 23/29 (2006.01)
H01L 23/495 (2006.01)
H01L 23/522 (2006.01)
H01L 23/528 (2006.01)
H01L 29/40 (2006.01)
H01L 29/417 (2006.01)

(52) **U.S. Cl.**
CPC *H01L 23/3192* (2013.01); *H01L 21/4828* (2013.01); *H01L 21/56* (2013.01); *H01L 23/293* (2013.01); *H01L 23/3171* (2013.01); *H01L 23/49513* (2013.01); *H01L 23/49562*

Embedded die packaging for semiconductor power switching devices, wherein the package comprises a laminated body comprising a layer stack of a plurality of dielectric layers and conductive metal layers. A thermal contact area on a back-side of the die is attached to a leadframe. A patterned layer of conductive metallization on a front-side of the die provides electrical contact areas of the power semiconductor device. Before embedding, a protective dielectric layer is provided on the front-side of the die, extending around edges of the die. The protective dielectric layer provides a protective region that acts a cushion to protect edges of the die from damage during lamination. The protective dielectric material may extend over the electrical contact areas to protect against etch damage and damage during laser drilling of vias, thereby mitigating physical damage, overheating or other potential damage to the active region of the semiconductor device.

