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(54) **ZERO GLITCH DIGITAL STEP ATTENUATOR**

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(57) **ABSTRACT**

A digital step attenuator (DSA) cell and related method are provided. The DSA cell includes a first branch comprising a first resistor connected, at a first side, to an input port and, at a second side, to an output port; a second resistor connected, at a first side, to the first resistor and, at a second side, to a first transistor and a third resistor connected, at a first side, to the first resistor and, at a second side, to a second transistor. Also included in the DSA cell is a second branch, in a parallel configuration with the first resistor, that includes a fourth resistor and a third transistor. Also included is a third branch, in a parallel configuration with the first resistor, that includes a fourth transistor. The first transistor, the second transistor, the third transistor, and the fourth transistor are configured to be operated independently.