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(54) **VERTICAL TRANSISTORS AND METHOD FOR PRODUCING THE SAME**

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(57) **ABSTRACT**

A vertical transistor with an outer region and a membrane region. At least a portion of a semiconductor substrate is arranged in the outer region. The semiconductor substrate is structured in such a way that a rear trench is arranged in the membrane region. The rear trench is free of semiconductor substrate. A masking layer is arranged in the outer region and/or in the membrane region. A layer stack is arranged in the membrane region, wherein the layer stack includes at least one drift layer, at least one component-defining layer system, and at least one control terminal, preferably a gate electrode. The masking layer is configured such that the region on the masking layer is substantially free of the layer stack so that the lateral extension of the layer stack is adjusted by means of the masking layer.