

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0215242 A1

Jun. 27, 2024 (43) **Pub. Date:**

(54) SEMICONDUCTOR MEMORY DEVICE AND ELECTRONIC SYSTEM INCLUDING THE

(71) Applicant: Samsung Electronics Co., Ltd.,

Suwon-si (KR)

Inventors: Gil Sung LEE, Suwon-si (KR); Suk

Kang SUNG, Suwon-si (KR)

Assignee: Samsung Electronics Co., Ltd.,

Suwon-si (KR)

Appl. No.: 18/475,784 (21)

(22)Filed: Sep. 27, 2023

(30)Foreign Application Priority Data

(KR) 10-2022-0185434

Publication Classification

(51) Int. Cl. H10B 43/27 (2006.01)G11C 16/04 (2006.01)H01L 25/065 (2006.01)H10B 43/10 (2006.01) H10B 43/35 (2006.01)H10B 43/40 (2006.01)H10B 80/00 (2006.01)

(52) U.S. Cl.

CPC H10B 43/27 (2023.02); G11C 16/0483 (2013.01); H01L 25/0652 (2013.01); H10B 43/10 (2023.02); H10B 43/35 (2023.02); H10B 43/40 (2023.02); H10B 80/00 (2023.02); H01L 2225/06503 (2013.01)

(57)**ABSTRACT**

A semiconductor memory device may include a cell substrate, a mold structure including gate electrodes stacked on the cell substrate, a channel structures penetrating the mold structure; and a first cutting structure cutting some of the gate electrodes. The first cutting structure may include a first portion having a line shape extending in a first direction and a second portion having a line shape extending in a second direction. The first portion and the second portion may be alternately connected to form a zigzag shape. The first cutting structure may include a first side wall and a second side wall opposing the first side wall. A first point of the first side wall connected from the second portion to the first portion and a second point of the second side wall connected from the first portion to the second portion may be in corresponding channel structures among the channel structures.

