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FUNAYAMA et al.(10) **Pub. No.: US 2022/0407519 A1**(43) **Pub. Date: Dec. 22, 2022**(54) **OUTPUT CIRCUIT, TRANSMISSION
CIRCUIT, AND SEMICONDUCTOR
INTEGRATED CIRCUIT**(52) **U.S. Cl.**
CPC . H03K 19/017509 (2013.01); H03K 17/6872 (2013.01)(71) Applicant: **Socionext Inc.**, Kanagawa (JP)(72) Inventors: **Takumi FUNAYAMA**, Kanagawa (JP);
Akiyoshi MATSUDA, Kanagawa (JP)(21) Appl. No.: **17/895,763**(22) Filed: **Aug. 25, 2022****Related U.S. Application Data**(63) Continuation of application No. PCT/JP2020/
008029, filed on Feb. 27, 2020.**Publication Classification**(51) **Int. Cl.**
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H03K 17/687 (2006.01)(57) **ABSTRACT**

An output circuit includes: a first input transistor that is provided between a first power supply line and a first intermediate node; a second input transistor that is provided between a second intermediate node and a second power supply line; a first cascode transistor that is provided between the first intermediate node and an output node, and receives a first clip voltage from a first voltage generation circuit; a second cascode transistor that is provided between the output node and the second intermediate node, and receives a second clip voltage from a second voltage generation circuit; a first switch transistor that is provided between the first intermediate node and a gate of the first cascode transistor, and turns on during power down; and a second switch transistor that is provided between the second intermediate node and a gate of the second cascode transistor, and turns on during power down.

