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(54) **MEMORY DEVICE FOR REDUCING THERMAL CROSSTALK**

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(57) **ABSTRACT**

The present disclosure relates to an integrated chip including a first word line and a second word line adjacent to the first word line. The first word line and the second word line both extend along a first direction. A first memory cell is over the first word line and a second memory cell is over the second word line. A first bit line extends over the first memory cell, over the second memory cell, and along a second direction transverse to the first direction. A first dielectric layer is arranged between the first memory cell and the second memory cell. The first dielectric layer extends in a first closed loop to form and enclose a first void within the first dielectric layer. The first void laterally separates the first memory cell from the second memory cell.