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(54) **MULTIPLIER-ACCUMULATOR CIRCUITRY, AND PROCESSING PIPELINE INCLUDING SAME**

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(57) **ABSTRACT**

An integrated circuit comprising a plurality of MACs, connected to form a pipeline, to perform a plurality of multiply and accumulate operations, wherein each MAC includes: (A) a multiplier, coupled to memory to (i) receive the multiplier weight data, (ii) multiply first data and the multiplier weight data and (iii) output product data, (B) an accumulator, coupled to the multiplier of the MAC, to add second data and the first product data and output sum data, and (C) a load-store register, coupled to: (i) an output of the accumulator of the associated MAC and (ii) an input of the load-store register of an immediately successive MAC. Each load-store register may include two interconnected registers, and is configurable to, on the same clock cycle, (a) load the initialization data into the accumulator of the immediately successive MAC and (b) store the sum data from the associated MAC into the load-store register.