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(54) **INTEGRATED ELECTRONIC SYSTEM WITH AN IMPROVED POWER-ON RESET CIRCUIT AND METHOD FOR CONTROLLING THE INTEGRATED ELECTRONIC SYSTEM**

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(57) **ABSTRACT**

A resettable digital stage operates when a supply voltage is higher than a threshold. A non-volatile memory stores a digital code read by a reading stage. A main power-on reset circuit generates a main reset signal controlling reset of the reading stage. A resettable volatile memory coupled to the reading stage stores a default value when reset. An auxiliary power-on reset circuit generates an auxiliary reset signal controlling reset of the volatile memory. Upon deactivation of the reset, the reading stage loads the digital code into the volatile memory. The main power-on reset circuit functions in a non-trimmed configuration response to the stored default value and in a trimmed configuration responsive to the stored digital code. The main power-on reset circuit has first and second operative thresholds which respectively fall within a first and second non-trimmed voltage range or within a first and second trimmed voltage range.