



(12) **Patent Application Publication**
KIM et al.

(43) **Pub. Date:** **Jun. 27, 2024**

Publication Classification

(51) **Int. Cl.**
H10B 43/27 (2006.01)
H10B 41/10 (2006.01)
H10B 41/27 (2006.01)
H10B 43/10 (2006.01)

(52) **U.S. Cl.**
CPC *H10B 43/27* (2023.02); *H10B 41/10*
(2023.02); *H10B 41/27* (2023.02); *H10B*
43/10 (2023.02)

(57) **ABSTRACT**

A semiconductor memory device includes a first stacked structure, a first supporter layer, a second stacked structure, a block cut structure, and a second supporter layer on the second stacked structure and separated by a second cut pattern. The first stacked structure includes a first and second stack, the second stacked structure includes a third stack separated by the block cut structure and a fourth stack, the first supporter layer is on the first stack and the second stack, the second supporter layer is on the third stack and the fourth stack, the first cut pattern includes a first connection on the block cut structure and connecting the first supporter layer and the second stack, and the second cut pattern of the second supporter layer includes a second connection on the block cut structure and connecting the second supporter layer placed on the third stack and the fourth stack.

(22) Filed: **Mar. 5, 2024**

Related U.S. Application Data

(63) Continuation of application No. 17/203,122, filed on Mar. 16, 2021, now Pat. No. 11,956,957.

(30) **Foreign Application Priority Data**

Jul. 24, 2020 (KR) 10-2020-0092598

