US 20220368354A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2022/0368354 A1

Lu (43) Pub. Date: Nov. 17, 2022

(54) TWO-LEVEL ERROR CORRECTING CODE WITH SHARING OF CHECK-BITS

(71) Applicant: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsinchu (TW)

(72) Inventor: **Shih-Lien Linus Lu**, Hsinchu (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsinchu (TW)

(21) Appl. No.: **17/815,624**

(22) Filed: **Jul. 28, 2022**

Related U.S. Application Data

(63) Continuation of application No. 16/925,361, filed on Jul. 10, 2020, now Pat. No. 11,438,015.

Publication Classification

(51) **Int. Cl.**

H03M 13/29	(2006.01)
G11C 29/42	(2006.01)
G11C 29/44	(2006.01)
H03M 13/11	(2006.01)
H03M 13/15	(2006.01)

(52) **U.S. Cl.**

CPC ***H03M 13/29*** (2013.01); ***G11C 29/42*** (2013.01); ***G11C 29/44*** (2013.01); ***H03M 13/1174*** (2013.01); ***H03M 13/1575*** (2013.01)

(57) **ABSTRACT**

A memory device includes: a memory device configured to store data bits to be written to the memory device; and a memory controller. The memory controller includes: a first level error correction code (ECC) circuit coupled to the memory device, wherein the first level ECC circuit is configured to generate a first plurality of first level check bits corresponding to the data bits based on a first error detection scheme; and a second level ECC circuit coupled to the memory device, wherein the second level ECC circuit is configured to generate a second plurality of second level check bits corresponding to both the data bits and the first plurality of first level check bits based on a first error correction scheme.