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**MOHAMMED et al.**

(54) **ENHANCED GAIN OF OPERATIONAL AMPLIFIERS THROUGH LOW-FREQUENCY ZERO POSITIONING**

(71) Applicant: **THE ROYAL INSTITUTION FOR THE ADVANCEMENT OF LEARNING/MCGILL UNIVERSITY**, Montréal (CA)

(72) Inventors: **Mahmood A. MOHAMMED**, Montreal (CA); **Gordon ROBERTS**, Montreal West (CA)

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(57) **ABSTRACT**

An amplifier circuit comprises a multi-stage amplifier having a plurality of amplifiers cascaded between an input port $V_{in}$ and an output port $V_{out}$ to form a differential input stage and N subsequent gain stages, a capacitive load $C_L$ coupled to the output port $V_{out}$, and a compensation network coupled to the multi-stage amplifier and configured for positioning Pole-Zero pairs of each stage of the multi-stage amplifier below a unity gain frequency $\omega_t$ of the multi-stage amplifier when compensated, with Zeros positioned lower than Poles so as to increase the unity gain frequency $\omega_t$.