



US 20240179922A1

(19) **United States**

(12) **Patent Application Publication**
HUA et al.

(10) **Pub. No.: US 2024/0179922 A1**

(43) **Pub. Date: May 30, 2024**

(54) **TRANSISTOR AND METHOD FOR
MANUFACTURING SAME,
SEMICONDUCTOR DEVICE AND METHOD
FOR MANUFACTURING SAME**

(71) Applicant: **ICLEAGUE TECHNOLOGY CO.,
LTD.**, Jiaxing, Zhejiang (CN)

(72) Inventors: **Wenyu HUA**, Jiaxing (CN); **Xilong
WANG**, Jiaxing (CN)

(73) Assignee: **ICLEAGUE TECHNOLOGY CO.,
LTD.**, Jiaxing, Zhejiang (CN)

(21) Appl. No.: **17/782,868**

(22) PCT Filed: **Aug. 6, 2021**

(86) PCT No.: **PCT/CN2021/111345**

§ 371 (c)(1),

(2) Date: **Jun. 6, 2022**

(30) **Foreign Application Priority Data**

Apr. 20, 2021 (CN) 202110421932.3

Apr. 20, 2021 (CN) 202110422036.9

Publication Classification

(51) **Int. Cl.**

H10B 63/00 (2006.01)

H10B 12/00 (2006.01)

H10B 63/10 (2006.01)

(52) **U.S. Cl.**

CPC **H10B 63/34** (2023.02); **H10B 12/05**

(2023.02); **H10B 12/33** (2023.02); **H10B**

63/10 (2023.02)

(57)

ABSTRACT

Embodiments provide a transistor and a method for manufacturing same, a semiconductor device and a method for manufacturing same. The method for manufacturing a transistor includes operations. A wafer is provided, the wafer has multiple transistor formation regions, each of which has a transistor pillar with an exposed gate formation surface. A gate oxide layer and a gate are sequentially formed on the gate formation surface of each of the transistor pillars. A source is formed at a first end of each of the transistor pillars. A drain is formed at a second end of each of the transistor pillars, here the first end and the second end are opposite ends of each of the transistor pillars in a first direction which is a thickness direction of the wafer; a part of each of the transistor pillars between the source and the drain forms a channel region of the transistor.

