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(54) **DEGLITCHING CIRCUIT**

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED**, Dallas, TX (US)

(72) Inventor: **Vibha Goenka**, Bangalore (IN)

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(57) **ABSTRACT**

A circuit includes a first delay filter, a first comparator, an inverter, a second delay filter, a second comparator, an OR gate, and a latch. A first delay filter input is coupled to an inverter input. The first comparator has a first comparator input coupled to a first delay filter output and a second comparator input. The second delay filter has an input coupled to an inverter output. The second comparator has a third comparator input coupled to a second delay filter output, and a fourth comparator input coupled to the second comparator input. The OR gate has an input coupled to a first comparator output and another input coupled to a second comparator output. The latch has a clock input coupled to an OR gate output and a latch input coupled to the inverter input. A latch output provides a deglitched signal.