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(19) **United States**(12) **Patent Application Publication**  
**Greenlee et al.**(10) **Pub. No.: US 2024/0237330 A1**(43) **Pub. Date: Jul. 11, 2024**(54) **ARRAY OF CAPACITORS, ARRAY OF  
MEMORY CELLS, AND METHODS USED IN  
FORMING AN ARRAY OF CAPACITORS**(71) Applicant: **Micron Technology, Inc.**, Boise, ID  
(US)(72) Inventors: **Jordan D. Greenlee**, Nampa, ID (US);  
**Andrea Gotti**, Boise, ID (US); **David  
McShannon**, Meridian, ID (US); **Silvia  
Borsari**, Boise, ID (US)(73) Assignee: **Micron Technology, Inc.**, Boise, ID  
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(57)

**ABSTRACT**

A method used in forming an array of capacitors comprises forming horizontally-spaced openings into sacrificial material and through insulative material that is between a top and bottom of the sacrificial material. The insulative material at least predominately comprises at least one of a silicon nitride, a silicon boronitride, and a silicon carbonitride. The insulative material with horizontally-spaced openings there-through comprises an insulative horizontal lattice. An insulative lining is deposited within the horizontally-spaced openings and directly above the sacrificial material. The insulative lining at least predominately comprises at least one of a silicon oxide and a silicon oxynitride. During the depositing, the insulative lining is intermittently exposed to a nitrogen-containing plasma. First capacitor electrodes that are individually within individual of the horizontally-spaced openings are formed laterally over the insulative lining that is in the horizontally-spaced openings. The sacrificial material is removed and a capacitor insulator is formed over the first capacitor electrodes and the insulative horizontal lattice. Second-capacitor-electrode material is formed over the capacitor insulator. Structure independent of method is disclosed.

