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CHENG et al.(10) **Pub. No.: US 2023/0230933 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **CHIP PACKAGE AND MANUFACTURING METHOD THEREOF**(52) **U.S. Cl.**CPC **H01L 23/544** (2013.01); **H01L 27/14618** (2013.01); **H01L 27/14683** (2013.01); **H01L 2223/54433** (2013.01)(71) Applicant: **XINTEC INC.**, Taoyuan City (TW)(72) Inventors: **Chia-Ming CHENG**, New Taipei City (TW); **Chaung-Lin LAI**, Taoyuan City (TW); **Shu-Ming CHANG**, New Taipei City (TW); **Tsang-Yu LIU**, Zhubei City (TW)

(57)

ABSTRACT

A chip package includes a sensing element, a dam layer, and a light transmissive cover. A surface of the sensing element has a sensing area and a conductive pad. The conductive pad is adjacent to an edge of the surface of the sensing element. The dam layer is located on the surface of the sensing element and surrounds the sensing area. The dam layer has a main portion and plural mark portions. The mark portions are respectively located in plural corners of the main portion, located in a sidewall of the main portion, respectively located on plural corners of the sensing element, respectively located on plural inner edges of the main portion, or respectively located on plural outer edges of the main portion. The light transmissive cover is located on the dam layer.

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