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(54) **POWER MANAGEMENT CIRCUIT OPERABLE WITH GROUP DELAY**

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(57) **ABSTRACT**

A power management circuit operable with group delay is provided. The power management circuit includes a transceiver circuit configured to generate a digital target voltage and digitally delay the digital target voltage to generate multiple delayed digital target voltages. Accordingly, the transceiver circuit can generate a windowed digital target voltage in multiple delay tolerance windows based on the delayed digital target voltages. Since the windowed digital target voltage can tolerate a certain amount of group delay in each of the group delay tolerance windows, an envelope tracking (ET) voltage generated based on an analog version of the windowed digital target voltage can therefore tolerate the group delay in each of the group delay tolerance windows as well. As a result, it is possible to avoid distortion in the ET voltage to help improve performance of the power management circuit.