US 20220376681A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2022/0376681 A1

Yajima (43) Pub. Date: Nov. 24, 2022

(54) **DETECTOR AND POWER CONVERSION CIRCUIT**

(71) Applicant: **JAPAN SCIENCE AND TECHNOLOGY AGENCY**, Kawaguchi-shi (JP)

(72) Inventor: **Takeaki Yajima**, Tokyo (JP)

(73) Assignee: **JAPAN SCIENCE AND TECHNOLOGY AGENCY**, Kawaguchi-shi (JP)

(21) Appl. No.: **17/880,821**

(22) Filed: **Aug. 4, 2022**

**Related U.S. Application Data**

(63) Continuation of application No. 17/408,599, filed on Aug. 23, 2021, now Pat. No. 11,444,605, which is a continuation of application No. PCT/JP2020/006045, filed on Feb. 17, 2020.

(30) **Foreign Application Priority Data**

Feb. 28, 2019 (JP) ..... 2019-036951

**Publication Classification**

(51) **Int. Cl.**

***H03K 3/02*** (2006.01)
***H03K 5/01*** (2006.01)
***H03K 19/20*** (2006.01)

(52) **U.S. Cl.**

CPC ..... ***H03K 3/02*** (2013.01); ***H03K 5/01*** (2013.01); ***H03K 19/20*** (2013.01); *H03K 2005/00013* (2013.01)

(57) **ABSTRACT**

A spike generation circuit includes a first CMOS inverter connected between a first power supply and a second power supply, an output node of the first CMOS inverter being coupled to a first node that is an intermediate node coupled to an input terminal to which an input signal is input, a switch connected in series with the first CMOS inverter, between the first power supply and the second power supply, a first inverting circuit that outputs an inversion signal of a signal of the first node to a control terminal of the switch, and a delay circuit that delays the signal of the first node, outputs a delayed signal to an input node of the first CMOS inverter, and outputs an isolated output spike signal to an output terminal.