



US 20230230999A1

(19) **United States**(12) **Patent Application Publication**  
**HIRAMATSU**(10) **Pub. No.: US 2023/0230999 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SOLID-STATE IMAGING DEVICE AND  
ELECTRONIC APPARATUS***H04N 25/79* (2006.01)*H04N 25/63* (2006.01)(71) Applicant: **SONY SEMICONDUCTOR  
SOLUTIONS CORPORATION,**  
Kanagawa (JP)(52) **U.S. Cl.**CPC ..... *H01L 27/1465* (2013.01); *H04N 25/77*  
(2023.01); *H04N 25/79* (2023.01); *H04N*  
*25/63* (2023.01); *H01L 27/14621* (2013.01);  
*H01L 27/14612* (2013.01); *H01L 27/1463*  
(2013.01); *H01L 27/14645* (2013.01)(72) Inventor: **Tomoki HIRAMATSU,** Kanagawa (JP)(21) Appl. No.: **18/021,312**

(57)

**ABSTRACT**(22) PCT Filed: **Sep. 16, 2021**(86) PCT No.: **PCT/JP2021/034067**

§ 371 (c)(1),

(2) Date: **Feb. 14, 2023**(30) **Foreign Application Priority Data**

Sep. 25, 2020 (JP) ..... 2020-161365

**Publication Classification**(51) **Int. Cl.***H01L 27/146* (2006.01)*H04N 25/77* (2006.01)

The quantum efficiency can be improved. A solid-state imaging device according to an embodiment includes: a plurality of pixels (110) arranged in a matrix, in which each of the pixels includes a first semiconductor layer (35), a photoelectric conversion section (PD1) disposed on the first semiconductor layer on a side of a first surface, an accumulation electrode (37) disposed on the first semiconductor layer close to a side of a second surface on a side opposite to the first surface, a wiring (61, 62, 63, 64) extending from the second surface of the first semiconductor layer, a floating diffusion region (FD1) connected to the first semiconductor layer via the wiring, and a first gate (11) that forms a potential barrier in a charge flow path from the first semiconductor layer to the floating diffusion region via the wiring.

