US 20240235556A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0235556 A1

Pugh et al. (43) Pub. Date: Jul. 11, 2024

(54) **FUSED MEMORY AND ARITHMETIC CIRCUIT**

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(21) Appl. No.: **18/612,278**

(22) Filed: **Mar. 21, 2024**

Related U.S. Application Data

(63) Continuation of application No. 16/940,878, filed on Jul. 28, 2020, which is a continuation of application No. 16/417,152, filed on May 20, 2019, now Pat. No. 10,790,830.

Publication Classification

(51) **Int. Cl.**
H03K 19/1776 (2006.01)
H03K 19/17736 (2006.01)

(52) **U.S. Cl.**
CPC ... ***H03K 19/1776*** (2013.01); ***H03K 19/17744*** (2013.01)

(57) **ABSTRACT**

A tile of an FPGA fuses memory and arithmetic circuits. Connections directly between multiple instances of the tile are also available, allowing multiple tiles to be treated as larger memories or arithmetic circuits. By using these connections, referred to as cascade inputs and outputs, the input and output bandwidth of the arithmetic circuit is further increased. The arithmetic unit accesses inputs from a combination of: the switch fabric, the memory circuit, a second memory circuit of the tile, and a cascade input. In some example embodiments, the routing of the connections on the tile is based on post-fabrication configuration. In one configuration, all connections are used by the memory circuit, allowing for higher bandwidth in writing or reading the memory. In another configuration, all connections are used by the arithmetic circuit.