US 20220407506A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0407506 A1**

FIEDLER (43) **Pub. Date: Dec. 22, 2022**

(54) **CLOCK MONITOR**

(71) Applicant: **Microsoft Technology Licensing, LLC**, Redmond, WA (US)

(72) Inventor: **Alan Scott FIEDLER**, Santa Barbara, CA (US)

(21) Appl. No.: **17/344,775**

(22) Filed: **Jun. 10, 2021**

Publication Classification

(51) **Int. Cl.**

H03K 5/24	(2006.01)
G06F 1/08	(2006.01)
G01R 31/08	(2006.01)

(52) **U.S. Cl.**

CPC ***H03K 5/24*** (2013.01); ***G06F 1/08*** (2013.01); ***G01R 31/088*** (2013.01); *H03K 2005/00078* (2013.01)

(57) **ABSTRACT**

A clock monitor circuit detects departures from expected values for clock period, clock high time duration, or clock low time duration. A delay line of the clock monitor circuit is composed of delay portions of delay cells. Each delay cell also has a comparator portion with logic to compare aspects of the monitored clock signal to corresponding expected values, and to output a failure detection signal indicating whether the expected values are met. Expected values may be read from a fuse set. The delay of the delay line may be programmatically adjusted. The clock monitor circuit may be combined with a circuit that detects narrow glitches in the monitored clock signal. Devices and systems with one or more monitored clock signals, and methods of clock signal monitoring, are also described.