



US 20230231008A1

(19) **United States**(12) **Patent Application Publication**
JANG et al.(10) **Pub. No.: US 2023/0231008 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SEMICONDUCTOR STRUCTURE AND
FABRICATION METHOD THEREOF***H01L 29/423* (2006.01)*H01L 29/40* (2006.01)(71) Applicant: **CHANGXIN MEMORY
TECHNOLOGIES, INC.**, Hefei (CN)(52) **U.S. Cl.**CPC *H01L 29/0607* (2013.01); *H01L 27/10814*
(2013.01); *H01L 27/10885* (2013.01); *H01L*
27/10891 (2013.01); *H01L 29/42392*
(2013.01); *H01L 29/401* (2013.01)(72) Inventors: **SEMYEONG JANG**, Hefei (CN);
JOONSUK MOON, Hefei (CN);
Deyuan XIAO, Hefei (CN); **MINKI**
HONG, Hefei (CN); **KYONGTAEK**
LEE, Hefei (CN); **JO-LAN CHIN**,
Hefei (CN)

(57)

ABSTRACT(21) Appl. No.: **17/895,065**(22) Filed: **Aug. 25, 2022****Related U.S. Application Data**(63) Continuation of application No. PCT/CN2022/
100397, filed on Jun. 22, 2022.(30) **Foreign Application Priority Data**

Jan. 19, 2022 (CN) 202210060771.4

Publication Classification(51) **Int. Cl.***H01L 29/06* (2006.01)*H01L 27/108* (2006.01)

Embodiments provide a semiconductor structure and a fabrication method. The method includes: providing a substrate provided with first trenches and including an active pillar positioned between adjacent two of the first trenches; forming, in the active pillar, a second trench whose bottom is greater than or equal to a bottom of the first trench in height; forming a first dielectric layer and a protective layer in the first trench, the first dielectric layer being positioned between the protective layer and the active pillar, and an upper surface of the first dielectric layer being lower than an upper surface of the active pillar; forming second dielectric layers on an exposed side wall of the first trench and a side wall of the second trench, a third trench being formed between each of the second dielectric layers and the protective layer, and a fourth trench being formed between the second dielectric layers.

