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An NOR-type memory device, a method of manufacturing the NOR-type memory device, and an electronic apparatus including the NOR-type memory device. The NOR-type memory device includes: a gate stack including a gate conductor layer and a memory functional layer; and a first semiconductor layer and a second semiconductor layer that surround a periphery of the gate stack. The first and second semiconductor layers are respectively located at different heights with respect to the substrate. The memory functional layer is located between the gate conductor layer and each of the first and second semiconductor layers. Each of the first and second semiconductor layers includes a first source/drain region, a channel region, and a second source/drain region that are disposed in sequence in a vertical direction. A memory cell is defined at an intersection of the gate stack and each of the first and second semiconductor layers.

