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(54) **TIME DOMAIN ANALOG-TO-DIGITAL CONVERTER AND ANALOG-TO-DIGITAL CONVERTING METHOD**

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(57) **ABSTRACT**

In analog-to-digital conversion, a plurality of stages configured in a sequence to sequentially decide a plurality of bits in successive-approximation, each of the plurality of stages configured to operate in response to a corresponding clock among a plurality of clocks, and decide a corresponding bit among the plurality of bits from a corresponding positive pulse among a plurality of positive pulses and a corresponding negative pulse among a plurality of negative pulses; and a plurality of clock generating circuits respectively corresponding to a plurality of first stages among the plurality of stages, each of the plurality of clock generating circuit configured to generate the corresponding clock of a corresponding stage among the plurality of first stages based on an operation of a previous stage among the plurality of stages, the previous stage being before the corresponding stage in the sequence.