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**HOSODA et al.**(10) **Pub. No.: US 2024/0179908 A1**(43) **Pub. Date: May 30, 2024**(54) **THREE-DIMENSIONAL MEMORY DEVICE  
INCLUDING A MID-STACK SOURCE LAYER  
AND METHODS FOR FORMING THE SAME****H10B 43/35** (2006.01)**H10B 80/00** (2006.01)(52) **U.S. Cl.**CPC ..... **H10B 43/27** (2023.02); **H01L 24/08**  
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**Masanori TSUTSUMI,** Yokkaichi (JP)(21) Appl. No.: **18/353,621**(22) Filed: **Jul. 17, 2023****Related U.S. Application Data**(60) Provisional application No. 63/385,311, filed on Nov.  
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(57)

**ABSTRACT**

A memory device includes a first-tier alternating stack of first insulating layers and first electrically conductive layers, a source layer overlying the first-tier alternating stack, a second-tier alternating stack of second insulating layers and second electrically conductive layers overlying the source layer, a memory opening vertically extending through the first-tier alternating stack, the source layer, and the second-tier alternating stack, and a memory opening fill structure located in the memory opening. The memory opening fill structure includes a vertical semiconductor channel that extends through the first-tier alternating stack, the source layer, and the second-tier alternating stack. The vertical semiconductor channel has sidewall in contact with the source layer.

