



(43) **Pub. Date:** **Jun. 27, 2024**

- Techniques are provided herein to form semiconductor devices that include a gate cut formed after the formation of source or drain contacts and with a top surface that is substantially coplanar with a top surface of the source or drain contacts. An example semiconductor device includes a gate structure around or otherwise on a semiconductor region and a dielectric layer present on a top surface of the gate structure. Conductive contacts are formed over source and drain regions along a source/drain contact recess or trench. The gate structure may be interrupted with a gate cut that extends through an entire thickness of the gate structure and includes a dielectric material. A top surface of the gate cut may be polished until it is substantially coplanar with a top surface of the dielectric layer over the gate structure and a top surface of the source or drain contacts.

