US 20220368287A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0368287 A1**

Klaren et al. (43) **Pub. Date: Nov. 17, 2022**

(54) **CASCODE AMPLIFIER BIAS CIRCUITS**

(71) Applicant: **pSemi Corporation**, San Diego, CA (US)

(72) Inventors: **Jonathan James Klaren**, San Diego, CA (US); **David Kovac**, Arlington Heights, IL (US); **Eric S. Shapiro**, San Diego, CA (US); **Christopher C. Murphy**, Lake Zurich, IL (US); **Robert Mark Englekirk**, Littleton, CO (US); **Keith Bargroff**, San Diego, CA (US); **Tero Tapio Ranta**, San Diego, CA (US)

(21) Appl. No.: **17/843,372**

(22) Filed: **Jun. 17, 2022**

Related U.S. Application Data

(62) Division of application No. 16/935,999, filed on Jul. 22, 2020, now Pat. No. 11,374,540, which is a division of application No. 16/250,889, filed on Jan. 17, 2019, now Pat. No. 10,756,678, which is a division of application No. 15/268,229, filed on Sep. 16, 2016, now Pat. No. 10,250,199.

Publication Classification

(51) **Int. Cl.**

H03F 1/22	(2006.01)
H03F 3/195	(2006.01)
H03F 3/213	(2006.01)
H03F 3/24	(2006.01)
H03F 1/30	(2006.01)
H03F 1/56	(2006.01)
H03F 3/193	(2006.01)

(52) **U.S. Cl.**

CPC ***H03F 1/223*** (2013.01); ***H03F 3/195*** (2013.01); ***H03F 3/213*** (2013.01); ***H03F 3/245*** (2013.01); ***H03F 1/301*** (2013.01); ***H03F 1/56*** (2013.01); ***H03F 3/193*** (2013.01); *H03F 2200/165* (2013.01); *H03F 2200/21* (2013.01); *H03F 2200/225* (2013.01); *H03F 2200/243* (2013.01); *H03F 2200/294* (2013.01); *H03F 2200/297* (2013.01); *H03F 2200/301* (2013.01); *H03F 2200/306* (2013.01); *H03F 2200/391* (2013.01); *H03F 2200/399* (2013.01); *H03F 2200/42* (2013.01); *H03F 2200/48* (2013.01); *H03F 2200/489* (2013.01); *H03F 2200/492* (2013.01); *H03F 2200/498* (2013.01); *H03F 2200/555* (2013.01); *H03F 2200/61* (2013.01); *H03F 2200/78* (2013.01); *H03F 2200/102* (2013.01); *H03F 2200/105* (2013.01); *H03F 2200/18* (2013.01); *H03F 2200/222* (2013.01); *H03F 2200/387* (2013.01); *H03F 2200/451* (2013.01)

(57) **ABSTRACT**

Bias circuits and methods for silicon-based amplifier architectures that are tolerant of supply and bias voltage variations, bias current variations, and transistor stack height, and compensate for poor output resistance characteristics. Embodiments include power amplifiers and low-noise amplifiers that utilize a cascode reference circuit to bias the final stages of a cascode amplifier under the control of a closed loop bias control circuit. The closed loop bias control circuit ensures that the current in the cascode reference circuit is approximately equal to a selected multiple of a known current value by adjusting the gate bias voltage to the final stage of the cascode amplifier. The final current through the cascode amplifier is a multiple of the current in the cascode reference circuit, based on a device scaling factor representing the relative sizes of the transistor devices in the cascode amplifier and in the cascode reference circuit.