

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0251560 A1 ISOME et al.

Jul. 25, 2024 (43) **Pub. Date:**

(54) THREE-DIMENSIONAL MEMORY DEVICE CONTAINING ETCH STOP STRUCTURES FOR WORD LINE CONTACTS AND

(52) U.S. Cl. CPC *H10B 43/27* (2023.02); *H10B 41/27* (2023.02)

METHODS OF EMPLOYING THE SAME

(57)**ABSTRACT**

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Appl. No.: 18/627,993 (21)

(22) Filed: Apr. 5, 2024

Related U.S. Application Data

- (63) Continuation-in-part of application No. 18/353,546, filed on Jul. 17, 2023.
- (60) Provisional application No. 63/385,051, filed on Nov. 28, 2022.

Publication Classification

(51) Int. Cl. H10B 43/27 (2006.01)H10B 41/27 (2006.01) A device includes an alternating stack of insulating layers and electrically conductive layers extending along a first horizontal direction through a first memory array region and a staircase region, where the alternating stack comprises stepped surfaces in the staircase region, vertical stacks of at least one insulating plate and at least one spacer material plate, where each of the vertical stacks is located on a respective horizontal surface segment of the stepped surfaces in the staircase region, a dielectric material portion located in the staircase region having a stepped bottom surface and contacting each of the vertical stacks, and layer contact via structures located in the staircase region and vertically extending through the dielectric material portion and a respective vertical stack of the vertical stacks and contacting a respective one of the electrically conductive layers.

