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**Chuang**(10) **Pub. No.: US 2023/0231020 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **FIELD PLATING AT SOURCE SIDE OF  
GATE BIAS MOSFETS TO PREVENT VT  
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**ABSTRACT**

The present disclosure introduces a microelectronic device including a source side field plate in a microelectronic device. The microelectronic device may be configured as a metal oxide semiconductor (MOS) transistor, a laterally diffused metal oxide semiconductor (LDMOS) transistor, a drain extended metal oxide semiconductor (DEMOS) transistor, a bipolar junction transistor, a junction field effect transistor, a CMOS transistor, or a gated bipolar device. The source side field plate extends over the source region by a distance which is more than a quarter of the width of the source region. Transistors may suffer from  $V_t$  shifts during gate and drain stress over time. The source side field plate reduces the electric field of the transistor near the gate electrode corner on the source side of the transistor. The gate injection current on the source side and electron trapping in the gate oxide thereby reduced which reduces  $V_t$  shifts over time.

