

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2022/0360263 A1

Nov. 10, 2022 (43) Pub. Date:

(54) INTEGRATED CIRCUIT INCLUDING BACK SIDE CONDUCTIVE LINES FOR CLOCK **SIGNALS**

(71) Applicant: TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY,

LTD., Hsinchu (TW)

Inventors: Kam-Tou SIO, Hsinchu County (TW); Jiun-Wei LU, Keelung City (TW)

Assignee: TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD., Hsinchu (TW)

Appl. No.: 17/872,490 (21)

(22) Filed: Jul. 25, 2022

Related U.S. Application Data

(63) Continuation of application No. 17/186,256, filed on Feb. 26, 2021, now Pat. No. 11,437,998.

Provisional application No. 63/017,905, filed on Apr. 30, 2020.

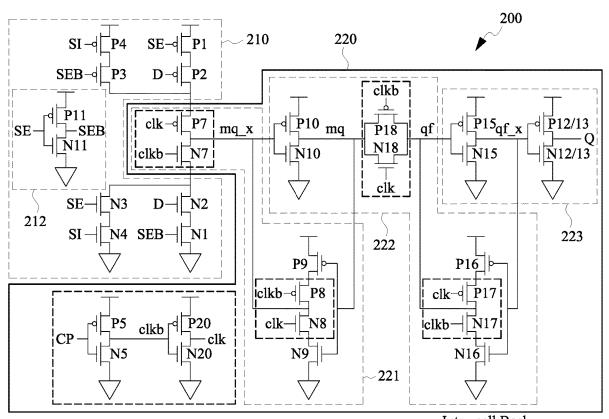
Publication Classification

(51) Int. Cl. H03K 19/17736 (2006.01)H03K 19/17784 (2006.01)G06F 1/10 (2006.01)

(52) U.S. Cl. CPC ... H03K 19/1774 (2013.01); H03K 19/17784 (2013.01); G06F 1/10 (2013.01)

(57)ABSTRACT

An integrated circuit is provided, including a first latch circuit, a second latch circuit, and a clock circuit. The first latch circuit transmits multiple data signals to the second latch circuit through multiple first conductive lines disposed on a front side of the integrated circuit. The clock circuit transmits a first clock signal and a second clock signal to the first latch circuit and the second latch circuit through multiple second conductive lines disposed on a backside, opposite of the front side, of the integrated circuit.



Inter-cell Back Side Routing