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(54) **3D SEMICONDUCTOR MEMORY DEVICES AND STRUCTURES**

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(57) **ABSTRACT**

A 3D semiconductor device, the device including: a first level including a first single crystal layer and a memory control circuit, the memory control circuit including a plurality of first transistors; a first metal layer overlaying the first single crystal layer; a second metal layer overlaying the first metal layer; a plurality of second transistors disposed atop the second metal layer; a third metal layer disposed atop the plurality of second transistors; and a memory array including word-lines and memory cells, where the memory array includes at least four memory mini arrays, where at least one of the plurality of second transistors includes a metal gate, where each of the memory cells includes at least one of the plurality of second transistors, and where the memory control circuit includes at least one Look Up Table circuit ("LUT").