



US 20240178753A1

(19) **United States**(12) **Patent Application Publication**
Xu et al.(10) **Pub. No.: US 2024/0178753 A1**(43) **Pub. Date: May 30, 2024**(54) **REGULATOR WITH FLIPPED VOLTAGE
FOLLOWER ARCHITECTURE**(71) Applicant: **Faraday Technology Corp.**, Hsin-Chu
City (TW)(72) Inventors: **Chen-Hui Xu**, Suzhou City (CN);
Xiao-Dong Fei, Suzhou City (CN);
Wen-Chi Huang, Hsin-Chu City (TW);
Hui-Wen Hu, Suzhou City (CN)(73) Assignee: **Faraday Technology Corp.**, Hsin-Chu
City (TW)(21) Appl. No.: **18/135,182**(22) Filed: **Apr. 16, 2023**(30) **Foreign Application Priority Data**

Nov. 24, 2022 (CN) 202211483125.5

Publication Classification(51) **Int. Cl.**
H02M 3/155 (2006.01)(52) **U.S. Cl.**
CPC **H02M 3/155** (2013.01)(57) **ABSTRACT**

The present invention discloses a regulator. The regulator includes a bias voltage generating circuit and a flipped voltage follower (FVF), wherein the bias voltage generating circuit is configured to generate a bias voltage, and the FVF is configured to generate an output voltage according to the bias voltage and a supply voltage. The FVF includes a first P-type transistor and a first N-type transistor. The P-type transistor is configured to receive the bias voltage via a gate electrode of the P-type transistor, to generate the output voltage on a source electrode of the P-type transistor. A drain electrode of the first N-type transistor is connected to the supply voltage, a source electrode of the first N-type transistor is connected to the source electrode of the first P-type transistor, and a gate electrode of the first N-type transistor receives a driving signal for compensating the output voltage.

