US 20220368327A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0368327 A1**

**CHANG et al.** (43) **Pub. Date: Nov. 17, 2022**

(54) **CIRCUIT FOR MITIGATING SINGLE-EVENT-TRANSIENTS**

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(21) Appl. No.: **17/767,016**

(22) PCT Filed: **Oct. 7, 2020**

(86) PCT No.: **PCT/SG2020/050568**

§ 371 (c)(1),
(2) Date: **Apr. 6, 2022**

(30) **Foreign Application Priority Data**

Oct. 8, 2019 (SG) ..... 10201909392R

**Publication Classification**

(51) **Int. Cl.**

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|---|---|
| ***H03K 19/003*** | (2006.01) |
| ***H03K 17/687*** | (2006.01) |
| ***G11C 7/10*** | (2006.01) |
| ***H03K 3/037*** | (2006.01) |

(52) **U.S. Cl.**

CPC ... ***H03K 19/00338*** (2013.01); ***H03K 17/6872*** (2013.01); ***G11C 7/1069*** (2013.01); ***G11C 7/1096*** (2013.01); ***H03K 3/0375*** (2013.01)

(57) **ABSTRACT**

A circuit for mitigating single-effect-transients (SETs) comprising: a first sub-circuit comprising a first p-type transistor arrangement configured to generate a first output and a first n-type transistor arrangement configured to generate a second output; and a second sub-circuit comprising a connecting p-type transistor arrangement and a connecting n-type transistor arrangement connected in series, wherein the first output and the second output are electrically coupled to each other through the second sub-circuit.