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(54) **MEMORY CONTROLLERS AND MEMORY SYSTEMS INCLUDING THE SAME**

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(57) **ABSTRACT**

A memory controller to control a memory module including a plurality of data chips, a first parity chip and a second parity chip, includes a system error correction code (ECC) engine and a processor to control the system ECC engine. The system ECC engine includes an ECC decoder and a memory to store a parity check matrix. The ECC decoder selects one of a plurality of ECC decoding schemes based on decoding status flags and corrects a plurality of symbol errors in a read codeword set from the memory module by performing an ECC decoding on the read codeword set based on the selected decoding scheme and the parity check matrix. The decoding status flags are provided from the plurality of data chips and each of the decoding status flags indicates whether at least one error bit is detected in respective one of the plurality of data chips.