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(19) **United States**(12) **Patent Application Publication**
Manipatruni et al.(10) **Pub. No.: US 2022/0393686 A1**(43) **Pub. Date: Dec. 8, 2022**(54) **FABRICATION OF A MAJORITY LOGIC GATE HAVING NON-LINEAR INPUT CAPACITORS**(71) Applicant: **Kepler Computing Inc.**, San Francisco, CA (US)(72) Inventors: **Sasikanth Manipatruni**, Portland, OR (US); **Rafael Rios**, Austin, TX (US); **Neal Reynolds**, Bremerton, WA (US); **Ikenna Odinaka**, Durham, NC (US); **Robert Menezes**, Portland, OR (US); **Rajeev Kumar Dokania**, Beaverton, OR (US); **Ramamoorthy Ramesh**, Moraga, CA (US); **Amrita Mathuriya**, Portland, OR (US)(73) Assignee: **Kepler Computing Inc.**, San Francisco, CA (US)(21) Appl. No.: **17/808,290**(22) Filed: **Jun. 22, 2022****Related U.S. Application Data**

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(57)

ABSTRACT

A new class of logic gates are presented that use non-linear polar material. The logic gates include multi-input majority gates. Input signals in the form of digital signals are driven to non-linear input capacitors on their respective first terminals. The second terminals of the non-linear input capacitors are coupled a summing node which provides a majority function of the inputs. The majority node is then coupled driver circuitry which can be any suitable logic gate such as a buffer, inverter, NAND gate, NOR gate, etc. In the multi-input majority or minority gates, the non-linear charge response from the non-linear input capacitors results in output voltages close to or at rail-to-rail voltage levels. Bringing the majority output close to rail-to-rail voltage eliminates the high leakage problem faced from majority gates formed using linear input capacitors.

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