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KIM et al.(10) **Pub. No.: US 2024/0179899 A1**(43) **Pub. Date: May 30, 2024**(54) **NAND FLASH DEVICE**(71) Applicant: **Samsung Electronics Co., Ltd.**,
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(57)

ABSTRACT

A NAND flash device may include a peripheral circuit including a transistor, a substrate, and a device isolation region defining an active region of the substrate. The transistor may include a first gate structure on the active region. The transistor may include source and drain regions extending in a first direction in the active region on both sides of the first gate structure, which may include a first lightly-doped source and drain region adjacent to the first gate structure and a second lightly-doped source and drain region integrally connected thereto. The second lightly-doped source and drain region may be arranged farther from the first gate structure than the first lightly-doped source and drain region. The second lightly-doped source and drain region may have a smaller width in the second direction than a width of the first lightly-doped source and drain region in the second direction.

