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(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0407520 A1****Kim et al.**(43) **Pub. Date: Dec. 22, 2022**(54) **TERNARY LOGIC CIRCUIT****Publication Classification**(71) Applicant: **UNIST(ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY)**, Ulsan (KR)(51) **Int. Cl.**
H03K 19/08 (2006.01)(72) Inventors: **Kyung Rok Kim**, Ulsan (KR); **Jae Won Jeong**, Ulsan (KR); **Youngeun Choi**, Ulsan (KR); **Wooseok Kim**, Ulsan (KR); **Jae Hyeon Jun**, Ulsan (KR)(52) **U.S. Cl.**
CPC **H03K 19/08** (2013.01); **H03K 19/20** (2013.01)(73) Assignee: **UNIST(ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY)**, Ulsan (KR)(57) **ABSTRACT**

A ternary logic circuit includes: a first inverter unit; a second inverter unit arranged in parallel with the first inverter unit; a first junction unit arranged between the first inverter unit and an output terminal and including a tunnel PN junction; and a second junction unit arranged between the second inverter unit and the output terminal and including a tunnel PN junction, wherein, when an absolute value of an input voltage applied to an input terminal is less than a first input voltage, the output terminal outputs a first output voltage, and when the absolute value of the input voltage is greater than the first input voltage and less than a second input voltage, the output terminal outputs a second output voltage, and when the absolute value of the input terminal is greater than the second input voltage, the output terminal outputs a third output voltage.

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