US 20240244819A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0244819 A1**

LAI et al. (43) **Pub. Date: Jul. 18, 2024**

(54) **SEMICONDUCTOR STRUCTURE AND METHOD FOR MANUFACTURING THE SAME**

(71) Applicant: **MACRONIX INTERNATIONAL CO., LTD.**, Hsinchu (TW)

(72) Inventors: **Erh-Kun LAI**, Taichung City (TW); **Feng-Min LEE**, Hsinchu City (TW)

(21) Appl. No.: **18/188,612**

(22) Filed: **Mar. 23, 2023**

Related U.S. Application Data

(60) Provisional application No. 63/438,796, filed on Jan. 13, 2023.

Publication Classification

(51) **Int. Cl.**
H10B 12/00 (2006.01)

(52) **U.S. Cl.**
CPC ***H10B 12/20*** (2023.02)

(57) **ABSTRACT**

A semiconductor structure is provided. The semiconductor structure has a device defining region. The device defining region includes a first portion and a second portion separated from each other. The semiconductor structure includes a stack. The stack includes first conductive layers and first dielectric layers disposed alternately. The stack has an opening through the stack in the device defining region. The semiconductor structure further includes a second conductive layer, a first conductive pillar, a third conductive layer, a second conductive pillar, and a third conductive pillar. The second conductive layer is disposed along a sidewall of the opening. The first conductive pillar is disposed in the opening in the first portion. The third conductive layer is disposed in the opening along an edge of the second portion. The second conductive pillar and the third conductive pillar are disposed in the second portion and separated from each other.