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(54) **VTFET CIRCUIT WITH OPTIMIZED MOL**

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(57) **ABSTRACT**

Integrated circuits and related logic circuits and structures employing VTFET logic devices. In particular, during middle-of-line (MOL) processing, method steps are employed for forming two-level MOL contact connector structures below first (M1) metallization level wiring formed during subsequent BEOL processing. Using damascene and subtractive metal etch techniques, respective MOL contact connector structures at two levels are formed with a second level above a first level contact. These contact connector structures at two levels below M1 metallization level can provide cross-connections to VTFET devices of logic circuits that enable increased scaling of the logic circuit designs, e.g., especially for multiplexor circuit layouts due to wiring access. The flexible MOL cross-connections made below M1 metallization level provides for much improved M1 and M2 wirability and enable semiconductor circuit layouts that allow for improved cell size reduction without creating significant connection issues at high wiring levels thereby increasing circuit design flexibility.