

# (19) United States

## (12) Patent Application Publication (10) Pub. No.: US 2024/0213263 A1 YANG et al.

Jun. 27, 2024 (43) **Pub. Date:** 

## (54) DUMMY PIXEL CIRCUIT, DISPLAY PANEL AND DISPLAY DEVICE

(71) Applicants: Chengdu BOE Optoelectronics

Technology Co., Ltd., Chengdu, Sichuan (CN); BOE Technology Group

Co., Ltd., Beijing (CN)

(72) Inventors: **Huijuan YANG**, Beijing (CN);

Maoying LIAO, Beijing (CN); Yang ZHOU, Beijing (CN); Lu BAI, Beijing (CN); Jie DAI, Beijing (CN); Dan

CAO, Beijing (CN)

(21) Appl. No.: 17/915,421

(22) PCT Filed: Oct. 29, 2021

(86) PCT No.: PCT/CN2021/127268

§ 371 (c)(1),

(2) Date: Sep. 28, 2022

#### (30)Foreign Application Priority Data

Apr. 7, 2021 (CN) ...... 202110373291.9

### **Publication Classification**

(51) Int. Cl. H01L 27/12 (2006.01) (52) U.S. Cl. CPC ...... H01L 27/124 (2013.01); H01L 27/1218 (2013.01)

#### ABSTRACT (57)

The present disclosure relates to a dummy pixel circuit, a display panel, and a display device, which belongs to the field of display. The dummy pixel circuit is applicable to a display panel provided with two through vias and disposed between the two through vias, and the dummy pixel circuit includes a pixel sub-circuit and a dummy sub-circuit. The pixel sub-circuit includes one or more first transistors, wherein a control electrode of the first transistor is electrically connected to the first gate line. The dummy sub-circuit includes one or more second transistors, wherein a control electrode of the dummy sub-circuit is electrically connected to the first gate line, a first electrode of the second transistor is electrically connected to a first electrode of a corresponding one of the one or more first transistors, and a second electrode of the second transistor is electrically connected to a second electrode of the corresponding first transistor. Each of the one or more first transistors corresponds to at least one of the one or more second transistors. The second transistor consumes the power transmitted transferred by the first gate line, and thus a total load of the pixel circuit electrically connected to the first gate line is increased. In this way, the pixel, to which the pixel circuit electrically connected to the first gate line corresponds, has an increased luminance, thereby mitigating display mura of display panel.

