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**JEONG et al.**(10) **Pub. No.: US 2022/0368351 A1**(43) **Pub. Date: Nov. 17, 2022**(54) **MEMORY AND OPERATION METHOD OF MEMORY**(71) Applicant: **SK hynix Inc.**, Gyeonggi-do (KR)(72) Inventors: **Jin Ho JEONG**, Gyeonggi-do (KR);  
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**Munseon JANG**, Gyeonggi-do (KR)(21) Appl. No.: **17/877,484**(22) Filed: **Jul. 29, 2022****Related U.S. Application Data**

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(57)

**ABSTRACT**

A memory includes a first check matrix calculation circuit suitable for generating a first parity by calculating a group indicator portion of a check matrix and a write data; a memory core suitable for storing the write data and the first parity; a first syndrome calculation circuit suitable for generating a first syndrome by adding the first parity which is read from the memory core to a first calculation result obtained by calculating the group indicator portion and the data which is read from the memory core; and a failure determination circuit suitable for accumulating the first syndromes for a region of the memory core to generate a vector and determining a presence of a failure of the region based on the vector.

