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(54) **METHODS AND APPARATUS FOR PROVIDING A HIGH-SPEED UNIVERSAL SERIAL BUS (USB) INTERFACE FOR A FIELD-PROGRAMMABLE GATE ARRAY (FPGA)**

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(57) **ABSTRACT**

A system containing a host and a device having a field-programmable gate array ("FPGA") is disclosed. The system includes a set of configurable logic blocks ("LBs"), a bus, and a Universal Serial Bus ("USB") interface. The configurable LBs, in one aspect, are able to be selectively programmed to perform one or more logic functions. The bus contains a P-channel and an N-channel operable to transmit signals in accordance with a high-speed USB protocol. The USB interface is configured to include a first differential comparator operable to identify a logic zero state at the P-channel and a second differential comparator operable to identify a logic zero state at the N-channel.