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(54) **DIGITAL TO ANALOG CONVERTER**

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(57) **ABSTRACT**

The present disclosure relates to a DAC that includes: a first pixel including a first transfer gate coupling a memory node of the first pixel and a capacitive sensing node (SN); a second pixel comprising a first transfer gate coupling a memory node of the second pixel and the capacitive SN; a reset transistor coupling the sensing node to a first voltage supply rail; and a control circuit configured to store electrical charge by activating the reset transistor to apply a reference voltage to the memory node of each of the first and second pixels; and generate a voltage of the DAC at the sensing node by deactivating the reset transistor and controlling the first transfer gates of the first and second pixels to transfer the charge stored.