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LIN et al.(10) **Pub. No.: US 2024/0251540 A1**(43) **Pub. Date: Jul. 25, 2024**(54) **INTEGRATED CIRCUIT DEVICE AND METHOD****Publication Classification**(51) **Int. Cl.**
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CPC **H10B 10/125** (2023.02); **H10B 10/18** (2023.02); **G11C 11/418** (2013.01)(71) Applicant: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**, Hsinchu (TW)(72) Inventors: **Kao-Cheng LIN**, Hsinchu (TW); **Hidehiro FUJIWARA**, Hsinchu (TW); **Yen Lin CHUNG**, Hsinchu (TW); **Wei Min CHAN**, Hsinchu (TW); **Yen-Huei CHEN**, Hsinchu (TW)(57) **ABSTRACT**

An integrated circuit (IC) device includes a memory array including a plurality of memory cells, a first word line over the memory array and electrically coupled to at least one first memory cell among the plurality of memory cells, and a second word line under the memory array and electrically coupled to at least one second memory cell among the plurality of memory cells. Each memory cell among the plurality of memory cells includes complementary field-effect transistor (CFET) devices.

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