US 20220416770A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0416770 A1**

AZAM et al. (43) **Pub. Date: Dec. 29, 2022**

(54) **METHODS AND DEVICES FOR DIGITAL CLOCK MULTIPLICATION OF A CLOCK TO GENERATE A HIGH FREQUENCY OUTPUT**

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(21) Appl. No.: **17/356,564**

(22) Filed: **Jun. 24, 2021**

Publication Classification

(51) **Int. Cl.**

H03K 5/00	(2006.01)
G06F 7/68	(2006.01)
H03K 5/02	(2006.01)

(52) **U.S. Cl.**

CPC ***H03K 5/00006*** (2013.01); ***G06F 7/68*** (2013.01); ***H03K 5/02*** (2013.01); *H03K 2005/00286* (2013.01)

(57) **ABSTRACT**

A digital clock multiplier (DCM) circuit including: a plurality of power amplifier (PA) rows, wherein each PA row comprises a plurality of cascade switched capacitor power amplifiers (SCPA) unit cells configured to: receive a phase shift of a driving clock phase; and one or more processors configured to: disable of one or more of the plurality of cascade SCPA unit cells based on a frequency of the phase shift; generate an output signal for each of the cascade SCPA unit cells; and combine the output signal for each of the cascade SCPA unit cells to generate an PA row output signal.