

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0223178 A1 Tang et al.

(43) **Pub. Date:**

Jul. 4, 2024

(54) INTEGRATED CIRCUIT FOR GATE OVERVOLTAGE PROTECTION OF POWER **DEVICES**

(71) Applicant: Efficient Power Conversion Corporation, El Segundo, CA (US)

(72) Inventors: Zhikai Tang, Sunnyvale, CA (US); Edward Lee, Fullerton, CA (US); Jianjun Cao, Torrance, CA (US)

(73) Assignee: Efficient Power Conversion Corporation, El Segundo, CA (US)

(21) Appl. No.: 18/398,302 Dec. 28, 2023 (22) Filed:

Related U.S. Application Data

(60) Provisional application No. 63/477,502, filed on Dec. 28, 2022.

Publication Classification

(51) Int. Cl. H03K 17/081 (2006.01)

U.S. Cl. CPC H03K 17/08104 (2013.01)

ABSTRACT (57)

An integrated gate overvoltage protection circuit for protecting the gate of a main field effect transistor (FET). The gate protection circuit includes a blocking FET and a discharge FET connected between the gate and the drain of the main FET. The gate overvoltage protection circuit is configured to turn on both the first FET and the second FET in the event of a fault condition, such that charge from the gate of the main FET is discharged through the first FET and the second FET to the drain of the main FET, thereby protecting the gate of the main FET.

