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(54) **D-TYPE WHOLLY DISSIMILAR HIGH-SPEED STATIC SET-RESET FLIP FLOP**

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(57) **ABSTRACT**

A circuit is provided. The circuit includes a first master stage, a second master stage, a first slave stage, a first slave stage, and a second slave stage. The first master stage includes a data input line. The second master stage includes an inverse data input line. The first slave stage is coupled to an output of the first master stage. The second slave stage is coupled to an output of the second master stage. The first slave stage generates an output signal during a rising edge of a clock cycle. The second slave stage generates an inverted output signal during the rising edge of the clock cycle. The output signal and the inverted output signal are available concurrently.