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(54) **VTFET CELL BOUNDARY HAVING AN IN-LINE CONTACT**

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(57) **ABSTRACT**

Embodiments of the invention provide a multi-layer integrated circuit (IC) structure that includes a cell having a cell boundary defined by a plurality of transistor-gate pitch (TGP) regions and an in-line contact region. The plurality of TGP regions include a reduced-area TGP region and non-reduced area TGP regions. The reduced-area TGP region is less than each of the non-reduced-area TGP regions. An in-line contact is within the in-line contact region and operable to electrically couple to a source or drain (S/D) region within the in-line contact region.