



US 20240215255A1

(19) **United States**

(12) **Patent Application Publication**
Chia et al.

(10) **Pub. No.: US 2024/0215255 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **METHOD FOR FABRICATING MEMORY DEVICE**

(60) Provisional application No. 63/051,880, filed on Jul. 14, 2020.

(71) Applicant: **Taiwan Semiconductor Manufacturing Company, Ltd.**,
Hsinchu (TW)

Publication Classification

(51) **Int. Cl.**
H10B 51/20 (2006.01)
G11C 11/22 (2006.01)
H10B 51/10 (2006.01)
H10B 51/40 (2006.01)

(72) Inventors: **Han-Jong Chia**, Hsinchu City (TW);
Meng-Han Lin, Hsinchu (TW);
Yu-Ming Lin, Hsinchu City (TW)

(52) **U.S. Cl.**
CPC *H10B 51/20* (2023.02); *G11C 11/2255*
(2013.01); *G11C 11/2257* (2013.01); *H10B*
51/10 (2023.02); *H10B 51/40* (2023.02)

(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**,
Hsinchu (TW)

(21) Appl. No.: **18/602,041**

(57) **ABSTRACT**

(22) Filed: **Mar. 12, 2024**

A memory device including a word line, memory cells, source lines and bit lines is provided. The memory cells are embedded in and penetrate through the word line. The source lines and the bit lines are electrically connected the memory cells. A method for fabricating a memory device is also provided.

Related U.S. Application Data

(62) Division of application No. 17/163,574, filed on Feb. 1, 2021, now Pat. No. 11,963,363.

