US 20240213983A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0213983 A1**

**TAKEUCHI** (43) **Pub. Date: Jun. 27, 2024**

(54) **CMOS CIRCUIT**

(71) Applicant: **Japan Aerospace Exploration Agency**, Chofu-shi, Tokyo (JP)

(72) Inventor: **Kozo TAKEUCHI**, Chofu-shi (JP)

(21) Appl. No.: **18/555,494**

(22) PCT Filed: **May 11, 2022**

(86) PCT No.: **PCT/JP2022/019955**

§ 371 (c)(1),
(2) Date: **Oct. 13, 2023**

(30) **Foreign Application Priority Data**

May 19, 2021 (JP) ..... 2021-084623

**Publication Classification**

(51) **Int. Cl.**
***H03K 19/003*** (2006.01)

(52) **U.S. Cl.**
CPC ..... ***H03K 19/00315*** (2013.01)

(57) **ABSTRACT**

A complementary metal oxide semiconductor (CMOS) circuit includes a logical operation circuit formed on a substrate of a first conductivity type and including at least a combination of a first transistor of the first conductivity type having a first well of a second conductivity type different from the first conductivity type and a second transistor of the second conductivity type having a second well of the first conductivity type, a third transistor of the first conductivity type having a gate terminal connected to the second well, and a fourth transistor of the second conductivity type having a gate terminal connected to the first well.