US 20230230955A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2023/0230955 A1**

HUH et al. (43) **Pub. Date: Jul. 20, 2023**

(54) **MULTI-CHIP STACKING METHOD**

(71) Applicant: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)

(72) Inventors: **Yeunhee HUH**, Namyangju-si (KR); **Chisung BAE**, Yongin-si (KR)

(73) Assignee: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)

(21) Appl. No.: **17/863,568**

(22) Filed: **Jul. 13, 2022**

(30) **Foreign Application Priority Data**

Jan. 18, 2022 (KR) 10-2022-0007404

Publication Classification

(51) **Int. Cl.**

H01L 25/065 (2006.01)
H01L 23/48 (2006.01)
H01L 25/00 (2006.01)

(52) **U.S. Cl.**

CPC ***H01L 25/0652*** (2013.01); ***H01L 23/481*** (2013.01); ***H01L 25/50*** (2013.01); *H01L 2225/06541* (2013.01)

(57) **ABSTRACT**

An integrated circuit having a plurality of stacked chips, and a method of manufacturing thereof are provided. The integrated circuit includes a substrate, a plurality of chips stacked on a printed circuit board, wherein each of the plurality of chips includes a plurality of circuits, and a plurality of interconnects configured to electrically connect each of the plurality of circuits included in the each of the plurality of chips to the substrate, wherein the plurality of chips are unconnected with regard to each other, and are stacked such that areas of each of the plurality of chips, to which the plurality of interconnects are connected, are disposed in a non-overlapping manner with each other.