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(19) **United States**(12) **Patent Application Publication****Jang et al.**(10) **Pub. No.: US 2024/0213231 A1**(43) **Pub. Date:****Jun. 27, 2024**(54) **SEMICONDUCTOR DEVICE AND METHOD OF FORMING VERTICAL INTERCONNECT STRUCTURE FOR POP MODULE**(71) Applicant: **STATS ChipPAC Pte. Ltd., Singapore (SG)**(72) Inventors: **Junghwan Jang, Incheon (KR);
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ABSTRACT

A semiconductor device has a substrate and a first light sensitive material formed over the substrate. A plurality of first conductive posts is formed over the substrate by patterning the first light sensitive material and filling the pattern with a conductive material. A plurality of electrical contacts is formed over the substrate and the conductive posts are formed over the electrical contacts. A first electric component is disposed over the substrate between the first conductive posts. A plurality of second conductive posts is formed over the first electrical component by patterning a second light sensitive material and filling the pattern with conductive material. A first encapsulant is deposited over the first electrical component and conductive posts. A portion of the first encapsulant is removed to expose the first conductive posts. A second electrical component is disposed over the first electrical component and covered with a second encapsulant.

