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(54) **DIVIDED QUAD CLOCK-BASED INTER-DIE CLOCKING IN A THREE-DIMENSIONAL STACKED MEMORY DEVICE**

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(57) **ABSTRACT**

A memory device includes a clock input configured to receive a clock from a host device. The memory device also includes a command input configured to receive command and address bits from the host device. The memory device further includes multiple die stacked in a three-dimensional stack. A first die of the plurality of die includes a first plurality of memory cells and first local control circuitry. The first local circuitry includes division circuitry configured to receive the clock from the clock input, generate a divided clock having a lower frequency than that of the clock, and generate multiple clocks from the divided clock with each of the multiple clocks having a lower frequency than the divided clock. The memory device also includes one or more transmitters configured to transmit the multiple clocks using inter-die interconnects between the multiple die.