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(54) **IMPLANTATIONS FOR FORMING SOURCE/DRAIN REGIONS OF DIFFERENT TRANSISTORS**

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(57) **ABSTRACT**

A method includes forming a first transistor including forming a first gate stack, epitaxially growing a first source/drain region on a side of the first gate stack, and performing a first implantation to implant the first source/drain region. The method further includes forming a second transistor including forming a second gate stack, forming a second gate spacer on a sidewall of the second gate stack, epitaxially growing a second source/drain region on a side of the second gate stack, and performing a second implantation to implant the second source/drain region. An inter-layer dielectric is formed to cover the first source/drain region and the second source/drain region. The first implantation is performed before the inter-layer dielectric is formed, and the second implantation is performed after the inter-layer dielectric is formed.