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(19) **United States**(12) **Patent Application Publication****Hwang et al.**(10) **Pub. No.: US 2024/0237349 A1**(43) **Pub. Date:****Jul. 11, 2024**(54) **THREE-DIMENSIONAL SEMICONDUCTOR
MEMORY DEVICE AND METHOD OF
FABRICATING THE SAME****H10B 43/35** (2006.01)**H10B 43/40** (2006.01)**H10B 80/00** (2006.01)(52) **U.S. Cl.****CPC** **H10B 43/27** (2023.02); **G11C 16/0483**(2013.01); **H01L 23/5283** (2013.01); **H01L****25/0652** (2013.01); **H10B 43/10** (2023.02);**H10B 43/35** (2023.02); **H10B 43/40**(2023.02); **H10B 80/00** (2023.02); **H01L****2225/06506** (2013.01)(71) Applicant: **Samsung Electronics Co., Ltd.**,
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Sanghoo Cho, Suwon-si (KR)(21) Appl. No.: **18/464,348**(22) Filed: **Sep. 11, 2023**(30) **Foreign Application Priority Data**

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A three-dimensional semiconductor memory device may include a bottom structure and a top structure thereon. The bottom structure may include a semiconductor substrate including a cell array region and a connection region extending therefrom, and a first stack including first gate electrodes and first interlayer insulating layers alternately stacked on the semiconductor substrate. The top structure may include a second stack including second gate electrodes and second interlayer insulating layers alternately stacked on the first stack. Respective lengths of the first gate electrodes in a second direction may decrease as a distance in a first direction increases, and respective lengths of the second gate electrodes in the second direction may increase as a distance in the first direction increases. The first direction may be perpendicular to a bottom surface of the semiconductor substrate, and the second direction may be parallel to the bottom surface of the semiconductor substrate.

