US 20240213146A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0213146 A1**

KIM et al. (43) **Pub. Date: Jun. 27, 2024**

(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: **SAMSUNG ELECTRONICS CO., LTD.**, SUWON-SI (KR)

(72) Inventors: **HYUNGJUNE KIM**, Suwon-si (KR); **BYUNGYUN KANG**, Suwon-si (KR); **DONGHYUN KIM**, Suwon-si (KR)

(21) Appl. No.: **18/352,552**

(22) Filed: **Jul. 14, 2023**

(30) **Foreign Application Priority Data**

Dec. 22, 2022 (KR) 10-2022-0182091

Publication Classification

(51) **Int. Cl.**

H01L 23/522 (2006.01)

H01L 23/528 (2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/5226*** (2013.01); ***H01L 23/528*** (2013.01); *H01L 27/0924* (2013.01)

(57) **ABSTRACT**

A semiconductor device according to the disclosure includes: a substrate including a first side and a second side opposite each other with a thickness therebetween, a first wire disposed on the first side of the substrate, a first dummy wire disposed on the first side of the substrate and spaced apart from the first wire, a second wire disposed on the second side of the substrate, a second dummy wire disposed on the second side of the substrate and spaced apart from the second wire, a through via passing through the substrate and connecting the first wire and the second wire, and a plurality of dummy through vias passing through the substrate , wherein the plurality of dummy through vias are laterally offset and physically separated from the first wire and the second wire, wherein a center of at least one of the plurality of dummy through vias is laterally offset from an edge of at least one of the first dummy wire and the second dummy wire.