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NAKACHI et al.(10) **Pub. No.: US 2024/0244852 A1**(43) **Pub. Date: Jul. 18, 2024**(54) **MEMORY DEVICE**(71) Applicant: **Kioxia Corporation**, Tokyo (JP)(72) Inventors: **Yuki NAKACHI**, Kuwana (JP); **Yuya SAEKI**, Yokkaichi (JP)(73) Assignee: **Kioxia Corporation**, Tokyo (JP)(21) Appl. No.: **18/538,551**(22) Filed: **Dec. 13, 2023**(30) **Foreign Application Priority Data**

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ABSTRACT

A memory device includes a first conductive layer; a second conductive layer arranged with the first conductive layer in a first direction in a first region; third conductive layers arranged in the first region and mutually separated in the first direction; a conductor extending in the first direction and intersecting extensions of the third conductive layers in a second region; and a memory pillar having portions intersecting the third conductive layers and functioning as memory cells. The second conductive layer includes a first portion extending in a plane and in contact with the memory pillar and a second portion arranged on a surface of the first conductive layer to protrude with respect to the first portion. The first conductive layer includes third and fourth portions in contact with the second portion and the conductor, respectively.

