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(54) **ARCHITECTURE FOR MULTIDECK MEMORY ARRAYS**

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(57) **ABSTRACT**

An array of memory cells in a multideck configuration comprising a plurality of superimposed decks, a plurality of access lines comprising at least a first plurality of access lines arranged in a first level, a second plurality of access lines arranged in a second level, and a third plurality of access lines arranged in a third level between the first plurality of access lines and the second plurality of access lines, the third plurality of access lines being arranged between two decks of the plurality of decks, a plurality of drivers configured to drive signals to the access lines, and connection elements configured to electrically connect the access lines to the respective drivers. The connections elements and the access lines are arranged so that a single driver of the plurality of drivers is configured to drive at least one access line of each level of the at least three levels.