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(54) **PULSE WIDTH CLOCK TOPOLOGY STRUCTURE CIRCUIT**

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(57) **ABSTRACT**

A pulse width clock topology structure circuit, comprising a clock pulse width generation module and a clock topology delay module. The clock pulse width generation module connects an input clock and n stages of delay sub-modules in series; an output end of each stage of delay sub-module is connected to an input end of a selector; a certain required delay clock is selected by means of m+1 control signals of the selector, and an "AND" operation is performed on the required delay clock and an original input clock to generate different pulse width clock outputs as inputs of the clock topology delay module; and the clock topology delay module can generate a plurality of different delay clocks for different latches to use.