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(19) **United States**(12) **Patent Application Publication****XIAN et al.**(10) **Pub. No.: US 2022/0360253 A1**(43) **Pub. Date: Nov. 10, 2022**(54) **METHOD FOR FORMING A TIMING
CIRCUIT ARRANGEMENTS FOR
FLIP-FLOPS****H03K 3/356** (2006.01)**H03K 3/3562** (2006.01)**H03K 3/289** (2006.01)(71) Applicants: **TAIWAN SEMICONDUCTOR
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A method of forming a semiconductor device includes forming active regions, forming S/D regions, forming MD contact structures and forming gate lines resulting in corresponding transistors that define a first time delay circuit having a first input configured to receive a first clock signal and having a first output configured to generate a second clock signal from the first clock signal; and corresponding transistors that define a second time delay circuit having a second input configured to receive the second clock signal and having a second output configured to generate a third clock signal from the first clock signal; forming a first gate via-connector in direct contact with the first gate line atop the first-type active region in the first area; and forming a second gate via-connector in direct contact with the second gate line atop the second-type active region in the second area.

