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(54) **MEMORY DEVICE HAVING 2-TRANSISTOR VERTICAL MEMORY CELL AND WRAPPED DATA LINE STRUCTURE**

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(57) **ABSTRACT**

Some embodiments include apparatuses and methods forming the apparatuses. One of the apparatuses includes a first transistor including a first channel region, and a charge storage structure separated from the first channel region; a second transistor including a second channel region formed over the charge storage structure; and a data line formed over and contacting the first channel region and the second channel region, the data line including a portion adjacent the first channel region and separated from the first channel region by a dielectric material.