US 20240213989A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0213989 A1**

TIEBOUT et al. (43) **Pub. Date: Jun. 27, 2024**

(54) **SYSTEM AND METHOD FOR TESTING A PHASE NOISE OR JITTER OF A PHASE-LOCKED LOOP**

(71) Applicant: **Intel Corporation**, Santa Clara, CA (US)

(72) Inventors: **Marc Jan Georges TIEBOUT**, Finkenstein (AT); **Edwin THALLER**, Faak am See (AT); **Kameran AZADET**, San Ramon, CA (US)

(21) Appl. No.: **18/145,867**

(22) Filed: **Dec. 23, 2022**

Publication Classification

(51) **Int. Cl.**

H03L 7/091	(2006.01)
H03L 7/07	(2006.01)
H03L 7/099	(2006.01)

(52) **U.S. Cl.**

CPC ***H03L 7/091*** (2013.01); ***H03L 7/07*** (2013.01); ***H03L 7/0991*** (2013.01)

(57) **ABSTRACT**

A system and method for testing or determining a phase noise and/or jitter of a phase locked loop (PLL). The system includes a first PLL configured to generate a first clock signal based on a reference clock signal, a first buffer for providing the reference clock signal to the first PLL, a mixer configured to mix the first clock signal with a second clock signal, an analog-to-digital converter (ADC) configured to convert an output of the mixer to digital data, and a processing circuit configured to process the digital data to determine a phase noise or jitter of the first PLL and generate an output indicative of the phase noise or jitter of the first PLL. The system may include a second PLL configured to generate the second clock signal based on the reference clock signal, and a second buffer for providing the reference clock signal to the second PLL.