



US 20240213147A1

(19) **United States**

(12) **Patent Application Publication**
HOSODA et al.

(10) **Pub. No.: US 2024/0213147 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **THREE-DIMENSIONAL MEMORY DEVICE
WITH SELF-ALIGNED MEMORY BLOCK
ISOLATION AND METHODS FOR FORMING
THE SAME**

H10B 43/10 (2023.01)

H10B 43/27 (2023.01)

H10B 43/35 (2023.01)

(52) **U.S. Cl.**

CPC **H01L 23/5226** (2013.01); **H01L 23/5283**
(2013.01); **H10B 43/10** (2023.02); **H10B**
43/27 (2023.02); **H10B 43/35** (2023.02)

(71) Applicant: **SANDISK TECHNOLOGIES LLC,**
ADDISON, TX (US)

(72) Inventors: **Naohiro HOSODA, Yokkaichi (JP);**
Tatsuya HINOUE, Yokkaichi (JP)

(21) Appl. No.: **18/355,067**

(22) Filed: **Jul. 19, 2023**

Related U.S. Application Data

(60) Provisional application No. 63/477,271, filed on Dec.
27, 2022.

Publication Classification

(51) **Int. Cl.**

H01L 23/522 (2006.01)

H01L 23/528 (2006.01)

(57)

ABSTRACT

A three-dimensional memory device may be formed by forming a vertically alternating sequence of insulating layers and sacrificial material layers over a substrate, forming memory openings, forming sacrificial memory opening fill structures in the memory openings, forming first cavities by removing a first subset of the sacrificial memory opening fill structures, forming laterally-extending cavities by performing an isotropic etch process that laterally recesses the sacrificial material layers, forming electrically conductive layers in the laterally-extending cavities, forming second cavities by removing the second subset of the sacrificial memory opening fill structures, and forming memory opening fill structures in each of the first cavities and the second cavities.

