



US 20240213144A1

(19) **United States**

(12) **Patent Application Publication**
Xue et al.

(10) **Pub. No.: US 2024/0213144 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **ON-CHIP CAPACITORS IN SEMICONDUCTOR DEVICES AND METHODS FOR FORMING THE SAME**

(71) Applicant: **YANGTZE MEMORY TECHNOLOGIES CO., LTD.**, Wuhan (CN)

(72) Inventors: **Lei Xue**, Wuhan (CN); **Wei Liu**, Wuhan (CN); **Liang Chen**, Wuhan (CN)

(21) Appl. No.: **18/599,597**

(22) Filed: **Mar. 8, 2024**

Related U.S. Application Data

(60) Continuation of application No. 17/488,287, filed on Sep. 28, 2021, now Pat. No. 11,955,422, which is a division of application No. 17/147,409, filed on Jan. 12, 2021, now Pat. No. 11,652,042, which is a continuation of application No. PCT/CN2020/128709, filed on Nov. 13, 2020.

Foreign Application Priority Data

Sep. 2, 2020 (WO) PCT/CN2020/112959
Sep. 2, 2020 (WO) PCT/CN2020/112962

Publication Classification

(51) **Int. Cl.**
H01L 23/522 (2006.01)
H01L 21/768 (2006.01)
H10B 43/27 (2006.01)
H10B 43/35 (2006.01)

(52) **U.S. Cl.**
CPC H01L 23/5223 (2013.01); **H01L 21/76832** (2013.01); **H01L 28/40** (2013.01); **H01L 28/56** (2013.01); **H10B 43/27** (2023.02); **H10B 43/35** (2023.02)

(57) **ABSTRACT**

A method for forming a three-dimensional (3D) memory device is disclosed. A stack is formed. The stack includes a first region and a second region disposed on a side of the first region along a first direction. The stack includes a first stack in the first region and a second stack in the second region. An interlayer dielectric (ILD) layer is formed over the second stack. Capacitors including first contacts each extending through the ILD layer and disposed on a first side of the second stack along a second direction are formed. The second direction is perpendicular to the first direction.

