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(54) LOGIC CELL FOR PROGRAMMABLE GATE ARRAY

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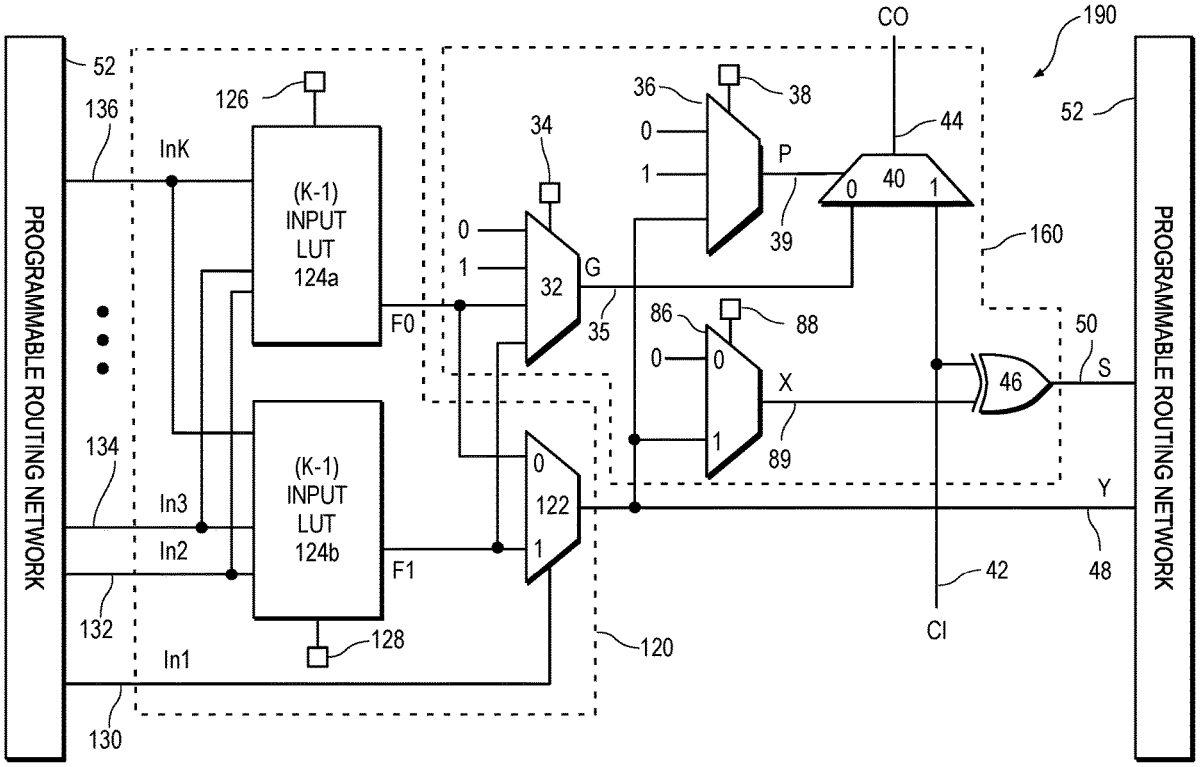
(57) **ABSTRACT**

A logic cell for a programmable logic integrated circuit apparatus includes a K-input lookup table (LUT) circuit having a primary output Y, wherein Y is any function of K inputs, and at least one additional output (F). A carry circuit receives the outputs of the LUT and a carry-in input CI. The carry circuit generates a sum output S and a carry-out output CO. The carry circuit can be configured to provide S=CI and select CO from the set {0, 1, F}. The carry circuit can alternatively be configured to provide S=EXOR(Y, CI) and select CO from the set {0, 1, F}. The carry circuit can alternatively be configured to provide S=EXOR(Y, CI) and CO=CI if Y=q or to select CO from the set {0, 1, F} if Y≠q, where q is a pre-determined value (e.g., such as 0 or 1).