



US 20220407459A1

(19) **United States**(12) **Patent Application Publication**
JUNG et al.(10) **Pub. No.: US 2022/0407459 A1**(43) **Pub. Date: Dec. 22, 2022**(54) **CLOCK INTEGRATED CIRCUIT
INCLUDING HETEROGENEOUS
OSCILLATORS AND APPARATUS
INCLUDING THE CLOCK INTEGRATED
CIRCUIT**(71) Applicant: **SAMSUNG ELECTRONICS CO.,
LTD.**, Suwon-si (KR)(72) Inventors: **Jaehong JUNG**, Bucheon-si (KR);
Seunghyun OH, Seoul (KR); **Jinhyeon
LEE**, Hwaseong-si (KR); **Gihyeok HA**,
Seoul (KR); **Seungjin KIM**, Yongin-si
(KR); **Joomyoung KIM**, Hwaseong-si
(KR); **Yelim YOUN**, Hwaseong-si
(KR); **Jaehoon LEE**, Suwon-si (KR)(73) Assignee: **SAMSUNG ELECTRONICS CO.,
LTD.**, Suwon-si (KR)(21) Appl. No.: **17/845,378**(22) Filed: **Jun. 21, 2022**(30) **Foreign Application Priority Data**Jun. 22, 2021 (KR) 10-2021-0081039
Sep. 24, 2021 (KR) 10-2021-0126725**Publication Classification**(51) **Int. Cl.**
H03B 5/32 (2006.01)
H03B 5/20 (2006.01)
H03B 5/04 (2006.01)
G06F 1/06 (2006.01)
(52) **U.S. Cl.**
CPC **H03B 5/32** (2013.01); **H03B 5/20**
(2013.01); **H03B 5/04** (2013.01); **G06F 1/06**
(2013.01); **H03B 2200/0082** (2013.01)(57) **ABSTRACT**

A clock integrated circuit is provided. The clock integrated circuit includes: a first clock generator which includes a crystal oscillator configured to generate a first clock signal; and a second clock generator which includes a resistance-capacitance (RC) oscillator and a first frequency divider, and is configured to: generate a second clock signal using the first frequency divider based on a clock signal output from the RC oscillator; perform a first calibration operation for adjusting a frequency division ratio of the first frequency divider to a first frequency division ratio based on the first clock signal; and perform a second calibration operation for adjusting the first frequency division ratio to a second frequency division ratio based on a sensed temperature.

