US 20220376694A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0376694 A1**

Shih (43) **Pub. Date: Nov. 24, 2022**

(54) **METHOD AND APPARATUS FOR PERFORMING ON-SYSTEM PHASE-LOCKED LOOP MANAGEMENT IN MEMORY DEVICE**

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(21) Appl. No.: **17/878,042**

(22) Filed: **Jul. 31, 2022**

Related U.S. Application Data

(63) Continuation of application No. 17/161,552, filed on Jan. 28, 2021, now Pat. No. 11,444,629.

(60) Provisional application No. 63/055,891, filed on Jul. 23, 2020.

Publication Classification

(51) **Int. Cl.**

H03L 7/23	(2006.01)
G11C 29/02	(2006.01)
H03L 7/085	(2006.01)
H03L 7/187	(2006.01)

(52) **U.S. Cl.**

CPC ***H03L 7/235*** (2013.01); ***G11C 29/028*** (2013.01); ***H03L 7/085*** (2013.01); ***H03L 7/187*** (2013.01)

(57) **ABSTRACT**

A method and apparatus for performing on-system phase-locked loop (PLL) management in a memory device are provided. The method may include: utilizing a processing circuit within the memory controller to set multiple control parameters among multiple parameters stored in a register circuit of a transmission interface circuit within the memory controller, for controlling parameter adjustment of a PLL of the transmission interface circuit; utilizing a trimming control circuit to perform the parameter adjustment of the PLL according to the multiple control parameters, to adjust a set of voltage parameters among the multiple parameters, for optimizing a control voltage of a voltage controlled oscillator (VCO); and during the parameter adjustment of the PLL, utilizing the trimming control circuit to generate and store multiple processing results in the register circuit, for being sent back to the processing circuit, to complete the parameter adjustment of the PLL, thereby achieving the on-system PLL management.