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(19) **United States**(12) **Patent Application Publication**  
**TANAKA et al.**(10) **Pub. No.: US 2024/0215244 A1**(43) **Pub. Date: Jun. 27, 2024**(54) **MEMORY DEVICE CONTAINING  
CONSTRICTED CHANNEL ENDS AND  
METHODS OF MAKING THE SAME***H01L 25/065* (2006.01)*H01L 25/18* (2006.01)*H10B 41/27* (2006.01)*H10B 80/00* (2006.01)(71) Applicant: **SANDISK TECHNOLOGIES LLC,**  
ADDISON, TX (US)(52) **U.S. Cl.**CPC ..... *H10B 43/27* (2023.02); *H01L 24/08*(2013.01); *H01L 25/0657* (2013.01); *H01L**25/18* (2013.01); *H10B 41/27* (2023.02);*H10B 80/00* (2023.02); *H01L 2224/08145*(2013.01); *H01L 2924/1431* (2013.01); *H01L**2924/14511* (2013.01)(72) Inventors: **Hiroyuki TANAKA**, Yokkaichi (JP);  
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**ABSTRACT**(22) Filed: **Mar. 5, 2024****Related U.S. Application Data**(63) Continuation-in-part of application No. 17/931,362,  
filed on Sep. 12, 2022, which is a continuation-in-part  
of application No. 17/684,975, filed on Mar. 2, 2022.**Publication Classification**(51) **Int. Cl.***H10B 43/27* (2006.01)*H01L 23/00* (2006.01)

A memory die includes an alternating stack of insulating layers and electrically conductive layers, a dielectric spacer layer underlying the alternating stack, memory opening vertically extending through the alternating stack, and through the dielectric spacer layer, a memory opening fill structure located in the memory opening and including a dielectric core, a vertical semiconductor channel having a hollow portion which surrounds the dielectric core and a pillar portion which does not surround the dielectric core, and a memory film, and a source layer located under the dielectric spacer layer and contacting the pillar portion of the vertical semiconductor channel.

