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LIM et al.(10) **Pub. No.: US 2022/0385277 A1**(43) **Pub. Date: Dec. 1, 2022**(54) **INTEGRATED CIRCUIT INCLUDING
FLIP-FLOP AND COMPUTING SYSTEM FOR
DESIGNING THE INTEGRATED CIRCUIT****Publication Classification**(51) **Int. Cl.****H03K 3/037** (2006.01)**H03K 17/687** (2006.01)(52) **U.S. Cl.****CPC** **H03K 3/0372** (2013.01); **H03K 17/6872**
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ABSTRACT

An integrated circuit includes a flip-flop configured to operate in synchronization with a clock signal. The flip-flop includes a multiplexer configured to output an inverted signal of a scan input signal to a first node based on a scan enable signal, or the multiplexer configured to output an inverted signal of a data input signal or a signal having a first level to a first node based on a reset input signal, a master latch configured to latch the signal output through the first node, and to output the latched signal, and a slave latch configured to latch an output signal of the master latch and to output the latched output signal of the master latch.

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