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(54) **SEMICONDUCTOR DEVICE HAVING PLURAL MEMORY CELL MATS**

(71) Applicant: **MICRON TECHNOLOGY, INC.**, Boise, ID (US)

(72) Inventors: **Hirokazu Matsumoto**, Hachioji (JP); **Makoto Sato**, Sagamihara (JP); **Ryota Suzuki**, Sagamihara (JP); **Kyoka Egami**, Yokohama (JP)

(73) Assignee: **MICRON TECHNOLOGY, INC.**, Boise, ID (US)

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(57) **ABSTRACT**

Disclosed herein is an apparatus that includes: a memory cell array including a plurality of first memory cell mats arranged in a first direction; a first voltage line supplied with a first voltage, the first voltage line extending in the first direction and being connected to a plurality of first vias each arranged over a corresponding one of even numbered ones of the plurality of first memory cell mats; and a second voltage line supplied with a second voltage different from the first voltage, the second voltage line extending in the first direction and being connected to a plurality of second vias each arranged over a corresponding one of odd numbered ones of the plurality of first memory cell mats.