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(54) PRODUCING STRESS IN NANOSHEET TRANSISTOR CHANNELS

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(57)ABSTRACT

A semiconductor device includes a first stacked structure and a second stacked structure disposed on a substrate. The first stacked structure comprises a first plurality of gate structures alternately stacked with a first plurality of channel layers, and the second stacked structure comprises a second plurality of gate structures alternately stacked with a second plurality of channel layers. A first plurality of epitaxial source/drain regions are disposed on sides of the first stacked structure, and a second plurality of epitaxial source/ drain regions are disposed on sides of the second stacked structure. A first dielectric layer is disposed between the first stacked structure and the substrate, and between the first plurality of epitaxial source/drain regions and the substrate. A second dielectric layer is disposed between the second stacked structure and the substrate. At least a portion of the second plurality of epitaxial source/drain regions contact the substrate.

