



US 20240213770A1

(19) **United States**

(12) **Patent Application Publication**
TANAKA et al.

(10) **Pub. No.: US 2024/0213770 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **SEMICONDUCTOR INTEGRATED CIRCUIT
DEVICE**

(52) **U.S. Cl.**

CPC **H02H 9/046** (2013.01); **H01L 23/5228**
(2013.01)

(71) Applicant: **Socionext Inc.**, Kanagawa (JP)

(72) Inventors: **Hidetoshi TANAKA**, Yokohama-shi
(JP); **Yuko NAGAI**, Yokohama-shi (JP)

(57)

ABSTRACT

(21) Appl. No.: **18/596,231**

(22) Filed: **Mar. 5, 2024**

Related U.S. Application Data

(63) Continuation of application No. PCT/JP2021/033115,
filed on Sep. 9, 2021.

Publication Classification

(51) **Int. Cl.**

H02H 9/04 (2006.01)

H01L 23/522 (2006.01)

An IO cell includes an output circuit having an ESD protection diode, a protective resistance, and an output transistor. The protective resistance is constituted by a plurality of resistor elements formed in a first interconnect layer that is formed in an interconnect process (back end of line (BEOL)). The resistor elements are connected to interconnects formed in a second interconnect layer through vias. In the second interconnect layer, first power supply lines supplying first power are formed above the ESD protection diode. The first power supply lines have overlaps at positions in the X direction with the resistor elements.

