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(57) **ABSTRACT**

A method for generating a clock signal from an AC power supply signal includes receiving a reference signal at a first input of a comparator and receiving the AC power supply signal at a second input of the comparator. A clock signal is output by the comparator based on a comparison of the reference signal and the AC power supply signal, such that transitions of the clock signal take place while the reference signal is at a trigger voltage. Following each clock signal transition, the reference signal is changed from the trigger voltage to a hysteresis voltage that reduces a likelihood of the comparator outputting, immediately after each clock signal transition, a spurious transition of the clock signal due to noise on the AC power supply signal. The reference signal is then returned from the hysteresis voltage to the trigger voltage prior to return of the AC power supply signal to a level intended to cause a further clock signal transition at the output of the comparator.