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(54) **THREE-DIMENSIONAL NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME**

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(57) **ABSTRACT**

A semiconductor device includes decks stacked over a semiconductor layer in a vertical direction. Each deck includes alternating word line layers and insulating layers. A gate line structure (GLS) extends through the word line layers and the insulating layers of the decks. A channel structure extends through the word line layers and the insulating layers of the decks. A sidewall of the GLS is discontinuous at a border between two neighboring decks, and a sidewall of the channel structure is discontinuous at an interface between two neighboring decks. The GLS includes a first GLS that includes a gate line slit, a second GLS that includes sub-GLSs spaced apart from each other in a horizontal direction, or a combination thereof.