



US 20230232537A1

(19) **United States**(12) **Patent Application Publication**
HUANG et al.(10) **Pub. No.: US 2023/0232537 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **PACKAGED CIRCUIT STRUCTURE****Publication Classification**(71) Applicants: **Leading Interconnect Semiconductor Technology Qinhuangdao Co., Ltd.**, Qinhuangdao (CN); **Qi Ding Technology Qinhuangdao Co., Ltd.**, Qinhuangdao (CN); **Leading Interconnect Semiconductor Technology (ShenZhen) Co., Ltd.**, Shenzhen (CN)(51) **Int. Cl.**
H05K 1/18 (2006.01)
H05K 3/46 (2006.01)
H05K 3/28 (2006.01)
(52) **U.S. Cl.**
CPC **H05K 1/186** (2013.01); **H05K 3/4697** (2013.01); **H05K 3/284** (2013.01); **H05K 2203/308** (2013.01)(72) Inventors: **CHUN-CHIEH HUANG**, Tayuan (TW); **CHIN-MING LIU**, Tayuan (TW)(57) **ABSTRACT**(21) Appl. No.: **18/123,881**(22) Filed: **Mar. 20, 2023****Related U.S. Application Data**

(62) Division of application No. 17/218,556, filed on Mar. 31, 2021.

(30) **Foreign Application Priority Data**

Jan. 25, 2021 (CN) 202110097582.X

A package circuit structure includes a multilayer circuit board, an electronic component, and an insulating layer. The multilayer circuit board includes a metal portion and an opening. The opening is extending from a first side of the multilayer circuit board toward the second side of the multilayer circuit board facing the first side. A bottom of the opening is sealed by the metal portion. The electronic component is received in the opening and adhered to the metal portion. The electronic component is electrically connected to the multilayer circuit board and encapsulated in the opening by the insulating layer. A method for manufacturing the package circuit structure is also provided.

