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**IVANOV et al.**(10) **Pub. No.: US 2024/0223130 A1**(43) **Pub. Date: Jul. 4, 2024**(54) **VOLTAGE BUFFER**(52) **U.S. Cl.**CPC ..... **H03F 1/086** (2013.01); **H03F 3/505**  
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**PULIJALA**, Tucson, AZ (US)(21) Appl. No.: **18/090,756**(22) Filed: **Dec. 29, 2022****Publication Classification**(51) **Int. Cl.**  
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**H03F 3/50** (2006.01)(57) **ABSTRACT**

In an example, a circuit includes a first field-effect transistor (FET) having a gate and first and second terminals. The circuit includes a second FET having a gate and first and second terminals, the second terminals of the first and second FETs coupled together. The circuit includes a first boosted follower coupled to the gate of the first FET and includes a second boosted follower coupled to the gate of the second FET. A third FET is coupled to the first boosted follower and the second voltage terminal and configured to turn off the first boosted follower responsive to a first level of an output voltage. A fourth FET is coupled to the second boosted follower and the first voltage terminal and configured to turn off the second boosted follower responsive to a second level of the output voltage.

