US 20220376695A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0376695 A1**

CHU (43) **Pub. Date: Nov. 24, 2022**

(54) **PIPELINE ANALOG TO DIGITAL CONVERTER AND SIGNAL CONVERSION METHOD**

(71) Applicant: **REALTEK SEMICONDUCTOR CORPORATION**, HSINCHU (TW)

(72) Inventor: **JUNG-HSIN CHU**, HSINCHU (TW)

(21) Appl. No.: **17/703,396**

(22) Filed: **Mar. 24, 2022**

(30) **Foreign Application Priority Data**

May 24, 2021 (TW) 110118690

Publication Classification

(51) **Int. Cl.**
H03M 1/10 (2006.01)

(52) **U.S. Cl.**
CPC ***H03M 1/1009*** (2013.01)

(57) **ABSTRACT**

A pipeline analog to digital converter includes converter circuitries and a calibration circuitry. The converter circuitries sequentially convert an input signal into first digital codes. A first converter circuitry in the converter circuitries performs a quantization according to a first signal to generate a first corresponding digital code in the first digital codes, and the first signal is a signal, which is processed by the first converter circuitry, of the input signal and a previous stage residue signal. The calibration circuitry combines the first digital codes to output a second digital code, detects whether the quantization is completed to generate first and second valid signals, and determines whether to set the second digital code to be a first predetermined digital code or a second predetermined digital code according to the first and the second valid signals. The second valid signal is a delay signal of the first valid signal.