



US 20220377898A1

(19) **United States**(12) **Patent Application Publication**
FORTIN-BLANCHETTE et al.(10) **Pub. No.: US 2022/0377898 A1**(43) **Pub. Date: Nov. 24, 2022**(54) **PRINTED CIRCUIT BOARD COMPRISING A PLURALITY OF POWER TRANSISTOR SWITCHING CELLS IN PARALLEL**(71) Applicant: **IDÉNERGIE INC., MONTREAL (CA)**(72) Inventors: **HANDY FORTIN-BLANCHETTE, MONTREAL (CA); PIERRE BLANCHET, MONTREAL (CA)**(73) Assignee: **IDÉNERGIE INC., MONTREAL (CA)**(21) Appl. No.: **17/326,407**(22) Filed: **May 21, 2021****Publication Classification**(51) **Int. Cl.**
H05K 1/18 (2006.01)
H05K 1/11 (2006.01)
H05K 1/02 (2006.01)(52) **U.S. Cl.**CPC **H05K 1/181** (2013.01); **H05K 1/11** (2013.01); **H05K 1/0204** (2013.01); **H05K 2201/10166** (2013.01); **H05K 2201/066** (2013.01); **H05K 2201/10409** (2013.01)

(57)

ABSTRACT

A printed circuit board comprises N power switching cells operating in parallel and respectively comprising a transistor leg, at least one decoupling capacitor and a gate driver circuit. Each transistor leg comprises respective first and second transistors in series, a drain of the first transistor being connected to a positive DC line, a source of the second transistor being connected to a negative DC line, a source of the first transistor being connected to a drain of the second through a connection middle-point connected to an output terminal. Each gate driver circuit controls respective switching ON and OFF of the corresponding first and second transistors. The N transistor legs of the corresponding N power switching cells are positioned to substantially form a convex polygon having N edges of substantially the same length, each one of the N transistor legs being positioned along one of the edges of the convex polygon.

