

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0237219 A1 UMOH et al.

Jul. 11, 2024 (43) **Pub. Date:**

(54) STAGGERED FLIP PIN SMT CONNECTOR TO REDUCE CROSSTALK ON HIGH-SPEED **CHANNELS**

(71) Applicant: Intel Corporation, Santa Clara, CA (US)

(72) Inventors: Ifiok UMOH, San Jose, CA (US); Luz Karine SANDOVAL GRANADOS, Zapopan (MX); Alberto CARRILLO VAZQUEZ, Zapopan (MX); Quresh BOHRA, San Jose, CA (US); Diego Mauricio CORTES HERNANDEZ, Beaverton, OR (US)

(21) Appl. No.: 18/610,141

Mar. 19, 2024 (22)Filed:

Publication Classification

(51) Int. Cl. H05K 1/18 (2006.01)H01R 12/57 (2006.01)

(52) U.S. Cl. CPC H05K 1/181 (2013.01); H01R 12/57 (2013.01); H05K 2201/10189 (2013.01)

(57)ABSTRACT

Methods and apparatus for staggered flip pin SMT (surface mount technology) connectors to reduce crosstalk on highspeed channels. Contact feet on the board-side of a connector are flipped to increase the physical separation between contacts carrying transmit (TX) and contacts carrying receive (RX) signals. Meanwhile, for some embodiments the input receptacle side of the connectors are the same as that defined by standards such as SFF-8482, SFF-8630, SFF-8680 standards and the PCI-SIG, SFF-8639 Module Specification. This enables the connectors to work with existing devices employing these standards, such as NVMe drives. In one aspect, the connectors comprise modified versions of U.2 and U.3 connectors where selected board-side contacts (e.g., TX-, TX+, optional GND) and the mating contact pads used for SMT dual mount termination are staggered. In one aspect, the connector solutions are targeted for PCIe 5.0 and later NVMe implementations, noting the principles and techniques disclosed may apply to other high-speed chan-

