



US 20240213364A1

(19) **United States**

(12) **Patent Application Publication**

MIURA et al.

(10) **Pub. No.: US 2024/0213364 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE**

(71) Applicant: **NATIONAL INSTITUTE OF ADVANCED INDUSTRIAL SCIENCE AND TECHNOLOGY,**
Tokyo (JP)

(72) Inventors: **Yoshinao MIURA,** Tsukuba-shi (JP);
Akira NAKAJIMA, Tsukuba-shi (JP);
Xu-Qiang SHEN, Tsukuba-shi (JP);
Hirohisa HIRAI, Tsukuba-shi (JP);
Shinsuke HARADA, Tsukuba-shi (JP)

(21) Appl. No.: **18/556,293**

(22) PCT Filed: **Apr. 15, 2022**

(86) PCT No.: **PCT/JP2022/017898**
§ 371 (c)(1),
(2) Date: **Oct. 19, 2023**

(30) **Foreign Application Priority Data**
Apr. 22, 2021 (JP) 2021-072595

Publication Classification

(51) **Int. Cl.**
H01L 29/78 (2006.01)
H01L 21/265 (2006.01)
H01L 29/20 (2006.01)
H01L 29/861 (2006.01)

(52) **U.S. Cl.**
CPC **H01L 29/7811** (2013.01); **H01L 21/265**
(2013.01); **H01L 29/2003** (2013.01); **H01L**
29/7813 (2013.01); **H01L 29/8613** (2013.01)

(57) **ABSTRACT**

There is provided a semiconductor equipment including: an element area having an n-type layer, a first p-type layer on the n-type layer, and a second p-type layer on the first p-type layer, the second p-type layer having an acceptor concentration higher than the first p-type layer; and an electric field relaxation region surrounding the element area, in which in the electric field relaxation region, a region containing an impurity element that inactivates a part of acceptors in the first p-type layer and the second p-type layer is provided in the first p-type layer and the second p-type layer.

