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HWANG et al.(10) **Pub. No.: US 2022/0416790 A1**(43) **Pub. Date: Dec. 29, 2022**(54) **BUFFER CIRCUIT CAPABLE OF REDUCING NOISE**(30) **Foreign Application Priority Data**

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(57)

ABSTRACT

A buffer circuit includes a power control circuit, an inverting circuit, and a voltage adjustment circuit. The power control circuit is configured to provide voltages based on an input signal and a mode signal, and the inverting circuit is configured to receive and invert the voltages to generate an output signal. The voltage adjustment circuit is configured to adjust voltage levels based on the mode signal and the output signal.

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