US 20220393671A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0393671 A1**

LEE et al. (43) **Pub. Date: Dec. 8, 2022**

(54) **FLIP FLOP CIRCUIT**

(71) Applicant: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)

(72) Inventors: **YOUNG O LEE**, HWASEONG-SI (KR); **MIN SU KIM**, HWASEONG-SI (KR); **JEONG JIN LEE**, HWASEONG-SI (KR); **WON HYUN CHOI**, SEONGNAM-SI (KR)

(21) Appl. No.: **17/693,026**

(22) Filed: **Mar. 11, 2022**

(30) **Foreign Application Priority Data**

Jun. 8, 2021 (KR) 10-2021-0074061
Aug. 20, 2021 (KR) 10-2021-0110439

Publication Classification

(51) **Int. Cl.**
H03K 3/037 (2006.01)
H03K 3/017 (2006.01)
H03K 3/012 (2006.01)

(52) **U.S. Cl.**
CPC ***H03K 3/0375*** (2013.01); ***H03K 3/017*** (2013.01); ***H03K 3/012*** (2013.01)

(57) **ABSTRACT**

A pulse-based flip flop circuit includes; a pulse generator generating a pulse signal and an inverted pulse signal, a scan hold buffer holding a scan input signal for a delay time, and a latch circuit including an intermediate node receiving one of a data signal and the scan input signal in response to a scan enable signal, the pulse signal and the inverted pulse signal. The pulse generator circuit includes; a direct path providing a clock signal as a direct path input to a NAND circuit, a delay path including a number of stages configured to delay the clock signal and provide a delayed clock signal as a delay path input to NAND circuit, wherein the NAND circuit performs a NAND operation on the direct path input and the delay path input to generate the inverted pulse signal, and a feedback path providing the pulse signal to a first stage among the number of stages of the delay path.