US 20230232627A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2023/0232627 A1**

**LEE et al.** (43) **Pub. Date: Jul. 20, 2023**

(54) **SEMICONDUCTOR MEMORY DEVICE**

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(21) Appl. No.: **17/879,874**

(22) Filed: **Aug. 3, 2022**

(30) **Foreign Application Priority Data**

Jan. 17, 2022 (KR) ..... 10-2022-0006319

**Publication Classification**

(51) **Int. Cl.**
***H01L 27/11582*** (2006.01)
***H01L 27/11573*** (2006.01)

(52) **U.S. Cl.**
CPC .. ***H01L 27/11582*** (2013.01); ***H01L 27/11573*** (2013.01)

(57) **ABSTRACT**

A semiconductor memory device includes a first substrate defining a cell array region, a mold structure including a plurality of gate electrodes sequentially spaced and stacked on the first substrate in a step form, and a channel hole defined as penetrating the plurality of gate electrodes on the cell array region in a vertical direction perpendicular to an upper surface of the first substrate. The device includes an information storage layer along side walls and a bottom surface of the channel hole, the information storage layer including a blocking insulation layer along the side walls and the bottom surface of the channel hole, a charge storage layer on the blocking insulation layer, and a tunneling insulation layer. The device includes a channel layer on the information storage layer inside the channel hole, and an insulation pattern arranged to fill the channel hole on the channel layer.