



US 20240215261A1

(19) **United States**

(12) **Patent Application Publication**
Shen et al.

(10) **Pub. No.: US 2024/0215261 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **SEMICONDUCTOR PACKAGES**

Publication Classification

(71) Applicant: **Taiwan Semiconductor Manufacturing Company, Ltd.,**
Hsinchu (TW)

(51) **Int. Cl.**
H10B 61/00 (2006.01)
G11C 11/16 (2006.01)
H01L 23/522 (2006.01)
H01L 23/528 (2006.01)
H10N 50/01 (2006.01)
H10N 50/10 (2006.01)
H10N 50/80 (2006.01)

(72) Inventors: **Hsiang-Ku Shen**, Hsinchu City (TW);
Ku-Feng Lin, New Taipei City (TW);
Liang-Wei Wang, Hsinchu City (TW);
Dian-Hau Chen, Hsinchu (TW)

(52) **U.S. Cl.**
CPC **H10B 61/22** (2023.02); **G11C 11/161**
(2013.01); **H01L 23/5226** (2013.01); **H01L**
23/5283 (2013.01); **H10N 50/01** (2023.02);
H10N 50/10 (2023.02); **H10N 50/80** (2023.02)

(21) Appl. No.: **18/596,625**

(22) Filed: **Mar. 6, 2024**

Related U.S. Application Data

(63) Continuation of application No. 17/362,936, filed on
Jun. 29, 2021, now Pat. No. 11,950,432.

(60) Provisional application No. 63/156,943, filed on Mar.
5, 2021.

(57) **ABSTRACT**

A semiconductor package includes a first integrated circuit and a second integrated circuit. The first integrated circuit includes a first semiconductor substrate, a first bonding structure bonded to the second integrated circuit, a ferro-magnetic layer surrounding the first bonding structure, and a memory cell between the first semiconductor substrate and the first bonding structure.

