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(54) **MEMORY DEVICE, METHOD, LAYOUT, AND SYSTEM**

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(57) **ABSTRACT**

A memory macro includes an input/output (I/O) circuit positioned in a semiconductor wafer, a column of memory cells including first and second subsets of contiguous memory cells extending away from the I/O circuit in the semiconductor wafer, wherein the first subset is positioned between the I/O circuit and the second subset, a first bit line coupled to the I/O circuit and extending on one of a frontside or a backside of the semiconductor wafer along the first subset and terminating at the second subset, and a second bit line coupled to the I/O circuit and extending on the other of the frontside or the backside along the first and second subsets. Each memory cell of the first subset is electrically connected to the first bit line, and each memory cell of the second subset is electrically connected to the second bit line.