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(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0376659 A1**
YU et al. (43) **Pub. Date: Nov. 24, 2022**(54) **MODEL ARCHITECTURE SEARCH AND OPTIMIZATION FOR HARDWARE****Publication Classification**(71) Applicant: **Analog Devices, Inc.**, Wilmington, MA (US)(51) **Int. Cl.****H03F 1/32** (2006.01)**G06K 9/62** (2006.01)**G06N 3/08** (2006.01)(72) Inventors: **Tao YU**, Somerville, MA (US);
Cristobal ALESSANDRI, Boston, MA (US); **Frank YAUL**, Somerville, MA (US); **Wenjie LU**, Arlington, MA (US); **Shyam Chandrasekhar NAMBIAR**, Boston, MA (US)(52) **U.S. Cl.**CPC **H03F 1/3247** (2013.01); **G06K 9/6267** (2013.01); **G06N 3/08** (2013.01); **H03F 1/3211** (2013.01)(73) Assignee: **Analog Devices, Inc.**, Wilmington, MA (US)(21) Appl. No.: **17/732,715**(22) Filed: **Apr. 29, 2022****Related U.S. Application Data**

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(57)

ABSTRACT

Systems, devices, and methods related to using model architecture search for hardware configuration are provided. An example apparatus includes an input node to receive an input signal; a pool of processing units to perform one or more arithmetic operations and one or more signal selection operations, wherein each of the processing units in the pool is associated with at least one parameterized model corresponding to a data transformation operation; and a control block to configure, based on a first parameterized model, a first subset of the processing units in the pool, where the first subset of the processing units processes the input signal to generate a first signal.

