

## (19) United States

# (12) Patent Application Publication (10) Pub. No.: US 2024/0251561 A1

#### Jul. 25, 2024 (43) **Pub. Date:**

#### (54) **SEMICONDUCTOR MEMORY**

(71) Applicant: Kioxia Corporation, Tokyo (JP)

(72) Inventors: Tomoo HISHIDA, Kamakura Kanagawa (JP); Sadatoshi

MURAKAMI, Yokohama Kanagawa (JP); Ryota KATSUMATA, Yokkaichi Mie (JP); Masao IWASE, Yokkaichi

Mie (JP)

(21) Appl. No.: 18/440,623

(22) Filed: Feb. 13, 2024

### Related U.S. Application Data

(63) Continuation of application No. 17/991,694, filed on Nov. 21, 2022, now Pat. No. 11,974,439, which is a continuation of application No. 17/214,710, filed on Mar. 26, 2021, now Pat. No. 11,552,095, which is a continuation of application No. 16/815,852, filed on Mar. 11, 2020, now Pat. No. 10,971,511, which is a continuation of application No. 16/262,827, filed on Jan. 30, 2019, now Pat. No. 10,622,372, which is a continuation of application No. 16/104,843, filed on Aug. 17, 2018, now Pat. No. 10,199,387, which is a continuation of application No. 15/708,033, filed on Sep. 18, 2017, now Pat. No. 10,056,403, which is a continuation of application No. 15/349,907, filed on Nov. 11, 2016, now Pat. No. 9,768,188, which is a continuation of application No. 14/475,440, filed on Sep. 2, 2014, now Pat. No. 9,502,299.

#### (30)Foreign Application Priority Data

Mar. 13, 2014 (JP) ...... 2014-050568

#### **Publication Classification**

(51) Int. Cl. H10B 43/35 (2006.01)H01L 21/8234 (2006.01)(2006.01)H10B 43/27 H10B 43/50 (2006.01)

(52) U.S. Cl. CPC ..... H10B 43/35 (2023.02); H01L 21/823437 (2013.01); H10B 43/27 (2023.02); H10B 43/50 (2023.02)

#### (57)**ABSTRACT**

A semiconductor memory includes a memory cell region that includes multiple memory cells stacked above a semiconductor substrate, first and second dummy regions on opposite sides of the memory cell region, each dummy region including multiple dummy cells stacked above the semiconductor substrate, and a wiring that electrically connects dummy cells of the first and second dummy regions that are at a same level above the semiconductor substrate.

