US 20230230942A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2023/0230942 A1**

Duan et al. (43) **Pub. Date: Jul. 20, 2023**

(54) **CHANNELIZED FILTER USING SEMICONDUCTOR FABRICATION**

(71) Applicant: **Northrop Grumman Systems Corporation**, Falls Church, VA (US)

(72) Inventors: **Dah-Weih Duan**, Redondo Beach, CA (US); **Elizabeth T. Kunkee**, Redondo Beach, CA (US); **Stephane Larouche**, Redondo Beach, CA (US)

(21) Appl. No.: **18/123,467**

(22) Filed: **Mar. 20, 2023**

Related U.S. Application Data

(63) Continuation of application No. 17/745,265, filed on May 16, 2022, now Pat. No. 11,658,136, which is a continuation of application No. 16/916,644, filed on Jul. 17, 2020, now Pat. No. 11,373,965.

Publication Classification

(51) **Int. Cl.**
H01L 23/66 (2006.01)
H01P 1/203 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 23/66*** (2013.01); ***H01P 1/20327*** (2013.01); *H01L 2223/6627* (2013.01); *H01L 2223/6655* (2013.01)

(57) **ABSTRACT**

A semiconductor technology implemented high-frequency channelized filter includes a dielectric substrate with metal traces disposed on one of two major surfaces of the substrate. An input and output port disposed on the substrate and one of the metal traces carrying a high-frequency signal to be filtered between the input and output port. Other of the metal traces are connected to the one metal trace at intervals along the length of the one metal trace each providing a reactance to the high-frequency signal where the reactance varies with frequency and additional traces of the metal traces serving as a reference ground for the one metal trace and the other metal traces. A silicon enclosure mounted to the substrate with a first planar surface with cavities in the enclosure that extend through the first surface, and internal walls within the silicon enclosure defining the cavities. A layer of conductive metal covers the first planar surface, cavities and the internal walls. The silicon enclosure having substantially continuous areas of metal on the first planar surface about the periphery of the silicon enclosure that engage corresponding areas of the additional traces about the periphery of the substrate. The cavities surround the respective other metal traces with the internal cavity walls engaging the additional traces adjacent the respective other metal traces to individually surround each of the other metal traces with a conductive metal thereby providing electromagnetic field isolation between each of the other metal traces.