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(54) **ALL-DIGITAL PHASE-LOCKED LOOP AND CALIBRATION METHOD THEREOF**

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(57) **ABSTRACT**

An all-digital phase-locked loop (ADPLL) and a calibration method thereof are provided. The ADPLL includes a digitally controlled oscillator (DCO), a time-to-digital converter (TDC) coupled to the DCO, and a normalization circuit coupled to the TDC. The DCO is configured to generate a clock signal according to a frequency control signal. The TDC is configured to generate a digital output signal according to a phase error between the clock signal and a reference signal. The normalization circuit is configured to convert the digital output signal into a clock phase value according to a gain parameter. More particularly, the normalization circuit may modify the gain parameter according to a phase error value between the clock phase value and a reference phase value.