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Lichtenwalner et al.(10) **Pub. No.: US 2023/0231047 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **POWER SEMICONDUCTOR DEVICES
INCLUDING A TRENCHED GATE AND
METHODS OF FORMING SUCH DEVICES****Publication Classification**

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McPherson, Plano, TX (US)(21) Appl. No.: **18/125,779**(22) Filed: **Mar. 24, 2023****Related U.S. Application Data**(63) Continuation of application No. 17/080,956, filed on
Oct. 27, 2020, now Pat. No. 11,640,990.**ABSTRACT**

Semiconductor devices and methods of forming the devices are provided. Semiconductor devices include a semiconductor layer structure comprising a trench in an upper surface thereof, a dielectric layer in a lower portion of the trench, and a gate electrode in the trench and on the dielectric layer opposite the semiconductor layer structure. The trench may include rounded upper corner and a rounded lower corner. A center portion of a top surface of the dielectric layer may be curved, and the dielectric layer may be on opposed sidewalls of the trench. The dielectric layer may include a bottom dielectric layer on a bottom surface of the trench and on lower portions of the sidewalls of the trench and a gate dielectric layer on upper portions of the sidewalls of the trench and on the bottom dielectric layer.

