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(19) **United States**(12) **Patent Application Publication**  
Sills et al.(10) **Pub. No.: US 2024/0244820 A1**(43) **Pub. Date: Jul. 18, 2024**(54) **MICROELECTRONIC DEVICES, AND  
RELATED MEMORY DEVICES, AND  
ELECTRONIC SYSTEMS**(52) **U.S. Cl.**CPC ..... **H10B 12/30** (2023.02)(71) Applicant: **Micron Technology, Inc.**, Boise, ID  
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**ABSTRACT**(72) Inventors: **Scott E. Sills**, Boise, ID (US); **Si-Woo  
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**Hiroki Fujisawa**, Tokyo (JP)(21) Appl. No.: **18/391,522**(22) Filed: **Dec. 20, 2023****Related U.S. Application Data**(60) Provisional application No. 63/479,894, filed on Jan.  
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A microelectronic device includes memory array regions of memory cells each including a vertical stack structure comprising conductive structures vertically spaced from one another and horizontally extending through a vertical stack of memory cells. A staircase region is horizontally between two of the memory array regions horizontally neighboring one another and includes a first staircase structure horizontally extending from the vertical stack structure of a first of the two of the memory array regions and a second staircase structure horizontally extending from the vertical stack structure of a second of the two of the memory array regions. Lateral conductive contacts provide a conductive path between the first steps of the first staircase structure and the second steps of the second staircase structure. Related microelectronic devices, memory devices, and electronic systems are also described.

