US 20240213192A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0213192 A1**

Cho (43) **Pub. Date: Jun. 27, 2024**

(54) **SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING THE SEMICONDUCTOR PACKAGE**

(71) Applicant: **Samsung Electronics Co., Ltd.**, Suwon-si (KR)

(72) Inventor: **Kyongsoon Cho**, Suwon-si (KR)

(21) Appl. No.: **18/358,478**

(22) Filed: **Jul. 25, 2023**

(30) **Foreign Application Priority Data**

Dec. 27, 2022 (KR) 10-2022-0185238

Publication Classification

(51) **Int. Cl.**

H01L 23/00	(2006.01)
H01L 23/48	(2006.01)
H01L 27/146	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 24/05*** (2013.01); ***H01L 23/481*** (2013.01); ***H01L 24/13*** (2013.01); ***H01L 24/32*** (2013.01); ***H01L 27/14618*** (2013.01); *H01L 2224/02372* (2013.01); *H01L 2224/05548* (2013.01); *H01L 2224/13025* (2013.01); *H01L 2224/32245* (2013.01); *H01L 2924/13091* (2013.01)

(57) **ABSTRACT**

A semiconductor package includes a silicon substrate including a plurality of through openings, and a redistribution wiring layer including a first surface and a second surface opposite the first surface, the second surface facing the silicon substrate, the redistribution wiring layer including a first pad area and a second pad area. The redistribution wiring layer includes a plurality of bonding pads on the first pad area at the first surface, a plurality of test pads on the second pad area at the first surface, a plurality of landing pads on the second pad area at the second surface, the plurality of landing pads in communication with the plurality of through openings, respectively, and a plurality of redistribution wires electrically connected to the plurality of bonding pads and the plurality of landing pads.