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(19) **United States**(12) **Patent Application Publication**
Hopkins et al.(10) **Pub. No.: US 2024/0244840 A1**(43) **Pub. Date: Jul. 18, 2024**(54) **MEMORY ARRAY AND METHOD USED IN FORMING A MEMORY ARRAY COMPRISING STRINGS OF MEMORY CELLS***H01L 21/3213* (2006.01)*H01L 21/3215* (2006.01)*H10B 41/10* (2023.01)*H10B 41/27* (2023.01)*H10B 43/27* (2023.01)(71) Applicant: **Micron Technology, Inc.**, Boise, ID (US)(52) **U.S. Cl.**CPC *H10B 43/10* (2023.02); *H01L 21/31111* (2013.01); *H01L 21/31155* (2013.01); *H01L**21/32134* (2013.01); *H01L 21/32155*(2013.01); *H10B 41/10* (2023.02); *H10B**41/27* (2023.02); *H10B 43/27* (2023.02)(72) Inventors: **John D. Hopkins**, Meridian, ID (US);
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(57)

ABSTRACT

A memory array comprises laterally-spaced memory blocks individually comprising a vertical stack comprising alternating insulative tiers and conductive tiers. Channel-material strings of memory cells extend through the insulative tiers and the conductive tiers. Intervening material is laterally-between and longitudinally-along immediately-laterally-adjacent of the memory blocks. The intervening material in a lowest of the conductive tiers comprises intervenor material. Bridges extend laterally-between the immediately-laterally-adjacent memory blocks. The bridges comprise bridging material that is of different composition from that of the intervenor material. The bridges are longitudinally-spaced-along the immediately-laterally-adjacent memory blocks by the intervenor material and extend laterally into the immediately-laterally-adjacent memory blocks. Other embodiments, including method, are disclosed.

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