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(54) **ARCHITECTURE FOR ANALOG MULTIPLIER-ACCUMULATOR WITH BINARY WEIGHTED CHARGE TRANSFER CAPACITORS**

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(57) **ABSTRACT**

An architecture for a multiplier-accumulator (MAC) uses a common Unit Element (UE) for each aspect of operation, the MAC formed as a plurality of MAC UEs, a plurality of Bias UEs, and a plurality of Analog to Digital Conversion (ADC) UEs which collectively perform a scalable MAC operation and generate a binary result. Each MAC UE, BIAS UE and ADC UE comprises groups of NAND gates with complementary outputs arranged in NAND-groups, each NAND gate coupled to a differential charge transfer bus through a binary weighted charge transfer capacitor to form an analog multiplication product as a charge applied to the differential charge transfer bus. The analog charge transfer bus is coupled to groups of ADC UEs with an ADC controller which enables and disables the ADC UEs using successive approximation to determine the accumulated multiplication result.