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(54) **A DUTY-CYCLE CORRECTOR CIRCUIT**

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(57) **ABSTRACT**

A duty-cycle corrector circuit produces a clock signal with a given duty cycle (e.g., fifty percent) or with a substantially given duty cycle. The DC corrector circuit includes a delay-locked loop (DLL) circuit and a duty-cycle correction (DCC) circuit. The DLL circuit is operable to adjust a delay between local clock signals until the phase difference between the local clock signals equals or is substantially equal to zero. The DCC circuit is operable to adjust the duty cycles of the local clock signals until the duty-cycle error equals or is substantially equal to zero. The duty-cycle error equals or substantially equals zero when the duty cycles of the local clock signals equal or are substantially equal to fifty percent.