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(54) **GALLIUM NITRIDE SUPERJUNCTION TRANSISTOR**

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(57) **ABSTRACT**

Techniques to increase the number of current paths (or "channels") in a GaN transistor, without increasing the device area, thereby decreasing the on-resistance. In addition, this disclosure describes techniques to utilize back-side field management to improve the device's performance. For example, the techniques can include using p-type implantation into the substrate, e.g., silicon carbide (SiC), as a field management tool to form a superjunction device, thereby increasing the effective field and reducing the on-resistance multiplied by the output charge (Qoss).