



US 20220399898A1

(19) **United States**(12) **Patent Application Publication**
ZHOU(10) **Pub. No.: US 2022/0399898 A1**(43) **Pub. Date: Dec. 15, 2022**(54) **SUCCESSIVE APPROXIMATION REGISTER
ANALOG TO DIGITAL CONVERTER AND
SIGNAL CONVERSION METHOD**(52) **U.S. Cl.**CPC **H03M 1/466** (2013.01); **H03M 1/1245**
(2013.01)(71) Applicant: **REALTEK SEMICONDUCTOR
CORPORATION**, Hsinichu (TW)(72) Inventor: **XIAO-BO ZHOU**, Suzhou (CN)(21) Appl. No.: **17/696,446**(22) Filed: **Mar. 16, 2022**(30) **Foreign Application Priority Data**

Jun. 11, 2021 (CN) 202110654962.9

Publication Classification(51) **Int. Cl.****H03M 1/46** (2006.01)**H03M 1/12** (2006.01)

(57)

ABSTRACT

A successive approximation register analog to digital converter includes a sampling circuitry, a comparator circuit, and a controller circuitry. The sampling circuitry generates first and second signals according to a sampled signal. The comparator circuit compares the first signal with the second signal to generate first decision signals. The controller circuitry generates digital codes according to the first decision signals, and controls the comparator circuit to perform comparisons repeatedly to generate second decision signals, in order to generate a digital output according to the digital codes, a statistical noise value, and the second decision signals. The controller circuitry further controls the sampling circuitry and the comparator circuit to perform comparisons repeatedly according to the sampled signal having an initial level during an initial phase, in order to generate third decision signals, and performs a statistical calculation to obtain the statistical noise value according to the third decision signals.

