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TADA et al.(54) **PRINTED CIRCUIT BOARD**(57) **ABSTRACT**(71) Applicant: **Itabashi Seiki Co., Ltd.**, Tokyo (JP)(72) Inventors: **Tetsuya TADA**, Tokyo (JP); **Kenji KUHARA**, Tokyo (JP); **Takeshi MIMURO**, Toyo (JP)(21) Appl. No.: **17/619,892**(22) PCT Filed: **Aug. 11, 2020**(86) PCT No.: **PCT/JP2020/030633**

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[Object] Provided is a printed circuit board ensuring a degree of freedom in circuit design and unlikely to cause a circuit connection failure.

[Solving Means] A middle interlayer circuit 11, an upper surface side interlayer circuit 12, and a lower surface side interlayer circuit 13 are formed from a connection surface-less integral conductor. In addition, a connection surface 33 between the upper surface side interlayer circuit 12 and an upper surface side surface layer circuit 14 and a connection surface 34 between the lower surface side interlayer circuit 13 and a lower surface side surface layer circuit 15 lack a connection surface in a plate thickness direction, and thus a satisfactory connection state is achieved. Accordingly, a first circuit 10 is unlikely to cause a connection failure. In addition, the upper surface side interlayer circuit 12 and the lower surface side interlayer circuit 13 can be disposed at misaligned positions in the plane direction of the printed circuit board, and thus the degree of freedom in circuit design increases. Plane circuits 24 and 16 not connected to the first circuit can be disposed with insulating layers 31 and 32 sandwiched below the upper surface side interlayer circuit 12 or above the lower surface side interlayer circuit 13.

