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(54) **SAMPLING FRACTIONAL-N  
PHASE-LOCKED LOOP WITH FEEDBACK  
SPUR COMPENSATION**

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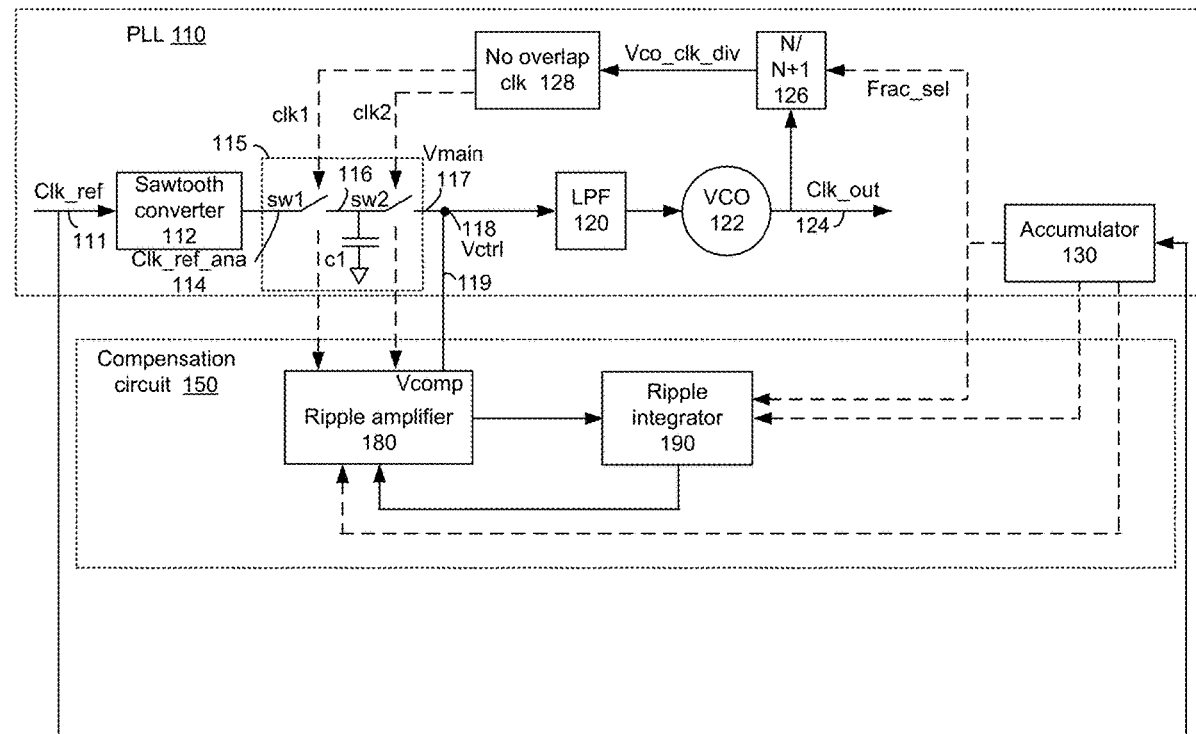
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(57) **ABSTRACT**

Embodiments herein relate to a sampling phase-locked loop (PLL) with a compensation circuit for reducing ripples due to the use of a fractional N divider. The compensation circuit includes a ripple amplifier and a ripple divider. The ripple amplifier receives an output voltage, Vmain, of a main sampling circuit of the PLL and amplifies its alternating current (AC) components. The amplified output voltage is provided to a ripple integrator which samples the minimum and maximum values to provide inputs to an operational amplifier (op amp). An output of the op amp is fed back to a digital-to-analog converter (DAC), which provides a corresponding compensation voltage, Vcomp. Vcomp is added to Vmain to provide a final output control voltage, Vctrl, to control a voltage-controlled oscillator (VCO) of the PLL.



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