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(54) **IEC PROTECTION OF HIGH-FREQUENCY TERMINALS**

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(57) **ABSTRACT**

An ESD trigger circuit is provided for protecting a pass transistor coupled to an integrated circuit terminal. The integrated circuit terminal couples through a diode to a voltage node. In response to an electrostatic shock at the integrated circuit terminal, the diode conducts charge to the voltage node to pulse a voltage of the voltage node. The ESD trigger circuit responds to the pulse of the voltage by coupling the voltage node to a gate of the pass transistor.