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(54) **THREE-DIMENSIONAL NAND MEMORY DEVICE AND METHOD OF FORMING THE SAME**

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(57) **ABSTRACT**

A semiconductor device includes N number of decks. Each deck includes alternating word line layers and insulating layers. Each deck includes two first gate line slit (GLS) structures and a second GLS structure positioned between the two first GLS structures. The two first GLS structures and the second GLS structures each extend in an X-Z plane and cut through the word line layers and the insulating layers of the respective deck. At least one second GLS structure of at least one deck in the N umber of decks includes multiple sub-GLS structures. The multiple sub-GLS structures are separate from each other.