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(19) **United States**(12) **Patent Application Publication****Gardner et al.**(10) **Pub. No.: US 2023/0231057 A1**(43) **Pub. Date:****Jul. 20, 2023**(54) **2D MATERIALS WITH INVERTED GATE ELECTRODE FOR HIGH DENSITY 3D STACKING**(71) Applicant: **Tokyo Electron Limited**, Tokyo (JP)(72) Inventors: **Mark I. Gardner**, Albany, NY (US);
H. Jim Fulford, Albany, NY (US)(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)(21) Appl. No.: **17/578,397**(22) Filed: **Jan. 18, 2022****Publication Classification**(51) **Int. Cl.****H01L 29/792** (2006.01)**H01L 27/12** (2006.01)**H01L 21/8234** (2006.01)**H01L 27/11582** (2017.01)(52) **U.S. Cl.**CPC **H01L 29/7926** (2013.01); **H01L 27/1225**(2013.01); **H01L 21/823431** (2013.01); **H01L****27/11582** (2013.01)

(57)

ABSTRACT

A semiconductor device may include a first dielectric layer, a first gate electrode, a first gate dielectric layer, a first source electrode, a first drain electrode, and a first two-dimensional (2D) semiconductor layer. The first dielectric layer may have a first top surface. The first gate electrode may extend from the first top surface into the first dielectric layer. The first gate dielectric layer may be disposed on the first gate electrode and have a second top surface. The first source electrode may extend from the second top surface, through the first gate dielectric layer and into the first dielectric layer. The first drain electrode may extend from the second top surface, through the first gate dielectric layer and into the first dielectric layer. The first 2D semiconductor layer may be disposed on the first gate dielectric layer.

