



(12) **Patent Application Publication**  
**CHEN et al.**

(43) **Pub. Date:** **Jul. 20, 2023**

(52) U.S. Cl.

CPC ..... ***H01L 24/24*** (2013.01); ***H01L 24/16***  
(2013.01); ***H01L 24/73*** (2013.01); ***H01L***  
***2924/35121*** (2013.01); ***H01L 2224/2402***  
(2013.01); ***H01L 2224/2405*** (2013.01); ***H01L***  
***2224/24226*** (2013.01); ***H01L 2224/16058***  
(2013.01); ***H01L 2224/16059*** (2013.01); ***H01L***  
***2224/16227*** (2013.01); ***H01L 2224/16238***  
(2013.01); ***H01L 2224/73209*** (2013.01)

(22) Filed: **Jan. 12, 2023**

### Related U.S. Application Data

(60) Provisional application No. 63/301,438, filed on Jan. 20, 2022.

## Publication Classification

(51) **Int. Cl.**  
**H01L 23/00** (2006.01)

(57) **ABSTRACT**

A semiconductor package includes a die and a first lamination layer on the die with openings through the first lamination layer. A redistribution layer is on the first lamination layer and extends through the openings to the die. A plurality of conductive extensions are on the redistribution layer with each stud including a first surface on the redistribution layer, a second surface opposite to the first surface, and a sidewall between the first surface and the second surface. A second lamination layer is on the redistribution layer and the first lamination layer with the die encapsulated in molding compound. The second lamination layer is removed around the conductive extensions to expose the second surface and at least a portion of the sidewall of each stud to improve solder bond strength when mounting the package to a circuit board.

