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(54) **METHOD FOR MANUFACTURING A MEMORY DEVICE AND MEMORY DEVICE MANUFACTURED THROUGH THE SAME METHOD**

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(57) **ABSTRACT**

A method for manufacturing a 3D vertical array of memory cells is disclosed. The method comprises: forming on a substrate a stack of dielectric material layers comprising first and second dielectric material layers alternated to each other; forming holes through the stack of dielectric material layers, said holes exposing the substrate; selectively removing the second material layers through said holes to form cavities between adjacent first dielectric material layers; filling said cavities with a conductive material through said holes to form corresponding conductive material layers; forming first memory cell access lines from said conductive material layers; carrying out a conformal deposition of a chalcogenide material through said holes; forming memory cell storage elements from said deposed chalcogenide material; filling said holes with conductive material to form corresponding second memory cell access lines.