



US 20240237350A1

(19) **United States**

(12) **Patent Application Publication**
SONDHI et al.

(10) **Pub. No.: US 2024/0237350 A1**

(43) **Pub. Date: Jul. 11, 2024**

(54) **THREE-DIMENSIONAL MEMORY DEVICE
AND METHOD OF MAKING THEREOF
INCLUDING NON-CONFORMAL
SELECTIVE DEPOSITION OF SPACERS IN
MEMORY OPENINGS**

(60) Provisional application No. 63/479,455, filed on Jan. 11, 2023.

Publication Classification

(51) **Int. Cl.**
H10B 43/27 (2006.01)
H10B 41/27 (2006.01)
(52) **U.S. Cl.**
CPC *H10B 43/27* (2023.02); *H10B 41/27* (2023.02)

(71) Applicant: **SANDISK TECHNOLOGIES LLC,**
ADDISON, TX (US)

(72) Inventors: **Kartik SONDHI,** Milpitas, CA (US);
Roshan Jayakhar TIRUKKONDA,
Milpitas, CA (US); **Bing ZHOU,** San
Jose, CA (US); **Senaka**
KANAKAMEDALA, San Jose, CA
(US)

(21) Appl. No.: **18/534,283**

(22) Filed: **Dec. 8, 2023**

Related U.S. Application Data

(63) Continuation-in-part of application No. 18/355,888,
filed on Jul. 20, 2023.

(57) **ABSTRACT**

A memory device includes an alternating stack of insulating layers and electrically conductive layers located over a substrate, a memory opening vertically extending through the alternating stack, a memory opening fill structure located in the memory opening and including a vertical stack of memory elements and a vertical semiconductor channel, and a vertical stack of insulating spacers located at levels of the insulating layers between the memory opening fill structure and the insulating layers. The insulating spacers have different thicknesses such that the thicknesses of the insulating spacers increase with an upward vertical distance from a horizontal plane including a top surface of the substrate.

