



US 20220385304A1

(19) **United States**(12) **Patent Application Publication**
Miki(10) **Pub. No.: US 2022/0385304 A1**(43) **Pub. Date: Dec. 1, 2022**(54) **STORAGE DEVICE AND CONTROL
METHOD FOR STORAGE DEVICE****Publication Classification**(51) **Int. Cl.****H03M 13/09** (2006.01)**H03M 13/15** (2006.01)(52) **U.S. Cl.****CPC** **H03M 13/098** (2013.01); **H03M 13/1515**
(2013.01); **H03M 13/152** (2013.01); **H03M**
13/095 (2013.01)(71) Applicant: **FUJITSU LIMITED**, Kawasaki-shi
(JP)(72) Inventor: **Atsushi Miki**, Yokohama (JP)(73) Assignee: **FUJITSU LIMITED**, Kawasaki-shi
(JP)(21) Appl. No.: **17/577,422**(22) Filed: **Jan. 18, 2022**(30) **Foreign Application Priority Data**

May 26, 2021 (JP) 2021-088729

(57)

ABSTRACT

A storage device includes: a memory; and a processor configured to, at the time of writing data into the memory, generate a first check code common to a plurality of types of error correction codes from the data on the basis of a correlation relationship between the plurality of types of error correction codes, add the first check code to the data and write the data into the memory, convert the first check code into a second check code based on any one of the plurality of types of error correction codes at the time of reading the data from the memory, and perform error correction by using the second check code.

