

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0179915 A1 Or-Bach et al.

May 30, 2024 (43) **Pub. Date:**

(54) 3D SEMICONDUCTOR DEVICE AND STRUCTURE WITH LOGIC AND MEMORY

- (71) Applicant: Monolithic 3D Inc., Klamath Falls, OR
- Inventors: Zvi Or-Bach, Haifa (IL); Jin-Woo Han, San Jose, CA (US)
- Assignee: Monolithic 3D Inc., Klamath Falls, OR
- (21)Appl. No.: 18/515,255
- (22) Filed: Nov. 21, 2023

Related U.S. Application Data

- (63) Continuation-in-part of application No. 17/665,560, filed on Feb. 6, 2022, which is a continuation-in-part of application No. 17/524,737, filed on Nov. 11, 2021, now Pat. No. 11,296,115, which is a continuation-inpart of application No. 17/396,711, filed on Aug. 8, 2021, now Pat. No. 11,233,069, which is a continuation-in-part of application No. 17/063,397, filed on Oct. 5, 2020, now Pat. No. 11,114,464, which is a continuation-in-part of application No. 16/526,763, filed on Jul. 30, 2019, now Pat. No. 10,847,540, which is a continuation-in-part of application No. 15/990,611, filed on May 26, 2018, now Pat. No. 10,418,369, which is a continuation of application No. 15/333,138, filed on Oct. 24, 2016, now Pat. No. 10,014,318.
- (60) Provisional application No. 62/307,568, filed on Mar. 14, 2016, provisional application No. 62/286,362, filed on Jan. 23, 2016, provisional application No. 62/276,953, filed on Jan. 10, 2016, provisional application No. 62/271,251, filed on Dec. 27, 2015, provisional application No. 62/266,610, filed on Dec. 12, 2015, provisional application No. 62/246,054, filed on Oct. 24, 2015.

Publication Classification

(51)	Int. Cl.	
	H10B 43/27	(2006.01)
	H01L 23/528	(2006.01)
	H01L 27/02	(2006.01)
	H01L 29/167	(2006.01)
	H01L 29/47	(2006.01)
	H01L 29/78	(2006.01)
	H01L 29/792	(2006.01)
	H10B 41/10	(2006.01)
	H10B 41/20	(2006.01)
	H10B 43/10	(2006.01)
	H10B 43/20	(2006.01)
	H10B 53/20	(2006.01)

(52) U.S. Cl.

CPC H10B 43/27 (2023.02); H01L 23/5283 (2013.01); H01L 27/0207 (2013.01); H01L 29/167 (2013.01); H01L 29/47 (2013.01); H01L 29/7827 (2013.01); H01L 29/792 (2013.01); H10B 43/10 (2023.02); H10B 43/20 (2023.02); H10B 41/10 (2023.02); H10B 41/20 (2023.02); H10B 53/20 (2023.02)

ABSTRACT

A 3D semiconductor device including: a first level including a single crystal layer, a memory control circuit which includes a plurality of first transistors; a first metal layer overlaying the single crystal layer; a second metal layer overlaying the first metal layer; a third metal layer overlaying the second metal layer; second transistors which include a metal gate are disposed atop the third metal layer; third transistors disposed atop the second transistors; a fourth metal layer disposed atop the third transistors; and a memory array including word-lines, the memory array includes at least four memory mini arrays, each including at least four rows by at least four columns of memory cells, where each of the memory cells includes at least one of the second transistors or at least one of the third transistors, the memory control circuit includes at least one digital to analog converter circuit.

