



US 20240213088A1

(19) **United States**

(12) **Patent Application Publication**
REN et al.

(10) **Pub. No.: US 2024/0213088 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **SUBTRACTIVE METALS AND
SUBTRACTIVE METAL SEMICONDUCTOR
STRUCTURES**

Publication Classification

(51) **Int. Cl.**
H01L 21/768 (2006.01)

(52) **U.S. Cl.**
CPC .. H01L 21/76843 (2013.01); **H01L 21/76879**
(2013.01)

(71) Applicant: **Applied Materials, Inc.**, Santa Clara,
CA (US)

(72) Inventors: **He REN**, San Jose, CA (US); **Hao
JIANG**, San Jose, CA (US); **Shi YOU**,
San Jose, CA (US); **Mehul B. NAIK**,
San Jose, CA (US)

(57) **ABSTRACT**

Embodiments of the present disclosure generally relate to subtractive metals, subtractive metal semiconductor structures, subtractive metal interconnects, and to processes for forming such semiconductor structures and interconnects. In an embodiment, a process for fabricating a semiconductor structure is provided. The process includes performing a degas operation on the semiconductor structure and depositing a liner layer on the semiconductor structure. The process further includes performing a sputter operation on the semiconductor structure, and depositing, by physical vapor deposition, a metal layer on the liner layer, wherein the liner layer comprises Ti, Ta, TaN, or combinations thereof, and a resistivity of the metal layer is about 30 $\mu\Omega\cdot\text{cm}$ or less.

(21) Appl. No.: **18/595,951**

(22) Filed: **Mar. 5, 2024**

Related U.S. Application Data

(62) Division of application No. 17/193,994, filed on Mar. 5, 2021, now Pat. No. 11,923,244.

305

