



US 20240178833A1

(19) **United States**(12) **Patent Application Publication**  
**STANZIONE**(10) **Pub. No.: US 2024/0178833 A1**(43) **Pub. Date: May 30, 2024**(54) **POWER-ON RESET CIRCUITRY, AN  
IMPLANT DEVICE AND A METHOD FOR  
GENERATING A POWER-ON RESET  
SIGNAL**(52) **U.S. Cl.**CPC ..... *H03K 17/223* (2013.01); *A61N 1/3787*  
(2013.01); *H03K 19/20* (2013.01); *H02J 50/00*  
(2016.02)(71) Applicant: **Stichting IMEC Nederland**, Eindhoven  
(NL)

(57)

**ABSTRACT**(72) Inventor: **Stefano STANZIONE**, Veldhoven (NL)(21) Appl. No.: **18/521,237**(22) Filed: **Nov. 28, 2023**(30) **Foreign Application Priority Data**

Nov. 30, 2022 (EP) ..... 22210609.8

**Publication Classification**(51) **Int. Cl.***H03K 17/22* (2006.01)*A61N 1/378* (2006.01)*H03K 19/20* (2006.01)

A power-on reset, POR, circuitry comprises: a comparator configured to output a POR trigger signal in dependence of a relation between a supply voltage and a target voltage level, wherein the comparator comprises a first output part configured to receive a balanced input; a trust unit comprising a second output part forming a replica of the first output part and configured to receive an unbalanced input, wherein the comparator and the trust unit are arranged in a common integrated circuit and wherein the trust unit is configured to output a trust signal indicating whether the POR trigger signal is trustable; and a decision unit configured to output a POR signal in dependence of the POR trigger signal and the trust signal.

