US 20240223176A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0223176 A1**

Nelson et al. (43) **Pub. Date: Jul. 4, 2024**

(54) **OPTIMIZATION OF POWER MODULE PERFORMANCE VIA PARASITIC MUTUAL COUPLING**

(71) Applicant: **Wolfspeed, Inc.**, Durham, NC (US)

(72) Inventors: **Blake Whitmore Nelson**, Fayetteville, AR (US); **Brian DeBoi**, Northport, AL (US); **Daniel John Martin**, Fayetteville, AR (US)

(21) Appl. No.: **18/429,613**

(22) Filed: **Feb. 1, 2024**

Related U.S. Application Data

(63) Continuation of application No. 17/849,676, filed on Jun. 26, 2022, now Pat. No. 11,936,368.

Publication Classification

(51) **Int. Cl.**

H03K 17/041	(2006.01)
H03K 17/687	(2006.01)

(52) **U.S. Cl.**

CPC ***H03K 17/04106*** (2013.01); ***H03K 17/687*** (2013.01); *H03K 2217/0063* (2013.01); *H03K 2217/0072* (2013.01)

(57) **ABSTRACT**

The present disclosure relates to a power module with a power path extending through a first field-effect transistor (FET) and a second FET. A primary conductive structure connecting the first FET and the second FET in series provides a primary parasitic inductor within the power path. A first secondary conductive structure connected to both a gate and a source of the first FET provides a first secondary parasitic inductor within a first gate path, and a second secondary conductive structure connected to both a gate and a source of the second FET provides a second secondary parasitic inductor within a second gate path. The first secondary conductive structure and the second secondary conductive structure are configured such that mutual coupling between the first secondary parasitic inductor and the primary parasitic inductor and mutual coupling between the second secondary parasitic inductor and the primary parasitic inductor are substantially symmetrical.