



US 20220352704A1

(19) **United States**(12) **Patent Application Publication**
LIN et al.(10) **Pub. No.: US 2022/0352704 A1**(43) **Pub. Date: Nov. 3, 2022**(54) **PROTECTION CIRCUIT AND HUB CHIP**(52) **U.S. Cl.**(71) Applicant: **VIA LABS, INC.**, New Taipei City
(TW)CPC **H02H 1/0061** (2013.01); **H02H 1/04**
(2013.01); **H02H 9/04** (2013.01)(72) Inventors: **Hsiao Chyi LIN**, New Taipei City
(TW); **Chia Ming TU**, New Taipei City
(TW); **Yi Shing LIN**, New Taipei City
(TW); **Shao-Yu CHEN**, New Taipei
City (TW)

(57)

ABSTRACT(21) Appl. No.: **17/411,289**(22) Filed: **Aug. 25, 2021**(30) **Foreign Application Priority Data**

May 3, 2021 (TW) 110115875

Publication Classification(51) **Int. Cl.****H02H 1/00** (2006.01)**H02H 1/04** (2006.01)**H02H 9/04** (2006.01)

A protection circuit applied in a hub chip including a power pin, a first data pin, and a second data pin is provided. A voltage generation circuit generates and adjusts output voltage according to the voltage of the power pin and the voltage of the first data pin. A PMOS transistor includes a first gate, a first electrode, a second electrode, and a first bulk. The first electrode is coupled to the power pin. The second electrode is coupled to the first data pin. The first bulk receives the output voltage. A detection circuit is coupled to the first gate and detects the voltage of the power pin. In response to the voltage of the power pin being equal to the first voltage, the detection circuit transmits the voltage of the first data pin to the first gate.

