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(54) **FIXED TIME-DELAY CIRCUIT OF HIGH-SPEED INTERFACE**

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(57) **ABSTRACT**

A fixed time-delay circuit of a high-speed interface is disclosed. The fixed time-delay circuit comprises: a counter circuit for generating a shift selection signal of any bit; a data selector circuit for receiving first parallel data signals and rearranging the first parallel data signals according to the shift selection signal and a first low-speed clock to obtain second parallel data signals; a clock selector circuit for selecting, according to the shift selection signal, one clock from multiple input clocks having different phases, for outputting, to form a second low-speed clock; and a synchronization circuit for synchronizing the second parallel data signals according to the second low-speed clock. According to the circuit, initialization alignment among multichannel data of the high-speed interface can be achieved.