



US 20240237555A9

(19) **United States**
(12) **Patent Application Publication**
Enderud et al.

(10) **Pub. No.: US 2024/0237555 A9**
(48) **Pub. Date: Jul. 11, 2024**
CORRECTED PUBLICATION

(54) **SYSTEMS AND METHODS FOR
FABRICATION OF SUPERCONDUCTING
INTEGRATED CIRCUITS WITH IMPROVED
COHERENCE**

H01L 25/18 (2006.01)
H10N 60/12 (2006.01)
H10N 60/80 (2006.01)
H10N 69/00 (2006.01)

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(52) **U.S. Cl.**
CPC *H10N 60/0912* (2023.02); *H01L 23/5223*
(2013.01); *H01L 23/5227* (2013.01); *H01L*
23/53285 (2013.01); *H01L 25/18* (2013.01);
H10N 60/12 (2023.02); *H10N 60/805*
(2023.02); *H10N 69/00* (2023.02)

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(21) Appl. No.: **18/277,688**
(22) PCT Filed: **Feb. 17, 2022**
(86) PCT No.: **PCT/US2022/016802**
§ 371 (c)(1),
(2) Date: **Aug. 17, 2023**

Prior Publication Data

(15) Correction of US 2024/0138268 A1 Apr. 25, 2024
See (86) PCT No.
(65) US 2024/0138268 A1 Apr. 25, 2024

Related U.S. Application Data

(60) Provisional application No. 63/151,232, filed on Feb.
19, 2021, provisional application No. 63/191,708,
filed on May 21, 2021, provisional application No.
63/194,364, filed on May 28, 2021.

Publication Classification

(51) **Int. Cl.**
H10N 60/01 (2006.01)
H01L 23/522 (2006.01)
H01L 23/532 (2006.01)

(57) **ABSTRACT**

A method of fabrication of a superconducting device includes forming a first portion of the superconducting device on a first chip, a second portion of the superconducting device on a second chip, and bonding the first chip to the second chip, arranged in a flip-chip configuration. The first portion of the superconducting device on the first chip includes a dissipative portion of the superconducting device. A multi-layer superconducting integrated circuit is implemented so that noise-susceptible superconducting devices are positioned in wiring layers formed from a low-noise superconductive material and that underlie wiring layers that are formed from a different superconductive material. A superconducting integrated circuit has a first stack with a first superconducting wiring layer formed from a first high kinetic inductance material and a second superconducting wiring layer communicatively coupled to the first superconducting wiring layer to form a first control circuit, a second stack comprising a third superconducting wiring layer formed from a second high kinetic inductance material and a fourth superconducting wiring layer communicatively coupled to the third superconducting wiring layer to form a second control circuit. The superconducting integrated circuit also has a third stack with a controllable device, and at least one of the first control circuit and the second control circuit is communicatively coupled to the controllable device.

