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(54) **LOW RESISTANCE BOTTOM ELECTRODE VIA**

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(57) **ABSTRACT**

An integrated circuit fabrication method comprises: providing a semiconductor wafer including a dielectric layer disposed over a copper or copper alloy layer; forming a via opening in the dielectric layer exposing a portion of the copper or copper alloy layer; disposing a copper-barrier layer in the via opening; disposing an oxophilic layer on the copper-barrier layer wherein the semiconductor wafer is not exposed to air between an end of the disposing of the copper-barrier layer and a start of the disposing of the oxophilic layer; after disposing the oxophilic layer, filling the via opening with tungsten to form a tungsten via; and forming an electronic device in electrical contact with the copper or copper alloy layer by way of the tungsten via.