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(54) **METHOD FOR PERFORMING DIVIDED-CLOCK PHASE SYNCHRONIZATION IN MULTI-DIVIDED-CLOCK SYSTEM, SYNCHRONIZATION CONTROL CIRCUIT, SYNCHRONIZATION CONTROL SUB-CIRCUIT, AND ELECTRONIC DEVICE**

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(57) **ABSTRACT**

A method for performing divided-clock phase synchronization in a multi-divided-clock system, an associated synchronization control circuit, an associated synchronization control sub-circuit and an associated electronic device are provided. The method may include: performing frequency division operations according to a source clock to generate a first divided clock and a second divided clock; performing phase relationship detection on the first divided clock according to the second divided clock to generate a phase relationship detection result signal; performing a logic operation on a first phase selection result output signal and the phase relationship detection result signal to generate a second phase selection result output signal; and outputting one of the second divided clock and an inverted signal of the second divided clock according to the second phase selection result output signal, for further use in a physical layer circuit.