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(19) **United States**(12) **Patent Application Publication**  
TSUTSUMI et al.(10) **Pub. No.: US 2024/0215243 A1**(43) **Pub. Date: Jun. 27, 2024**(54) **THREE-DIMENSIONAL MEMORY DEVICE  
WITH THROUGH-STACK CONTACT VIA  
STRUCTURES AND METHOD OF MAKING  
THE SAME**(60) Provisional application No. 63/476,488, filed on Dec.  
21, 2022, provisional application No. 63/499,819,  
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CPC ..... **H10B 43/27** (2023.02)(57) **ABSTRACT**

A memory device includes an alternating stack of insulating layers and electrically conductive layers, and comprising stepped surfaces, a memory opening vertically extending through each layer within the alternating stack, a memory opening fill structure located in the memory opening and including a vertical stack of memory elements and a vertical semiconductor channel, a dielectric material layer that extends from a bottommost vertical step of the stepped surfaces to a topmost vertical step of the stepped surfaces, and a contact via structure including an upper contact via portion having an annular bottom surface that contacts an annular top surface of a first electrically conductive layer of the electrically conductive layers, and a lower contact via portion that vertically extends through a first subset of the electrically conductive layers that underlie the first electrically conductive layer, and the lower contact via portion is narrower than the upper contact via portion.

(71) Applicant: **WESTERN DIGITAL  
TECHNOLOGIES, INC.,** SAN JOSE,  
CA (US)(72) Inventors: **Masanori TSUTSUMI**, Yokkaichi (JP);  
**Koichi MATSUNO**, Fremont, CA (US);  
**Tomohiro KUBO**, Yokkaichi (JP);  
**Masato MIYAMOTO**, Yokkaichi (JP);  
**Takumi MORIYAMA**, Yokkaichi (JP);  
**Shunsuke TAKUMA**, Yokkaichi (JP);  
**Michio ORYOJI**, Yokkaichi (JP)(21) Appl. No.: **18/532,221**(22) Filed: **Dec. 7, 2023****Related U.S. Application Data**(63) Continuation-in-part of application No. 18/351,828,  
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