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**XIONG et al.**(10) **Pub. No.: US 2022/0385309 A1**(43) **Pub. Date: Dec. 1, 2022**(54) **CONCATENATED ERROR CORRECTING  
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**ABSTRACT**(72) Inventors: **Chenrong XIONG**, San Jose, CA (US);  
**Jie CHEN**, Milpitas, CA (US)(21) Appl. No.: **17/335,640**(22) Filed: **Jun. 1, 2021****Publication Classification**(51) **Int. Cl.***H03M 13/31* (2006.01)*H03M 13/15* (2006.01)*H03M 13/11* (2006.01)*H03M 13/43* (2006.01)(52) **U.S. Cl.**CPC ..... *H03M 13/31* (2013.01); *H03M 13/152*  
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Systems and methods are provided for concatenated error-correcting coding. An apparatus may include a Low-Density Parity-Check (LDPC) decoder configured to perform an iterative LDPC decoding process on bits of an LDPC codeword, a Bose—Chaudhuri—Hocquenghem (BCH) decoder coupled to the LDPC decoder and a BCH scheduler coupled to the LDPC decoder and the BCH decoder. The LDPC codeword may be generated by LDPC encoding a Bose—Chaudhuri—Hocquenghem (BCH) codeword and the BCH codeword may be generated by BCH encoding a data unit. The BCH scheduler may be configured to determine whether a triggering condition for the BCH decoder is met after each iteration of the iterative LDPC decoding process and activate the BCH decoder to operate on an intermediate decoding result of the LDPC decoder if the triggering condition for the BCH decoder is met.

