



US 20240215173A1

(19) **United States**

(12) **Patent Application Publication**  
**Ortiz et al.**

(10) **Pub. No.: US 2024/0215173 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **FLEXIBLE INTERCONNECT CIRCUITS FOR BATTERY PACKS**

(71) Applicant: **Cellink Corporation**, San Carlos, CA (US)

(72) Inventors: **Jean-Paul Ortiz**, White Lake, MI (US); **Malcolm Parker Brown**, Mountain View, CA (US); **Casey Anderson**, San Carlos, CA (US); **Will Findlay**, San Carlos, CA (US); **Gabrielle Tate**, Royal Oak, MI (US); **Shawn D’Gama**, Wixom, MI (US); **Arturo Cantu-Chavez**, San Carlos, CA (US)

(73) Assignee: **Cellink Corporation**, San Carlos, CA (US)

(21) Appl. No.: **18/595,910**

(22) Filed: **Mar. 5, 2024**

**Related U.S. Application Data**

(63) Continuation of application No. 18/300,828, filed on Apr. 14, 2023, now Pat. No. 11,950,377.

(60) Provisional application No. 63/363,032, filed on Apr. 15, 2022.

**Publication Classification**

(51) **Int. Cl.**  
**H05K 3/46** (2006.01)  
**H05K 1/02** (2006.01)  
**H05K 1/11** (2006.01)  
(52) **U.S. Cl.**  
CPC ..... **H05K 3/46** (2013.01); **H05K 1/0201** (2013.01); **H05K 1/118** (2013.01); **H05K 2201/10037** (2013.01)

(57) **ABSTRACT**

Provided are flexible interconnect circuits comprising signal circuit elements. For example, a signal circuit element can be formed from the same metal sheet as a signal trace, thereby being monolithic with the signal circuit element. This integration of signal circuit elements into a flexible interconnect circuit reduces the number of additional operations and components (e.g., attaching external circuit elements). In some examples, a flexible interconnect circuit is used in a battery pack for interconnecting batteries while providing external terminals on the same side of the pack. Specifically, a flexible interconnect circuit comprises an interconnecting conductive layer (for connecting to batteries) and a return conductive layer, both extending between the first and second circuit edges. Each of these conductive layers comprises a corresponding external terminal at the first edge, while these layers are interconnected at the second edge. Otherwise, these layers are isolated from each other between the circuit edges.

