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Hsu et al.(10) **Pub. No.: US 2023/0231051 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SEMICONDUCTOR DEVICE***H01L 29/165* (2006.01)*H01L 21/02* (2006.01)(71) Applicant: **UNITED MICROELECTRONICS CORP.**, Hsin-Chu City (TW)(52) **U.S. Cl.**CPC *H01L 29/7848* (2013.01); *H01L 29/0847* (2013.01); *H01L 29/165* (2013.01); *H01L 21/0245* (2013.01); *H01L 21/02502* (2013.01); *H01L 21/0251* (2013.01); *H01L 21/02532* (2013.01); *H01L 21/0262* (2013.01); *H01L 21/02639* (2013.01)(72) Inventors: **Chia-Jhe Hsu**, Kaohsiung City (TW);
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A semiconductor device includes a gate structure on a substrate and an epitaxial layer adjacent to the gate structure, in which the epitaxial layer includes a first buffer layer, a second buffer layer on the first buffer layer, a bulk layer on the second buffer layer, a first cap layer on the bulk layer, and a second cap layer on the first cap layer. Preferably, the bottom surface of the first buffer layer includes a linear surface, a bottom surface of the second buffer layer includes a curve, and the second buffer layer includes a linear sidewall.

