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(54) **MEMORY DEVICE HAVING 2-TRANSISTOR VERTICAL MEMORY CELL AND SHIELD STRUCTURES**

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(57) **ABSTRACT**

Some embodiments include apparatuses and methods of forming the apparatuses. One of the apparatuses includes a conductive region, a first data line, a second data line, a first memory cell coupled to the first data line and the conductive region, a second memory cell coupled to the second data line and the conductive region, a conductive structure, and a conductive line. The first memory cell includes a first transistor coupled to a second transistor, the first transistor including a first charge storage structure. The second memory cell includes a third transistor coupled to a fourth transistor, the third transistor including a second charge storage structure. The conductive structure is located between and electrically separated from the first and second charge storage structures. The conductive line forms a gate of each of the first, second, third, and fourth transistors.