

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0213223 A1 JUNG et al.

Jun. 27, 2024 (43) Pub. Date:

(54) SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING THE SEMICONDUCTOR PACKAGE

(71) Applicant: SAMSUNG ELECTRONICS CO.,

LTD., Suwon-si (KR)

(72) Inventors: Jaemok JUNG, Suwon-si (KR);

Dowan KIM, Suwon-si (KR); Sungkeun PARK, Suwon-si (KR); Jongho PARK, Suwon-si (KR); Juil

CHOI, Suwon-si (KR)

Assignee: SAMSUNG ELECTRONICS CO.,

LTD., Suwon-si (KR)

Appl. No.: 18/516,367

(22)Filed: Nov. 21, 2023

(30)Foreign Application Priority Data

Dec. 22, 2022 (KR) 10-2022-0182247

Publication Classification

(51)	Int. Cl.	
	H01L 25/065	(2006.01)
	H01L 23/00	(2006.01)
	H01L 23/31	(2006.01)
	H01L 23/498	(2006.01)
	H01L 23/522	(2006.01)

(52) U.S. Cl.

CPC H01L 25/0657 (2013.01); H01L 23/3107 (2013.01); H01L 23/49816 (2013.01); H01L 23/49838 (2013.01); H01L 23/5226 (2013.01); H01L 24/08 (2013.01); H01L 24/16 (2013.01); H01L 24/32 (2013.01); H01L 24/48 (2013.01); H01L 24/73 (2013.01); H01L 2224/08056 (2013.01); H01L 2224/08245 (2013.01); H01L 2224/16245 (2013.01); H01L 2224/32145 (2013.01); H01L 2224/32245 (2013.01); H01L 2224/48145 (2013.01); H01L 2224/48227 (2013.01); H01L 2224/73204 (2013.01); H01L 2224/73265 (2013.01); H01L 2225/06506 (2013.01); H01L 2225/06544 (2013.01); H01L 2924/181 (2013.01)

(57)ABSTRACT

A semiconductor package includes a first redistribution wiring layer having a first region and a second region surrounding the first region, a semiconductor chip disposed on the first region of the first redistribution wiring layer, a sealing member covering the semiconductor chip on the first redistribution wiring layer, vertical conductive wires penetrating the sealing member on the second region of the first redistribution wiring layer, a second redistribution wiring layer disposed on the sealing member and including second redistribution wirings electrically connected to the vertical conductive wires, and bonding pads provided on an upper surface of the first redistribution wiring layer or a lower surface of the second redistribution wiring layer, each bonding pad having a concavo-convex pattern on an upper surface of the bonding pad. The vertical conductive wires are bonded to the concavo-convex patterns of the bonding pads, respectively.

