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(54) **GATE LINE STRUCTURE TO REDUCE WAFER BOW**

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(57) **ABSTRACT**

A three-dimensional (3D) memory device includes a memory array device, a peripheral device, an etch stop layer, and a backside gate line slit. The memory array device includes a frontside and a backside, a plurality of memory strings, and a plurality of word lines in a staircase structure coupled to the plurality of memory strings. The peripheral device is above the frontside of the memory array device. The etch stop layer is between the memory array device and the peripheral device. The backside gate line slit extends through the backside of the memory array device to the etch stop layer. The backside gate line slit includes a conductive gate line layer and an insulating gate line layer. The 3D memory device can increase manufacturing efficiency, increase yield, reduce thermal stress, reduce fluorine contamination, increase an overlay window, and decrease overlay errors.

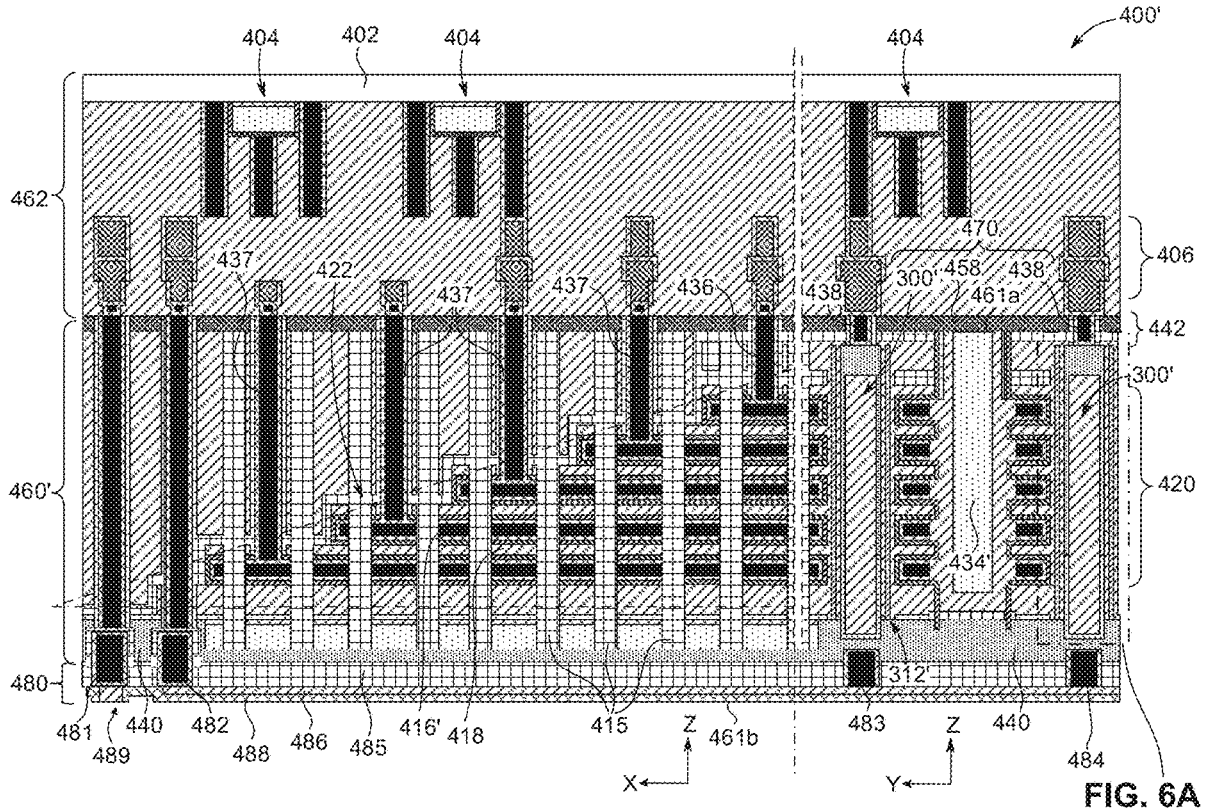


FIG. 6A