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(54) **MODIFIED INTERNAL CLEARANCE(S) AT CONNECTOR PIN APERTURE(S) OF A CIRCUIT BOARD**

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(57) **ABSTRACT**

A method of fabricating a multilayer circuit board is provided which includes forming a layer of a the multilayer circuit board with an internal clearance region having a modified voltage-to-ground clearance of conductive material adjacent to an aperture of the multilayer circuit board. The modified voltage-to-ground clearance of conductive material is based on a configuration of a connector pin to be press-fit connected within the aperture of the multilayer circuit board, and the internal clearance region is enlarged in a direction of greatest normal force outward from the aperture with insertion of the connector pin into the aperture.