



US 20220376696A1

(19) **United States**(12) **Patent Application Publication**
HUANG(10) **Pub. No.: US 2022/0376696 A1**(43) **Pub. Date: Nov. 24, 2022**(54) **PIPELINE ANALOG TO DIGITAL
CONVERTER AND SIGNAL CONVERSION
METHOD**(52) **U.S. Cl.**
CPC *H03M 1/1019* (2013.01); *H03M 1/123*
(2013.01)(71) Applicant: **REALTEK SEMICONDUCTOR
CORPORATION, HSINCHU (TW)**(57) **ABSTRACT**(72) Inventor: **SHIH-HSIUNG HUANG, Hsinchu
(TW)**

A pipeline analog to digital converter includes converter circuitries and a calibration circuitry. The converter circuitries sequentially convert an input signal into a plurality of first digital codes, in which a first converter circuitry in the converter circuitries is configured to perform a quantization according to a first signal to generate a first corresponding digital code in the first digital codes, and the first signal is a signal, which is processed by the first converter circuitry, of the input signal and a previous stage residue signal. The calibration circuitry combines the first digital codes to output a second digital code, detects whether the quantization is completed to generate control signals, and determines whether to set the second digital code to be a second corresponding digital code in predetermined digital codes according to the control signals.

(21) Appl. No.: **17/688,942**(22) Filed: **Mar. 8, 2022**(30) **Foreign Application Priority Data**

May 24, 2021 (TW) 110118688

Publication Classification(51) **Int. Cl.**
H03M 1/10 (2006.01)
H03M 1/12 (2006.01)