US 20220352829A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0352829 A1**

Lin (43) **Pub. Date: Nov. 3, 2022**

(54) **VOLTAGE-CONTROLLED DELAY BUFFER OF WIDE TUNING RANGE**

(71) Applicant: **Realtek Semiconductor Corp.**, Hsinchu (TW)

(72) Inventor: **Chia-Liang (Leon) Lin**, Fremont, CA (US)

(21) Appl. No.: **17/242,396**

(22) Filed: **Apr. 28, 2021**

Publication Classification

(51) **Int. Cl.**
H02M 7/537 (2006.01)

(52) **U.S. Cl.**
CPC .. ***H02M 7/537*** (2013.01); *H03K 2005/00078* (2013.01)

(57) **ABSTRACT**

A voltage-controlled delay buffer includes a plurality of inverters configured in a cascade topology to receive an input signal from a source circuit and output an output signal to an output circuit. The plurality of inverters includes a voltage-controlled inverter controlled by a control signal having a first voltage and a second voltage. The voltage-controlled inverter includes a PMOS transistor configured to assist a low-to-high transition of an outgoing signal, and an NMOS transistor configured to assist a high-to-low transition of the outgoing signal. Two varactors, one forward connected and the other backward connected are configured to adjust a delay of a transition of an incoming signal.; Another two varactors, one forward connected and the other backward connected, configured to adjust a delay of a transition of the outgoing signal in accordance with the first voltage and the second voltage.