US 20230403867A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2023/0403867 A1**

Ramaswamy (43) **Pub. Date: Dec. 14, 2023**

(54) **MEMORY ARRAYS COMPRISING VERTICALLY-ALTERNATING TIERS OF INSULATIVE MATERIAL AND MEMORY CELLS AND METHODS OF FORMING A MEMORY ARRAY**

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(21) Appl. No.: **18/239,063**

(22) Filed: **Aug. 28, 2023**

Related U.S. Application Data

(60) Continuation of application No. 17/867,544, filed on Jul. 18, 2022, now Pat. No. 11,778,838, which is a continuation of application No. 17/001,906, filed on Aug. 25, 2020, now Pat. No. 11,411,002, which is a division of application No. 16/119,835, filed on Aug. 31, 2018, now Pat. No. 10,804,273.

(60) Provisional application No. 62/554,972, filed on Sep. 6, 2017.

Publication Classification

(51) **Int. Cl.**

H10B 99/00	(2006.01)
G11C 11/24	(2006.01)
G11C 11/22	(2006.01)
H01L 27/06	(2006.01)
H10B 12/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H10B 99/00*** (2023.02); ***G11C 11/24*** (2013.01); ***G11C 11/221*** (2013.01); ***G11C 11/223*** (2013.01); ***H01L 27/0688*** (2013.01); ***H10B 12/30*** (2023.02); ***H10B 12/37*** (2023.02); *G11C 5/02* (2013.01)

(57) **ABSTRACT**

A memory array comprises vertically-alternating tiers of insulative material and memory cells. The memory cells individually comprise a transistor and a capacitor. The capacitor comprises a first electrode electrically coupled to a source/drain region of the transistor. The first electrode comprises an annulus in a straight-line horizontal cross-section and a capacitor insulator radially inward of the first electrode annulus. A second electrode is radially inward of the capacitor insulator. A capacitor-electrode structure extends elevationally through the vertically-alternating tiers. Individual of the second electrodes of individual of the capacitors are electrically coupled to the elevationally-extending capacitor-electrode structure. A sense line is electrically coupled to another source/drain region of multiple of the transistors that are in different memory-cell tiers. Additional embodiments and aspects are disclosed, including methods.