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(19) **United States**(12) **Patent Application Publication****Kim et al.**(10) **Pub. No.: US 2023/0403854 A1**(43) **Pub. Date: Dec. 14, 2023**(54) **SEMICONDUCTOR MEMORY DEVICES  
AND ELECTRONIC SYSTEMS**(52) **U.S. Cl.**CPC ..... **H10B 43/27** (2023.02); **H10B 80/00**  
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(57)

**ABSTRACT**

According to some implementations of the present disclosure, a semiconductor memory device includes a semiconductor layer including a first face and a second face opposite to the first face in a first direction directed upward from the first face to the second face; a source structure including: a plate disposed on the second face of the semiconductor layer; and a plug extending from the plate through the semiconductor layer; a plurality of gate electrodes disposed on the first face of the semiconductor layer and sequentially stacked on one another; and a channel structure that extends through the plurality of gate electrodes and that is disposed on the plug, wherein the channel structure is electrically connected to the source structure.

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