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(54) **HIGH PERFORMANCE PHASE LOCKED LOOP FOR MILLIMETER WAVE APPLICATIONS**

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(57) **ABSTRACT**

A phase lock loop (PLL) includes an input comparison circuit configured to compare a reference signal to a divided feedback signal and generate at least one charge pump control signal based thereupon. A charge pump generates a charge pump output signal in response to the at least one charge pump control signal. A loop filter is coupled to receive and filter the charge pump output signal to produce an oscillator control signal. An oscillator generates an output signal in response to the oscillator control signal, with the output signal divided by a divisor using divider circuitry to produce the divided feedback signal. Divisor generation circuitry is configured to change the divisor over time so that a frequency of the divided feedback signal changes from a first frequency to a second frequency over time.