

## (19) United States

# (12) Patent Application Publication (10) Pub. No.: US 2023/0230963 A1

## Jul. 20, 2023 (43) **Pub. Date:**

#### (54) SEMICONDUCTOR STRUCTURE AND FORMING METHOD THEREOF

(71) Applicants: Semiconductor Manufacturing International (Shanghai) Corporation, Shanghai (CN); Semiconductor Manufacturing International (Beijing) Corporation, Beijing (CN)

(72) Inventor: Jisong JIN, Shanghai (CN)

(73) Assignees: Semiconductor Manufacturing International (Shanghai) Corporation, Shanghai (CN); Semiconductor Manufacturing International (Beijing) Corporation, Beijing (CN)

(21) Appl. No.: 18/123,484

(22) Filed: Mar. 20, 2023

### Related U.S. Application Data

(62) Division of application No. 17/218,831, filed on Mar. 31, 2021, now Pat. No. 11,637,092.

(30)Foreign Application Priority Data

Oct. 21, 2020 (CN) ...... 202011133059.X

### **Publication Classification**

(51) **Int. Cl.** H01L 25/07 (2006.01)H01L 25/18 (2006.01) H01L 25/065 (2006.01)(2006.01)H01L 25/00

U.S. Cl.

CPC ...... H01L 25/074 (2013.01); H01L 25/18 (2013.01); H01L 25/0657 (2013.01); H01L 25/50 (2013.01); H01L 24/29 (2013.01)

#### (57)**ABSTRACT**

A semiconductor structure and a forming method thereof are provided. One form of a semiconductor structure includes: a first device structure, including a first substrate and a first device formed on the first substrate, the first device including a first channel layer structure located on the first substrate, a first device gate structure extending across the first channel layer structure, and a first source-drain doping region located in the first channel layer structure on two sides of the first device gate structure; and a second device structure, located on a front surface of the first device structure, including a second substrate located on the first device structure and a second device formed on the second substrate, the second device including a second channel layer structure located on the second substrate, a second device gate structure extending across the second channel layer structure, and a second source-drain doping region located in the second channel layer structure on two sides of the second device gate structure, where projections of the second channel layer structure and the first channel layer structure onto the first substrate intersect non-orthogonally. The electricity of the first device can be led out according to the present disclosure.

