US 20230232629A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2023/0232629 A1**

Ma et al. (43) **Pub. Date: Jul. 20, 2023**

(54) **METHOD AND APPARATUS TO MITIGATE WORD LINE STAIRCASE ETCH STOP LAYER THICKNESS VARIATIONS IN 3D NAND DEVICES**

(71) Applicant: **Intel Corporation**, Santa Clara, CA (US)

(72) Inventors: **Hong Ma**, Singapore (SG); **Sha Tao**, Dalian (CN); **Qun Li**, Liaoning (CN)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(21) Appl. No.: **18/002,513**

(22) PCT Filed: **Jul. 23, 2020**

(86) PCT No.: **PCT/CN2020/103811**

§ 371 (c)(1),
(2) Date: **Dec. 20, 2022**

Publication Classification

(51) **Int. Cl.**

H10B 43/27	(2006.01)
G11C 16/04	(2006.01)
H10B 43/35	(2006.01)
H01L 23/522	(2006.01)
H01L 23/528	(2006.01)
H10B 41/35	(2006.01)
H10B 41/27	(2006.01)
H01L 21/768	(2006.01)

(52) **U.S. Cl.**

CPC ***H10B 43/27*** (2023.02); ***G11C 16/0483*** (2013.01); ***H10B 43/35*** (2023.02); ***H01L 23/5226*** (2013.01); ***H01L 23/5283*** (2013.01); ***H10B 41/35*** (2023.02); ***H10B 41/27*** (2023.02); ***H01L 21/76877*** (2013.01)

(57) **ABSTRACT**

An apparatus, a method and a system. The apparatus comprises a memory array including word lines defining a staircase structure, and a staircase etch stop layer including: a sandwich etch stop layer disposed on a top region the staircase and including a first etch stop layer and a third etch stop layer of a first material, and a second etch stop layer sandwiched between the first etch stop layer and the third etch stop layer and made of a second material having etch properties different from the first material; a precut etch stop layer disposed at a region of the staircase structure below the top region and including the second etch stop layer and the third etch stop layer and not the first etch stop layer; and contact structures extending through a dielectric layer and the staircase etch stop layer and landing on the word lines at the staircase structure.