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(54) **NAND PLANE BOUNDARY SHRINK**

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(57) **ABSTRACT**

Technology is disclosed herein for a memory device having a narrow gap between planes and a method of shrinking the gap between planes. A first and second adjacent planes each has a word line (WL) hookup region at mid-plane. A dummy array region resides between the two planes. The dummy array region may contain a stack of alternating layers of a first insulating material and a second insulating material. There is a first electrical isolation structure between the dummy array region and a stack in the first plane. There is a second electrical isolation structure between the dummy array region and a stack in a second plane. The electrical isolation structures may be formed in narrow trenches. The combination of the dummy array region and the two electrical isolation structures results in a very short gap between the adjacent planes.