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**Ge et al.**(10) **Pub. No.: US 2024/0237359 A1**(43) **Pub. Date: Jul. 11, 2024**(54) **SYSTEM-ON-A-CHIP (SOC) INTEGRATION  
OF RESISTIVE RANDOM-ACCESS MEMORY  
DEVICES WITH VARYING SWITCHING  
CHARACTERISTICS**(52) **U.S. CL.**CPC ..... *H10B 63/84* (2023.02); *H10B 63/30*  
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*H10N 70/8833* (2023.02)(71) Applicant: **TetraMem Inc.**, Fremont, CA (US)

(57)

**ABSTRACT**(72) Inventors: **Ning Ge**, Danville, CA (US); **Minxian  
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An apparatus including a plurality of resistive random-access memory (RRAM) devices is provided. The RRAM devices are fabricated on a single substrate in some embodiments. The apparatus includes an interconnect layer fabricated on the substrate. A first RRAM device of the RRAM devices includes a first bottom electrode, a first top electrode; and a first filament-forming layer fabricated between the first bottom electrode and the first top electrode. A second RRAM device of the RRAM devices includes a second bottom electrode, a second top electrode, and a second filament-forming layer fabricated between the second bottom electrode and the second top electrode. The first bottom electrode and the second bottom electrode are fabricated on multiple metallic pads or metallic vias of the interconnect layer. The first filament-forming layer and the second filament-forming layer include different switching oxides.

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