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(54) **RDAC LADDER WITH ADAPTIVE BIASING TO REDUCE THE REFERENCE VARIATION ACROSS TEMPERATURE**

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(57) **ABSTRACT**

A low current, adaptively-biased switched resistor digital-to-analog converter (RDAC) circuit, method and apparatus are provided with a coarse trim ladder and a fine trim ladder connected with a plurality of NFET switches to generate an output reference voltage from an input supply voltage, where the bulk semiconductor substrate regions for the NFET switches in at least the fine trim ladder are driven by a unity gain buffer which is connected in feedback to receive the output reference voltage and to generate a buffered reference voltage which is directly connected to bulk semiconductor regions of the NFET switches, thereby providing a low current, low circuit area solution with reduced leakage current and temperature variation.