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(19) **United States**(12) **Patent Application Publication**  
**ARAI**(10) **Pub. No.: US 2023/0403857 A1**(43) **Pub. Date: Dec. 14, 2023**(54) **THREE-DIMENSIONAL SEMICONDUCTOR  
MEMORY DEVICE**(71) Applicant: **KIOXIA CORPORATION**, Tokyo (JP)(72) Inventor: **Shinya ARAI**, Yokkaichi (JP)(73) Assignee: **KIOXIA CORPORATION**, Tokyo (JP)(21) Appl. No.: **18/456,927**(22) Filed: **Aug. 28, 2023****Related U.S. Application Data**

- (63) Continuation of application No. 17/848,789, filed on Jun. 24, 2022, now Pat. No. 11,778,828, which is a continuation of application No. 17/011,517, filed on Sep. 3, 2020, now Pat. No. 11,417,679, which is a continuation of application No. 16/137,702, filed on Sep. 21, 2018, now Pat. No. 10,804,288, which is a continuation of application No. 15/344,021, filed on Nov. 4, 2016, now Pat. No. 10,109,643, which is a continuation of application No. 14/597,580, filed on Jan. 15, 2015, now Pat. No. 9,524,979.
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(57)

**ABSTRACT**

According to one embodiment, a semiconductor memory device includes a substrate; an insulating layer provided on the substrate; a conductive layer provided on the insulating layer; a stacked body provided on the conductive layer and including a plurality of electrode layers and a plurality of insulating layers respectively provided among the plurality of electrode layers; a columnar section piercing through the stacked body to reach the conductive layer and extending in a first direction in which the stacked body is stacked; and a source layer. The columnar section includes a channel body and a charge storage film provided between the channel body and the respective electrode layers. The conductive layer includes a first film having electric conductivity and in contact with the lower end portion of the channel body; and an air gap provided to be covered by the first film.

