

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2022/0393684 A1 Huffman

Dec. 8, 2022 (43) **Pub. Date:**

(54) LOW POWER INTERCONNECT USING RESONANT DRIVE CIRCUITRY

(71) Applicant: Power Down Semiconductor, Inc., Fremont, CA (US)

Inventor: **David A Huffman**, Fremont, CA (US)

(21) Appl. No.: 17/750,398

(22) Filed: May 23, 2022

Related U.S. Application Data

(60) Provisional application No. 63/196,080, filed on Jun. 2, 2021, provisional application No. 63/212,530, filed on Jun. 18, 2021.

Publication Classification

(51) Int. Cl. H03K 19/17736 (2006.01)H03K 19/17728 (2006.01) H03K 19/17704 (2006.01)(2006.01)H03K 19/1776

(52) U.S. Cl.

CPC . H03K 19/17744 (2013.01); H03K 19/17728 (2013.01); H03K 19/17704 (2013.01); H03K 19/1776 (2013.01)

(57)ABSTRACT

A field programmable gate array (FPGA) comprises a set of configurable logic blocks (CLBs), input/output blocks (IOBs), and interconnect wiring for communicating data between the CLBs and IOBs. A resonating circuit provides a resonating signal to the circuit blocks. The circuit blocks provide the resonating signal to the interconnect wires to communicate a first binary value, and a static voltage to communicate a second binary value. The output signals of the circuit blocks change state when the resonating signal is at or near the static voltage. This reduces switching losses that exist within prior art FPGAs.

