

# (19) United States

## (12) Patent Application Publication (10) Pub. No.: US 2024/0251551 A1 ZHU et al.

Jul. 25, 2024 (43) **Pub. Date:** 

(54) THREE-DIMENSIONAL MEMORY DEVICE AND METHOD OF MAKING THEREOF INCLUDING EXPANDED SUPPORT OPENINGS AND DOUBLE SPACER WORD LINE CONTACT FORMATION

(71) Applicant: SANDISK TECHNOLOGIES LLC, ADDISON, TX (US)

(72) Inventors: Ruogu Matthew ZHU, San Jose, CA (US); Koichi MATSUNO, Fremont, CA (US); Seyyed Ehsan Esfahani RASHIDI, Milpitas, CA (US); Jixin YU, Milpitas, CA (US); Johann ALSMEIER, San Jose, CA (US)

(21) Appl. No.: 18/358,727

(22) Filed: Jul. 25, 2023

### Related U.S. Application Data

(60) Provisional application No. 63/480,640, filed on Jan. 19, 2023.

### **Publication Classification**

(51) **Int. Cl.** H10B 43/27

(2006.01)H01L 23/00 (2006.01)H01L 25/00 (2006.01)

H01L 25/065 (2006.01)(2006.01)H01L 25/18 H10B 41/27 (2006.01)H10B 80/00 (2006.01)

(52) U.S. Cl.

CPC ...... H10B 43/27 (2023.02); H01L 24/08 (2013.01); H01L 24/80 (2013.01); H01L 25/0657 (2013.01); H01L 25/18 (2013.01); H01L 25/50 (2013.01); H10B 41/27 (2023.02); H10B 80/00 (2023.02); H01L 2224/08145 (2013.01); H01L 2224/80006 (2013.01); H01L 2224/80895 (2013.01); H01L 2224/80896 (2013.01); H01L 2924/1431 (2013.01); H01L 2924/14511 (2013.01)

#### (57)ABSTRACT

A memory device includes at least one alternating stack of respective insulating layers and respective electrically conductive layers and memory stack structures vertically extending through the at least one alternating stack. A layer contact via structure contacts a top surface of one of the electrically conductive layers, and is laterally surrounded by at least one dielectric spacer, which may include a plurality of dielectric spacers, and optionally by a plurality of dielectric support pillar structures. Additionally or alternatively, the layer contact via structure may comprise a convex surface segment that is adjoined to a straight sidewall segment.

