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(54) **SRAM CELL LAYOUT INCLUDING ARRANGEMENT OF MULTIPLE ACTIVE REGIONS AND MULTIPLE GATE REGIONS**

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(57) **ABSTRACT**

A memory cell including a set of active regions that overlay a set of gate regions to form a pair of cross-coupled inverters. A first active region extends along a first axis. A first gate region extends transversely to the first active region and overlays the first active region to form a first transistor of the pair of cross-coupled inverters. A second gate region extends transversely to the first active region and overlays the first active region to form a second transistor of the pair of cross-coupled inverters. A second active region extends along a second axis and overlays the first gate region to form a third transistor of the pair of cross-coupled inverters. A fourth active region extending along a third axis and overlays a gate region to form a transistor of a read port.