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(54) **MEMORY SYSTEM**

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(57) **ABSTRACT**

A memory system for low power consumption and high speed read operation in the memory system includes a source line, a string select line having i layers, a first word line having i layers, a second word line having i layers, a select gate line having 1 layer which is divided into 2n, a plurality of memory pillars and a control circuit. Each of the plurality of memory pillars includes a first string and a second string. The first string includes a first transistor, i first memory cells and j second memory cells. The first transistor, the i first memory cells, and the j second memory cells are electrically connected in series. The second string includes a second transistor, i third memory cells, and j fourth memory cells. The second transistor, the i third memory cells, and the j fourth memory cells are electrically connected in series.