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(54) **MEMORY-ELEMENT-INCLUDING SEMICONDUCTOR DEVICE**

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(57) **ABSTRACT**

In a memory cell including a first gate insulating layer **5** and a first gate conductor layer **6** surrounding a P layer **3***a* constituting a lower portion of a pillar-shaped P layer **3** standing on a P layer substrate **1**, a second gate insulating layer **9** surrounding a P layer **3***b* constituting an upper portion of the P layer **3**, a second gate conductor layer **10**, and N^+ layers **11***a* and **11***b* at both ends of the P layer **3***b* and a MOS transistor including a pillar-shaped P layer **3**A standing on a P layer substrate **1***a* connecting to the same P layer substrate **1**, a third gate insulating layer **9***a* surrounding an upper P layer **3***ba* of the P layer **3**A, a third gate conductor layer **10***a*, and N^+ layers **11***aa* and **11***ba* at both ends of the P layer **3***ba*, bottom portions and top portions of the P layer **3** and the P layer **3**A are located at substantially the same heights of line A and line C, respectively, in a perpendicular direction, and bottom portions of the P layer **3***b* and the P layer **3***ba* are located at substantially the same height of line B.