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(54) THREE-DIMENSIONAL MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

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(57) **ABSTRACT**

A memory device includes a first stacking structure, a second stacking structure, a plurality of first isolation structures, gate dielectric layers, channel layers and conductive pillars. The first stacking structure includes a plurality of first gate layers, and a second stacking structure includes a plurality of second gate layers, where the first stacking structure and the second stacking structure are located on a substrate and separated from each other through a trench. The first isolation structures are located in the trench, where a plurality of cell regions are respectively confined between two adjacent first isolation structures of the first isolation structures in the trench, where the first isolation structures each includes a first main layer and a first liner surrounding the first main layer, where the first liner separates the first main layer from the first stacking structure and the second stacking structure. The gate dielectric layers are respectively located in one of the cell regions, and cover opposing sidewalls of the first stacking structure and the second stacking structure as well as opposing sidewalls of the first isolation structures. The channel layers respectively cover an inner surface of one of the gate dielectric layers. The conductive pillars stand on the substrate within the cell regions, and are laterally surrounded by the channel layers, where at least two of the conductive pillars are located in each of the cell regions, and the at least two conductive pillars in each of the cell regions are laterally separated from one another.