

(19) **United States**

(12) **Patent Application Publication**
Or-Bach et al.

(10) **Pub. No.: US 2024/0213073 A1**

(43) **Pub. Date: Jun. 27, 2024**

- (54) **3D SEMICONDUCTOR DEVICE AND STRUCTURE WITH BONDING AND DRAM MEMORY CELLS**
- (71) Applicant: **Monolithic 3D Inc.**, Klamath Falls, OR (US)
- (72) Inventors: **Zvi Or-Bach**, Haifa (IL); **Brian Cronquist**, Klamath Falls, OR (US); **Deepak C. Sekar**, Sunnyvale, CA (US)
- (73) Assignee: **Monolithic 3D Inc.**, Klamath Falls, OR (US)
- (21) Appl. No.: **18/424,790**
- (22) Filed: **Jan. 27, 2024**

Related U.S. Application Data

- (63) Continuation-in-part of application No. 18/382,468, filed on Oct. 20, 2023, now Pat. No. 11,923,230, (Continued)

Publication Classification

- (51) **Int. Cl.**
H01L 21/683 (2006.01)
G11C 8/16 (2006.01)
(Continued)
- (52) **U.S. Cl.**
CPC **H01L 21/6835** (2013.01); **G11C 8/16** (2013.01); **H01L 21/743** (2013.01); **H01L 21/76254** (2013.01); **H01L 21/76898** (2013.01); **H01L 21/8221** (2013.01); **H01L 21/823828** (2013.01); **H01L 21/84** (2013.01); **H01L 23/481** (2013.01); **H01L 23/5252** (2013.01); **H01L 27/0207** (2013.01); **H01L 27/0688** (2013.01); **H01L 27/092** (2013.01); **H01L 27/10** (2013.01); **H01L 27/105** (2013.01); **H01L 27/11807** (2013.01); **H01L 27/11898** (2013.01); **H01L 27/1203** (2013.01); **H01L 29/4236** (2013.01); **H01L 29/66272** (2013.01); **H01L 29/66621** (2013.01); **H01L**

29/66825 (2013.01); **H01L 29/66833** (2013.01); **H01L 29/66901** (2013.01); **H01L 29/78** (2013.01); **H01L 29/7841** (2013.01); **H01L 29/7843** (2013.01); **H01L 29/7881** (2013.01); **H01L 29/792** (2013.01); **H10B 10/00** (2023.02); **H10B 10/125** (2023.02); **H10B 12/053** (2023.02); **H10B 12/09** (2023.02); **H10B 12/20** (2023.02); **H10B 12/50** (2023.02); **H10B 20/00** (2023.02); **H10B 41/20** (2023.02); **H10B 41/40** (2023.02); **H10B 41/41** (2023.02); **H10B 43/20** (2023.02); **H10B 43/40** (2023.02); **H01L 23/3677** (2013.01); **H01L 24/13** (2013.01); **H01L 24/16** (2013.01); **H01L 24/45** (2013.01); **H01L 24/48** (2013.01); **H01L 25/0655** (2013.01); **H01L 25/0657** (2013.01); **H01L 25/50** (2013.01); **H01L 27/1214** (2013.01); **H01L 27/1266** (2013.01); **H01L 2221/68368** (2013.01); **H01L 2223/5442** (2013.01); **H01L 2223/54426** (2013.01); **H01L 2224/131** (2013.01); **H01L 2224/16145** (2013.01); **H01L 2224/16146** (2013.01); **H01L 2224/16227** (2013.01); **H01L 2224/16235** (2013.01); **H01L 2224/32145** (2013.01); **H01L 2224/32225** (2013.01); **H01L 2224/45124** (2013.01); (Continued)

(57) **ABSTRACT**

A 3D semiconductor device, the device including: a first level including a first single crystal layer, the first level including first transistors, where each of the first transistors includes a single crystal channel; first metal layer; a second metal layer overlaying the first metal layer; and a second level including a second single crystal layer, the second level including second transistors and at least one third metal layer, where the second level overlays the first level, where at least one of the second transistors includes a transistor channel, where the second level includes a plurality of DRAM memory cells, where each of the plurality of DRAM memory cells includes at least one of the second transistors and one capacitor, where the second level is directly bonded to the first level, and where the bonded includes metal to metal bonds.

