



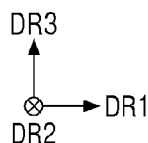
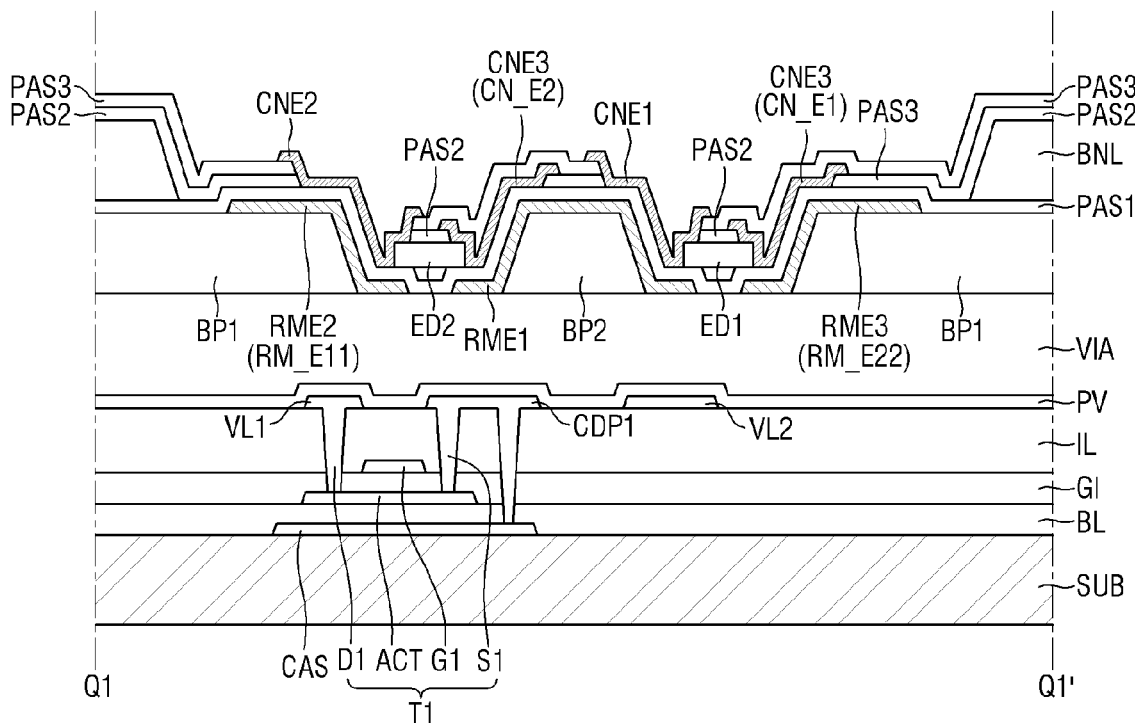
US 20230230967A1

(19) **United States**(12) **Patent Application Publication**
KIM et al.(10) **Pub. No.: US 2023/0230967 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **DISPLAY DEVICE AND METHOD OF
MANUFACTURING THE SAME**(71) Applicant: **Samsung Display Co., LTD.**, Yongin-si
(KR)(72) Inventors: **In Woo KIM**, Asan-si (KR); **Chang
Woo KWON**, Seoul (KR); **Dae Cheol
KIM**, Hwaseong-si (KR); **Jong Hwan
PARK**, Hwaseong-si (KR); **Yong Tae
CHO**, Yongin-si (KR); **Kook Hyun
CHOI**, Asan-si (KR)(73) Assignee: **Samsung Display Co., LTD.**, Yongin-si
(KR)(21) Appl. No.: **17/889,916**(22) Filed: **Aug. 17, 2022**(30) **Foreign Application Priority Data**

Jan. 20, 2022 (KR) 10-2022-0008380

Publication Classification(51) **Int. Cl.**
H01L 25/16 (2006.01)
H01L 27/12 (2006.01)
H01L 23/00 (2006.01)(52) **U.S. Cl.**CPC **H01L 25/167** (2013.01); **H01L 27/124**
(2013.01); **H01L 27/1288** (2013.01); **H01L**
24/24 (2013.01); **H01L 24/25** (2013.01);
H01L 24/82 (2013.01); **H01L 24/95** (2013.01);
H01L 2224/24051 (2013.01); **H01L**
2224/24145 (2013.01); **H01L 2224/25175**
(2013.01); **H01L 2224/24991** (2013.01); **H01L**
2224/95133 (2013.01); **H01L 2224/82106**
(2013.01); **H01L 2224/82007** (2013.01)(57) **ABSTRACT**

A display device includes a conductive pattern on a substrate, a via layer on the conductive pattern with a via hole exposing the conductive pattern, a first electrode and a second electrode on the via layer and spaced apart from each other, a first insulating layer on the first electrode and the second electrode, a bank layer on the first insulating layer defining an emission area and a subarea, a light-emitting element on the first insulating layer, and a first connection electrode and a second connection electrode on the first insulating layer and the light-emitting element. The first connection electrode electrically contacts an end of the light-emitting element, and the second connection electrode electrically contacts another end of the light-emitting element. The bank layer includes a bank extension portion extended to the subarea and the bank extension portion overlaps at least a portion of the via hole.

ED: ED1, ED2
RME: RME1, RME2, RME3
CNE: CNE1, CNE2, CNE3