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(54) **TERNARY LOGIC CIRCUIT DEVICE**

(71) Applicant: **POSTECH Research and Business Development Foundation**, Pohang-si (KR)

(72) Inventors: **Seokhyeong KANG**, Pohang-si (KR); **Sunmean KIM**, Pohang-si (KR); **SungYun LEE**, Busan (KR); **Sunghye PARK**, Daegu (KR)

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(57) **ABSTRACT**

A circuit includes a plurality of first counting gates, a first ternary half adder (THA) and a second THA that are connected to the plurality of first counting gates, a third THA configured to receive a sum output signal of the first THA and a sum output signal of the second THA, a first ternary sum gate configured to receive a carry output signal of the first THA and a carry output signal of the second THA, and a second ternary sum gate configured to receive a carry output signal of the third THA and an output signal of the first ternary sum gate, wherein the third THA and the second ternary sum gate may be configured to output voltage signals corresponding to a number of drain voltages among input signals applied to the plurality of first counting gates.