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(54) **SEMICONDUCTOR MEMORY DEVICE**

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(57) **ABSTRACT**

Disclosed are semiconductor memory devices comprising a peripheral region including a substrate, high voltage transistors on the substrate, first lower lines connected to the high voltage transistors, and second lower lines connected to the first lower lines, and a cell region on the peripheral region. The first and the second lower lines extend along a first direction parallel to an upper surface of the substrate. The first lower lines include first high voltage lines and first low voltage lines. The second lower lines include second high voltage lines and second low voltage lines. The second high voltage lines and the first low voltage lines separated in a second direction parallel to the upper surface of the substrate and a third direction perpendicular to the upper surface of the substrate, and the second low voltage lines and the first high voltage lines separated in the second direction and the third direction.