



US 20230231543A1

(19) **United States**

(12) **Patent Application Publication**
Van Zyl

(10) **Pub. No.: US 2023/0231543 A1**

(43) **Pub. Date: Jul. 20, 2023**

(54) **TWO-STAGE SOLID-STATE MATCH**

(52) **U.S. Cl.**

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CPC **H03H 11/28** (2013.01); **H01J 37/32183**
(2013.01); **H01J 2237/24564** (2013.01)

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ABSTRACT

(21) Appl. No.: **18/097,472**

This disclosure describes systems, methods, and apparatuses for a two-stage solid state match having a load side and a source side; a first coarse stage and a second precision stage, wherein the first coarse stage is coupled between the second precision stage and the load side, and wherein the second precision stage is coupled between the source side and an input of the first coarse stage; the coarse first stage comprising at least one switched variable reactance element, wherein the coarse first stage is configured to map a load impedance connected to the load side to a first number of intermediate impedances at the input of the first coarse stage; and wherein the second precision stage is configured to map at least one of the intermediate impedances to a second number of input impedances at the source side.

(22) Filed: **Jan. 16, 2023**

Related U.S. Application Data

(60) Provisional application No. 63/299,766, filed on Jan. 14, 2022.

Publication Classification

(51) **Int. Cl.**

H03H 11/28 (2006.01)
H01J 37/32 (2006.01)

