

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0251554 A1 Scarbrough et al.

Jul. 25, 2024 (43) **Pub. Date:**

(54) INTEGRATED ASSEMBLIES AND METHODS OF FORMING INTEGRATED ASSEMBLIES

(71) Applicant: Micron Technology, Inc., Boise, ID

Inventors: Alyssa N. Scarbrough, Boise, ID (US); Jordan D. Greenlee, Boise, ID (US); John D. Hopkins, Meridian, ID (US)

Assignee: Micron Technology, Inc., Boise, ID (US)

Appl. No.: 18/584,275 (21)

(22) Filed: Feb. 22, 2024

Related U.S. Application Data

(62) Division of application No. 17/162,524, filed on Jan. 29, 2021, now Pat. No. 11,950,415.

Publication Classification

(51) Int. Cl. H10B 43/27 (2006.01)H10B 41/27 (2006.01)H10B 41/35 (2006.01)

H10B 41/41 (2006.01)H10B 43/35 (2006.01)H10B 43/40 (2006.01)

U.S. Cl.

CPC H10B 43/27 (2023.02); H10B 41/27 (2023.02); H10B 41/35 (2023.02); H10B 41/41 (2023.02); H10B 43/35 (2023.02); H10B 43/40 (2023.02)

(57) ABSTRACT

Some embodiments include an integrated assembly having a memory region and another region adjacent the memory region. Channel-material-pillars are arranged within the memory region, and conductive posts are arranged within said other region. A source structure is coupled to lower regions of the channel-material-pillars. A panel extends across the memory region and the other region. Dopedsemiconductor-material is directly adjacent to the panel within the memory region and the other region. The dopedsemiconductor-material is at least part of the source structure within the memory region. Liners are directly adjacent to the conductive posts and laterally surround the conductive posts. The liners are between the conductive posts and the doped-semiconductor-material. Some embodiments include methods of forming integrated assemblies.

