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(54) **PHASE ADJUSTMENT CIRCUIT AND ENDOSCOPE SYSTEM**

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(57) **ABSTRACT**

In a phase adjustment circuit, a binary circuit is configured to output a binary signal on the basis of an edge of a video signal. A phase-delayed clock signal generation circuit is configured to generate a phase-delayed clock signal having a later phase than a phase of a clock signal by a first delay amount. A delay time control circuit is configured to cause a phase of the binary signal and the phase of the phase-delayed clock signal to match each other by adjusting the first delay amount. A sampling signal generation circuit is configured to generate a sampling signal having a later phase than the phase of the clock signal by a second delay amount. The second delay amount is in accordance with both a phase shift amount, which is based on the clock signal, and the first delay amount.