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(54) **MICROELECTRONIC DEVICES WITH ISOLATION TRENCHES IN UPPER PORTIONS OF TIERED STACKS, AND RELATED METHODS**

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(57) **ABSTRACT**

Methods for forming microelectronic devices include forming lower and upper stack structures, each comprising vertically alternating sequences of insulative and other structures arranged in tiers. Lower and upper pillar structures are formed to extend through the lower and upper stack structures, respectively. An opening is formed through the upper stack structure, and at least a portion of the other structures of the upper stack are replaced by (e.g., chemically converted into) conductive structures, which may be configured as select gate structures. Subsequently, a slit is formed, extending through both the upper and lower stack structures, and at least a portion of the other structures of the lower stack structure are replaced by a conductive material within a liner to form additional conductive structures, which may be configured as access lines (e.g., word lines). Microelectronic devices and structures and related electronic systems are also disclosed.