

## (19) United States

# (12) Patent Application Publication (10) Pub. No.: US 2023/0230956 A1

#### Jul. 20, 2023 (43) **Pub. Date:**

### SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING THE SAME

Applicant: SAMSUNG ELECTRONICS CO., LTD., SUWON-SI (KR)

Inventor: Seong Gwan Lee, Hwaseong-Si (KR)

Appl. No.: 18/189,647

(22) Filed: Mar. 24, 2023

#### Related U.S. Application Data

Continuation of application No. 17/036,465, filed on Sep. 29, 2020, now Pat. No. 11,637,085.

#### (30)Foreign Application Priority Data

Jan. 30, 2020 (KR) ...... 10-2020-0011060

#### **Publication Classification**

(51) Int. Cl. H01L 25/065 (2006.01)H01L 25/18 (2006.01) H01L 25/00 (2006.01) (52) U.S. Cl.

CPC ...... H01L 25/0652 (2013.01); H01L 25/18 (2013.01); H01L 25/50 (2013.01); H01L 2225/06506 (2013.01); H01L 2225/06527 (2013.01), H01L 2225/06562 (2013.01)

#### (57)**ABSTRACT**

A semiconductor package is provided. The semiconductor package includes: a substrate; a first buffer chip and a second buffer chip located on an upper part of the substrate; a plurality of nonvolatile memory chips located on the upper part of the substrate and including a first nonvolatile memory chip and a second nonvolatile memory chip, the first nonvolatile memory chip being electrically connected to the first buffer chip, and the second nonvolatile memory chip being electrically connected to the second buffer chip; a plurality of external connection terminals connected to a lower part of the substrate; and a rewiring pattern located inside the substrate. The rewiring pattern is configured to diverge an external electric signal received through one of the plurality of external connection terminals into first and second signals, transmit the first signal to the first buffer chip, and transmit the second signal to the second buffer chip.

