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(54) **APPARATUSES, SYSTEMS, AND METHODS FOR IDENTIFYING MULTI-BIT ERRORS**

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(57) **ABSTRACT**

Apparatuses, systems, and methods for multi-bit error detection. A memory device may store data bits and parity bits in a memory array. An error correction code (ECC) circuit may generate syndrome bits based on the data and parity bits and use the syndrome bits to correct up to a single bit error in the data and parity bits. A multi-bit error (MBE) detection circuit may detect an MBE in the data and parity based on at least one of the syndrome bits or the parity bits. For example, the MBE detection circuit may determine if the syndrome bits have a mapped or unmapped state and/or may compare the parity bits, data bits, and an additional parity bit to determine if there is an MBE. When an MBE is detected an MBE signal is activated. In some embodiments, an MBE flag may be set based on the MBE signal being active.