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(54) **DELAY-LOCKED LOOP, CONTROL METHOD FOR DELAY-LOCKED LOOP, AND ELECTRONIC DEVICE**

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(57) **ABSTRACT**

The present disclosure relates to the technical field of integrated circuits, and specifically to a delay-locked loop, a control method for a delay-locked loop, and an electronic device. The delay-locked loop includes: a secondary path configured to perform frequency division on an input clock signal to generate a frequency-divided clock signal, adjust the frequency-divided clock signal having a first frequency to obtain an output clock signal in a locking process of the delay-locked loop, and adjust the frequency-divided clock signal to make the frequency-divided clock signal have a second frequency when the delay-locked loop is locked in a standby state, wherein the second frequency is lower than the first frequency; and a primary path configured to output, when obtaining a target instruction, an output clock replica signal having a same phase as the output clock signal.