



US 20230230946A1

(19) **United States**(12) **Patent Application Publication**
KIM et al.(10) **Pub. No.: US 2023/0230946 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SEMICONDUCTOR PACKAGE**(71) Applicant: **Samsung Electronics Co., Ltd.**,
Suwon-si (KR)(72) Inventors: **Seongyo KIM**, Asan-si (KR);
UN-BYOUNG KANG, Hwaseong-Si
(KR); **MINSOO KIM**, Gumi-si (KR);
SANG-SICK PARK, Hwaseong-si
(KR); **Seungyeon JUNG**, Asan-si (KR)(21) Appl. No.: **17/939,127**(22) Filed: **Sep. 7, 2022**(30) **Foreign Application Priority Data**

Jan. 14, 2022 (KR) 10-2022-0006089

Publication Classification(51) **Int. Cl.**
H01L 23/00 (2006.01)
H01L 25/065 (2006.01)(52) **U.S. Cl.**
CPC **H01L 24/09** (2013.01); **H01L 24/16**
(2013.01); **H01L 24/17** (2013.01); **H01L 24/32**
(2013.01); **H01L 24/08** (2013.01); **H01L 24/73**
(2013.01); **H01L 25/0652** (2013.01); **H01L**
25/0657 (2013.01); **H01L 2224/81203**
(2013.01); **H01L 24/81** (2013.01); **H01L**
2924/3511 (2013.01); **H01L 2924/182**
(2013.01); **H01L 2225/06513** (2013.01); **H01L**
2225/06524 (2013.01); **H01L 2225/06527**
(2013.01); **H01L 2225/06544** (2013.01); **H01L**
2225/06589 (2013.01); **H01L 2224/16145**
(2013.01); **H01L 2224/16227** (2013.01); **H01L****2224/32145** (2013.01); **H01L 2224/32225**
(2013.01); **H01L 2224/1703** (2013.01); **H01L**
2224/17055 (2013.01); **H01L 2224/17104**
(2013.01); **H01L 2224/17179** (2013.01); **H01L**
2224/17132 (2013.01); **H01L 2224/16012**
(2013.01); **H01L 2224/16055** (2013.01); **H01L**
2224/16059 (2013.01); **H01L 2224/16104**
(2013.01); **H01L 2224/0801** (2013.01); **H01L**
2224/08056 (2013.01); **H01L 2224/08055**
(2013.01); **H01L 2224/0903** (2013.01); **H01L**
2224/09179 (2013.01); **H01L 2224/09132**
(2013.01); **H01L 2224/73204** (2013.01)

(57)

ABSTRACT

A semiconductor package comprises a first die having a central region and a peripheral region that surrounds the central region; a plurality of through electrodes that penetrate the first die; a plurality of first pads at a top surface of the first die and coupled to the through electrodes; a second die on the first die; a plurality of second pads at a bottom surface of the second die, the bottom surface of the second die facing the top surface of the first die; a plurality of connection terminals that connect the first pads to the second pads; and a dielectric layer that fills a space between the first die and the second die and surrounds the connection terminals. A first width of each of the first pads in the central region may be greater than a second width of each of the first pads in the peripheral region. Each of the connection terminals may include a convex portion at a lateral surface thereof, which protrudes beyond a lateral surface of a respective first pad and a lateral surface of a respective second pad. The convex portion may protrude in a direction away from a center of the first die. Protruding distances of the convex portions may increase in a direction from the center of the first die toward an outside of the first die.

