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(54) **DELAY CIRCUIT, PULSE GENERATION CIRCUIT, CHIP AND SERVER**

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(57) **ABSTRACT**

A delay circuit, a pulse generation circuit, a chip, and a server is disclosed. The delay circuit includes a control unit and at least two delay sub-circuits. Input ends of the delay sub-circuits are connected to each other. Output ends of the delay sub-circuits are connected to each other. The output end of each delay sub-circuit is connected to an input end of an adjacent delay sub-circuit through a switch unit. Each delay sub-circuit includes a delay unit and a switch unit. The delay unit is configured to perform delay processing on an input pulse signal. The switch unit is configured to control the delay sub-circuit to or not to be connected. The control unit is connected to all the switch units, and is configured to separately control a plurality of switch units to be turned on or off, so as to perform corresponding delay processing on the pulse signal.