US 20240213357A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0213357 A1**

IMAI et al. (43) **Pub. Date: Jun. 27, 2024**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

(71) Applicant: **Renesas Electronics Corporation**, Tokyo (JP)

(72) Inventors: **Tomohiro IMAI**, Tokyo (JP); **Yoshito NAKAZAWA**, Tokyo (JP)

(21) Appl. No.: **18/391,388**

(22) Filed: **Dec. 20, 2023**

(30) **Foreign Application Priority Data**

Dec. 23, 2022 (JP) 2022-206230

Publication Classification

(51) **Int. Cl.**

H01L 29/739 (2006.01)
H01L 29/06 (2006.01)
H01L 29/417 (2006.01)
H01L 29/66 (2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/7397*** (2013.01); ***H01L 29/0696*** (2013.01); ***H01L 29/41708*** (2013.01); ***H01L 29/66348*** (2013.01)

(57) **ABSTRACT**

Performance of a semiconductor device is enhanced. A floating region covers a bottom surface of a trench in an active cell. In addition, the floating region covers a bottom surface of a trench in an inactive cell so as to reach a semiconductor substrate between a pair of trenches in the inactive cell. A distance between a base region and the floating region in the inactive cell is smaller than a distance between the base region and the floating region in the active cell.