

(19) **United States**

(12) **Patent Application Publication**
Jefremow et al.

(10) **Pub. No.: US 2022/0399886 A1**

(43) **Pub. Date: Dec. 15, 2022**

(54) **ELECTRONIC DEVICE**

(71) Applicant: **Infineon Technologies AG**, Neubiberg (DE)

(72) Inventors: **Mihail Jefremow**, Augsburg (DE);
David Zipperstein, Muenchen (DE);
Juergen Schaefer, Oberhaching (DE);
Holger Dienst, Feldkirchen (DE);
Markus Bichl, Feldkirchen-Westerham (DE);
Ralph Mueller-Eschenbach, Muenchen (DE);
Arndt Voigtlaender, Ottobrunn (DE)

(21) Appl. No.: **17/836,181**

(22) Filed: **Jun. 9, 2022**

(30) **Foreign Application Priority Data**

Jun. 10, 2021 (DE) 10 2021 115 021.3

Publication Classification

(51) **Int. Cl.**
H03K 17/56 (2006.01)
H03M 3/00 (2006.01)

(52) **U.S. Cl.**

CPC **H03K 17/56** (2013.01); **H03M 3/50** (2013.01); **H03M 3/458** (2013.01); **G01S 7/03** (2013.01)

(57) **ABSTRACT**

According to an example, an electronic device includes a component, a supply line providing a supply voltage, a transistor with a control input, a linear first control loop, and a non-linear second control loop. The transistor outputs an output voltage to the component depending on a signal applied to the control input. The linear first control loop includes an ADC to convert an analog output voltage level into a digital measurement signal, a controller to generate a digital control signal for the transistor depending on the digital measurement signal, and a DAC to convert the digital control signal into a first analog control signal. The non-linear second control loop is configured to generate a second analog control signal depending on the analog output voltage level. The second analog control signal is superimposed with the first analog control signal and the combined control signals are fed to the control input of the transistor.

