US 20240213984A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0213984 A1**

KISHINAMI et al. (43) **Pub. Date: Jun. 27, 2024**

(54) **SEMICONDUCTOR INTEGRATED CIRCUIT, INTERFACE DEVICE, AND MEMORY SYSTEM**

(71) Applicant: **Kioxia Corporation**, Tokyo (JP)

(72) Inventors: **Keisuke KISHINAMI**, Kamakura Kanagawa (JP); **Koji OOIWA**, Yokohama Kanagawa (JP)

(21) Appl. No.: **18/460,489**

(22) Filed: **Sep. 1, 2023**

(30) **Foreign Application Priority Data**

Dec. 21, 2022 (JP) 2022-204702

Publication Classification

(51) **Int. Cl.**

H03K 19/0185	(2006.01)
G11C 16/04	(2006.01)
G11C 16/06	(2006.01)
H03K 19/00	(2006.01)

(52) **U.S. Cl.**

CPC . ***H03K 19/018514*** (2013.01); ***G11C 16/0483*** (2013.01); ***G11C 16/06*** (2013.01); ***H03K 19/0013*** (2013.01)

(57) **ABSTRACT**

A semiconductor integrated circuit includes a first circuit generating a differential third signal based on a first signal, a second circuit generating a second signal from a third signal, wherein the second circuit includes a first signal line and a second signal line for transmitting the third signal from the first circuit to the second circuit, and a third circuit including a first terminal connected to the first signal line and a second terminal connected to the second signal line. The third circuit includes first and second electrical paths with different electrical resistances, that are connected in parallel between the first terminal and the second terminal, and is controlled to switch between the first and second electrical paths.