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THEREOF**

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ABSTRACT

The present disclosure is directed to a semiconductor device. The semiconductor device includes a multi-layer interconnect structure disposed over a substrate, a dielectric layer disposed over the multi-layer interconnect structure, and a metal-insulator-metal (MIM) capacitor disposed over the dielectric layer. The MIM capacitor includes a bottom electrode disposed on a top surface of the dielectric layer, a top electrode disposed above the bottom electrode, and an insulating layer interposed between the bottom electrode and the top electrode. The bottom electrode has a slanted sidewall with respect to the top surface of the dielectric layer. The top electrode has a vertical sidewall with respect to the top surface of the dielectric layer. The insulating layer covers the slanted sidewall of the bottom electrode.

