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(54) **THREE-DIMENSIONAL MEMORY DEVICE WITH REDUCED NEIGHBORING WORD LINE INTERFERENCE AND METHODS OF FORMING THE SAME**

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(57) **ABSTRACT**

A memory device includes an alternating stack of insulating layers and electrically conductive layers, a memory opening vertically extending through the alternating stack, a memory opening fill structure located in the memory opening and containing a memory film and a vertical semiconductor channel; and a neighboring electrically conductive layer interference reduction feature provided for a first subset of the electrically conductive layers, such that a second subset of the electrically conductive layers lacks the neighboring electrically conductive layer interference reduction feature.