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(54) **SILICON-OXIDE-NITRIDE-OXIDE-SILICON MEMORY CELL**

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(57) **ABSTRACT**

A silicon-oxide-nitride-oxide-silicon (SONOS) memory cell includes a memory gate disposed on a substrate, a dielectric layer and two charge trapping layers, wherein the dielectric layer is disposed between the substrate and the memory gate, and the two charge trapping layers are disposed at two opposite sides of the memory gate, wherein each of the charge trapping layers comprises an L-shape cross-sectional profile, and two selective gates disposed on the substrate, thereby constituting a two bit memory cell, wherein a top surface of each selective gate is higher than a top surface of the memory gate.