



US 20220393673A1

(19) **United States**(12) **Patent Application Publication**
YOON(10) **Pub. No.: US 2022/0393673 A1**(43) **Pub. Date: Dec. 8, 2022**(54) **DIGITAL PHASE INTERPOLATOR, CLOCK
SIGNAL GENERATOR, AND VOLATILE
MEMORY DEVICE INCLUDING THE
CLOCK SIGNAL GENERATOR**(52) **U.S. Cl.**
CPC *H03K 5/133* (2013.01); *G11C 11/4076*
(2013.01); *G11C 11/4093* (2013.01); *H03K*
2005/00052 (2013.01)(71) Applicant: **SAMSUNG ELECTRONICS CO.,
LTD.**, Suwon-si (KR)(57) **ABSTRACT**(72) Inventor: **Junsub YOON**, Seoul (KR)(21) Appl. No.: **17/575,020**(22) Filed: **Jan. 13, 2022**(30) **Foreign Application Priority Data**

Jun. 3, 2021 (KR) 10-2021-0072399

Publication Classification(51) **Int. Cl.**
H03K 5/133 (2014.01)
G11C 11/4076 (2006.01)
G11C 11/4093 (2006.01)
H03K 5/00 (2006.01)

Provided are a digital phase interpolator, a clock signal generator, and a volatile memory device including the clock signal generator. The clock signal generator includes an internal signal generator configured to generate a first internal signal and a second internal signal, which mutually have a phase difference, based on an external clock signal, a first phase interpolator configured to interpolate the first internal signal with the second internal signal in response to a first control signal and generate a first interpolation signal, a second phase interpolator configured to interpolate the first internal signal with the second internal signal in response to a second control signal and generate a second interpolation signal, and a selector configured to select any one of the first interpolation signal and the second interpolation signal in response to a selection signal and output the selected interpolation signal as an internal clock signal.

