

(19) **United States**

(12) **Patent Application Publication**
ARRAZAT et al.

(10) **Pub. No.: US 2024/0215233 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **ELECTRONIC CIRCUIT COMPRISING A TRANSISTOR CELL**

Publication Classification

(71) Applicant: **STMicroelectronics International N.V.**, Geneva (CH)

(51) **Int. Cl.**
H10B 41/35 (2006.01)
H01L 21/762 (2006.01)
H10B 41/10 (2006.01)

(72) Inventors: **Brice ARRAZAT**, Bouc-bel-air (FR);
Christian RIVERO, Rousset (FR);
Julien DELALLEAU, Rousset (FR);
Joel METZ, Gardanne (FR)

(52) **U.S. Cl.**
CPC **H10B 41/35** (2023.02); **H01L 21/76224** (2013.01); **H10B 41/10** (2023.02)

(73) Assignee: **STMicroelectronics International N.V.**, Geneva (CH)

(57) **ABSTRACT**

(21) Appl. No.: **18/540,482**

An electronic circuit includes a transistor cell with multiple transistors arranged inside and on top of a semiconductor substrate. Each transistor has an active area. First insulating regions are at least partially located around the transistors and extend down to a first depth in the semiconductor substrate. Second insulating regions are positioned to insulate the active areas the transistors from one another. The second insulating regions extend down to a second depth in the semiconductor substrate, the second depth being greater than the first depth.

(22) Filed: **Dec. 14, 2023**

(30) **Foreign Application Priority Data**

Dec. 21, 2022 (FR) 2214170

