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(54) **NOISE DISTURBANCE REJECTION FOR POWER SUPPLY**

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(57) **ABSTRACT**

Apparatus and associated methods relate to a power supply noise disturbance rejection circuit (NDRC) having a first circuit reference potential (CRP**1**), a second circuit reference potential (CRP**2**), and a galvanic link conductively connecting CRP**1** and CRP**2** and providing a non-zero resistance return path for at least one current mode signal (CMS). In an illustrative example, a power supply monitor circuit (PSMC) may be referenced to CRP**1** and a control circuit to CRP**2**. The PMSC may, for example, generate a voltage mode signal (VMS) relative to CRP**1** and representing an output parameter of a power supply circuit (PSC), and convert the VMS into a first CMS (CMS**1**). The control circuit may, for example, generate a control signal for the PSC from CMS**1**. Various embodiments may advantageously attenuate a noise margin of a CMS presented at the control circuit by a factor of at least 10 relative to an equivalent VMS.