



US 20220416775A1

(19) **United States**(12) **Patent Application Publication**  
**Colles et al.**(10) **Pub. No.: US 2022/0416775 A1**(43) **Pub. Date: Dec. 29, 2022**(54) **NOISE-TOLERANT DELAY CIRCUIT****Publication Classification**(71) Applicant: **Silanna Asia Pte Ltd**, Singapore (SG)(51) **Int. Cl.**  
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CPC ... **H03K 5/134** (2014.07); **H03K 2005/00202** (2013.01)(73) Assignee: **Silanna Asia Pte Ltd**, Singapore (SG)(21) Appl. No.: **17/823,019**(22) Filed: **Aug. 29, 2022****Related U.S. Application Data**

(63) Continuation of application No. 17/454,207, filed on Nov. 9, 2021, now Pat. No. 11,451,220.

(60) Provisional application No. 63/198,931, filed on Nov. 23, 2020.

(57) **ABSTRACT**

In a delay circuit, first and second sets of transistors are connected in series between a supply voltage and a ground. The first and second sets of transistors both include a current source transistor, a cascode transistor, and a control transistor. The first set of transistors generates a current that charges a capacitor to generate a ramp signal with a positive slope. A first bias transistor may cause the ramp signal to be biased to ground upon activating the first set of transistors. The second set of transistors generates a current that discharges the capacitor to generate the ramp signal with a negative slope. A second bias transistor may cause the ramp signal to be biased to the supply voltage upon activating the second set of transistors. The delay circuit transitions the state of the output signal based on a voltage level of the ramp signal.

