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(54) **PHASE-LOCKED LOOP REFERENCE CLOCK MANAGEMENT**

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(57) **ABSTRACT**

A device includes a phase-locked loop (PLL) having a reference input. The device has a storage element and a reference clock generator having an interface clock input, a reference clock output, and a programmable clock divider. The reference clock generator is coupled to the storage element. The reference clock output is coupled to the reference input. The reference clock generator is configured to change a divide ratio for the programmable clock divider based on a value in the storage element such that a frequency of the reference clock output remains unchanged when a frequency of the interface clock input changes.