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MURAMATSU(10) **Pub. No.: US 2023/0230774 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **MULTILAYER CERAMIC CAPACITOR****H01G 4/012** (2006.01)**H01G 4/12** (2006.01)(71) Applicant: **Murata Manufacturing Co., Ltd.**,
Nagaokakyo-shi (JP)(52) **U.S. CL.**CPC **H01G 4/30** (2013.01); **H01G 2/02**
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4/1218 (2013.01)(72) Inventor: **Satoshi MURAMATSU**,
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(57)

ABSTRACT**Related U.S. Application Data**(63) Continuation of application No. 17/665,758, filed on
Feb. 7, 2022, now Pat. No. 11,646,162, which is a
continuation of application No. 16/747,632, filed on
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A multilayer ceramic capacitor includes a stacked body and external electrodes. The stacked body includes stacked dielectric layers and internal electrodes. The external electrodes are disposed on lateral surfaces of the stacked body and are connected to the internal electrodes. The dielectric layers include outer layer portions and an effective layer portion. Each outer layer portion is adjacent to a corresponding main surface of the stacked body. Each outer layer portion is a dielectric layer located between a corresponding main surface and an internal electrode closest to the main surface. A ratio of a dimension of the effective layer portion in a stacking direction to a dimension of the stacked body in the stacking direction is not less than about 53% and not more than about 83%.

