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ASANO et al.(10) **Pub. No.: US 2024/0223174 A1**(43) **Pub. Date: Jul. 4, 2024**(54) **LOW POWER COMPARATOR**(71) Applicant: **Renesas Design (UK) Limited**, Bourne  
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**ABSTRACT**

A comparator is presented. The comparator includes an input port for receiving an input voltage; an output port for providing an output voltage; a resistive divider, first and second transistors, and a differential amplifier. The resistive divider has a first node for providing a first voltage and a second node for providing a second voltage. The first transistor has a control terminal coupled to the first node, a first terminal coupled to the input port, and a second terminal coupled to a common node. The second transistor has a control terminal coupled to the second node, a first terminal coupled to the input port, and a second terminal coupled to the common node. The differential amplifier has a first input coupled to the first terminal of the first transistor, a second input coupled to the first terminal of the second transistor and an output coupled to the output port.

