US 20240235561A9

(19) **United States**

(12) **Patent Application Publication**

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(10) **Pub. No.: US 2024/0235561 A9**

(48) **Pub. Date: Jul. 11, 2024**

CORRECTED PUBLICATION

(54) **SAMPLING FRACTIONAL-N PHASE-LOCKED LOOP WITH FEEDBACK SPUR COMPENSATION**

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(21) Appl. No.: **17/970,477**

(22) Filed: **Oct. 20, 2022**

Prior Publication Data

(15) Correction of US 2024/0137029 A1 Apr. 25, 2024
See (22) Filed

(65) US 2024/0137029 A1 Apr. 25, 2024

Publication Classification

(51) **Int. Cl.**
H03L 7/099 (2006.01)
H03L 7/093 (2006.01)

(52) **U.S. Cl.**
CPC ***H03L 7/0992*** (2013.01); ***H03L 7/093*** (2013.01); *H03L 2207/50* (2013.01)

(57) **ABSTRACT**

Embodiments herein relate to a sampling phase-locked loop (PLL) with a compensation circuit for reducing ripples due to the use of a fractional N divider. The compensation circuit includes a ripple amplifier and a ripple divider. The ripple amplifier receives an output voltage, Vmain, of a main sampling circuit of the PLL and amplifies its alternating current (AC) components. The amplified output voltage is provided to a ripple integrator which samples the minimum and maximum values to provide inputs to an operational amplifier (op amp). An output of the op amp is fed back to a digital-to-analog converter (DAC), which provides a corresponding compensation voltage, Vcomp. Vcomp is added to Vmain to provide a final output control voltage, Vctrl, to control a voltage-controlled oscillator (VCO) of the PLL.