



US 20230230975A1

(19) **United States**(12) **Patent Application Publication**  
Nandakumar et al.(10) **Pub. No.: US 2023/0230975 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SEMICONDUCTOR DEVICE WITH  
DIFFUSION SUPPRESSION AND LDD  
IMPLANTS AND AN EMBEDDED NON-LDD  
SEMICONDUCTOR DEVICE***H01L 29/78* (2006.01)*H01L 29/66* (2006.01)*H01L 21/265* (2006.01)*H01L 21/266* (2006.01)(71) Applicant: **Texas Instruments Incorporated,**  
Dallas, TX (US)(52) **U.S. Cl.**CPC .... *H01L 21/823418* (2013.01); *H01L 27/088*  
(2013.01); *H01L 29/7833* (2013.01); *H01L**29/66492* (2013.01); *H01L 21/26513*(2013.01); *H01L 21/26586* (2013.01); *H01L**21/266* (2013.01)(72) Inventors: **Mahalingam Nandakumar,**  
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**Hornung,** Richardson, TX (US)(21) Appl. No.: **18/188,812**(22) Filed: **Mar. 23, 2023****Related U.S. Application Data**(62) Division of application No. 17/117,421, filed on Dec.  
10, 2020, now Pat. No. 11,616,058.**Publication Classification**(51) **Int. Cl.***H01L 21/8234* (2006.01)*H01L 27/088* (2006.01)

(57)

**ABSTRACT**

The present disclosure provides a method for forming a semiconductor device containing MOS transistors both with and without source/drain extension regions in a semiconductor substrate having a semiconductor material on either side of a gate structure including a gate electrode on a gate dielectric formed in a semiconductor material. In devices with source/drain extensions, a diffusion suppression species of one or more of indium, carbon and a halogen are used. The diffusion suppression implant can be selectively provided only to the semiconductor devices with drain extensions while devices without drain extensions remain diffusion suppression implant free.

