

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0215164 A1 YAMAMURA

(43) **Pub. Date:**

Jun. 27, 2024

(54) WIRING BOARD

(71) Applicant: SHINKO ELECTRIC INDUSTRIES CO., LTD., Nagano (JP)

Inventor: Kyota YAMAMURA, Nagano (JP)

Appl. No.: 18/540,013

(22)Filed: Dec. 14, 2023

(30)Foreign Application Priority Data

Dec. 27, 2022 (JP) 2022-209741

Publication Classification

(51)	Int. Cl.	
	H05K 1/11	(2006.01)
	H01L 23/498	(2006.01)
	H05K 3/10	(2006.01)
	H05K 3/18	(2006.01)
	H05K 3/46	(2006.01)

(52) U.S. Cl.

CPC H05K 1/113 (2013.01); H01L 23/49822 (2013.01); H05K 3/108 (2013.01); H05K 3/18 (2013.01); H05K 3/4644 (2013.01); H05K 2201/09481 (2013.01); H05K 2201/096 (2013.01); H05K 2203/0723 (2013.01)

(57)

A wiring board includes a first interconnect layer, an insulating layer covering the first interconnect layer, a via interconnect penetrating the insulating layer, and a second interconnect layer provided on an upper surface of the insulating layer and electrically connected to the first interconnect layer through the via interconnect. The via interconnect includes a first seed layer that covers an inner wall surface of a via hole penetrating the insulating layer, and an upper surface of the first interconnect layer exposed inside the via hole, and a first electrolytic plating layer provided on the first seed layer. The second interconnect layer includes a second seed layer provided on the upper surface of the insulating layer and on an upper surface of the first electrolytic plating layer, and a second electrolytic plating layer provided on the second seed layer.

