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BAHARMAST et al.(10) **Pub. No.: US 2024/0178806 A1**(43) **Pub. Date: May 30, 2024**(54) **COMPARATOR WITH REDUCED POWER CONSUMPTION**

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(71) Applicant: **NORDIC SEMICONDUCTOR ASA,**
Trondheim (NO)(72) Inventors: **Aram BAHARMAST,** Oulu (FI);
Jarmo VÄÄNÄNEN, Oulu (FI)(21) Appl. No.: **18/516,003**(22) Filed: **Nov. 21, 2023**(30) **Foreign Application Priority Data**

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(2013.01); **H03F 3/4565** (2013.01); **H03F**(57) **ABSTRACT**

According to an aspect, there is provided a comparator comprising input terminals, first, second and third biasing current sources configured to output first, second and third biasing currents, an input circuit driven by the first biasing current source and comprising an amplification circuit and a load circuit configured to provide positive feedback for the amplification circuit, first and second current mirroring circuits for forming, with the input circuit, first and second current mirrors producing first and second current mode signals, first and second current-controlled driver circuits configured to be controlled by the second and third biasing currents, respectively, and the first and second current mode signals, respectively, a latch circuit comprising first and second cross-coupled complementary metal-oxide semiconductor transistors acting as a latch having substantially rail-to-rail output voltage swing and being driven, respectively, by the first and second current-controlled driver circuits and an output circuit implementing a current starved inverter.

