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(54) **CLOCK ADJUSTMENT CIRCUIT WITH BIAS SCHEME**

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(57) **ABSTRACT**

Some embodiments include apparatuses comprising a first node; a second node; a first transistor and a second transistor, the first and second transistors including a common gate coupled to the node and a common terminal coupled to the second node; first additional transistors coupled in parallel with each other between a terminal of the first transistor and a first supply node, the first additional transistors including gates; and second additional transistors coupled in parallel with each other between a terminal of the second transistor and a second supply node, the second additional transistors including gates.