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(54) **VOLTAGE ADJUST CIRCUIT AND OPERATION METHOD THEREOF**

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(57) **ABSTRACT**

The disclosure provides a voltage adjust circuit. The voltage adjust circuit includes a buffer circuit, a bias circuit, a level shifter and a cross voltage limit circuit. The buffer circuit includes a plurality of pull-up transistors and a plurality of pull-down transistors. The pull-up transistors coupled in series between an output terminal of the circuit and a high voltage system terminal. The pull-down transistors coupled in series between the output terminal and a low voltage system terminal. The cross voltage limit circuit is configured to limit transient and static bias voltages across two terminals of the pull-up transistors or the pull-down transistors.