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(54) **ITERATIVE ERROR CORRECTION IN MEMORY SYSTEMS**

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(57) **ABSTRACT**

A system and method for detecting and correcting memory errors in CXL components is presented. The method includes receiving, into a decoder, a memory transfer block (MTB), wherein the MTB comprises data and parity information, wherein the MTB is arranged in a first dimension and a second dimension. An error checking and a correction function on the MTB is performed using a binary hamming code logic within the decoder in the first dimension. An error checking and a correction function on the MTB is performed using a non-binary hamming code logic within the decoder in the second dimension. Further, the binary hamming code logic and the non-binary hamming code logic perform the error checking on the MTB simultaneously.