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**GHANI et al.**(10) **Pub. No.: US 2023/0232605 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **FIN CUT AND FIN TRIM ISOLATION FOR  
ADVANCED INTEGRATED CIRCUIT  
STRUCTURE FABRICATION**(60) Provisional application No. 62/593,149, filed on Nov.  
30, 2017.**Publication Classification**(71) Applicant: **Intel Corporation**, Santa Clara, CA  
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**H01L 27/06** (2006.01)(72) Inventors: **Tahir GHANI**, Portland, OR (US);  
**Byron HO**, Hillsboro, OR (US); **Curtis  
W. WARD**, Hillsboro, OR (US);  
**Michael L. HATTENDORF**, Portland,  
OR (US); **Christopher P. AUTH**,  
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**27/0924** (2013.01); **H01L 27/0688** (2013.01)(21) Appl. No.: **18/124,936**(57) **ABSTRACT**(22) Filed: **Mar. 22, 2023****Related U.S. Application Data**(60) Continuation of application No. 17/233,063, filed on  
Apr. 16, 2021, now Pat. No. 11,646,359, which is a  
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Sep. 20, 2019, now Pat. No. 10,777,656, which is a  
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29, 2017, now Pat. No. 10,460,993.

Embodiments of the disclosure are in the field of advanced integrated circuit structure fabrication and, in particular, 10 nanometer node and smaller integrated circuit structure fabrication and the resulting structures. In an example, an integrated circuit structure includes a fin. A first isolation structure separates a first end of a first portion of the fin from a first end of a second portion of the fin, the first end of the first portion of the fin having a depth. A gate structure is over the top of and laterally adjacent to the sidewalls of a region of the first portion of the fin. A second isolation structure is over a second end of a first portion of the fin, the second end of the first portion of the fin having a depth different than the depth of the first end of the first portion of the fin.

