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(54) **INTEGRATED CIRCUIT YIELD IMPROVEMENT**

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(57) **ABSTRACT**

Circuits and methods for improving IC yield during automated test equipment (ATE) calibration of circuit designs which require I_{DD} calibration and use a closed feedback bias circuit, such as amplifier circuits. The circuit designs include bias branch/active circuit architectures where the active circuit includes one or more active devices. An example first embodiment uses an on-chip calibration switch between the on-chip grounds of a bias network and an active circuit comprising an amplifier. During calibration of the active circuit by the ATE, the calibration switch is closed, and after completion of calibration, the calibration switch is opened. An example second embodiment utilizes an active on-chip feedback loop calibration circuit to equalize voltages between the on-chip grounds of a bias network and an active circuit comprising an amplifier during calibration of the active circuit. Both embodiments mitigate or overcome miscalibration of active circuit current settings resulting from ATE test probe resistance.