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(54) **ASYMMETRIC NAND GATE CIRCUIT, CLOCK GATING CELL AND INTEGRATED CIRCUIT INCLUDING THE SAME**

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(57) **ABSTRACT**

A clock gating cell is provided. The clock gating cell includes: an inverter circuit configured to generate an inverted clock signal by inverting a clock signal; a first control circuit configured to receive the inverted clock signal, an enable signal, and a scan enable signal, and output a first internal signal at a first node; a second control circuit configured to receive the first internal signal, the clock signal, the enable signal, and the scan enable signal, and output a second internal signal at a second node; and an output driver configured to receive the second internal signal, and output an output clock signal to an output node and a third internal signal to a third node. The first control circuit and the second control circuit are configured to receive the third internal signal at the third node.