



US 20230231036A1

(19) **United States**
(12) **Patent Application Publication** (10) **Pub. No.: US 2023/0231036 A1**
GUO et al. (43) **Pub. Date: Jul. 20, 2023**

(54) **MANUFACTURING METHOD OF SEMICONDUCTOR STRUCTURE AND SEMICONDUCTOR STRUCTURE**

H01L 21/8234 (2006.01)

(71) Applicant: **CHANGXIN MEMORY TECHNOLOGIES, INC.**, Hefei City (CN)

(52) **U.S. Cl.**
CPC ... *H01L 29/66742* (2013.01); *H01L 21/823412* (2013.01); *H01L 21/823481* (2013.01); *H01L 29/78696* (2013.01)

(72) Inventors: **Shuai GUO**, Hefei City (CN);
Mingguang Zuo, Hefei City (CN); **Shijie Bai**, Hefei City (CN)

(57) **ABSTRACT**

(21) Appl. No.: **17/661,359**

(22) Filed: **Apr. 29, 2022**

Related U.S. Application Data

(63) Continuation of application No. PCT/CN2022/078671, filed on Mar. 1, 2022.

(30) **Foreign Application Priority Data**

Jan. 17, 2022 (CN) 202210049426.0

Publication Classification

(51) **Int. Cl.**
H01L 29/66 (2006.01)
H01L 29/786 (2006.01)

The present disclosure provides a semiconductor structure and a manufacturing method thereof. The manufacturing method includes: depositing a thin-film stacked structure on a substrate; forming a first hole in the thin-film stacked structure; growing an epitaxial silicon pillar in the first hole; etching the thin-film stacked structure and the epitaxial silicon pillar along a first direction to form a first trench, the first trench passing through a center of the epitaxial silicon pillar and dividing the epitaxial silicon pillar into a first half pillar and a second half pillar; forming a first isolation layer; forming a first channel region of a first doping type, and forming a second channel region of a second doping type; and forming a gate dielectric layer and a gate conductive layer on a surface of each of the first channel region and the second channel region.

