US 20240179886A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0179886 A1**

HARADA et al. (43) **Pub. Date: May 30, 2024**

(54) **MEMORY-ELEMENT-INCLUDING SEMICONDUCTOR DEVICE**

(71) Applicant: **Unisantis Electronics Singapore Pte. Ltd.**, Singapore (SG)

(72) Inventors: **Nozomu HARADA**, Tokyo (JP); **Masakazu KAKUMU**, Tokyo (JP); **Koji SAKUI**, Tokyo (JP)

(21) Appl. No.: **18/517,572**

(22) Filed: **Nov. 22, 2023**

(30) **Foreign Application Priority Data**

Nov. 28, 2022 (WO) PCT/JP2022/043781
May 26, 2023 (WO) PCT/JP2023/019722

Publication Classification

(51) **Int. Cl.**
H10B 12/00 (2006.01)
G11C 11/405 (2006.01)
G11C 11/4096 (2006.01)

(52) **U.S. Cl.**
CPC ***H10B 12/20*** (2023.02); ***G11C 11/405*** (2013.01); ***G11C 11/4096*** (2013.01)

(57) **ABSTRACT**

In a memory cell including a first gate insulating layer **5** and a first gate conductor layer **6** surrounding a pillar-shaped P layer **3***a* standing on a P layer substrate **1**, a second gate insulating layer **9** in contact with a P layer **3***b* in contact with an upper surface of the P layer **3***a*, and N^+ layers **11***a* and **11***b* at both ends of the P layer **3***b* and a MOS transistor including a pillar-shaped P layer **3***aa* standing on a P layer substrate **1***a* connecting to the same P layer substrate **1**, a third gate insulating layer **9***a* in contact with the P layer **3***aa*, a third gate conductor layer **10***a*, and N^+ layers **11***aa* and **11***ba* at both ends of a P layer **3***ba*, bottom portions of the P layer **3***b* and the P layer **3***ba* are located at substantially the same position.