

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2024/0213225 A1 SEIDEMANN et al.

Jun. 27, 2024 (43) **Pub. Date:**

(54) PACKAGE STACKING USING CHIP TO WAFER BONDING

(71) Applicant: Intel Corporation, Santa Clara, CA

(72) Inventors: Georg SEIDEMANN, Landshut (DE); Klaus REINGRUBER, Langquaid (DE); Christian GEISSLER, Teugn (DE); Sven ALBERS, Regensburg (DE); Andreas WOLTER, Regensburg (DE); Marc DITTES, Regensburg (DE); Richard PATTEN, Langquaid

(21) Appl. No.: 18/601,774

(22) Filed: Mar. 11, 2024

(DE)

Related U.S. Application Data

(63) Continuation of application No. 17/553,679, filed on Dec. 16, 2021, now Pat. No. 11,955,462, which is a continuation of application No. 15/774,906, filed on May 9, 2018, now Pat. No. 11,239,199, filed as application No. PCT/US2015/000394 on Dec. 26, 2015.

Publication Classification

(51)	Int. Cl.	
	H01L 25/065	(2006.01)
	H01L 21/48	(2006.01)
	H01L 21/56	(2006.01)
	H01L 23/00	(2006.01)
	H01L 23/31	(2006.01)
	H01L 23/48	(2006.01)
	H01L 23/498	(2006.01)

H01L 23/538 (2006.01)H01L 25/00 (2006.01)

U.S. Cl. CPC H01L 25/0657 (2013.01); H01L 21/486 (2013.01); H01L 23/3107 (2013.01); H01L 23/48 (2013.01); H01L 23/49827 (2013.01); H01L 23/5384 (2013.01); H01L 24/19 (2013.01); H01L 24/20 (2013.01); H01L 24/25 (2013.01); H01L 24/81 (2013.01); H01L 24/96 (2013.01); H01L 24/97 (2013.01); H01L 25/0652 (2013.01); H01L 25/50 (2013.01); H01L 21/561 (2013.01); H01L 21/568 (2013.01); H01L 23/3135 (2013.01); H01L 23/49816 (2013.01); H01L 23/5389 (2013.01); H01L 2224/04105 (2013.01); H01L 2224/12105 (2013.01); H01L 2224/16235 (2013.01); H01L 2224/16238 (2013.01); H01L 2224/2518 (2013.01); H01L 2224/73259 (2013.01); H01L 2224/81005 (2013.01); H01L 2224/92224 (2013.01); H01L 2224/97 (2013.01); H01L 2225/06524 (2013.01); H01L 2225/06541 (2013.01); H01L 2225/06548 (2013.01); H01L 2924/15311 (2013.01); H01L

2924/18161 (2013.01); H01L 2924/3511

(2013.01)

(57)ABSTRACT

Embodiments are generally directed to package stacking using chip to wafer bonding. An embodiment of a device includes a first stacked layer including one or more semiconductor dies, components or both, the first stacked layer further including a first dielectric layer, the first stacked layer being thinned to a first thickness; and a second stacked layer of one or more semiconductor dies, components, or both, the second stacked layer further including a second dielectric layer, the second stacked layer being fabricated on the first stacked layer.

