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(54) **MEMORY DEVICE AND METHOD OF FORMING THE SAME**

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(57) **ABSTRACT**

A memory device includes a semiconductor layer and a stack structure over the semiconductor layer. The stack structure includes a cell array region and a staircase structure region. The cell array region includes multiple vertical levels of stacked transistor-magnetic tunnel junction (TMTJ) elements and a plurality of channel structures vertically extending through the stack structure. At least one channel structure includes a vertical core, a vertical magnetic reference layer, and a vertical tunnel barrier layer, which are shared by a set of magnetic tunnel junction (MTJ) elements associated with the at least one channel structure. The set of MTJ elements are located at different vertical levels of the stack structure.