

# (19) United States

## (12) Patent Application Publication (10) Pub. No.: US 2024/0237358 A1 Fantini et al.

Jul. 11, 2024 (43) Pub. Date:

### (54) IMPROVED VERTICAL 3D MEMORY DEVICE AND ACCESSING METHOD

(71) Applicant: Micron Technology, Inc., Boise, ID

(72) Inventors: **Paolo Fantini**, Vimercate (MB) (IT);

Corrado Villa, Sovico (MB) (IT); Stefan Frederik Schippers, Peschiera del Garda (VR) (IT); Efrem

Bolandrina, Fiorano al Serio (BG) (IT)

(21) Appl. No.: 18/407,074

(22) Filed: Jan. 8, 2024

#### Related U.S. Application Data

(62) Division of application No. 16/976,411, filed on Aug. 27, 2020, now Pat. No. 11,877,457, filed as application No. PCT/IB2020/020028 on May 25, 2020.

#### **Publication Classification**

(51) Int. Cl. H10B 63/00 (2006.01)G11C 13/00 (2006.01)

(52) U.S. Cl. H10B 63/34 (2023.02); G11C 13/0004 CPC ...... (2013.01); G11C 13/003 (2013.01); H10B **63/845** (2023.02); *G11C* 2213/71 (2013.01); *G11C* 2213/79 (2013.01)

(57)ABSTRACT

The present disclosure provides a memory device and accessing/de-selecting methods thereof. The memory device comprises a memory layer including a vertical three-dimensional (3D) memory array of memory cells formed therein, wherein a memory cell is accessed through a word line and a digit line orthogonal to each other, and the digit line is in a form of conductive pillar extending vertically; a pillar selection layer formed under the memory layer and having thin film transistors (TFTs) formed therein for accessing memory cells; and a peripheral circuit layer formed under the pillar selection layer and having a sense amplifier and a decoding circuitry for word lines and bit lines, wherein a TFT is configured for each pillar.



