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(10) **Pub. No.: US 2023/0232625 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SEMICONDUCTOR DIE AND METHOD FOR FORMING THE SAME**(52) **U.S. Cl.**CPC .. *H01L 27/11582* (2013.01); *H01L 27/11556* (2013.01)(71) Applicant: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**, Hsinchu (TW)

(57)

**ABSTRACT**(72) Inventors: **Meng-Han LIN**, Hsinchu City (TW); **Chia-En HUANG**, Hsinchu County (TW)(73) Assignee: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**, Hsinchu (TW)(21) Appl. No.: **17/580,500**(22) Filed: **Jan. 20, 2022****Publication Classification**(51) **Int. Cl.***H01L 27/11582* (2006.01)*H01L 27/11556* (2006.01)

The method includes forming a multi-layered stack having insulating layers and spacer layers alternately stacked on top of each other in a vertical direction over a substrate in a chip area having a first memory region and a second memory region; forming a first mask layer covering the second memory region, while leaving the first memory region partially exposed; etching the multi-layered stack to form first trenches in the first memory region; forming first gate layers, a first memory layer, and a first channel layer; removing the first mask layer; forming a second mask layer covering the first memory region, while leaving the second memory region partially exposed; etching the multi-layered stack to form second trenches; forming second gate layers, a second memory layer, and a second channel layer in the second trenches.

