



US 20230230937A1

(19) **United States**(12) **Patent Application Publication**
Jeon et al.(10) **Pub. No.: US 2023/0230937 A1**(43) **Pub. Date: Jul. 20, 2023**(54) **SEMICONDUCTOR DEVICE AND
ELECTRONIC SYSTEM INCLUDING THE
SAME****H01L 27/11529** (2006.01)**H01L 27/11582** (2006.01)**H01L 27/11573** (2006.01)(71) Applicant: **Samsung Electronics Co., Ltd.,**
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(2013.01); **H01L 23/5329** (2013.01); **H01L**
27/11556 (2013.01); **H01L 27/11529**
(2013.01); **H01L 27/11582** (2013.01); **H01L**
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(57)

ABSTRACT

Disclosed are a three-dimensional semiconductor memory device and an electronic system including the same. A semiconductor device includes a substrate, a cell array structure including a plurality of electrodes stacked on the substrate, a vertical channel structure that penetrates the cell array structure and is connected to the substrate, a conductive pad in an upper portion of the vertical channel structure, an interlayer insulating layer on the cell array structure, a bit line on the cell array structure, a bit line contact electrically connecting the bit line to the conductive pad, and a first stress release layer between the cell array structure and the bit line on a top surface of the interlayer insulating layer. The first stress release layer includes organosilicon polymer, and a carbon concentration of the first stress release layer is higher than that of the interlayer insulating layer.

(21) Appl. No.: **17/930,820**(22) Filed: **Sep. 9, 2022**(30) **Foreign Application Priority Data**

Jan. 17, 2022 (KR) 10-2022-0006435

Publication Classification(51) **Int. Cl.****H01L 23/00** (2006.01)**H01L 23/535** (2006.01)**H01L 23/532** (2006.01)**H01L 27/11556** (2006.01)