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(54) **SAR ADC**

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(57) **ABSTRACT**

A SAR ADC (50) is disclosed. It comprises a differential input port having a first input (V_{inP}) configured to receive a first input voltage and a second input (V_{inN}) configured to receive a second input voltage, of opposite polarity compared with first input voltage. Furthermore, it comprises a (300) having a first sub circuit (310P) comprising a first plurality of capacitors ($2C_u$, C_u), each connected to a common node (320P) of the first sub circuit (310P) with a first terminal, and a second sub circuit (310N) comprising a second plurality of capacitors ($2C_u$, C_u), each connected to a common node (320N) of the second sub circuit (310N) with a first terminal. For each capacitor ($2C_u$, C_u) of the first plurality of capacitors, the first sub circuit (310P) comprises a first switch (S4) connected between the first input (V_{inP}) of the SAR ADC and a second terminal of that capacitor, a second switch (S2) connected between a first reference-voltage input (V_{rP}) and the second terminal of that capacitor, a third switch (S1) connected between a second reference-voltage input (V_{rN}) and the second terminal of that capacitor, and a capacitive device (X_P) connected between the second input (V_{inN}) of the SAR ADC and the second terminal of that capacitor. The second sub circuit is arranged in a similar way.

