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(54) **CYCLIC REDUNDANCY CHECK, CRC,DECODING USING THE INVERSE CRC GENERATOR POLYNOMIAL**

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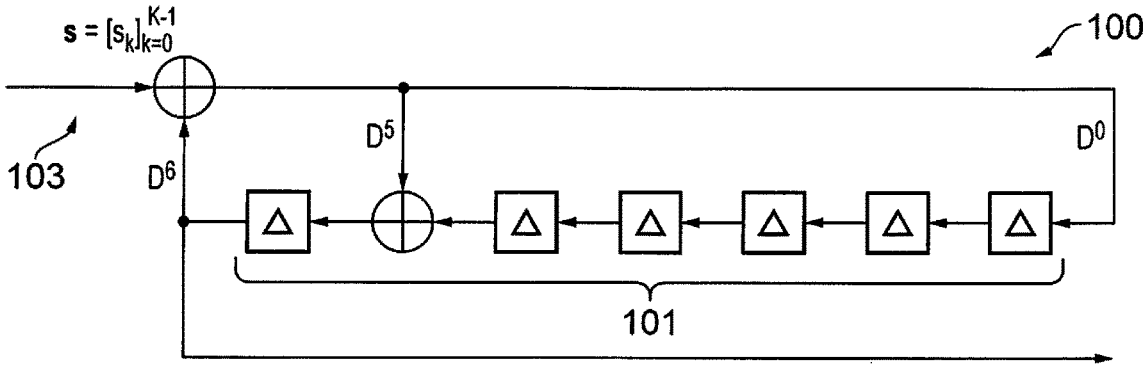
(57) **ABSTRACT**

A cyclic redundancy check, CRC, decoder circuit having a K-bit input bit sequence, s, comprising information bits and CRC bits; and at least one processor (P) configured to perform a CRC decode computation and configured to: use an inverse of a predefined CRC generator polynomial that encoded the K-bit input bit sequence, s, to produce a data set; compute a CRC syndrome from the data set; and determine whether the CRC syndrome contains any one-valued bits indicative of a CRC error. An LUT stores one or more rows of a CRC generator matrix (G) generated from the inverse of the predefined CRC generator polynomial. A set of mod(−K,P) zero-valued filler bits are appended to an end of the K-bit input bit sequence, wherein an order of the rows in the CRC generator matrix (G) is reversed and aligned with the input bits of the input stream.



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k	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
s_k	0	1	1	0	0	1	1	1	0	1	1	0						
p_{k-K}													1	0	0	1	0	1