



US 20220393700A1

(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0393700 A1**
(43) **Pub. Date: Dec. 8, 2022**(54) **ZERO PADDING APPARATUS FOR
ENCODING FIXED-LENGTH SIGNALING
INFORMATION AND ZERO PADDING
METHOD USING SAME**(71) Applicant: **Electronics and Telecommunications
Research Institute, Daejeon (KR)**(72) Inventors: **Sung-Ik PARK, Daejeon (KR);
Sun-Hyoung KWON, Daejeon (KR);
Jae-Young LEE, Daejeon (KR);
Heung-Mook KIM, Daejeon (KR)**(73) Assignee: **Electronics and Telecommunications
Research Institute, Daejeon (KR)**(21) Appl. No.: **17/891,189**(22) Filed: **Aug. 19, 2022****Related U.S. Application Data**(63) Continuation of application No. 17/202,475, filed on
Mar. 16, 2021, now Pat. No. 11,463,106, which is a
continuation of application No. 16/390,316, filed on
Apr. 22, 2019, now Pat. No. 10,992,316, which is a
continuation of application No. 15/553,458, filed on
Aug. 24, 2017, now Pat. No. 10,320,418, filed as
application No. PCT/KR2016/001756 on Feb. 23,
2016.**Foreign Application Priority Data**Feb. 27, 2015 (KR) 10-2015-0028060
Mar. 6, 2015 (KR) 10-2015-0031947
Feb. 22, 2016 (KR) 10-2016-0020636**Publication Classification**(51) **Int. Cl.**
H03M 13/11 (2006.01)
H03M 13/25 (2006.01)
H03M 13/27 (2006.01)
H03M 13/29 (2006.01)
H03M 13/00 (2006.01)
(52) **U.S. Cl.**
CPC H03M 13/1148 (2013.01); **H03M 13/1165**
(2013.01); **H03M 13/255** (2013.01); **H03M**
13/27 (2013.01); **H03M 13/2906** (2013.01);
H03M 13/618 (2013.01); **H03M 13/6362**
(2013.01); **H03M 13/1105** (2013.01); **H03M**
13/2778 (2013.01); **H03M 13/1102** (2013.01);
H03M 13/1111 (2013.01); **H03M 13/152**
(2013.01)(57) **ABSTRACT**

A zero padding apparatus and method for fixed length signaling information are disclosed. A zero padding apparatus according to an embodiment of the present invention includes a processor configured to generate a LDPC information bit string by deciding a number of groups whose all bits are to be filled with 0 using a difference between a length of the LDPC information bit string and a length of a BCH-encoded bit string, selecting the groups using a shortening pattern order to fill all the bits of the groups with 0, and filling at least a part of remaining groups, which are not filled with 0, with the BCH-encoded bit string; and memory configured to provide the LDPC information bit string to an LDPC encoder.

