



US 20240213300A1

(19) **United States**(12) **Patent Application Publication**
SOBUE et al.(10) **Pub. No.: US 2024/0213300 A1**(43) **Pub. Date: Jun. 27, 2024**(54) **SEMICONDUCTOR DEVICE**(71) Applicant: **Socionext Inc.**, Kanagawa (JP)(72) Inventors: **Isaya SOBUE**, Yokohama (JP);
Hideyuki KOMURO, Yokohama (JP)(21) Appl. No.: **18/598,870**(22) Filed: **Mar. 7, 2024****Related U.S. Application Data**

(60) Division of application No. 17/546,463, filed on Dec. 9, 2021, now Pat. No. 11,955,508, which is a continuation of application No. PCT/JP2019/024107, filed on Jun. 18, 2019.

Publication Classification(51) **Int. Cl.****H01L 27/092** (2006.01)**H01L 27/06** (2006.01)**H01L 23/528** (2006.01)(52) **U.S. Cl.**CPC **H01L 28/20** (2013.01); **H01L 27/0629**
(2013.01); **H01L 23/5286** (2013.01); **H01L**
27/092 (2013.01); **H01L 27/0924** (2013.01)

(57)

ABSTRACT

A semiconductor device includes a substrate; a first semiconductor region formed over the substrate; a second semiconductor region formed over the substrate, and electrically connected to the first semiconductor region; a third semiconductor region formed over the substrate, and positioned between the first semiconductor region and the second semiconductor region; a fourth semiconductor region formed over the first semiconductor region; a fifth semiconductor region formed over the second semiconductor region, and electrically connected to the fourth semiconductor region; a sixth semiconductor region formed over the third semiconductor region, and positioned between the fourth semiconductor region and the fifth semiconductor region; and wires formed between the first semiconductor region and the second semiconductor region, and between the fourth semiconductor region and the fifth semiconductor region, to cover the third semiconductor region and the sixth semiconductor region, the wires including conductors.

