US 20240223192A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0223192 A1**

Jayaraman et al. (43) **Pub. Date: Jul. 4, 2024**

(54) **MULTI-PHASE CLOCK GATING WITH PHASE SELECTION**

(71) Applicant: **Advanced Micro Devices, Inc.**, Santa Clara, CA (US)

(72) Inventors: **Pradeep Jayaraman**, San Jose, CA (US); **Ramon Mangaser**, Arlington, MA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Santa Clara, CA (US)

(21) Appl. No.: **18/092,222**

(22) Filed: **Dec. 31, 2022**

Publication Classification

(51) **Int. Cl.**
H03L 7/07 (2006.01)
H03L 7/081 (2006.01)

(52) **U.S. Cl.**
CPC ***H03L 7/07*** (2013.01); ***H03L 7/0814*** (2013.01); ***H03L 7/0816*** (2013.01)

(57) **ABSTRACT**

A multi-phase clock gating circuit receives a plurality of respective phased clock signals, and a one-hot stop phase select signal indicating a first selected phase for which gating of the phased clock signals is to be started. Responsive to a clock control signal indicating the phased clock signals are to be gated, the clock signals are gated beginning at the first selected phase, in order of phase, including looping from a last phase to a first phase.