



US 20240215237A1

(19) **United States**

(12) **Patent Application Publication**
YANG et al.

(10) **Pub. No.: US 2024/0215237 A1**

(43) **Pub. Date: Jun. 27, 2024**

(54) **THREE DIMENSIONAL (3D) MEMORY
DEVICE AND FABRICATION METHOD**

Publication Classification

(51) **Int. Cl.**

H10B 43/27 (2006.01)

H10B 41/27 (2006.01)

H10B 80/00 (2006.01)

(52) **U.S. Cl.**

CPC **H10B 43/27** (2023.02); **H10B 41/27**
(2023.02); **H10B 80/00** (2023.02)

(71) Applicant: **Yangtze Memory Technologies Co.,
Ltd., Wuhan (CN)**

(72) Inventors: **Yi YANG**, Wuhan (CN); **Tingting
GAO**, Wuhan (CN); **Xiaoxin LIU**,
Wuhan (CN); **Wei YUAN**, Wuhan
(CN); **Xiaolong DU**, Wuhan (CN);
Changzhi SUN, Wuhan (CN); **Zhihao
SONG**, Wuhan (CN); **Shan LI**, Wuhan
(CN); **Zhiliang XIA**, Wuhan (CN);
Zongliang HUO, Wuhan (CN)

(21) Appl. No.: **18/090,049**

(22) Filed: **Dec. 28, 2022**

(30) **Foreign Application Priority Data**

Dec. 21, 2022 (CN) 202211651307.9

(57) **ABSTRACT**

A method for fabricating a 3D memory device includes forming a sacrificial layer over a substrate, forming a first dielectric stack over the sacrificial layer, forming a channel hole structure, forming an opening that exposes the sacrificial layer, removing the sacrificial layer to create a cavity and expose a part of the channel hole structure, forming a semiconductor layer to fill the cavity, filling the opening with a filling structure, and forming a second dielectric stack over the filling structure. The opening is made for a gate line slit (GLS) structure.

190

