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(54) **PHASE-LOCKED LOOP (PLL) WITH DIRECT FEEDFORWARD CIRCUIT**

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(57) **ABSTRACT**

A phase-locked loop (PLL) device includes: 1) a detector configured to output an error signal to indicate a phase offset between a feedback clock signal and a reference clock signal; 2) a charge pump coupled to the detector and configured to output a charge pump signal based on the error signal; 3) an integrator with a feedback path, an input node, a reference node, and an output node, wherein the input node is coupled to the charge pump and receives the charge pump signal; 4) a voltage-controlled oscillator (VCO) coupled to the output node of the integrator via a resistor; and 5) a feedforward circuit coupled directly to the detector and configured to apply an averaged version of the error signal to correct a voltage level received by the VCO.