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(54) **INTEGRATED CIRCUIT AND METHOD OF FORMING THE SAME**

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(57) **ABSTRACT**

A flip-flop includes a first input circuit, a first NOR logic gate, a stacked gate circuit, a first NAND logic gate and an output circuit. The first input circuit generates a first signal responsive to at least a first data signal, a first or a second clock signal. The first NOR logic gate is coupled between a first and a second node, and generates a second signal responsive to the first signal and a first reset signal. The stacked gate circuit is coupled between the first and a third node, and generates a third signal responsive to the first signal. The first NAND logic gate is coupled between the third and a fourth node, and generates a fourth signal responsive to the third signal and a second reset signal. The output circuit is coupled to the fourth node, and generates a first output signal responsive to the fourth signal.