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(54) **USER-CONFIGURABLE HIGH-SPEED LINE DRIVER**

(71) Applicant: **Brookhaven Science Associates, LLC**, Upton, NY (US)

(72) Inventors: **Grzegorz W. Deptuch**, Great Neck, NY (US); **Nicholas Benjamin St. John**, East Patchogue, NY (US); **Soumyajit Mandal**, Merrick, NY (US)

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(57) **ABSTRACT**

An adaptive line driver circuit configured to transmit a signal over a wired link includes a delay-locked loop (DLL) circuit, which includes a phase detector (PD) circuit, charge pump (CP) circuit, and voltage-controlled delay line (VCDL) circuit operatively coupled together. The delay-locked loop circuit provides pre-emphasis and feed-forward equalization of the signal. The delay locked loop circuit also provides a user-configurable parameter including at least one of pre-data tap amplitude, data tap amplitude, post-data tap amplitude, pre-data tap duration, post-data tap duration, pre-data tap quantity, and post-data tap quantity. The adaptive line driver circuit further includes a source-series terminated (SST) driver circuit operatively coupled to the delay-locked loop circuit.