

# (19) United States

## (12) Patent Application Publication (10) Pub. No.: US 2024/0179907 A1 TOKITA et al.

May 30, 2024 (43) **Pub. Date:** 

## (54) THREE-DIMENSIONAL MEMORY DEVICE CONTAINING ETCH STOP STRUCTURES FOR WORD LINE CONTACTS AND

(52) U.S. Cl. CPC ...... *H10B 43/27* (2023.02); *H10B 41/27* (2023.02)

METHODS OF EMPLOYING THE SAME

(57)ABSTRACT

(71) Applicant: SANDISK TECHNOLOGIES LLC, ADDISON, TX (US)

(72) Inventors: Hirofumi TOKITA, Yokkaichi (JP); Akihisa SAI, Yokkaichi (JP); Masato

MIYAMOTO, Yokkaichi (JP)

(21) Appl. No.: 18/353,546

(22) Filed: Jul. 17, 2023

### Related U.S. Application Data

(60) Provisional application No. 63/385,051, filed on Nov. 28, 2022.

#### **Publication Classification**

(51) Int. Cl.

H10B 43/27 (2006.01)H10B 41/27 (2006.01) A method of making a semiconductor structure includes forming an alternating stack of insulating layers and sacrificial material layers, forming initial vertical stacks of at least one initial insulating plate and at least one initial dielectric material plate, and performing a plurality of pattern transfer process sequences that transfers the pattern of the initial vertical stacks by different numbers of underlying layers to form final vertical stacks of at least one final insulating plate and at least one final dielectric material plate. Sacrificial material layers that underlie the final vertical stacks are replaced with electrically conductive layers. The final dielectric material plates or conductive material plates formed by replacement of the dielectric material plates are employed as etch stop structures during subsequent formation of layer contact via structures.

