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(19) **United States**(12) **Patent Application Publication**
GRUBER et al.(10) **Pub. No.: US 2024/0223198 A1**(43) **Pub. Date: Jul. 4, 2024**(54) **SEGMENTED DIGITAL-TO-ANALOG
CONVERTER WITH DIGITAL SEGMENT
MISMATCH CORRECTION AND
SUBTRACTIVE SEGMENT MISMATCH
DITHERING**(52) **U.S. Cl.**
CPC **H03M 1/10** (2013.01)(57) **ABSTRACT**(71) Applicant: **Intel Corporation**, Santa Clara, CA
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Martin CLARA, Santa Clara, CA (US)(21) Appl. No.: **18/147,717**(22) Filed: **Dec. 29, 2022****Publication Classification**(51) **Int. Cl.**
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A segmented digital-to-analog converter (DAC). The segmented DAC includes at least two DAC segments. The DAC includes at least one overrange DAC configured to generate a dither subtraction signal based on an overrange DAC control data, and a dither control circuit configured to add a dither to the input data for the segmented DAC and generate the overrange DAC control data to compensate the dither. The dither subtraction signal is combined with the output signals of the DAC segments in an analog domain. The DAC includes a segment mismatch correction circuit configured to modify the input data for the segmented DAC or input data for at least one segment to correct a mismatch error of one or more of the segments and/or the at least one overrange DAC.

