



US 20220376709A1

(19) **United States**(12) **Patent Application Publication****Wu et al.**(10) **Pub. No.: US 2022/0376709 A1**(43) **Pub. Date: Nov. 24, 2022**(54) **FAILURE-TOLERANT ERROR
CORRECTION LAYOUT FOR MEMORY
SUB-SYSTEMS****Publication Classification**(51) **Int. Cl.**
H03M 13/15 (2006.01)
G06F 11/10 (2006.01)(52) **U.S. Cl.**
CPC H03M 13/1525 (2013.01); **G06F 11/1076**
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Shen**, Milpitas, CA (US); **Zhengang
Chen**, San Jose, CA (US)(57) **ABSTRACT**(21) Appl. No.: **17/880,144**(22) Filed: **Aug. 3, 2022****Related U.S. Application Data**(63) Continuation of application No. 16/205,075, filed on
Nov. 29, 2018, now Pat. No. 11,438,012.

Codewords of an error correcting code can be received. The codewords can be separated into multiple segments. The segments of the codewords can be distributed in an error correcting layout across a plurality of dies where at least a portion of the error correcting (EC) layout constitutes a first layout in the form of a Latin Square.

