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(19) **United States**(12) **Patent Application Publication**
Chen(10) **Pub. No.: US 2022/0353985 A1**(43) **Pub. Date: Nov. 3, 2022**(54) **PRINTED CIRCUIT BOARD DESIGN FOR
HIGH SPEED APPLICATION**(71) Applicant: **MediaTek Inc.**, Hsinchu City (TW)(72) Inventor: **Nan-Jang Chen**, Hsinchu City (TW)(21) Appl. No.: **17/858,445**(22) Filed: **Jul. 6, 2022****Publication Classification**(51) **Int. Cl.****H05K 1/02** (2006.01)**H01P 3/08** (2006.01)**H05K 1/05** (2006.01)(52) **U.S. Cl.**CPC **H05K 1/0219** (2013.01); **H05K 1/0224**(2013.01); **H01P 3/08** (2013.01); **H05K 1/05**(2013.01); **H05K 1/0227** (2013.01); **H05K****1/0298** (2013.01); **H05K 1/0218** (2013.01);**H05K 1/18** (2013.01)**Related U.S. Application Data**

(60) Division of application No. 16/929,651, filed on Jul. 15, 2020, which is a division of application No. 16/581,734, filed on Sep. 24, 2019, now Pat. No. 10,772,191, which is a division of application No. 15/877,396, filed on Jan. 23, 2018, now Pat. No. 10,485,095, which is a continuation-in-part of application No. 13/408,062, filed on Feb. 29, 2012, now Pat. No. 9,949,360.

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(57)

ABSTRACT

A printed circuit board includes a reference plane embedded in a substrate and adjacent to the top surface of the substrate. The printed circuit board also includes a first signal net and a second signal net being in close proximity to each other and disposed within a specific region on the top surface of the substrate. An outermost insulating layer on the top surface of the substrate covers the substrate, the first signal net and the second signal net, and includes an opening to expose a portion of the second signal net. A conductive layer is disposed in the opening and on the outermost insulating layer corresponding to the specific region, such that the conductive layer overlaps with the first signal net. A fifth signal net is embedded in the substrate and between the reference plane and the outermost insulating layer.

