US 20220352905A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2022/0352905 A1

SHIN (43) Pub. Date: Nov. 3, 2022

(54) ECC DECODERS HAVING LOW LATENCY

(71) Applicant: **SK hynix Inc.**, Icheon-si Gyeonggi-do (KR)

(72) Inventor: **Won Gyu SHIN**, Seoul (KR)

(73) Assignee: **SK hynix Inc.**, Icheon-si Gyeonggi-do (KR)

(21) Appl. No.: **17/865,630**

(22) Filed: **Jul. 15, 2022**

Related U.S. Application Data

(62) Division of application No. 16/883,845, filed on May 26, 2020, now Pat. No. 11,424,765.

(30) **Foreign Application Priority Data**

Jul. 29, 2019 (KR) 10-2019-0092049

Publication Classification

(51) **Int. Cl.**
H03M 13/15 (2006.01)

(52) **U.S. Cl.**
CPC ***H03M 13/1575*** (2013.01); ***H03M 13/157*** (2013.01); ***H03M 13/1545*** (2013.01); ***H03M 13/1525*** (2013.01)

(57) **ABSTRACT**

An ECC decoder includes a syndrome calculation block, a fast path controller, a KES block, a CSEE block, an UED, and a multiplexer. The KES block includes a plurality of KES-stages to calculate and output an error location/magnitude polynomial of a syndrome outputted from the syndrome calculation block. Each of a second to last KES-stages of the plurality of KES-stages receives the error location/magnitude polynomial from the previous KES-stage to output an error location/magnitude polynomial generated by an additional calculating operation. The additionally calculated error location/magnitude polynomial is not transmitted to the next KES-stage but directly outputted when an error location and an error magnitude are identified by the additionally calculated error location/magnitude polynomial.