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(54) **METHOD FOR PRODUCING A STRUCTURE FOR STUD-BASED INTERCONNECTION BETWEEN MICROCIRCUITS**

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(57) **ABSTRACT**

The invention relates to a method for manufacturing an electronic circuit which uses CMOS technology, the method comprising: (a) a step of metal deposition (**200**) and etching to form metal connections (P, P', . . .) at a first level in a substrate, (b) a step of depositing a layer of dielectric material (**110**, . . .) covering the metal connections, (c) a step of producing through-passages (**112**) in the thickness of the dielectric material, (d) a step of filling these passages with an interconnect metal (**300**), in order to form vias (V) connecting the levels. Steps (a) to (d) are repeated to form the metal connections (P, P', . . .) at different depths, connected by interconnection vias (V) in the thickness of the circuit.