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(54) **DEVICE AND METHOD FOR MULTI-CHIP CLOCK SYNCHRONIZATION**

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(57) **ABSTRACT**

The present disclosure relates to a multi-chip clock synchronization device and a method capable of reducing an operating frequency and power consumption when a plurality of chips share clocks for multi-chip clock synchronization, which may include a reference clock supply unit connected to a plurality of chips and supplying a reference clock of a first frequency to each chip and a target clock generation unit generating a target clock of a second frequency based on the reference clock of the first frequency, wherein the reference clock supply unit may generate the reference clock of the first frequency which is N times lower than the second frequency of the target clock to supply the generated reference clock to each chip, and the target clock generation unit may multiply the first frequency of the reference clock by N times when the reference clock of the first frequency is input to generate the target clock of the second frequency.