



US 20240237231A9

(19) **United States**  
(12) **Patent Application Publication**  
**TERAUCHI**

(10) **Pub. No.: US 2024/0237231 A9**  
(48) **Pub. Date: Jul. 11, 2024**  
**CORRECTED PUBLICATION**

(54) **METHOD FOR MANUFACTURING WIRING SUBSTRATE**

**Publication Classification**

(71) Applicant: **IBIDEN CO., LTD.**, Ogaki, Gifu (JP)

(72) Inventor: **Ikuya TERAUCHI**, Ogaki (JP)

(73) Assignee: **IBIDEN CO., LTD.**, Ogaki, Gifu (JP)

(51) **Int. Cl.**  
**H05K 3/40** (2006.01)  
**H05K 3/00** (2006.01)  
(52) **U.S. Cl.**  
CPC ..... **H05K 3/4038** (2013.01); **H05K 3/0055**  
(2013.01); **H05K 3/4007** (2013.01); **H05K**  
**2203/107** (2013.01)

(21) Appl. No.: **18/489,884**

(22) Filed: **Oct. 19, 2023**

**Prior Publication Data**

(15) Correction of US 2024/0138076 A1 Apr. 25, 2024  
See (22) Filed.  
See (30) Foreign Application Priority Data.

(65) US 2024/0138076 A1 Apr. 25, 2024

**Foreign Application Priority Data**

Oct. 20, 2022 (JP) ..... 2022-168667

(57) **ABSTRACT**

A method for manufacturing a wiring substrate includes forming first conductor pads and second conductor pads having a shorter inter-pad distance than the first conductor pads, forming a second insulating layer covering the first conductor pads and the second conductor pads, forming first via holes exposing the first conductor pads, applying a first desmear treatment such that residues are removed from the first via holes, forming second via holes in the second insulating layer after the first desmear treatment such that the second via holes expose the second conductor pads, applying a second desmear treatment such that residues are removed from the second via holes, forming first via conductors in the first via holes such that the first via conductors are formed on the first conductor pads, and forming second via conductors in the second via holes such that the second via conductor are formed on the second conductor pads.

