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(54) **MEMORY ARRAY AND METHODS USED IN FORMING A MEMORY ARRAY**

(71) Applicant: **Micron Technology, Inc.**, Boise, ID (US)

(72) Inventors: **Luan C. Tran**, Meridian, ID (US); **Guangyu Huang**, Boise, ID (US); **Haitao Liu**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

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(57) **ABSTRACT**

A method used in forming a memory array, comprises forming a substrate comprising a conductive tier, an insulator etch-stop tier above the conductive tier, a select gate tier above the insulator etch-stop tier, and a stack comprising vertically-alternating insulative tiers and wordline tiers above the select gate tier. Etching is conducted through the insulative tiers, the wordline tiers, and the select gate tier to and stopping on the insulator etch-stop tier to form channel openings that have individual bottoms comprising the insulator etch-stop tier. The insulator etch-stop tier is penetrated through to extend individual of the channel openings therethrough to the conductive tier. Channel material is formed in the individual channel openings elevationally along the insulative tiers, the wordline tiers, and the select gate tier and is directly electrically coupled with the conductive material in the conductive tier. Structure independent of method is disclosed.