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(54) HOLE-TYPE SADP FOR 2D DRAM **CAPACITOR**

(71) Applicant: Applied Materials, Inc., Santa Clara, CA (US)

(72) Inventor: Fredrick Fishburn, Aptos, CA (US)

(73) Assignee: Applied Materials, Inc., Santa Clara, CA (US)

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ABSTRACT (57)

Memory devices and methods of forming memory devices are described. Methods of forming electronic devices are described where a spacer is formed around each of the bit line contact pillars, the spacer in contact with the spacer of an adjacent bit line contact pillar. A doped layer is then epitaxially grown on the memory stack and bit line is formed on the memory stack. The bit line is self-aligned with the active region.

