US 20220416797A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2022/0416797 A1**

WANG (43) **Pub. Date: Dec. 29, 2022**

(54) **FPGA-BASED DESIGN METHOD AND DEVICE FOR EQUALLY DIVIDING INTERVAL**

(71) Applicant: **INSPUR SUZHOU INTELLIGENT TECHNOLOGY CO., LTD.**, Suzhou, Jiangsu (CN)

(72) Inventor: **Xiankun WANG**, Suzhou, Jiangsu (CN)

(21) Appl. No.: **17/778,473**

(22) PCT Filed: **Aug. 26, 2020**

(86) PCT No.: **PCT/CN2020/111357**

§ 371 (c)(1),
(2) Date: **May 20, 2022**

(30) **Foreign Application Priority Data**

Dec. 31, 2019 (CN) 201911421769.X

Publication Classification

(51) **Int. Cl.**
H03L 7/191 (2006.01)
G06F 30/34 (2006.01)

(52) **U.S. Cl.**
CPC ***H03L 7/191*** (2013.01); ***G06F 30/34*** (2020.01)

(57) **ABSTRACT**

Provided is a FPGA-based design method for equally dividing an interval, including the following steps: dividing the oscillation periods of a second pulse signal of a crystal oscillator clock of a FPGA board by the number of equally divided sampling pulses, and obtaining the remainder thereof; dividing the remainder by the number of the equally divided sampling pulses to serve as an error within each sampling interval; using a counter to count from the second pulse, and stopping the counting of the counter once whenever the error within the sampling interval, which is accumulated within the second pulse interval, is greater than or equal to the vibration period. Further provided is a FPGA-based design device for equally dividing an interval. The present application makes full use of the feature of interval equal division calculation, has high precision, and is easy to implement.