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(54) **FERROELECTRIC MEMORY DEVICE AND METHOD FOR FORMING THE SAME**

(71) Applicant: **Wuxi Smart Memories Technologies Co., Ltd.**, Wuxi (CN)

(72) Inventors: **Meilan Guo**, Wuxi (CN); **Yushi Hu**, Wuxi (CN); **Zhenyu Lu**, Wuxi (CN)

(73) Assignee: **Wuxi Smart Memories Technologies Co., Ltd.**, Wuxi (CN)

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(57) **ABSTRACT**

A memory device includes a plurality of memory cells and a routing interconnection structure in electric contact with the memory cells. Each memory cell includes at least one first transistor, a cell interconnection structure formed over the transistor and in electrical contact with the transistor, the cell interconnection structure including a cell plate disposed at a top layer of the cell interconnection structure, and at least one capacitor electrically coupled to the first transistor through the cell interconnection structure. Each capacitor includes a first electrode, a second electrode, and a ferroelectric layer disposed between the first electrode and the second electrode. The routing interconnection structure includes a first conductive layer, and a first via structure disposed on the first conductive layer. The first via structure is in electrical contact with the first electrode through a second conductive layer. The first conductive layer is beneath the second conductive layer.