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(54) **MEMORY STRUCTURE AND MANUFACTURING METHOD THEREOF**

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(57) **ABSTRACT**

A memory structure includes a semiconductor substrate, two word line structures, an isolation structure, and a bit line contact layer. The semiconductor substrate has a first trench, a second trench, a first top surface, and a second top surface adjoining the first and second trenches and lower than the first top surface. The two word line structures are respectively located in the first and second trenches. The isolation structure is located on the two word line structures and in contact with a sidewall of the first trench and a sidewall of the second trench, in which the isolation structure has a top surface extending to and coplanar with the second top surface of the semiconductor substrate. The bit line contact layer is located on the second top surface of the semiconductor substrate and surrounded by the isolation structure.