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(54) **PACKET CLASSIFICATION USING LOOKUP TABLES WITH DIFFERENT KEY-WIDTHS**

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(57) **ABSTRACT**

A multistaged packet processor includes a lookup table at each stage. In one configuration, the match criteria in the lookup tables across the stages of a four-stage packet processor allocate 32 bits of space to hold IPv4 addresses and IPv6 addresses. In one configuration, the 32 bits store an entire IPv4 address or a 32-bit segment. An IPv6 address can be stored across the four lookup tables in 32-bit segments. The configuration allows for accommodating the varying key widths presented by IPv4 and IPv6 addresses while at the same time improving storage utilization in the lookup tables.