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Agarwal et al.

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(54) **PROCESS-VOLTAGE-TEMPERATURE TOLERANT REPLICA FEEDBACK PULSE GENERATOR CIRCUIT FOR PULSED LATCH**

(52) **U.S. Cl.**

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(71) Applicant: **Intel Corporation**, Santa Clara, CA (US)

(57)

ABSTRACT

(72) Inventors: **Amit Agarwal**, Hillsboro, OR (US); **Steven K. Hsu**, Lake Oswego, OR (US); **Mark A. Anders**, Hillsboro, OR (US); **Ram K. Krishnamurthy**, Portland, OR (US)

Embodiments herein relate to a pulse generator which provides first and second clock pulses to one or more pulsed latches, where the pulse generator replicates a delay of the pulsed latches in providing the first and second clock pulses. The pulse generator can include a replica of latch components in the pulsed latches such as a tri-state inverter, a transmission gate and inverters, where an output of the tri-state inverter is coupled to the transmission gate and to an input of the inverter, and an output of the inverter is coupled to an input of the tri-state inverter. The tri-state inverter can be a modified tri-state inverter with an output forced to “1” when a clock signal is “0.” In one approach, the latch components of the pulse generator are to write a logic 1 when a clock signal goes high.

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