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(54) **UNIDIRECTIONAL COMMAND BUS PHASE DRIFT COMPENSATION**

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(57) **ABSTRACT**

A system has an unmatched communication architecture for a unidirectional command bus and compensates for drift on the command bus based on data provided on a bidirectional data bus. The memory device has an oscillator to measure drift or an amount of delay for the command bus over a time interval. The memory device can return a value over the data bus to the memory controller based on the delay measured with the oscillator. Based on receiving the value, the memory controller can adjust configuration settings for communication on the command bus.