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(54) **FREQUENCY MULTIPLIER CALIBRATION**

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(57) **ABSTRACT**

In some examples, an apparatus includes a delay-based frequency multiplier and an error detection circuit. The delay-based frequency multiplier has a clock input, a multiplier clock output, and a delay calibration input. The error detection circuit has a detection input and a detection output. The detection input is coupled to the multiplier clock output, and the detection output is coupled to the delay calibration input. The error detection circuit is configured to receive a clock signal at the detection input, and provide a period error signal at the detection output based on a time difference between a first edge of the clock signal and a second edge of a delayed version of the clock signal.