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(54) **DATA MULTIPLEXER SINGLE PHASE FLIP-FLOP**

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(57) **ABSTRACT**

A single-phase clocked data multiplexer (MUX-D) scan capable flipflop (FF) design that improves over existing transmission-gate (t-gate) based master-slave flipflops in terms of dynamic capacitance (Cdyn) as well as performance while remaining comparable in area. Unique features of the design are a complementary metal oxide semiconductor (non-t-gate) style structure with an improvement in circuit parameters achieved by eliminating clock inversions and maximally sharing NMOS devices across NAND structures. The core of the flipflop adopts an all CMOS NAND, And-OR-Inverter (AOI) complex logic structure to implement a true edge-triggered flip-flop functionality.