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(54) **MEMORY DEVICE AND FABRICATION METHOD THEREOF**

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(57) **ABSTRACT**

A semiconductor device fabrication method includes providing a processing wafer. The processing wafer has core and staircase structure (SS) regions, and includes a bottom conductor layer, conductor/dielectric tier(s) over the bottom conductor layer, and a channel hole (CH) in the core region and extending approximately vertically through the conductor/dielectric tier(s). The CH includes a channel layer and a memory film surrounding the channel layer. A protrusion portion of the channel layer and a protrusion portion of the memory film extend into the bottom conductor layer. The method further includes patterning the bottom conductor layer to remove a portion of the bottom conductor layer in the core region to expose the protrusion portion of the memory film, performing etching to remove the protrusion portion of the memory film to expose the protrusion portion of the channel layer, performing impurity implantation, and performing laser activation.