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(54) **PACKAGE COMPRISING A SUBSTRATE WITH POST INTERCONNECTS AND A SOLDER RESIST LAYER HAVING A CAVITY**

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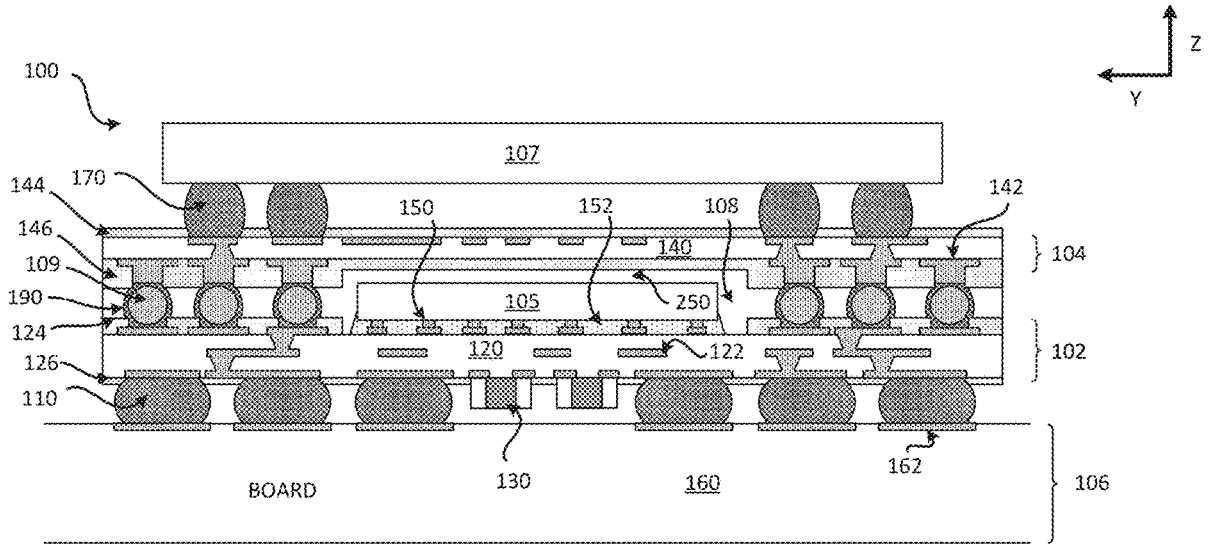
(57) **ABSTRACT**

A package comprising a first substrate, a first integrated device coupled to the first substrate, and a second substrate, and a plurality of solder interconnects coupled to the first substrate and the second substrate. The first substrate comprises at least one first dielectric layer; a first plurality of interconnects, wherein the first plurality of interconnects include a first plurality of post interconnects; and a first solder resist layer coupled to a first surface of the first substrate. The second substrate comprises a first surface and a second surface; at least one second dielectric layer; a second plurality of interconnects, wherein the second plurality of interconnects comprises a second plurality of post interconnects; and a second solder resist layer coupled to the second surface of the second substrate. The second surface of the second substrate faces the first substrate. The second solder resist layer includes a cavity.




CROSS SECTIONAL PROFILE VIEW