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(54) **CLUSTERING FINE PITCH MICRO-BUMPS FOR PACKAGING AND TEST**

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(57) **ABSTRACT**

An apparatus includes a chip package that has a chip connection surface and has an array of micro-bumps on the chip connection surface. The array of micro-bumps includes a plurality of subarrays of micro-bumps. Micro-bumps within each subarray are spaced apart by a chip pitch and the subarrays within the array are spaced apart by a card pitch that is an integer multiple of the chip pitch. The apparatus also includes a laminate circuit card that has a card connection surface that faces the chip connection surface of the chip package and that has an array of card pads adjacent to the card connection surface. The card pads are spaced apart by the card pitch, and each of the card pads is aligned to and electrically connected with a corresponding subarray of micro-bumps. In some embodiments, an interposer connects the card pads to the micro-bumps, and may include decoupling capacitors.