



(12) **Patent Application Publication**  
**Ko et al.**

(43) **Pub. Date:** **Jun. 27, 2024**

*H01L 25/065* (2006.01)

(52) U.S. Cl.

CPC ..... ***H01L 23/3178*** (2013.01); ***H01L 23/291***  
(2013.01); ***H01L 24/08*** (2013.01); ***H01L 24/16***  
(2013.01); ***H01L 24/94*** (2013.01); ***H01L 24/96***  
(2013.01); ***H01L 25/0652*** (2013.01); ***H01L***  
***25/0657*** (2013.01); ***H01L 2924/1435***  
(2013.01); ***H10B 80/00*** (2023.02)

(72) Inventors: **Yeongkwon Ko**, Suwon-si (KR);  
**Unbyoung Kang**, Suwon-si (KR);  
**Soyeon Kwon**, Suwon-si (KR);  
**Chungsun Lee**, Suwon-si (KR)

(73) Assignee: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)

(57)

## ABSTRACT

(21) Appl. No.: 18/371,714

(22) Filed: **Sep. 22, 2023**

(30) **Foreign Application Priority Data**

Dec. 26, 2022 (KR) ..... 10-2022-0185018

## Publication Classification

(51) **Int. Cl.**

*H01L 23/31* (2006.01)

*H01L 23/00* (2006.01)

Provided is a semiconductor package including a first semiconductor device including a first semiconductor substrate, a first interconnect structure on the first semiconductor substrate, and a trench extending into the first interconnect structure and a portion of the first semiconductor substrate, a second semiconductor device on the first semiconductor device, and a cover insulating layer on the first semiconductor device and a side surface of the second semiconductor device, the cover insulating layer including a first portion filling the trench included in the first semiconductor device and contacting the first semiconductor substrate.

