



(54) **PROGRAMMABLE LOGIC BLOCK WITH MULTIPLE TYPES OF PROGRAMMABLE ARRAYS AND FLEXIBLE CLOCK SELECTION**

(71) Applicant: **STMICROELECTRONICS (ROUSSET) SAS**, Rousset (FR)

(72) Inventors: **Mark WALLIS**, Mouans Sartoux (FR); **Jean-Francois LINK**, Trets (FR); **Joran PANTEL**, Marseille (FR)

(73) Assignee: **STMICROELECTRONICS (ROUSSET) SAS**, Rousset (FR)

(21) Appl. No.: **18/435,913**

(22) Filed: **Feb. 7, 2024**

Related U.S. Application Data

(63) Continuation of application No. 17/861,067, filed on Jul. 8, 2022, now Pat. No. 11,942,935.

Publication Classification

(51) **Int. Cl.**
H03K 19/17724 (2006.01)
H03K 19/173 (2006.01)
H03K 19/17736 (2006.01)
H03K 19/20 (2006.01)
(52) **U.S. Cl.**
CPC ... *H03K 19/17724* (2013.01); *H03K 19/1737* (2013.01); *H03K 19/1774* (2013.01); *H03K 19/17744* (2013.01); *H03K 19/20* (2013.01)

(57) **ABSTRACT**

An integrated circuit includes a programmable logic block. The programmable logic block includes a programmable logic array (PLA) and a field programmable gate array (FPGA). The PLA includes logic cells having a first architecture. The FPGA includes logic cells having a second architecture more complex than the first architecture. The programmable logic block includes an interface coupled to the PLA and the FPGA. An integrated circuit may also include circuitry for selecting one of plurality of clock signals for logic cells of a PLA.

