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(54) **ADAPTIVE BIAS CIRCUITS AND METHODS FOR CMOS MILLIMETER-WAVE POWER AMPLIFIERS**

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(57) **ABSTRACT**

Adaptive bias networks include small transistors connected to adjust gate bias voltage of one or more transistors of an amplifier or amplifier stage, or in a main or auxiliary path of a compound amplifier such as a Doherty amplifier. The small transistors are sized to avoid additional loading of the input. The adaptive bias circuits of preferred embodiments adjust the gate bias to produce a boost in gate bias voltage of an nFET transistor when the input power is in an upper portion of the amplifier or amplifier stage's input power range, thereby increasing the gain, and reduce gate bias voltage of a pFET transistor in the upper portion of the amplifier's input power range, thereby also increasing the gain. The adaptive bias networks can be implemented with varactors to vary DC voltage across the varactor to change its capacitance and compensate changing input capacitance of the amplifier input FET.