CS6135 VLSI Physical Design Automation

Homework 1: P&R Tool

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2. Record different configurations of the core utilization, clock period,DRC violations, slack, chip area, and wire length. (Try more than 5different configurations) Explain how the adjustments of the clockperiod and the core utilization affect the metrics (DRC violations, slack,chip area, and wire length).

A:

Core Utilization	Clock Period	DRC violations	Slack	Chip Area (um^2)	Wire length
0.468	1870	0	-0.1	40323.806	206640.7000
0.450	1900	0	0.9	41107.357	202823.1920
0.504	1850	3	0.2	38240.502	207117.7960
0.490	1850	1	0.0	39603.852	209132.1960
0.456	1850	0	-0.4	42699.758	209188.2360
0.477	1850	0	-0.1	41107.357	208861.8800
0.462	1875	0	0.1	41107.357	204544.2720
0.460	1870	0	0.5	41107.357	204802.6440

Clock Period 越小(例如 1850)時序要求嚴格，Slack 容易變成負值，甚至在高 utilization 時出現 DRC。Clock Period 增加(例如 1900) Slack 提升明顯，變成正值；但代表設計工作頻率下降，效能較差。

Core Utilization 越高 ，晶片面積縮小(chip area 減少)，wire length 也有下降趨勢；但 routing 擁塞上升，容易出現 DRC。

Core Utilization 越低, Routing 較鬆，DRC 容易清零，但 chip area 與 wire length 顯著增加。

Slack vs. Utilization：在 0.46–0.49 區間，配合適度放鬆 clock period (1870–1875)，能同時達到 Slack ≥ 0、DRC=0。

3. Explain the purpose of inserting well tap cell.

A:

穩定電源分佈：Well tap cell 用來將 P-substrate 連接至 VSS、N-well 連接至 VDD，避免基板電位浮動，確保電路穩定性。

降低雜訊與漏電流：提供穩定的基板偏壓，減少 latch-up、基板雜訊與漏電流問題，提升電路可靠性。

佈局規律性：在實際 P&R 流程中，通常 每隔幾排 standard cells 插入一次 well tap cell，確保整個晶片的基板都能良好接地。

4. Show the configuration from your best result.

```
--- Summary of the Current Result ---
 Slack Time:           0.500
 DRC Violations:       0
 Clock Period:         1870.000
 Total area of chip: 41107.357
 Total wire length:  204802.6440
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5. Show the final chip layout of your best result generated by Innovus