

$$D_a = E_a - 2a = 11 - 23 = -12$$

$$D_b = E_b - 2b = 15 - 15 = 0$$

$$g_{ab} = D_a - D_b - 2w_{ab} = -12 - 2w_{ab} \leq 0$$

Partial

## CS6135 VLSI Physical Design Automation

Final Exam: 10:10 a.m. - 13:10 p.m., December 26, 2023

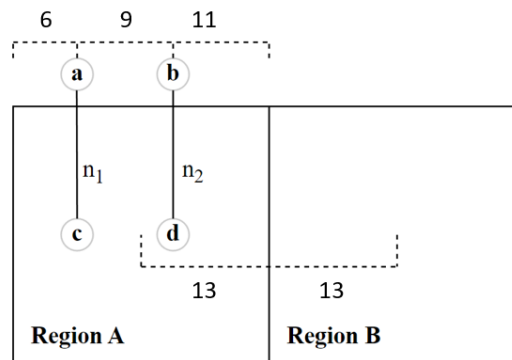
KL algo

1. (5 points) Vertex  $a$  and vertex  $b$  are two vertices in an edge-weighted complete graph, where the weight of each edge is a non-negative integer. Suppose that the vertex set of this graph is partitioned into two subsets, and vertices  $a$  and  $b$  are not in the same subset. Assume that the respective external and internal costs of vertex  $a$  are 11 and 23, and the respective external and internal costs of vertex  $b$  are 15 and 15. Can the cut cost be reduced by swapping vertices  $a$  and  $b$ ? Justify your answer.

No.

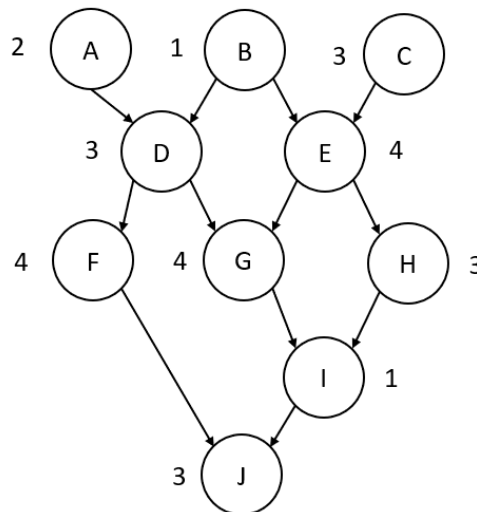
2. (5 points) Consider the figure below where cells  $a$  and  $b$  are fixed cells that are placed at the given locations, cells  $c$  and  $d$  are movable cells that can be moved to the center of either region  $A$  or  $B$ , net  $n_1$  connects cells  $a$  and  $c$ , and net  $n_2$  connects cells  $b$  and  $d$ . The center-to-center distance between regions  $A$  and  $B$  is 26. Use the exact net-weight model discussed in class to find the cut weights for nets  $n_1$  and  $n_2$  for capturing the wirelength cost precisely.

exact-net cost



3. (15 points) Consider the circuit shown below. Assume the area of each gate is 1 unit, the area constraint of each cluster is 4 units, and the interconnection delay between two clusters is 3 units. The gate delay is given next to each gate. Show your work by applying the clustering algorithm discussed in class to the circuit below.

clustering for  
delay minimization



# floorplan

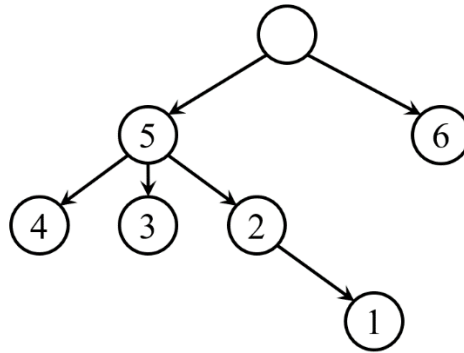
4. Consider a set of modules in the following table.

Module	Width	Height
1	3	2
2	2	4
3	3	1
4	1	2
5	3	4
6	4	1

seq-pair

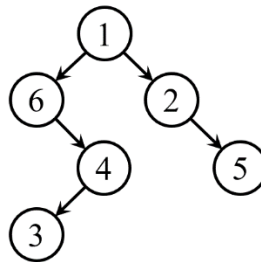
- (a) (7 points) Assume that each module cannot be rotated. Show your work to find the optimal packing for the sequence-pair (516423, 135624).
- (b) (4 points) Assume that each module cannot be rotated. Show your work to find the placement for the following horizontal O-tree.

O-tree



- (c) (4 points) Assume that each module cannot be rotated. Show your work to find the placement for the following B\*-tree.

B\*-tree



Polish expression (Stockmeyer)

- (d) (10 points) Assume that each module can be rotated by 90-degree. Perform the Stockmeyer algorithm to find a minimum-area floorplan for the Polish expression 426HV315HVH.

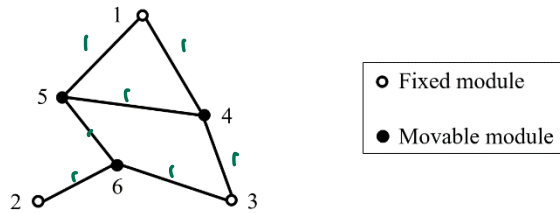
Force-directed method

5. (5 points) You are asked to place a cell on a chip. The cell connects to four other cells located at (6, 4), (3, 5), (7, 4), and (9, 2) with the weights 4, 2, 3, and 1, respectively. Find an appropriate position to place the cell by using the force-directed method.

6. (10 points) Consider a circuit with movable and fixed modules as represented by the graph below. In the graph, each vertex denotes a module, while each edge denotes a two-pin net and is associated with a weight 1.

# placement

quadratic placement

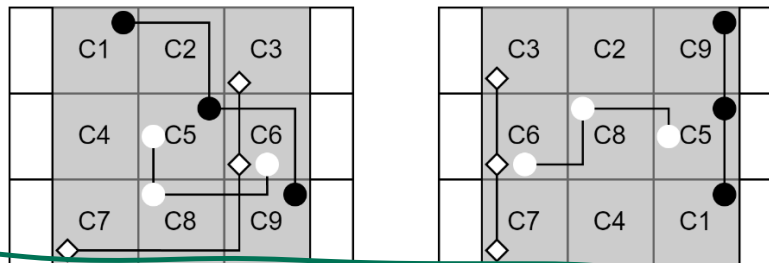


For the three fixed modules, module 1 is at (7, 9), module 2 is at (3, 4), and module 3 is at (11, 4). Determine the locations of the three movable modules such that the total weighted quadratic wirelength of the circuit is minimized. To answer this question, you only need to show your work for getting the x-coordinates of the three movable modules.

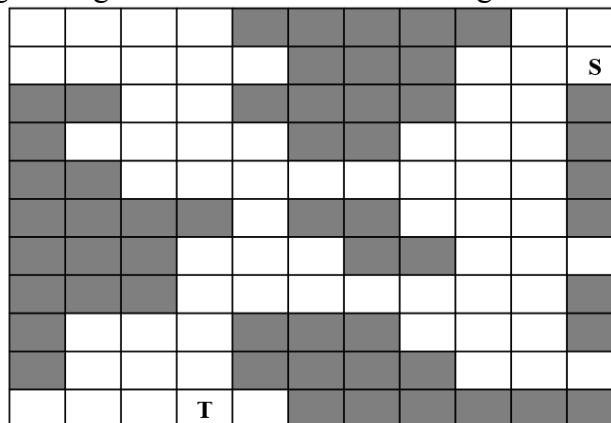
7. (10 points) Consider the following two placement results for 9 standard cells  $c_1, c_2, \dots, c_9$ , where each cell has the same width and height. The one on the left is a legalized placement result in which the cells are placed side by side and in three rows. The one on the right is the optimal placement result that is obtained by applying a sequence of the following two kinds of local optimization operations to the legalized placement result:

- *Swap*( $c_i, c_j$ ): Swap cells  $c_i$  and  $c_j$ .
- *SlidingWindow*( $c_i, c_j, c_k$ ): Find the best order of  $c_i, c_j$  and  $c_k$ , where cells  $c_i, c_j$  and  $c_k$  are in the same row.

Find such a sequence that has as few operations as possible. You should draw the placement result after each operation. If you can use 4 operations or less to transform the legalized placement result to the optimal one, you will get full points; otherwise, you will get partial points.



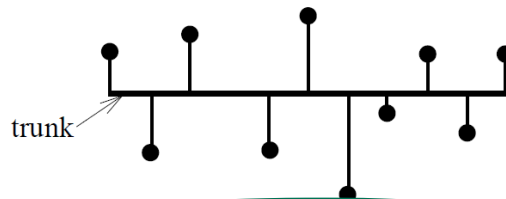
8. Consider the following routing instance with shaded blockages.



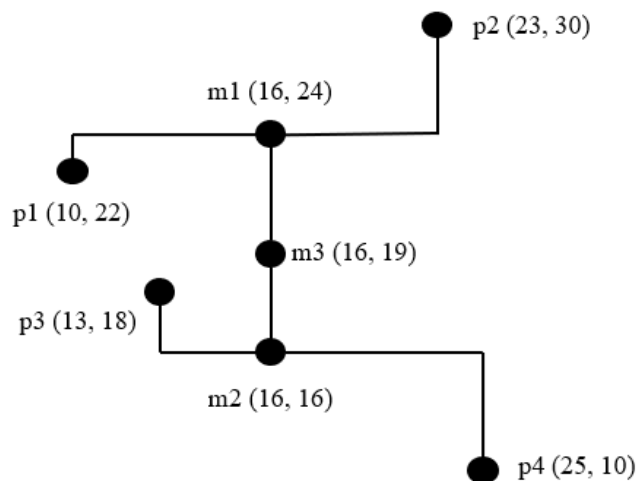
- (5 points) Show your work for finding a shortest path between  $S$  and  $T$  using the Lee algorithm.
- (5 points) Show your work for finding a shortest path between  $S$  and  $T$  using the A\*-search algorithm which defines the cost function of each grid cell  $x$  to be  $f(x) = g(x) + h(x)$ , where  $g(x)$  is the label of  $x$  (i.e., the label given by the Lee algorithm) and  $h(x)$  is the Manhattan distance between  $x$  and  $T$ . Break the tie by picking the grid cell toward  $T$ .

9. (5 points) For a net with all its pins located on a two-dimensional plane, a single horizontal-trunk Steiner tree for the net consists of a signal horizontal trunk (i.e., a horizontal line segment) and all the pins of the net are connected to the trunk by vertical line segments. See the following figure for an example. Note that it is possible for a single horizontal-trunk Steiner tree to have the trunk or a vertical line segment degenerate as a point. Also note that there are many possible single horizontal-trunk Steiner trees for a net. Given a  $k$ -pin net with the pin coordinates,  $(x_i, y_i)$ ,  $1 \leq i \leq k$ , in a plane, develop an algorithm for constructing a single horizontal-trunk Steiner tree that has the minimum wirelength among all possible single horizontal-trunk Steiner trees. Your algorithm should be as efficient as possible. You should also analyze the time complexity of your algorithm.

Horizontal trunk  
Steiner tree



10. A routing tree for four clock pins  $p_1$ ,  $p_2$ ,  $p_3$ , and  $p_4$  is given below. Suppose  $m_1$  is the tapping point for  $(p_1, p_2)$ ,  $m_2$  is the tapping point for  $(p_3, p_4)$ , and  $m_3$  is the tapping point for  $(m_1, m_2)$ . (Note that it is possible that a tapping point may not achieve zero skew in this problem.) The coordinates of  $p_1$ ,  $p_2$ ,  $p_3$ ,  $p_4$ ,  $m_1$ ,  $m_2$ , and  $m_3$  are also shown below. The loading capacitances of  $p_1$ ,  $p_2$ ,  $p_3$ , and  $p_4$  are  $3F$ ,  $1F$ ,  $4F$  and  $2F$ , respectively. For a wire segment, the resistance and capacitance per unit length are  $\alpha = 0.3\Omega$  and  $\beta = 0.2F$ , respectively. The point  $m_3$  is the final clock entry point. Assume the  $\pi$ -model is used for wires, and the Elmore delay model (i.e., the RC delay model discussed in class) is used for calculating delays. Note that the unit length is  $1\mu m$ , and therefore the unit RC delay is  $1\mu s$ .



- (a) (6 points) What are the delay and skew of the routing tree?  
 (b) (4 points) Assume the switch-resistor model discussed in class is used for buffers, and the intrinsic delay of each buffer is negligible. If two identical buffers with resistance  $r_b = 0.3\Omega$  and capacitance  $c_b = 0.1F$  are inserted at  $m_1$  and  $m_2$ , what are the resultant delay and skew of the routing tree?