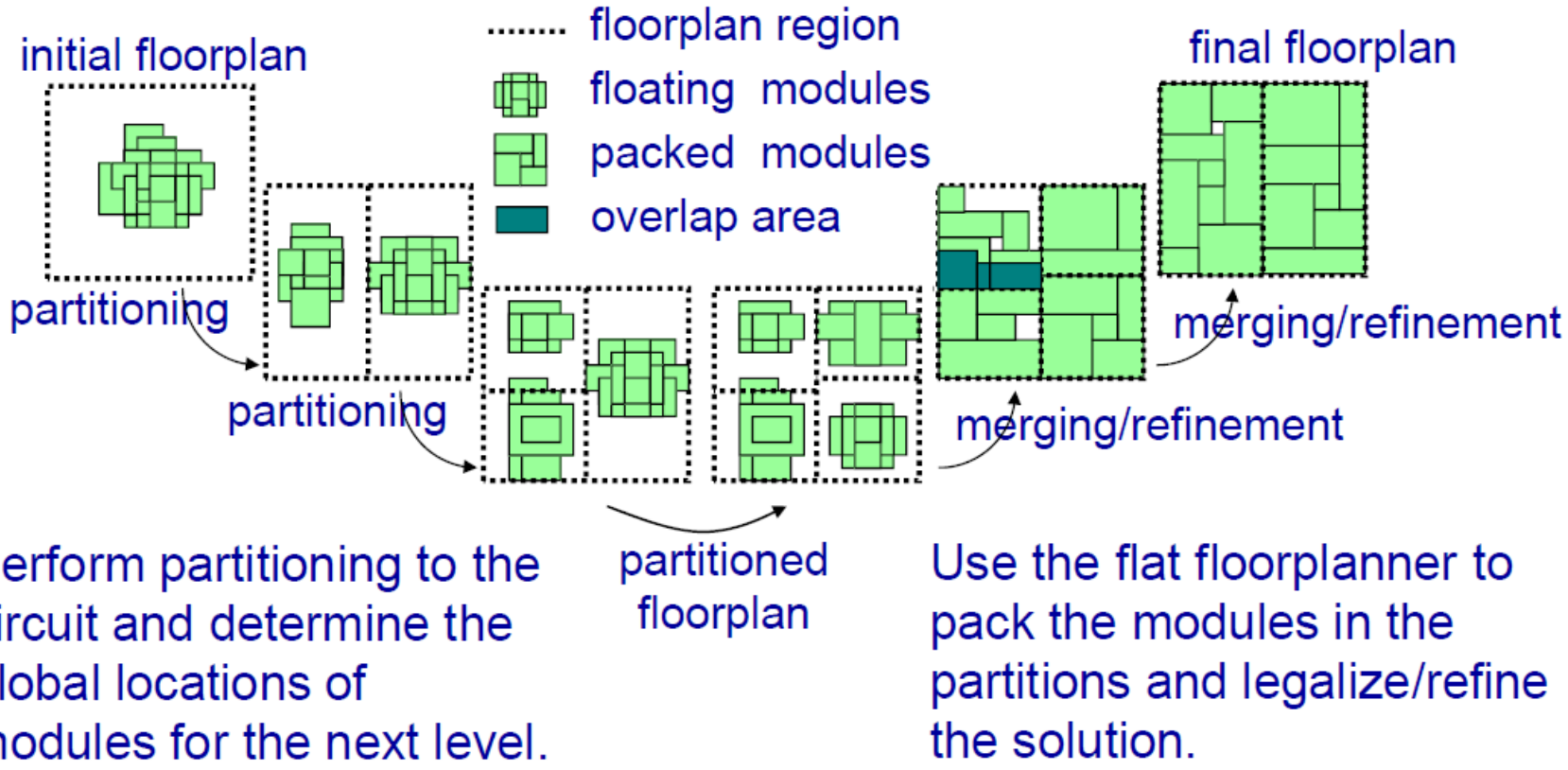
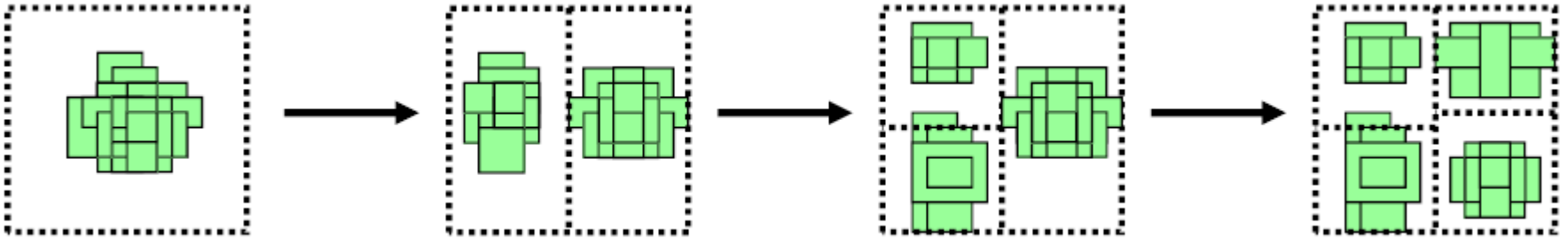
IMF: V-Shaped Multilevel Floorplanning

- Chen, Chang, Lin, "IMF: interconnect-driven floorplanning for large-scale building-module designs," ICCAD'05



Stage 1: Partitioning Stage

- All modules are set to the center of the chip region initially
- Partition the circuit recursively to minimize the interconnect and assign the regions of the modules
- The partitioning stage continues until the number of modules in each partition is smaller than a threshold, and the partitioned floorplan is obtained.

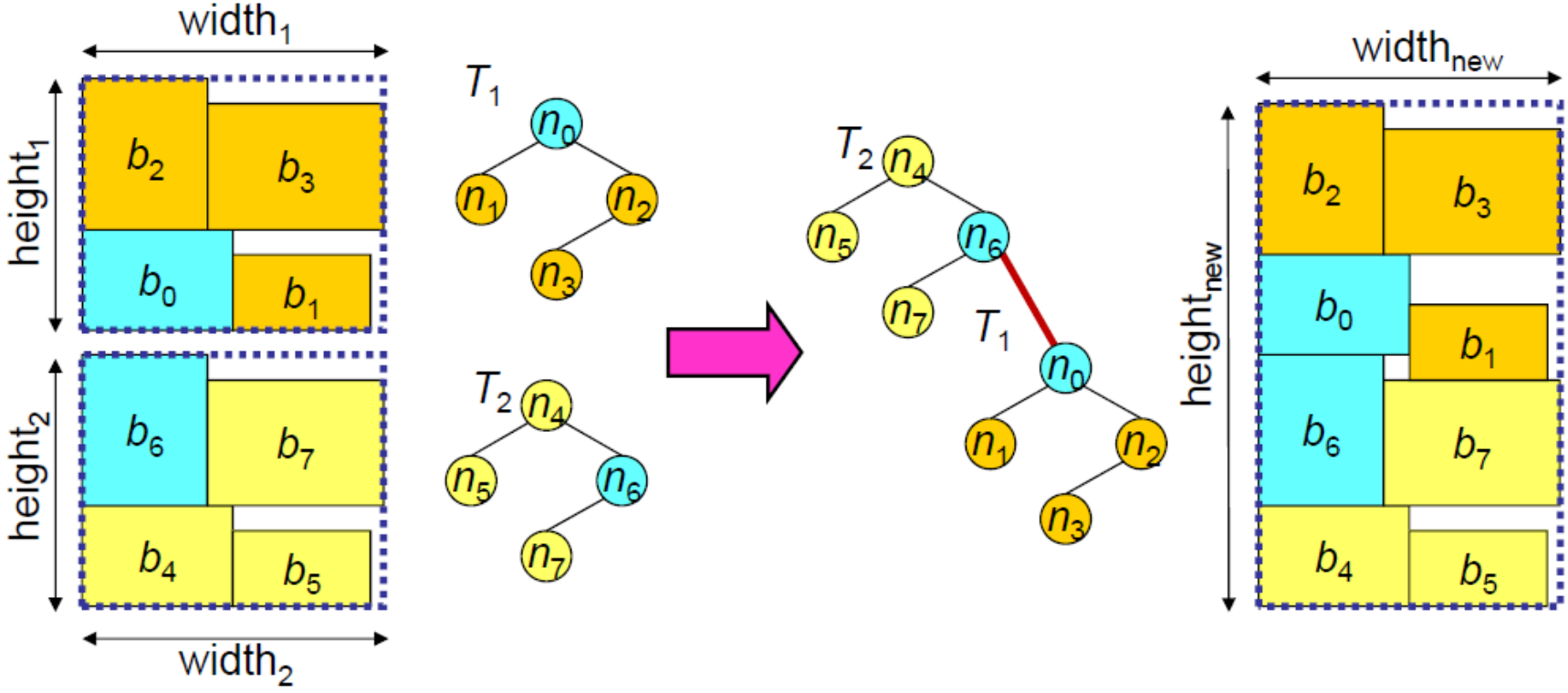


Stage 2: Merging Stage

- Construct a B*-tree and find the sub-floorplan for each sub-region (fixed-outline floorplanning)
- Cost function for the simulated annealing: area, wirelength, and aspect ratio penalty
- Merge two B*-trees (sub-floorplans) to form a new B*-tree (floorplan) recursively
- Refine the merged sub-floorplan using fixed-outline floorplanning again

Vertical Merging

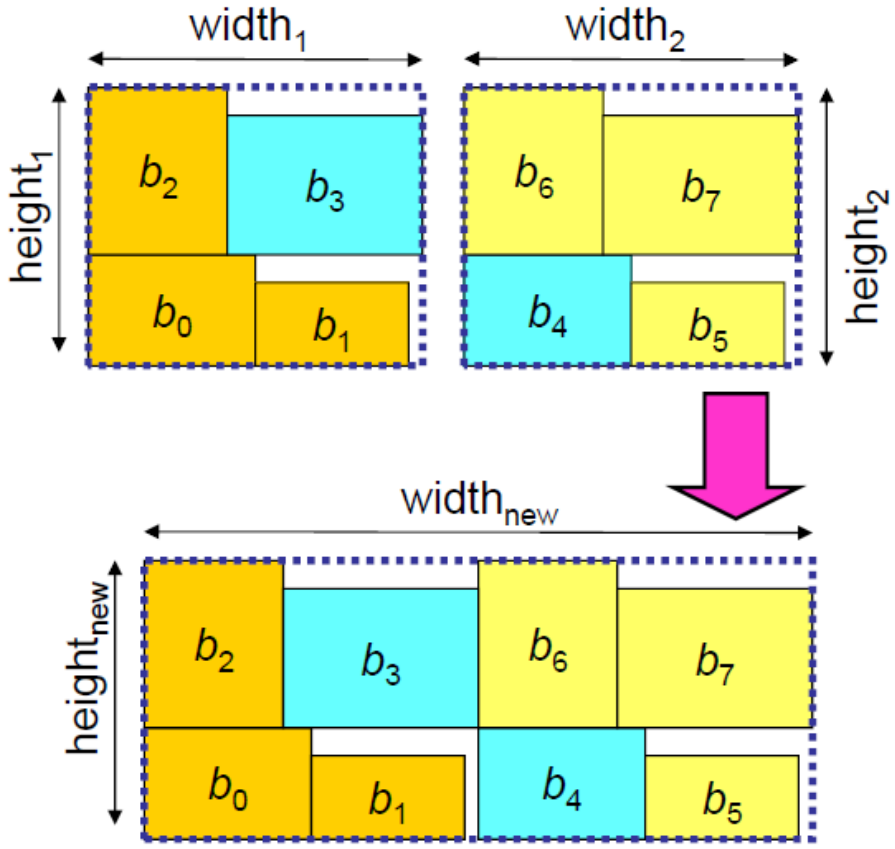
Make the root of the top B*-tree as the right child of the right-most node of the bottom B*-tree.

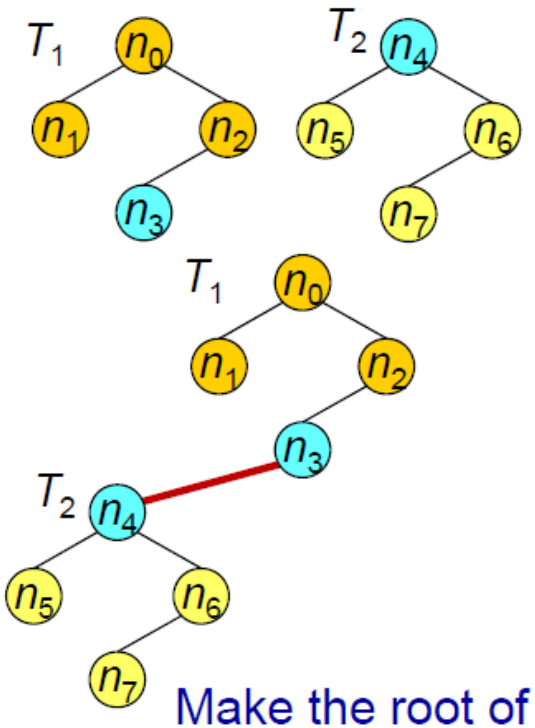


$height_{new} \le height_1 + height_2$

$width_{new} = \max(width_1, width_2)$

Horizontal Merging



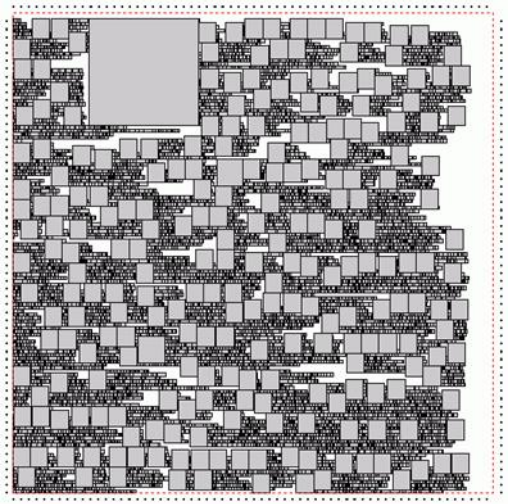


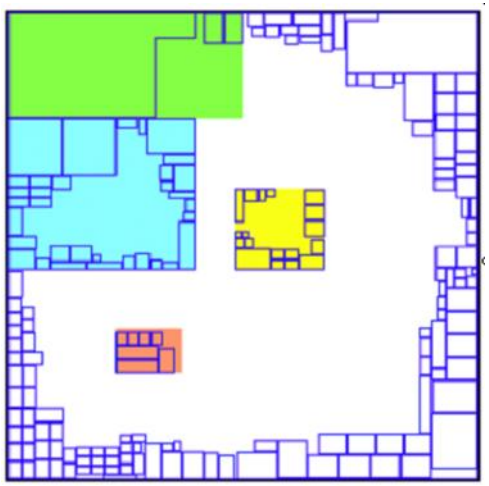
$height_{new} = max(height_1, height_2)$
$width_{new} = width_1 + width_2$

Make the root of the right B*-tree as the left child of the node corresponding to the right-most module of the left B*-tree.

Macro Placement/Floorplanning

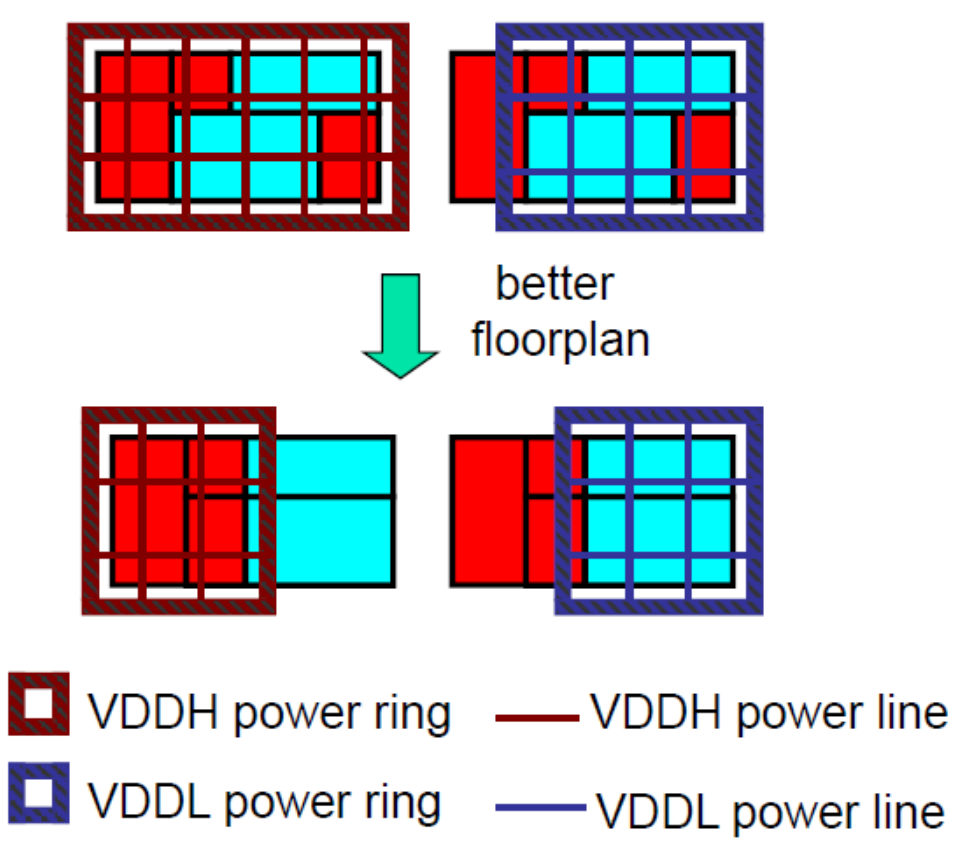
- Mixed sized cell/block placement/floorplanning: apply floorplanning techniques for macros to address various design constraints, e.g., range constraints, block rotation, block sizing

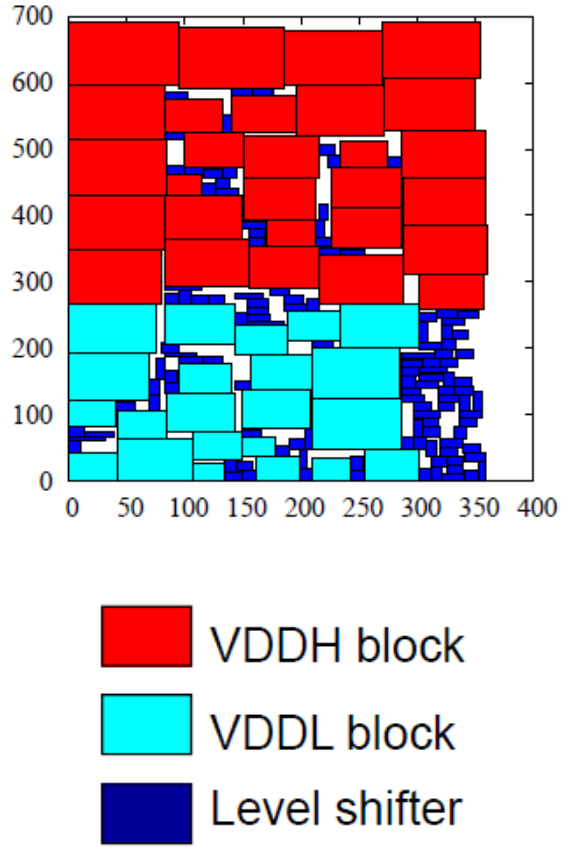




Voltage Island Aware Floorplanning

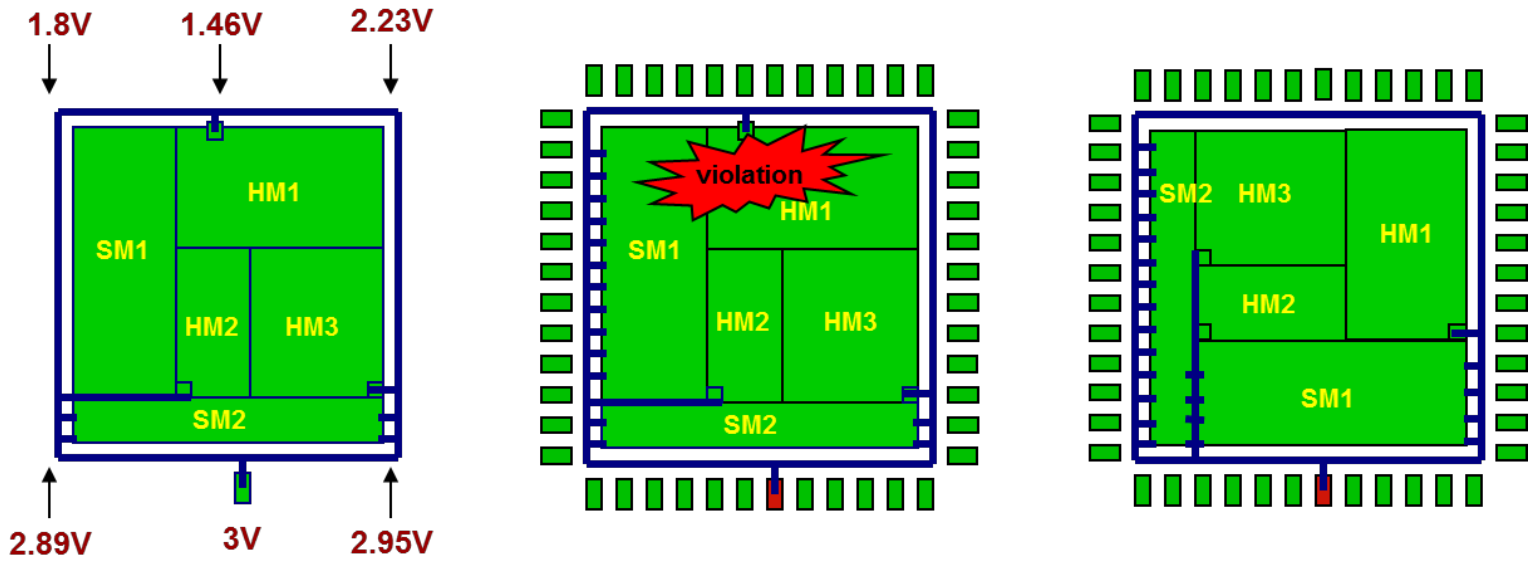
- Multiple supply voltages (voltage islands)





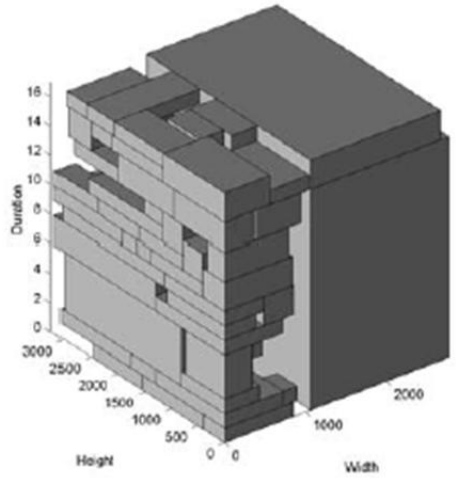
Voltage Drop Aware Floorplanning

- Power/ground networks for static/dynamic IR drop minimization (voltage drop aware floorplanning)



Beyond 2D Floorplanning

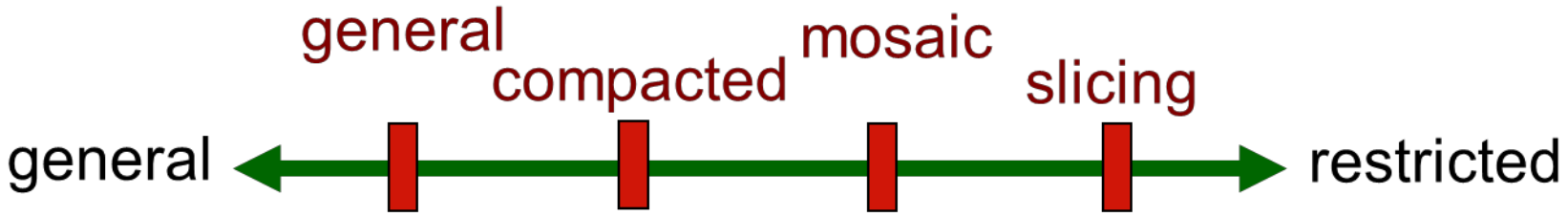
- Floorplanning for reconfigurable computing



- Floorplanning for digital microfluidic biochips
- SiP/2.5D/3D floorplanning

Existing Floorplan Representations

- Slicing: slicing tree, normalized Polished expression
- Mosaic: corner block list (ICCAD'00), twin binary tree (ISPD'01)
- Compacted: O-tree, B*-tree, corner sequence (TVLSI'03)
- General: sequence pair, bounded-sliceline grid (ICCAD'96), transitive closure graph (DAC'01), TCG-S (DAC'02), adjacent constraint graph (ICCD'04)



Comparison

Representation	Solution Space	Packing Time	Flexibility
Normalized Polish Expression	$O(n!2^{3n}/n^{1.5})$	$O(n)$	Slicing
Corner Block List	$O(n!2^{3n})$	$O(n)$	Mosaic
Twin Binary Sequence	$O(n!2^{3n}/n^{1.5})$	$O(n)$	Mosaic
O-tree	$O(n!2^{2n}/n^{1.5})$	$O(n)$	Compacted
B*-tree	$O(n!2^{2n}/n^{1.5})$	$O(n)$	Compacted
Corner Sequence	$\leq (n!)^2$	$O(n)$	Compacted
Sequence Pair	$(n!)^2$	$O(n^2)$	General
BSG	$O(n!C(n^2, n))$	$O(n^2)$	General
Transitive Closure Graph	$(n!)^2$	$O(n^2)$	General
TCG-S	$(n!)^2$	$O(n \lg n)$	General
Adjacent Constraint Graph	$O((n!)^2)$	$O(n^2)$	General

Existing Floorplanning Problems

- Outline free (variable die)
- Fixed outline (fixed die)
- Hard modules only
- Soft (and hard) modules
- Large scale
- Mixed size
- Pre-placed modules
- Range-constrained modules
- Boundary-constrained modules
- Abutment-constrained modules
- Symmetry-constrained modules
- Rectilinear modules
- Analog placement
- Beyond 2D

Existing Floorplanning Problems (cont'd)

- Co-synthesis with
  - Voltage islands
  - Power supply planning (voltage drop)
  - Interconnect planning
  - Bus planning
  - Buffer planning
  - ...