



PCB & RELIABILITY @ AT&S

Basic Training
Steinberger Anke

August 2023

PCB & RELIABILITY @ AT&S

01 Introduction Round & Agenda

02 AT&S at a Glance

03 PCBs?

04 Materials

05 Process Flow

06 Reliability

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06 Reliability



ADVANCED TECHNOLOGIES & SOLUTIONS

July 2023



WHAT GUIDES US

VISION

**FIRST CHOICE FOR
ADVANCED SOLUTIONS**

MISSION

We set the highest quality standards in our industry
We industrialise leading-edge technology
We care about people
We reduce our ecological footprint
We create value



ABOUT US

AT&S

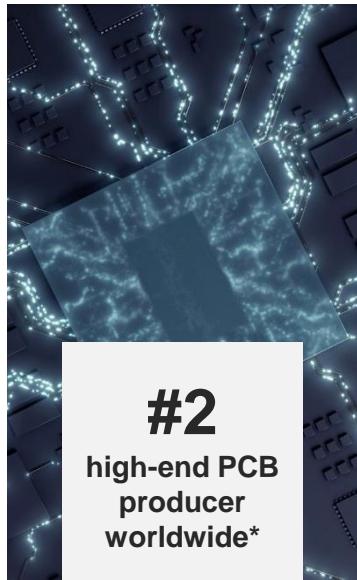


Information shared is covered within NDA

WORLD LEADING HIGH-TECH PCB & IC SUBSTRATES COMPANY



€ 1.8bn
revenue in
FY 2022/23



#2
high-end PCB
producer
worldwide*



#5
IC substrates
producer
worldwide**



~15,000
employees



6
plants in
Europe and
Asia

*Source: Prismark, CY2022, as of 15.05.2023

**Source: Prismark, CY2021, as of 15.05.2023

GLOBAL FOOTPRINT FOR FAST SUPPLY CHAIN & COST EFFICIENCY



**Leoben Hinterberg
Headquarters**
Austria

Fehring
Austria

Nanjangud
India

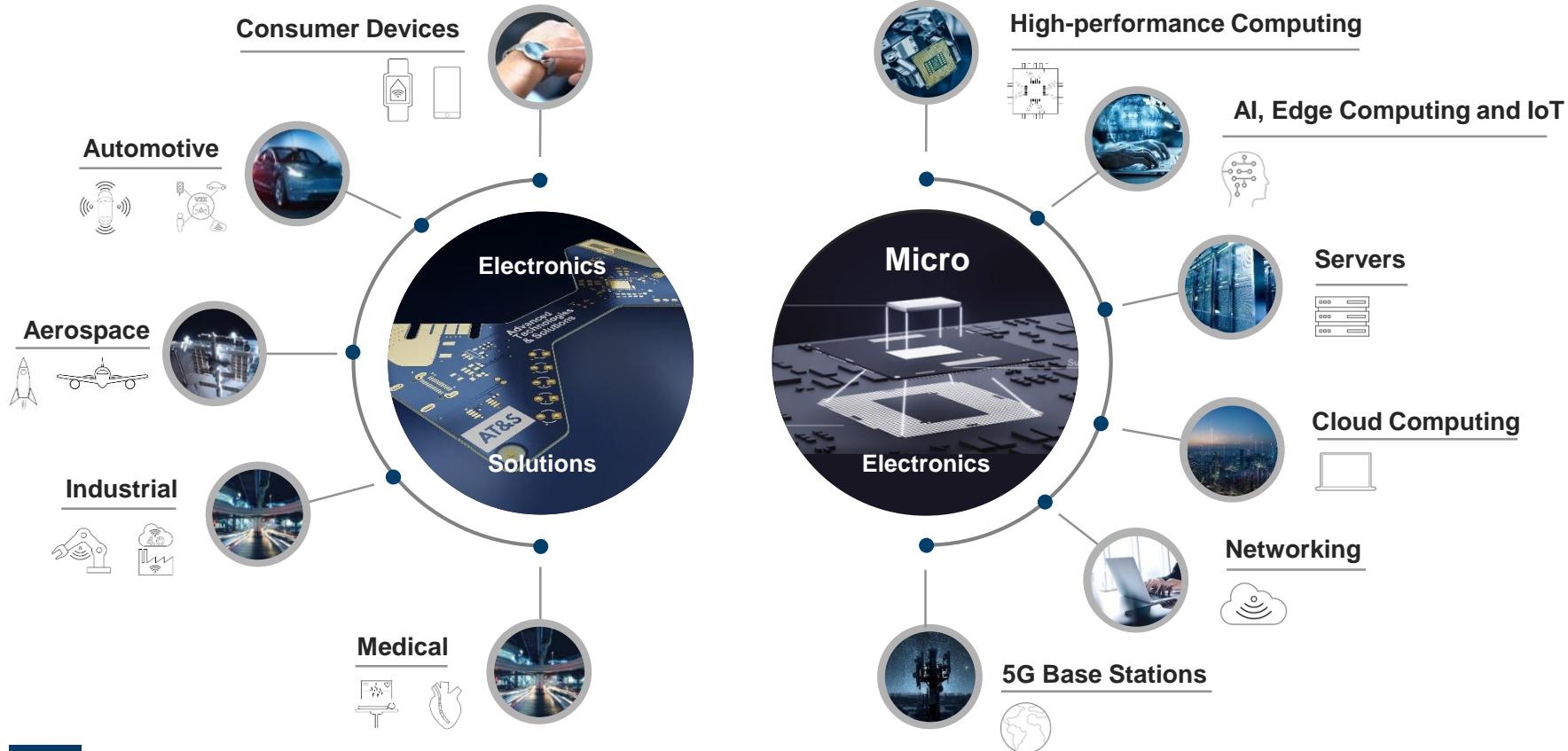
Chongqing
China

Shanghai
China

Ansan
Korea

Kulim
Malaysia
Start of Production
2024

MARKET SEGMENTS & PRODUCT APPLICATIONS



MILESTONES IN THE GROUP'S HISTORY (1/3)

Group is founded,
emerging from
several companies
owned by the
Austrian State



Indal Electronics Ltd.,
largest Indian printed
circuit board plant
(Nanjangud) is acquired
– today, AT&S India
Private Limited

Korean flexible PCB
manufacturer, Tofic
Co. Ltd. is acquired
– today, AT&S Korea
Co., Ltd.

New production setup:
Austrian plants produce
for high-value niches in
the automotive and
industrial segment;
Shanghai focuses on
the high-end mobile
devices segment

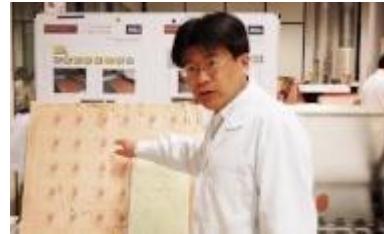
1987 **94**



Group is
privatized
and acquired
by Androsch,
Dörflinger,
Zoidl

99

Initial public
offering on
Frankfurt Stock
Exchange.



2001

06

Move to
Shanghai – to
set up one of
the leading HDI
production
sites in the
world

08 **09**

AT&S changes
to Vienna Stock
Exchange

MILESTONES IN THE GROUP'S HISTORY (2/3)



Construction on new plant in Chongqing, China starts. Capacity increase in Shanghai by 30%

2010

Production starts at plant II in India

11

AT&S enters the IC substrate market in cooperation with a leading manufacturer of semiconductors

13

After record high sales and earnings, AT&S decides to increase the investment program in Chongqing

15



AT&S starts serial production of IC substrates at the plant in Chongqing

16



AT&S introduces mSAP technology in Shanghai and Chongqing

17

MILESTONES IN THE GROUP'S HISTORY (3/3)

Construction of plant 3
in Chongqing for IC
substrates starts



Ramp-up of
Chongqing plant 3



Roof closing
plant 1 in Leoben
Hinterberg

18

19

21

22

23

Second expansion
phase at plant 1 in
Chongqing starts

Construction of
plant in Kulim,
Malaysia, starts



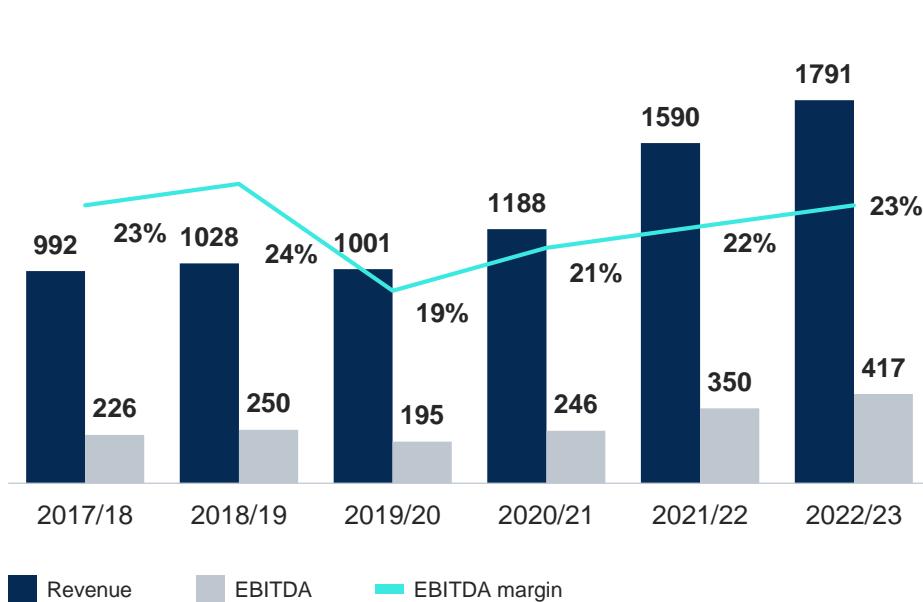
Construction of plant 3
in Leoben Hinterberg
for R&D center and
IC substrates starts



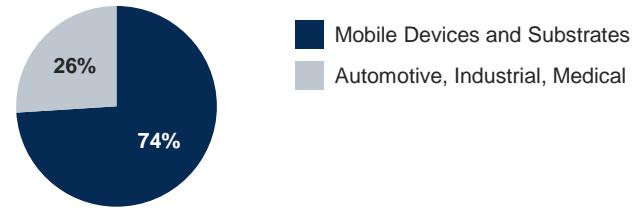
Roof closing of
plant 1 in Kulim and
move in of tools

A SUSTAINABLY GROWING COMPANY

In € mn

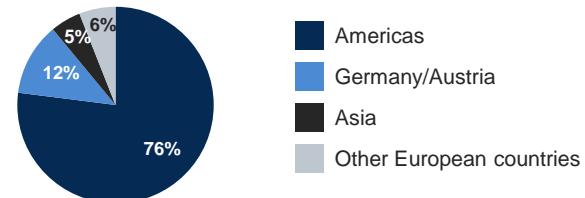


Revenue split by segment: FY 22/23



Revenue split by customer: FY 22/23

Based on customer's headquarters



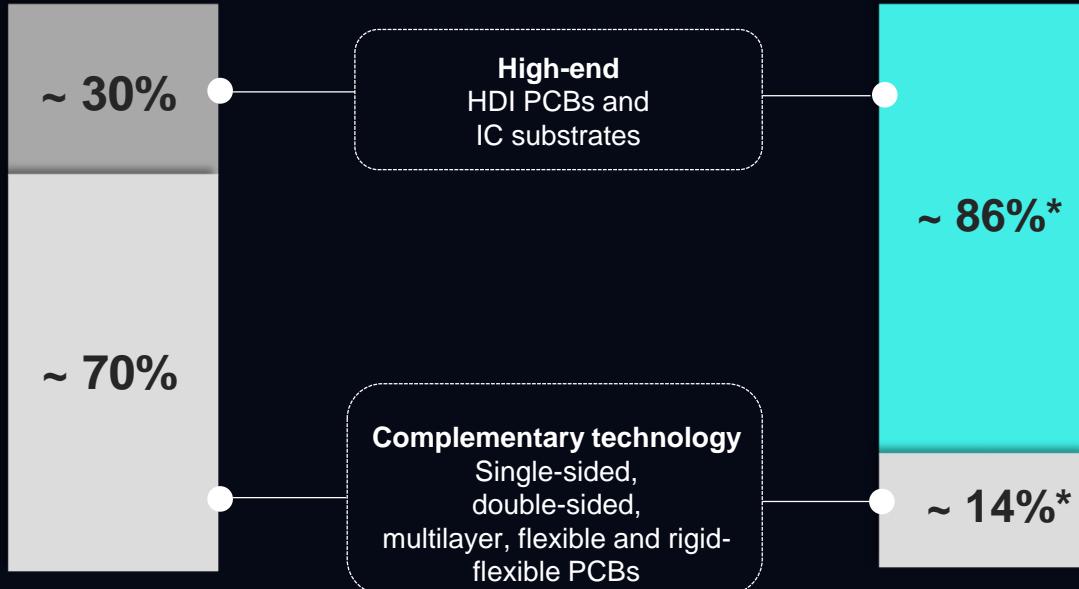
WHAT WE DO

AT&S



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STRATEGIC FOCUS ON HIGH-END TECHNOLOGIES

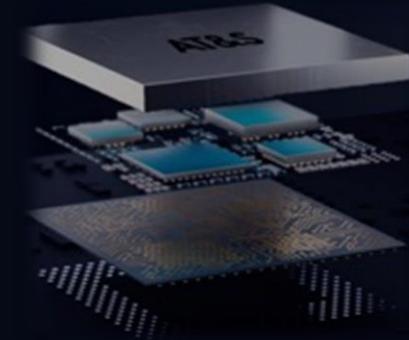


**General PCB and IC
substrate market**

AT&S revenue

*for FY 2021/22; Source: ACT, AT&S

Information shared is covered within NDA



R&D – BASIS FOR TECHNOLOGY LEADERSHIP

10.2%

R&D rate
(corresponds to
€ 183 mn)

R&D

HQ Austria
Development up to
series production at
the production sites

More than
700
Patents

35.6%

Vitality Index*

International
R&D partners ➤

Status: FY 2022/23

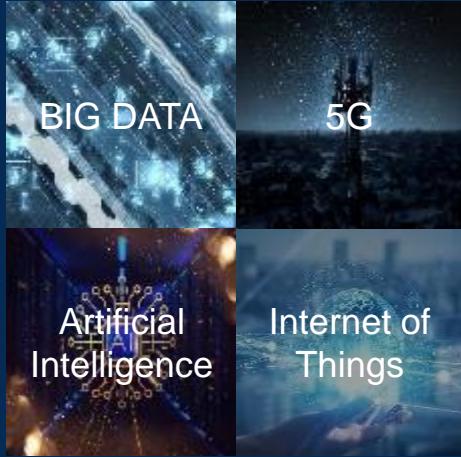
*Share of revenue of technologically innovative products made
in the last three years



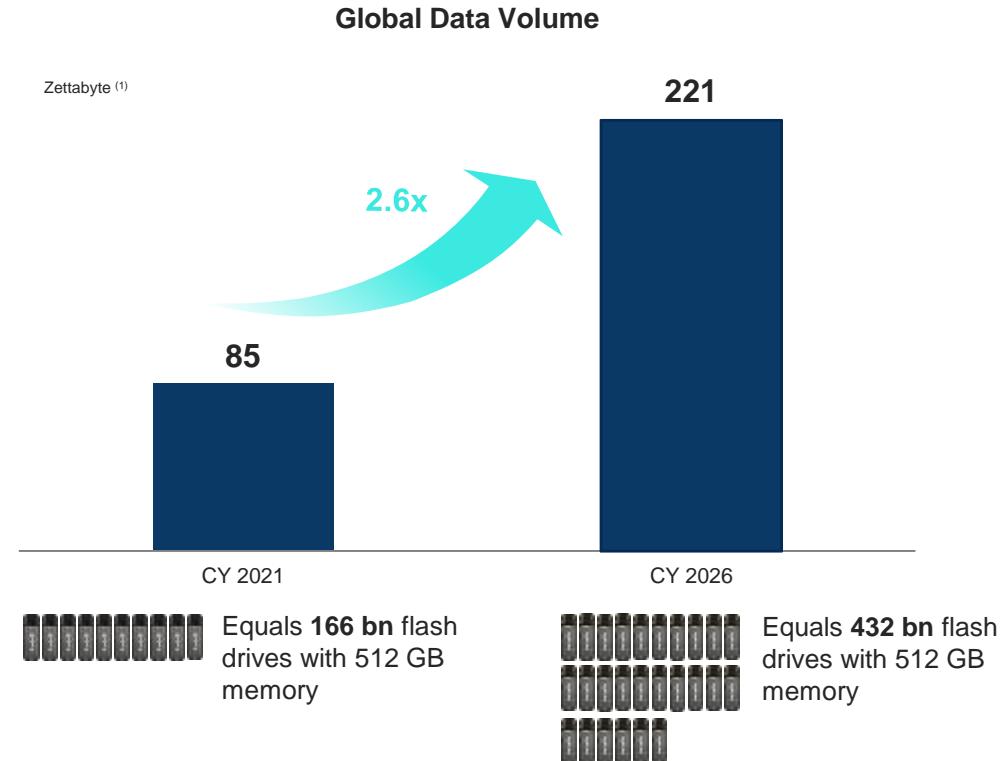
STRATEGIC BUSINESS DRIVERS

AT&S





... IN THE MICROELECTRONICS INDUSTRY



DATA AS THE KEY GROWTH DRIVER

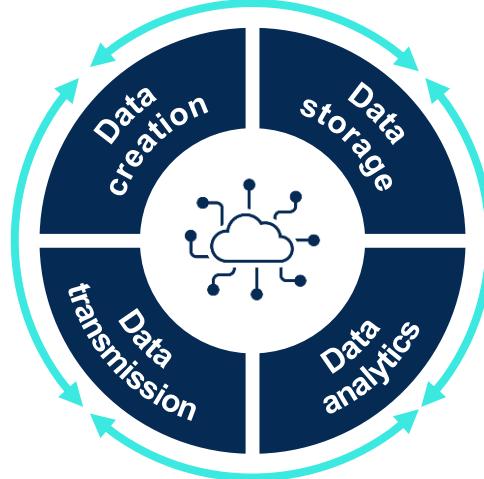
SIGNIFICANT DATA VOLUME GROWTH

Digitalisation requires data management

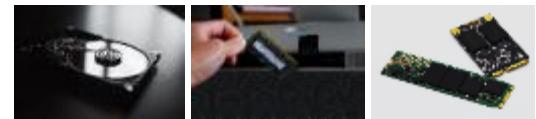
Consumer electronics | ADAS |
Industry 4.0 | Medical applications |
Internet of Things | ...



Wireless infrastructure |
Wireline infrastructure | Satellites



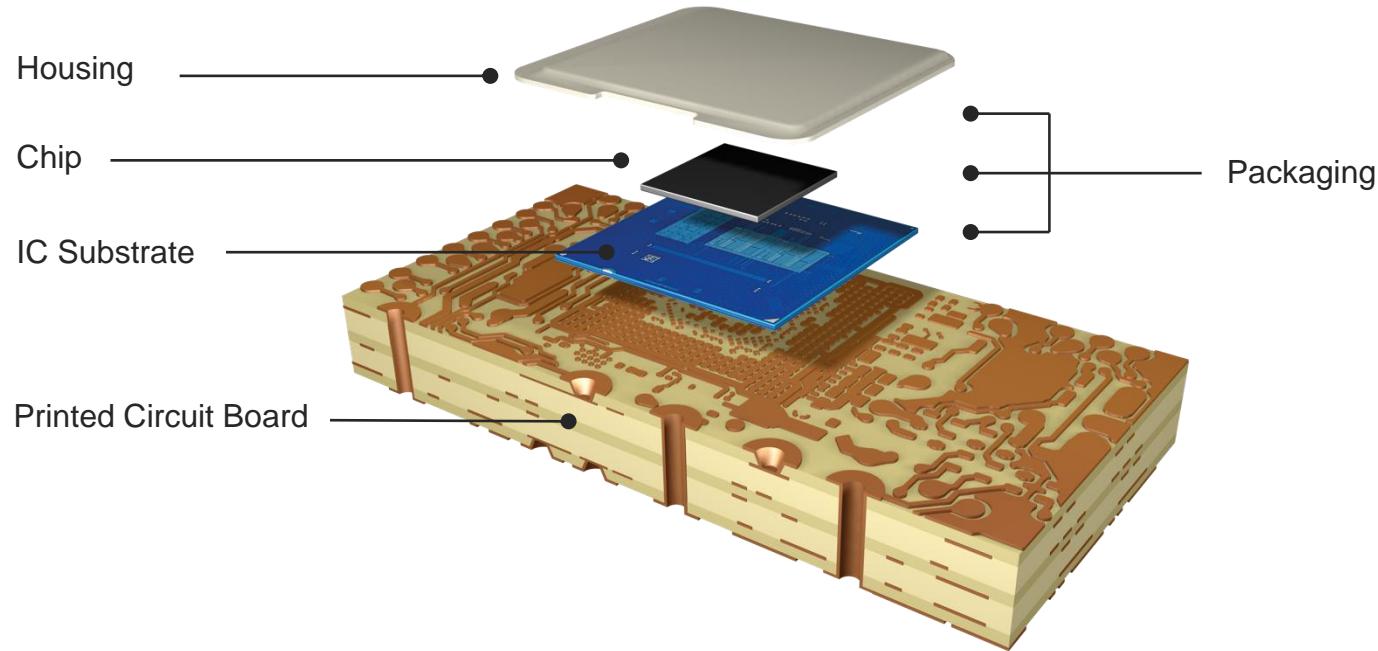
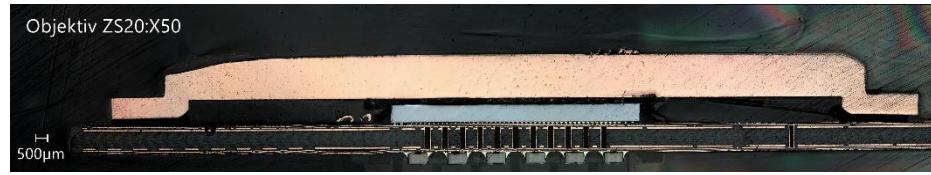
HDDs | DRAMs | NANDs



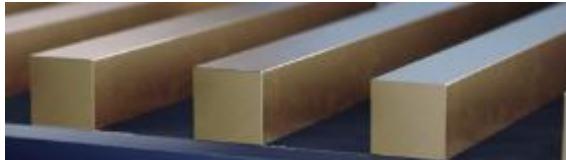
Data centres | Servers |
Big Data | In-Memory

MICROELECTRONICS PACKAGING

- Energy efficient
- Cost efficient
- More powerful



AT&S IS ENABLING GLOBAL DIGITALISATION



Miniaturisation

Increased computing power for fast data processing



Modularisation

More functionality at same or reduced space



Increased speed / Low latency

Communication of high data volumes (5G, Autonomous Driving)



Increased power / Power efficiency

Reducing non-value adding electrical loss

**WE INVEST
IN OUR
FUTURE**

AT&S



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KULIM – THE PROGRESSION

High-end production

- **Gross floor area:** 255,000 sqm
- **Production area / Cleanroom:** 111,200 sqm
ISO 5-7 (100* – 100,000)

Number of planned workforce: 6,000

Construction started: November 2021

Setting up first machines: February 2023

Moving into office: September 2023

Start of serial production: end of 2024

*3.531 <0.5um particle per m³



LEOBEN – COMPETENCE CENTER FOR EUROPE

High-end production

- **Gross floor area:** 39,000 sqm on 3 levels
- **Cleanroom:** 11,000 sqm ISO 5-7 (100* – 100,000)
- **R&D-area:** 2,300 sqm

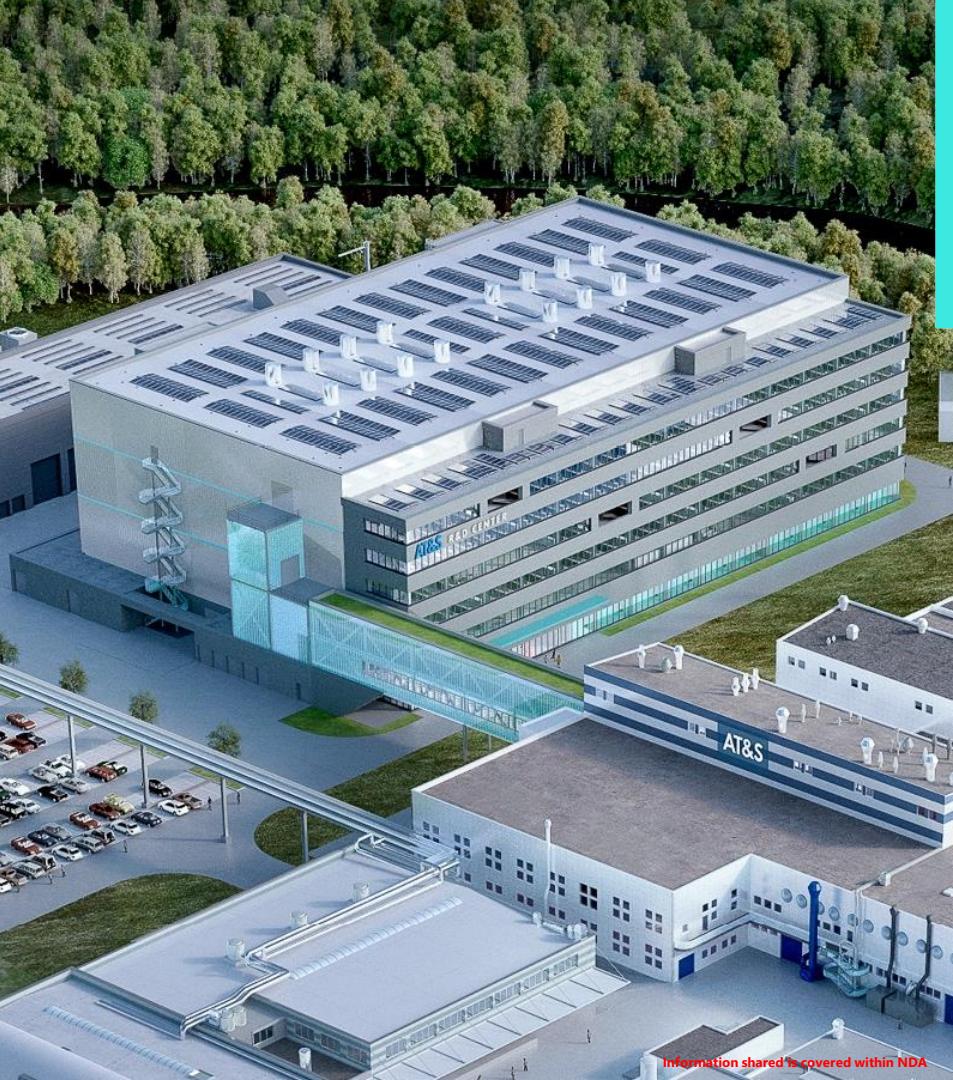
Number of planned workforce: 800

Construction started : February 2022

Setting up first machines : April 2023

Start of production: 2024

*3.531 <0.5um particle per m³





AT&S

ADVANCED TECHNOLOGIES & SOLUTIONS

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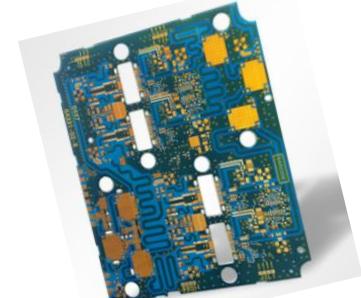
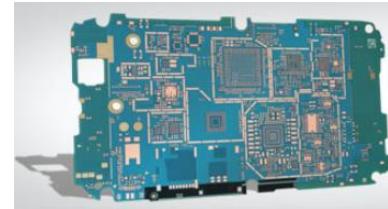
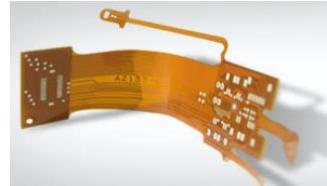
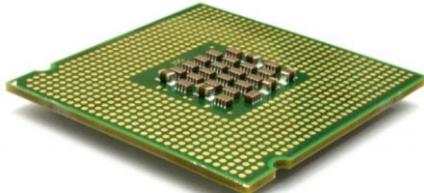
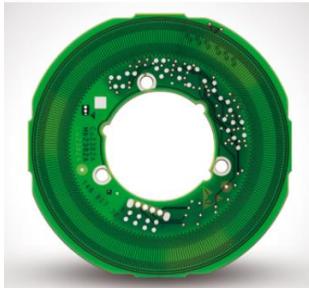
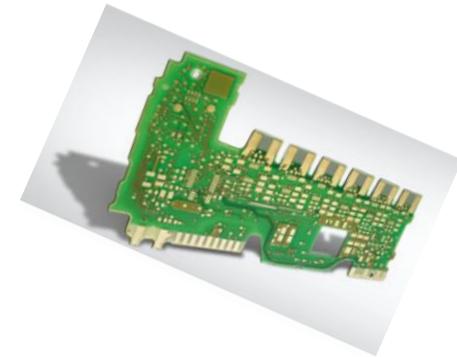
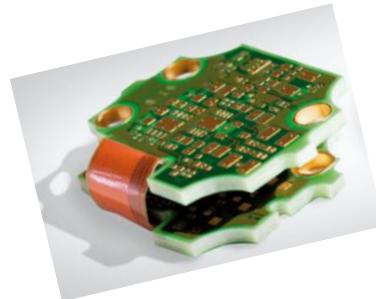
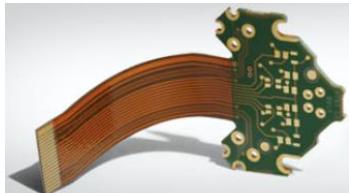
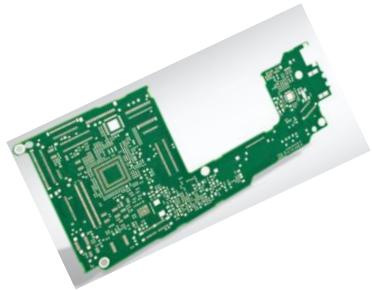
03 PCBs?

04 Materials

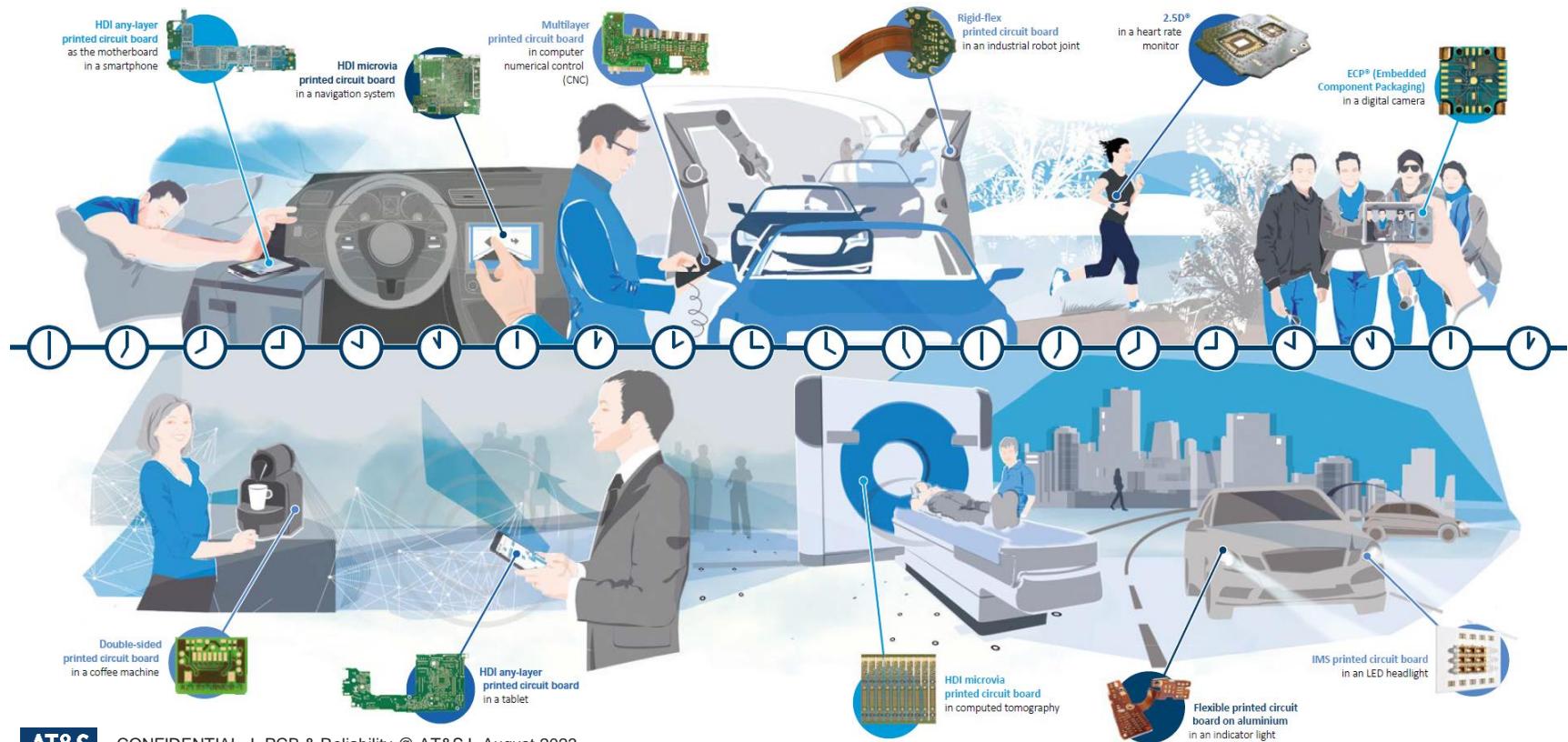
05 Process Flow

06 Reliability

PCB? PRINTED CIRCUIT BOARD



A DAY WITH AT&S



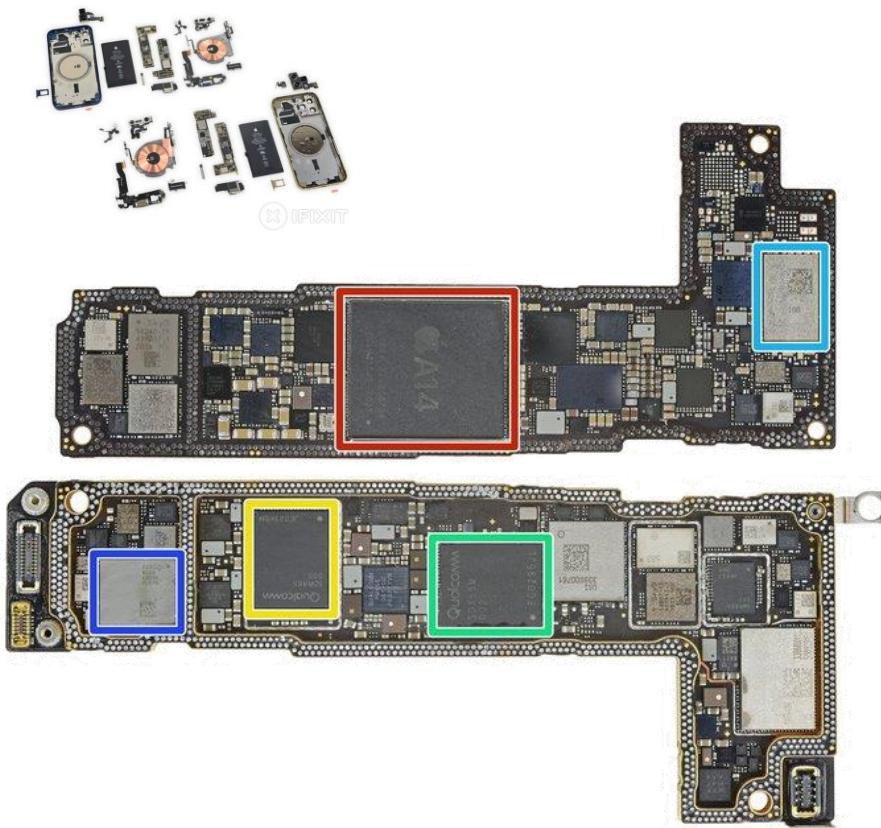
FUNCTIONS OF A PCB

Backbone of Electronic Systems

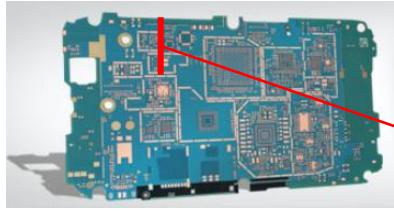
A PCB is the “**neural system**” of any electronic device.

A PCB is the part of an electrical system that ...

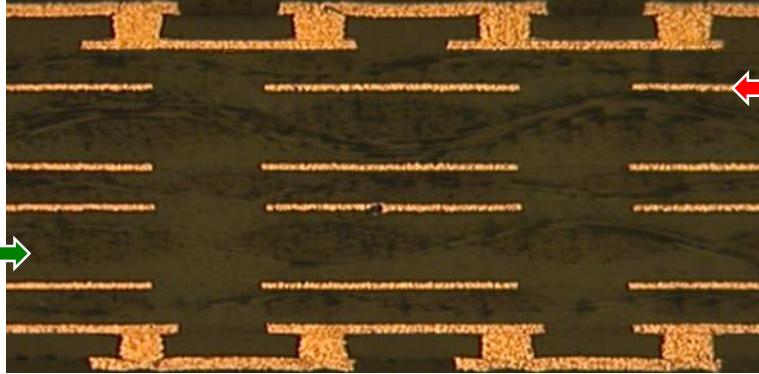
- **supports / carries** electronic components mechanically and
- **connects** the components electrically.



WHAT'S INSIDE?



Cross sectional view:



Copper

- Mainly Epoxy based materials
- Resin sheets
- Plain weave ($0^\circ/90^\circ$ fabric) laminates or preprints
- Different fabrics

- Electrodeposited copper foils
- Plated copper
- Thickness 12 μm to 70 μm

A PCB is a highly complex composite

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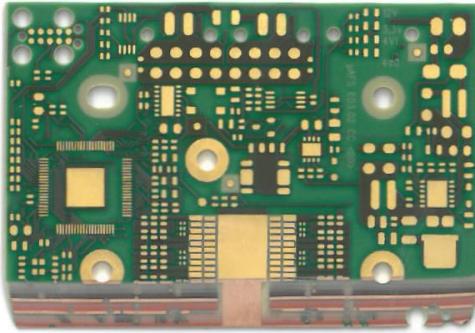
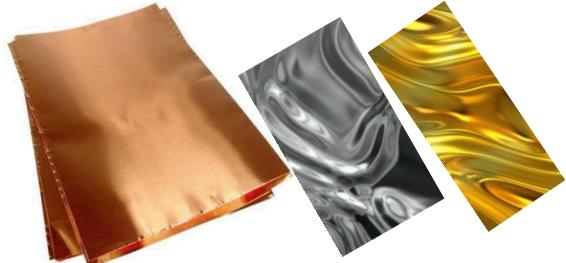
06 Reliability

MATERIALS WITHIN A PCB

Overview

Metallic materials:

- **Copper Cu** as conductive material within each layer
- **Gold Au** as conductive and inert surface finish
- **Nickel Ni** as conductive barrier layer between Cu & Au
- Other metallic surface finishes like tin Sn, silver Ag, palladium Pd (in combination with Ni/Au)...



Ceramic materials:

- **Glass fabric/ balls** as non-conductive stiffeners within the dielectric layers

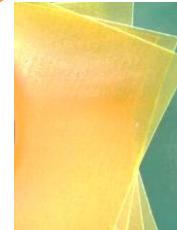
Organic materials:

- **Epoxy resins** as non-conductive polymeric components of the dielectric layers; acts as adhesive & connects the different layers
- **Epoxy resins** as non-conductive surface finishes like solder masks

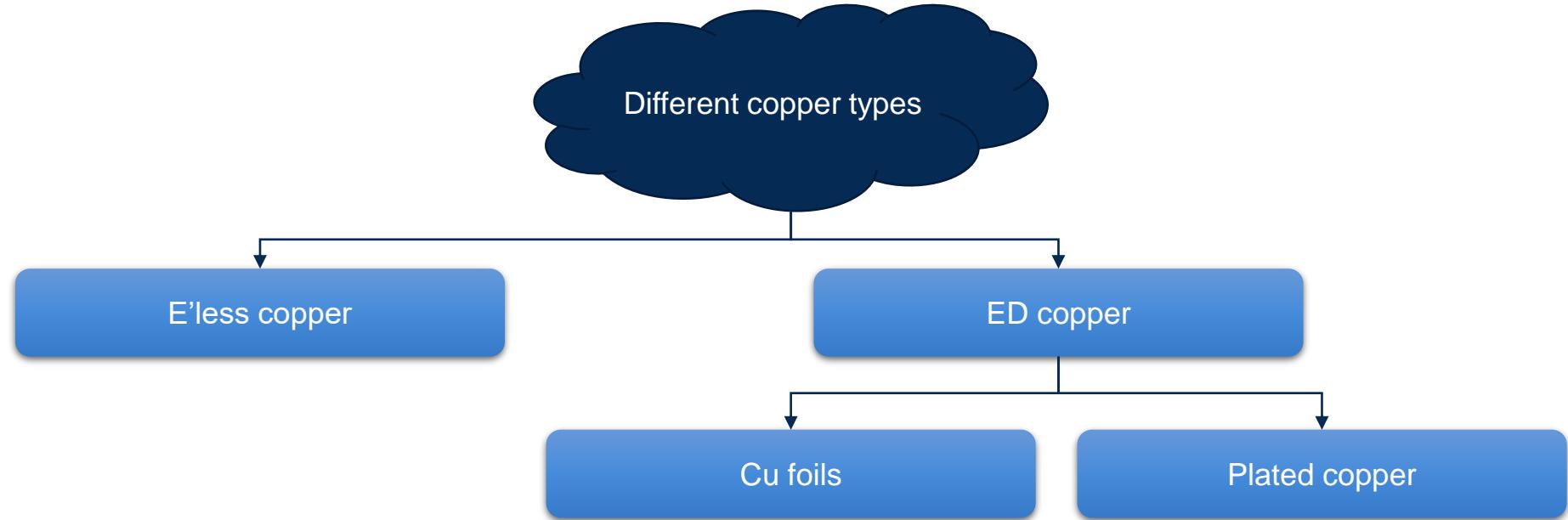


Compound materials:

- **Prepregs** (pre-impregnated glass fabrics) as dielectric materials for each layer of the PCB (compound made of glass fabrics + epoxy resins)



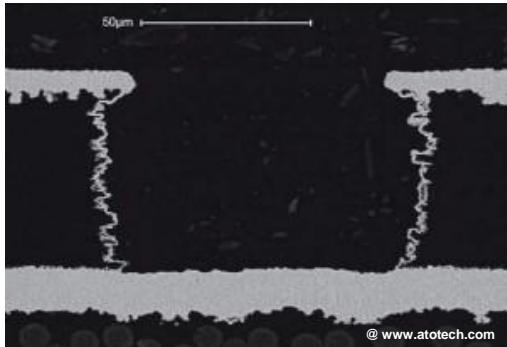
COPPER



COPPER

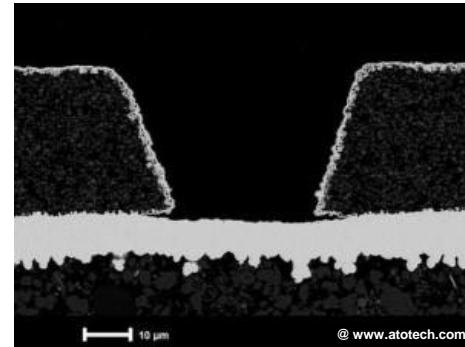
E'less (chemical) Copper

Creates a very thin conductive layer all over the panel:



Used before the plating process:

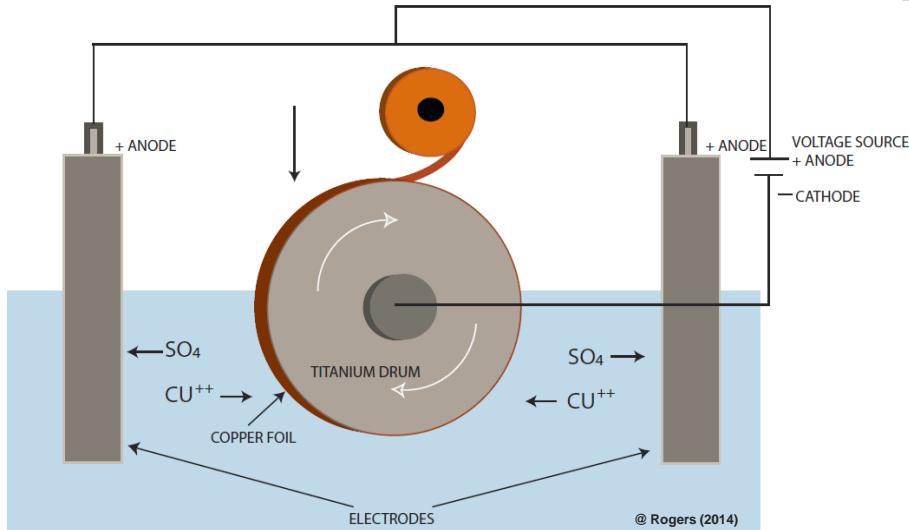
- All over the full surface including the hole walls
- To ensure a conductive surface and to be able to use the electrolytic plating
- “Copper seed layer”
- Layer thickness: 0,5μm – 1μm



COPPER

ED (electro deposited) Copper

Electro deposition process for copper foils:



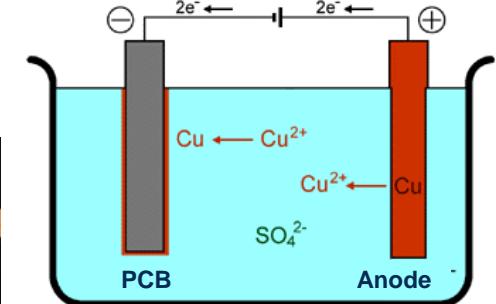
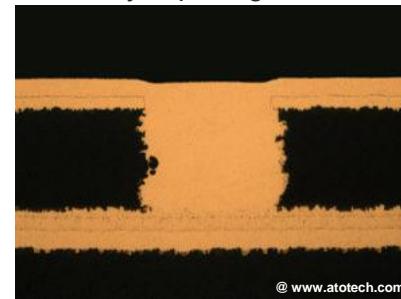
Used as foils:

- On the core
- For every lamination step to cover the prepreg



Used in/ as plating process:

- To achieve the needed Cu surface thickness
- To make the connection holes to the inner layers conductive
- "Electrolytic plating"



Used chemistry: CuSO_4

DIELECTRIC MATERIALS

Material Type	Base Material Construction	Flame Retardant
FR-1,-FR-2	Phenol-Cotton Paper laminate	No
FR-3	Epoxy-Cotton Paper laminate	Yes
FR-4	Epoxy-Glass / UV Block / Green Bi / Tetra / Multifunctional	Yes
FR-5	Epoxy-Glass High Tg	Yes
CEM-1	Composite Epoxy Material, Paper Core-Woven Glass Surfaces	Yes
CEM-3	Composite Epoxy Material, Non Woven Glass Core-Woven Glass Surfaces	Yes
Rigid-Flex	Epoxy-Glass-Polyimide	Yes
Rigid-PI	Polyimide	Yes

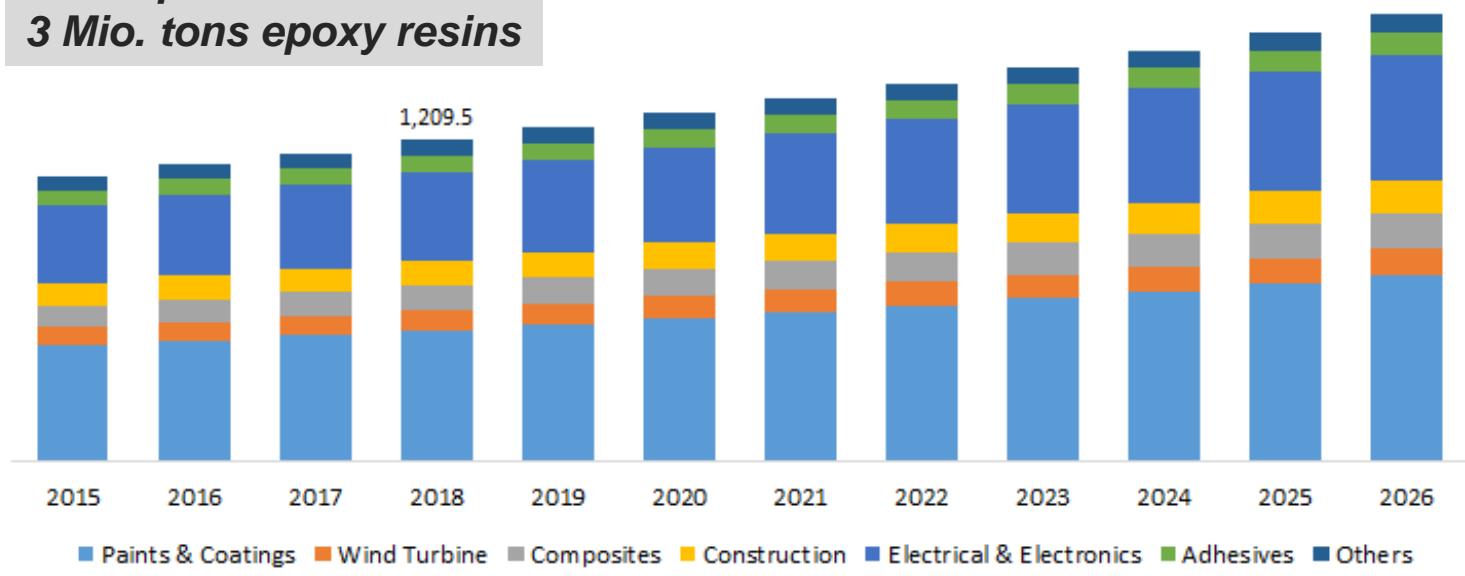
DIELECTRIC MATERIALS – SPECIAL RESINS

Material Type	Base Material Construction	Flame Retardant
Flex	Polyimide	No
Cyanate Ester	Cyanate Ester	Yes
BT	Bizmaelide Triazine	Yes
PTFE	Teflon	Yes*
Aramid	Epoxy-Polyaramide	Yes
Rogers 4000	Hydrocarbon-Glass Ceramic	Yes
PPE/PPO	Polyphenylenether/Oxide	Yes

EPOXY RESIN MARKET

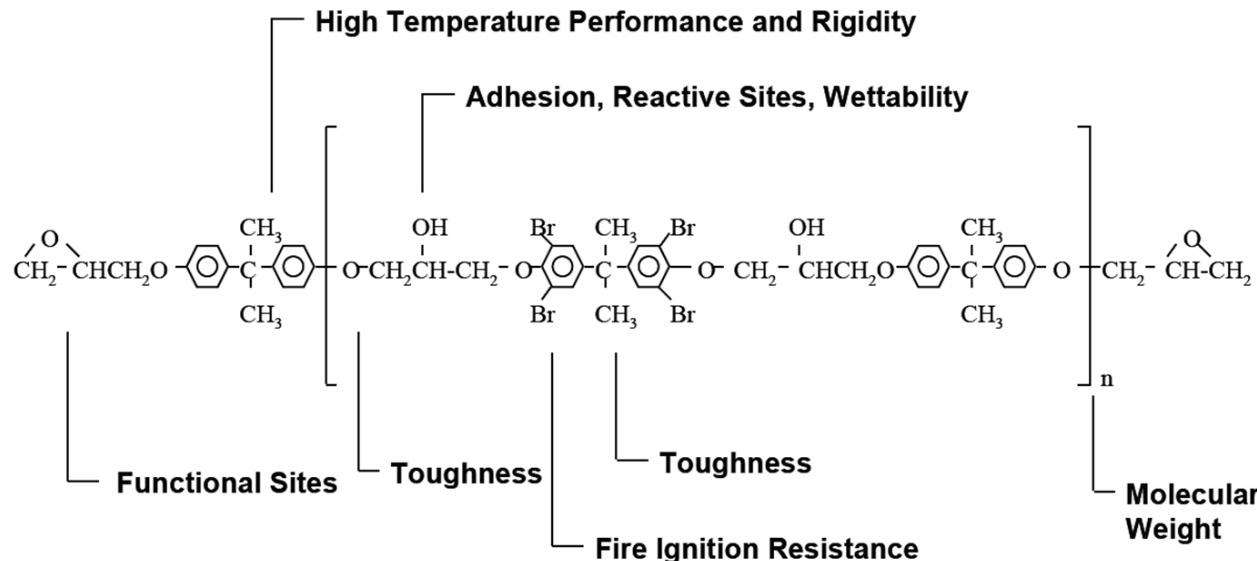
Europe Epoxy Resins Market, By Application, 2015 - 2026
(USD Million)

*World production 2017:
3 Mio. tons epoxy resins*



■ Source: The Socio-economic Value of Epoxy Resins, 2015

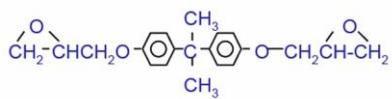
CHARACTERISTICS OF EPOXY RESINS



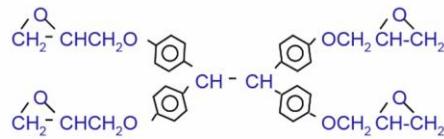
Diglycidyl Ether of Tetrabromo Bisphenol-A (DGETBA)

CHARACTERSITICS OF EPOXY RESINS

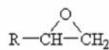
Difunctional Epoxy Resin



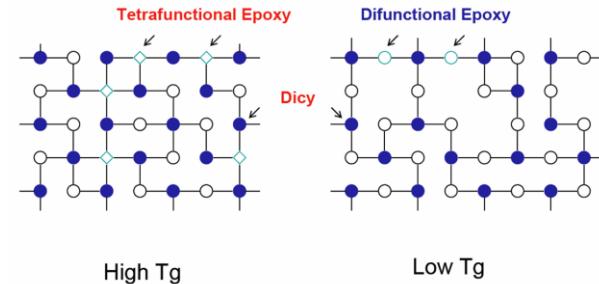
Tetrafunctional Epoxy Resin



Multifunctional Epoxy Resin



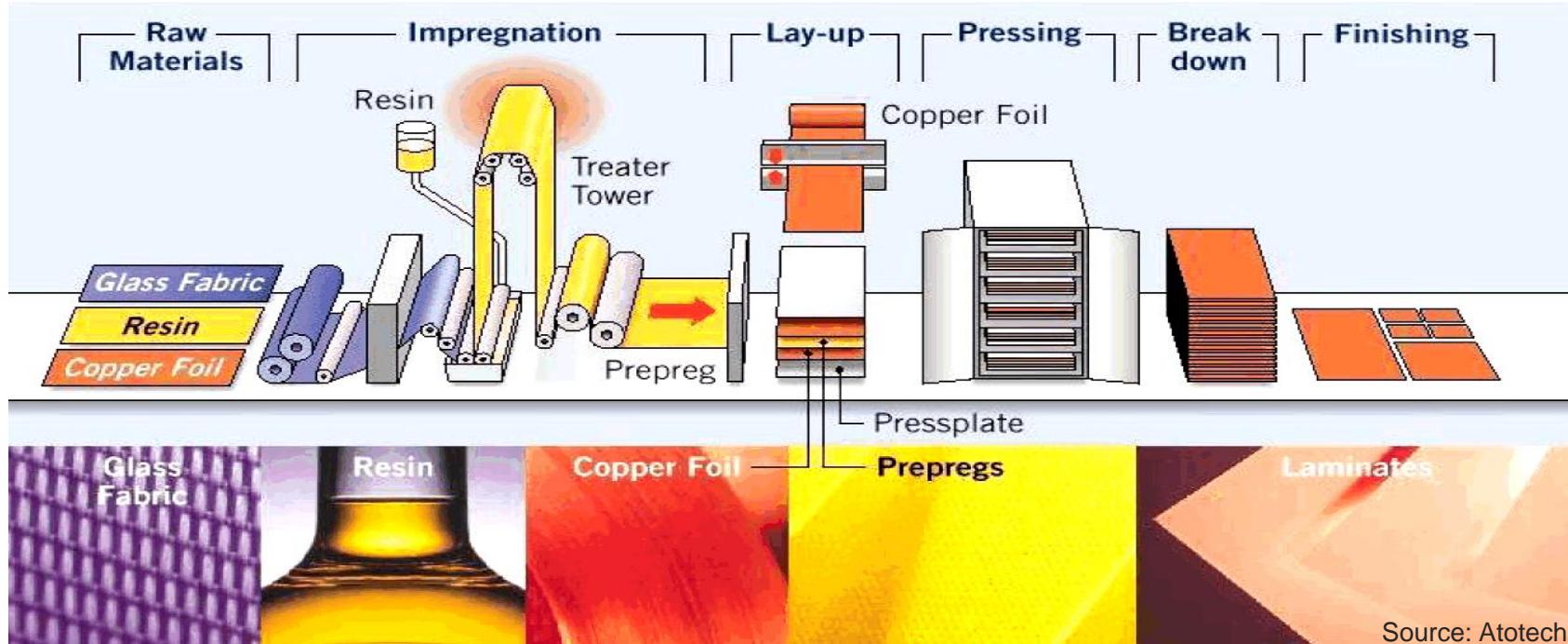
The epoxy group >=4



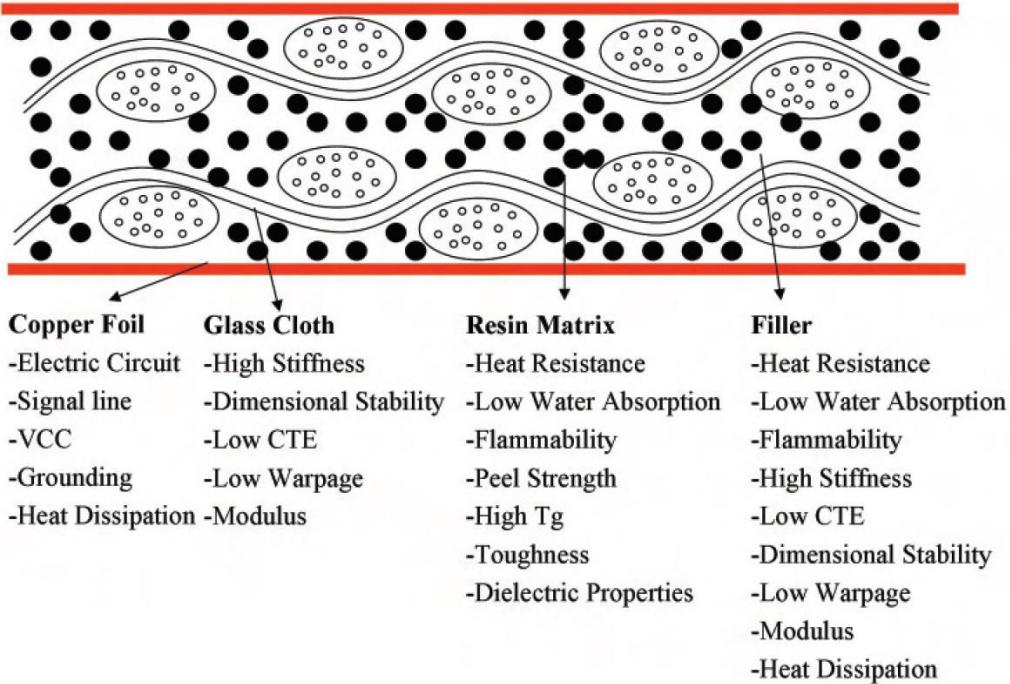
High degree of crosslinking („High Tg materials“)
preferred for high quality applications

- Better mechanics
- Lower thermal expansion (reliability!)
- Higher heat stability

MANUFACTURING OF LAMINATES



COMPOSITION OF A LAMINATE



Blended Varnish Composition

- Multifunctional Epoxy Resin(s)
- Functional Copolymer (e.g. PPE for low electrical loss)
- Curing agent (e.g. Dicyandiamide "Dicy", Phenolic hardener)
- Filler (Al_2O_3 , SiO_2 , AlN, BN)
- Flame retardant (Bromide, Phosphor based)

MATERIAL PROPERTIES

Direction-dependencies of material properties

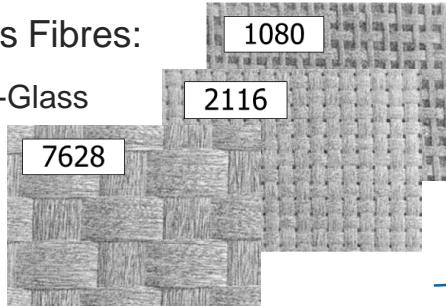
FR4-Resin:

- Epoxy
- Curing Agent
- Modifiers

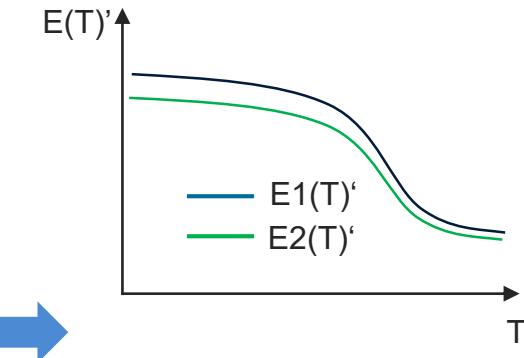
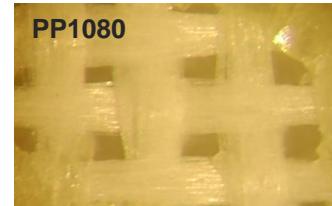
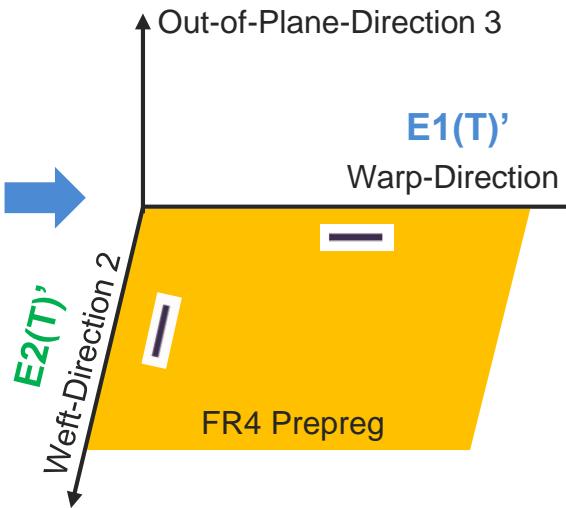


Glass Fibres:

- E-Glass



FR4-Prepreg



- The storage modulus in warp ($E1(T)'$) and weft direction ($E2(T)'$) is needed to set up a material model for simulation
- Both moduli can differ, even when the fabric is balanced
- Fabrics are defined in IPC4412A

FR4 MATERIALS TYPICAL PROPERTIES

Property	Value	Unit
T _G (Glass Transition)	+130 to +170	DegC
Density	1,4 – 2,0	g/cm ³
E-Modulus (tensile)	12 – 20	GPa
Ultimate strength	250 – 350	Mpa
Ultimate strain	2	%
CTE, z-axis below T _g	25 – 45	ppm
CTE, z-axis above T _g	90 – 250	ppm
Electrical Breakdown Voltage	40 – 80	kV
Permittivity, Dk	3,5 – 5,0	-
Flammability	UL94 V0	-
Thermal conductivity	0,3 – 0,8	W/mK

CTE

Coefficient of thermal expansion CTE

- Important value for all materials
- Describes the expansion of any material as a function of temperature
- Example values:

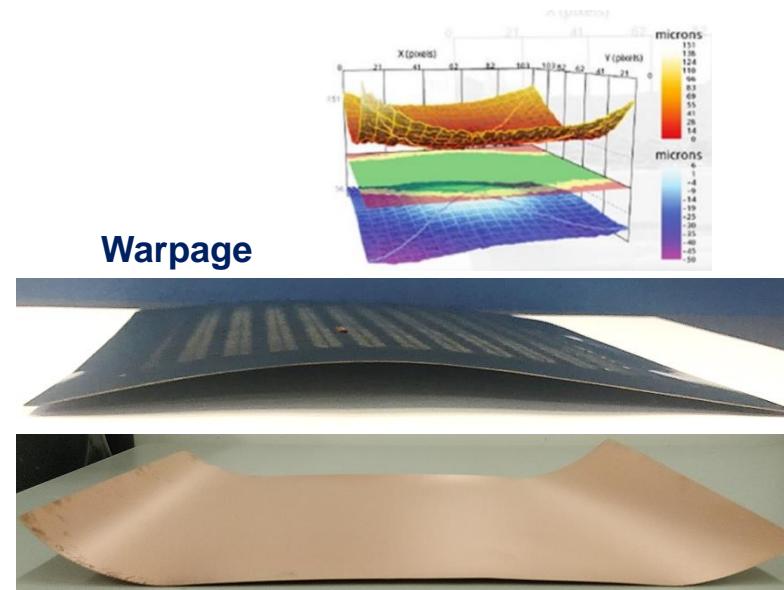
 CTE of copper: ~18ppm/K

 CTE of PP below TG: ~30ppm/K

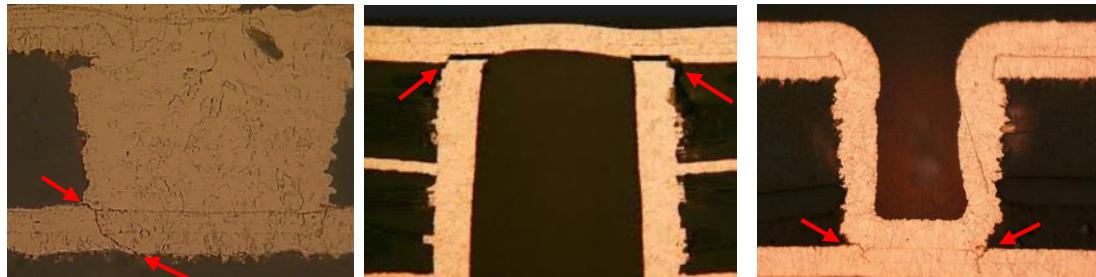
 CTE of PP above TG: ~150ppm/K

 CTE of Silicium: ~2,6ppm/K

- Causes warpage issues as well as thermo-mechanical fatigue failures



Cracks in copper/ thermo-mechanical fatigue failures



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03 PCBs?

04 Materials

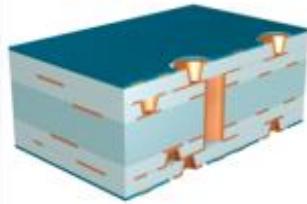
05 Process Flow

06 Reliability

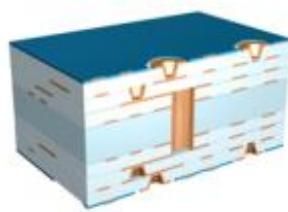
DIFFERENT BUILD-UPS

HDI Technology

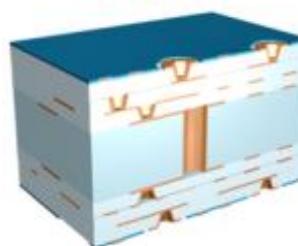
1-N-1



2-N-2

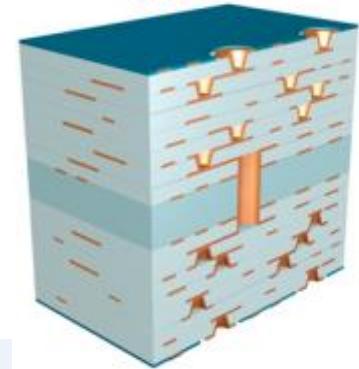


3-N-3

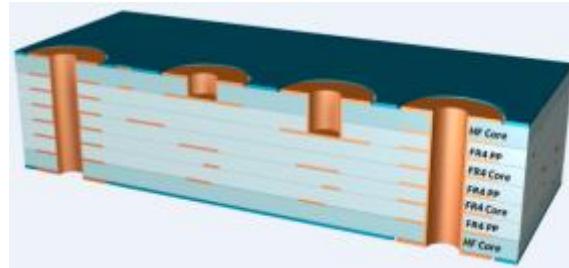
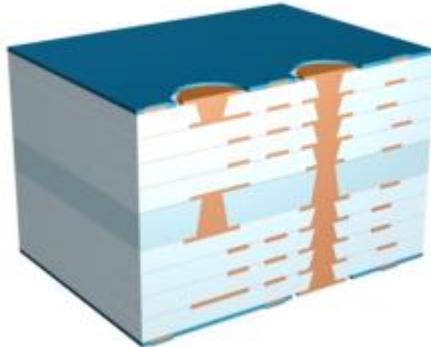


.....

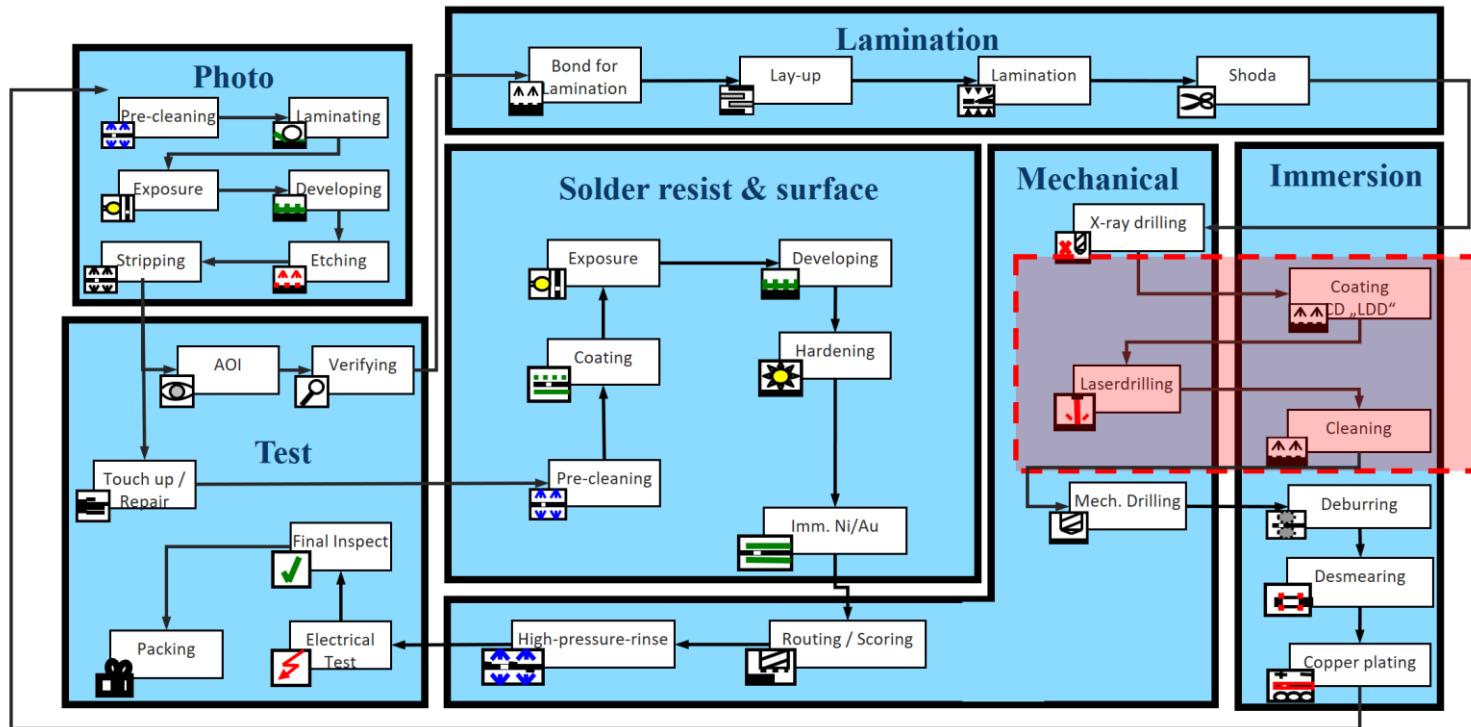
6-N-6



Anylayer 10 layers



PROCESS FLOW - OVERVIEW



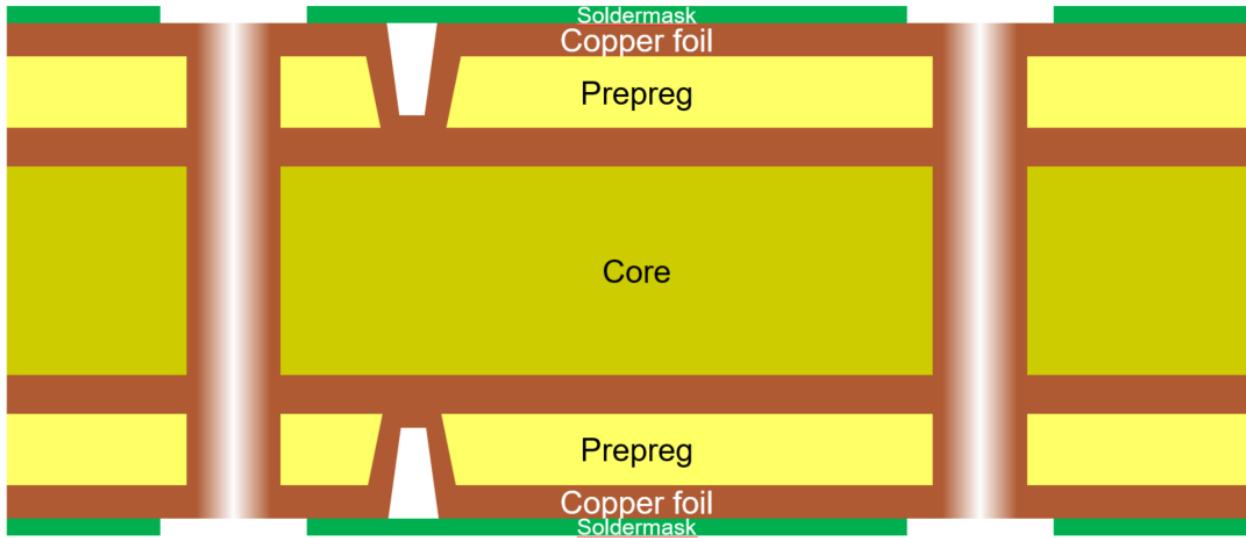
IP = Inner plane

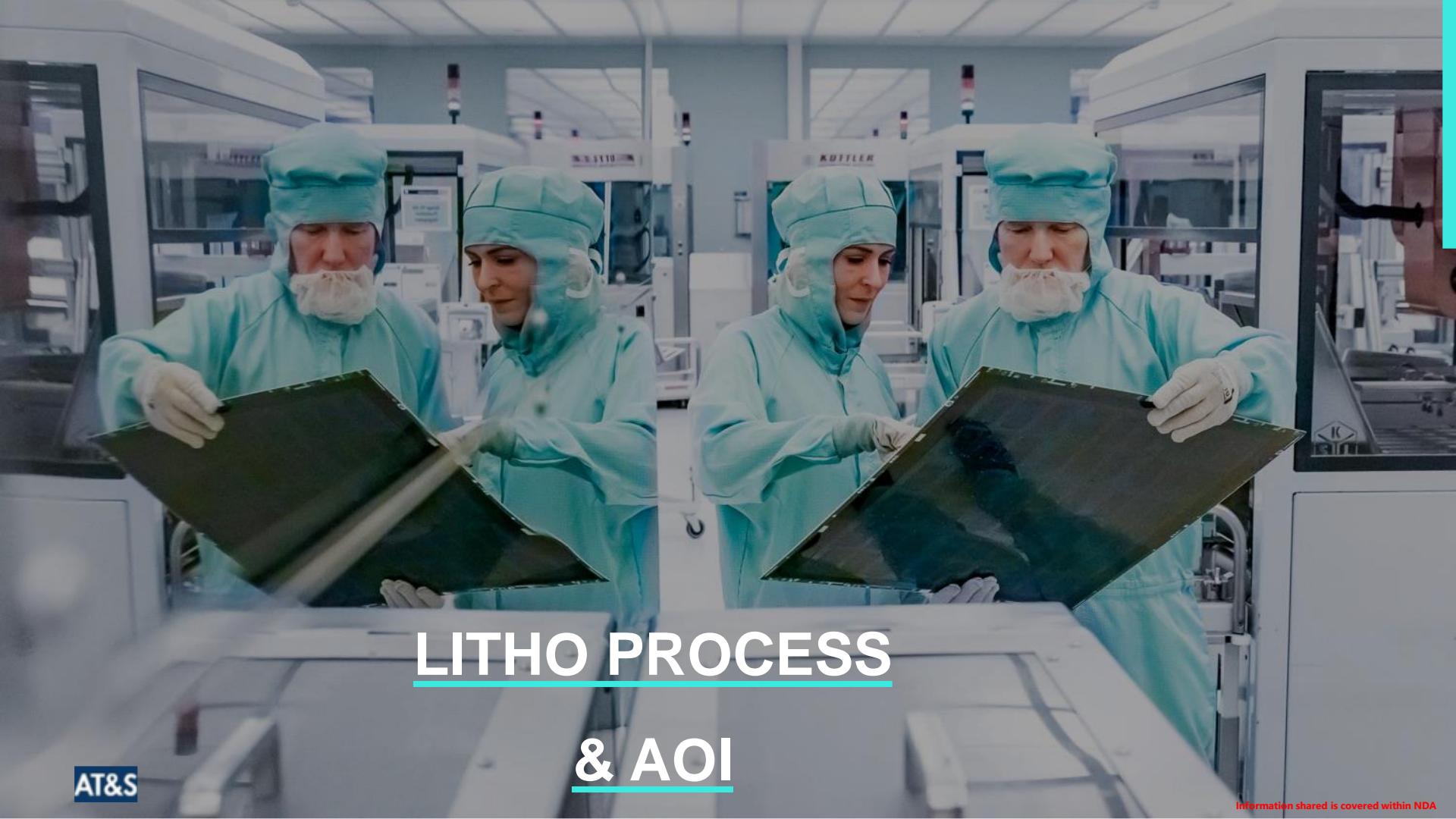
EP = External plane

HDI Laser process

PROCESS FLOW

Valid for a „4 layer multilayer with laser drilling from L1-L2 and L4-L3 and mechanical drilled holes from L1-L4 “ using the standard subtractive process



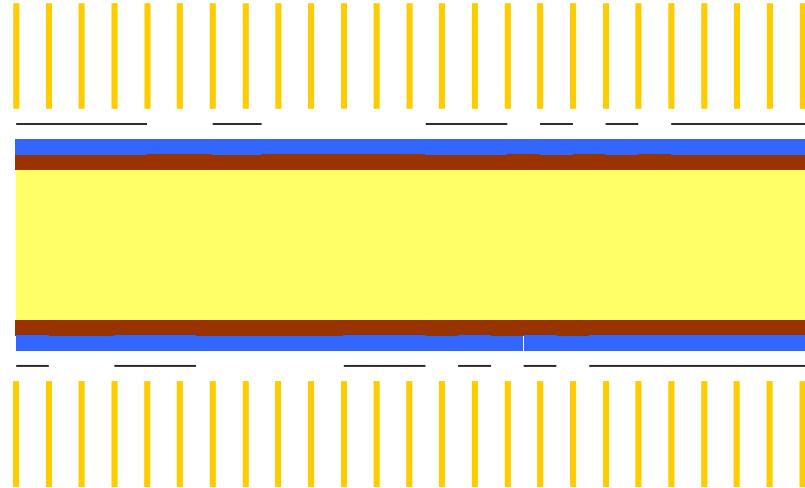
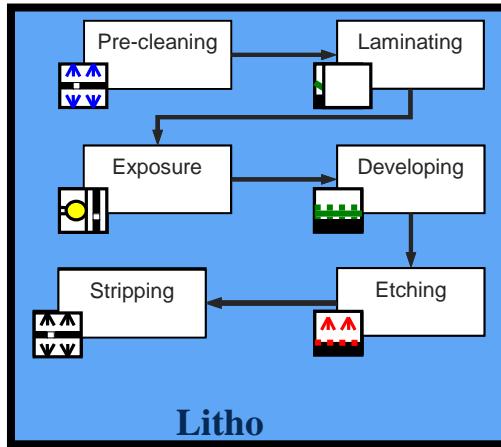


A photograph showing two technicians in full-body blue protective suits and hairnets working in a cleanroom. They are holding up large, dark rectangular panels, likely wafers or substrates, and examining them closely. The background shows various pieces of industrial equipment and monitors. The overall lighting is bright and clinical.

LITHO PROCESS

& AOI

LITHO PROCESS



Pre-cleaning

Removal of oxidation and residues, as well as light roughening of the surface

Laminating

Photosensitive dry film resist is applied to the panels

Exposure

UV light is used to expose the layout onto the film. For this purpose, either a plotted template is used, or directly exposed with laser (LDI).

Developing

All resist that has not been exposed to UV light is washed off.

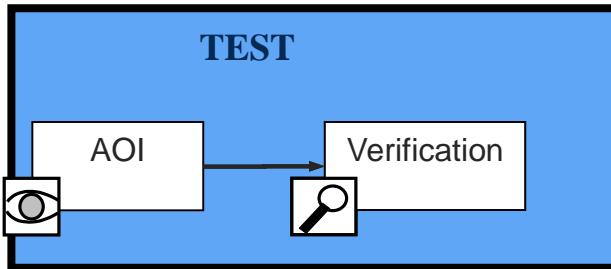
Etching

All areas with exposed copper are etched away

Stripping

The remaining resist, which is still on the panels, is stripped down => finished layout

AOI & VERIFICATION



In AOI (Automatic Optical Inspection), the entire panel is scanned. During verification, the scanned image is compared with the original customer data. The camera automatically moves to all the places where it has detected a deviation. However, the employee decides whether this is actually a defect or a pseudo-defect (dust, etc.).

Scanning Front

Front side of the panel is scanned

Scanning Back

Back side of the panel is scanned

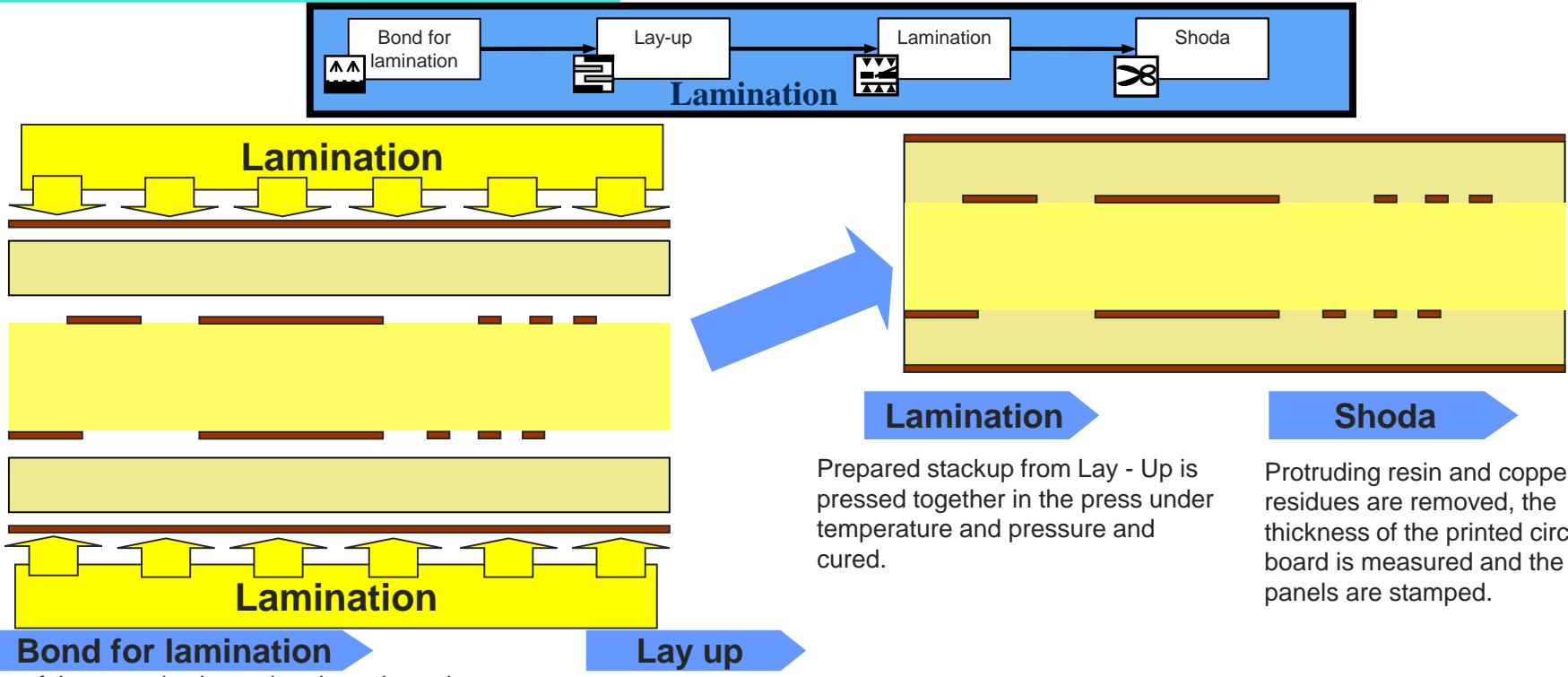
Verification

Comparison of the scanned image with the original data. Checking all places where a deviation was found

LAY UP & LAMINATION



LAY UP & LAMINATION



Surface of the cores is cleaned and roughened to obtain a better bond between copper and prepreg.

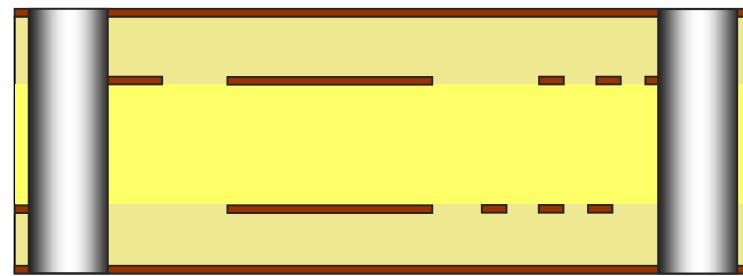
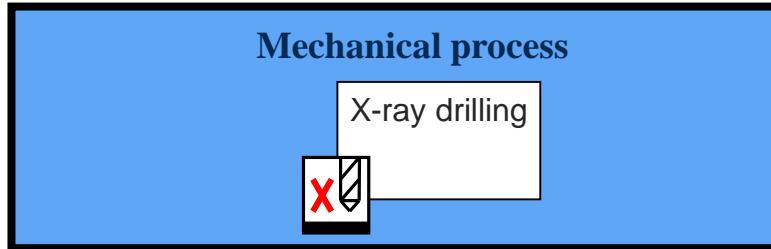
All layers of the printed circuit board are placed together according to the specified structure.

A professional photograph of a young woman with long brown hair, wearing a white lab coat, smiling warmly at the camera. She is holding a large, blue-colored printed circuit board (PCB) with intricate gold-plated metal traces and component pads. The background is slightly blurred, showing what appears to be a workshop or laboratory environment with other equipment and materials.

DRILLING:

- X-RAY
- LASER
- MECHANICAL

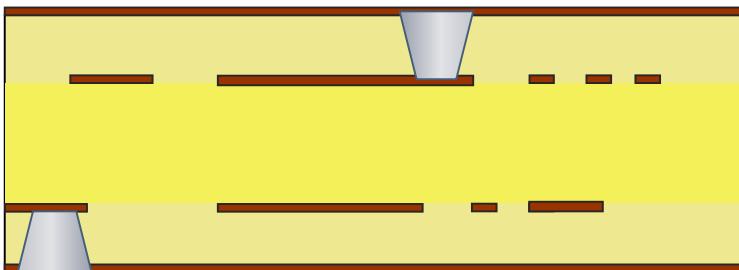
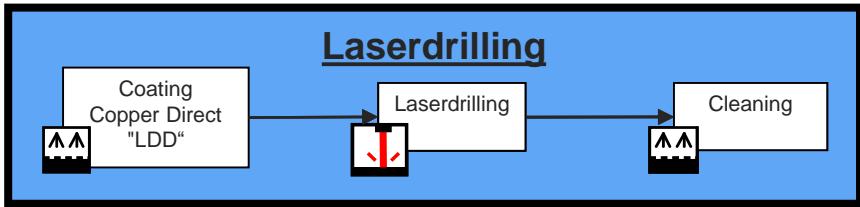
X-RAY DRILLING



X-ray drilling

Panels are X-rayed and mounting holes are drilled for mech. drilling, laser and litho. The spread is also determined here.

LASER DRILLING

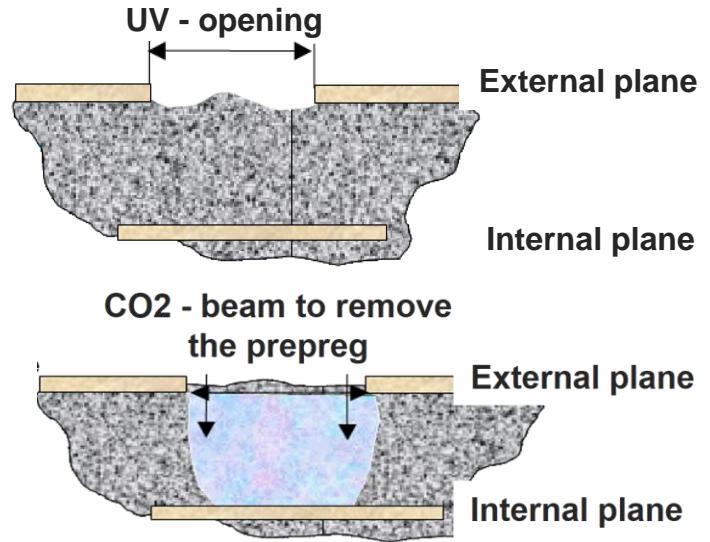


Coating Copper Direct "LDD"

Roughening the copper surface for the laser process (brown surface)

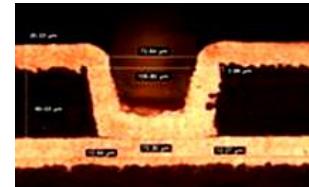
Laserdrilling

The holes are produced by using a pure CO₂ laser (or UV/CO₂ laser process).

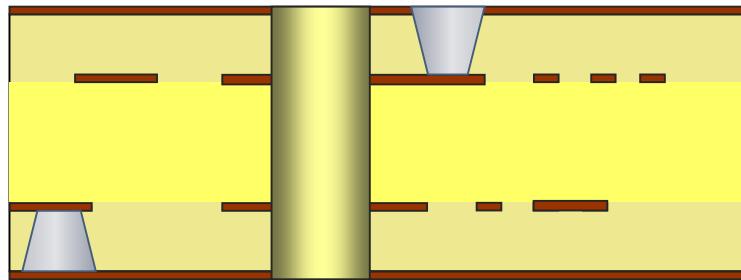
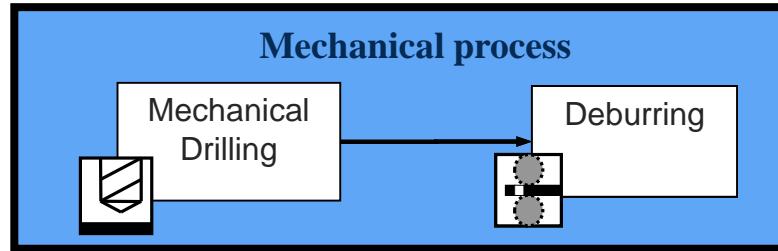


Cleaning

Removing the previously applied layer (brown surface)



MECHANICAL DRILLING

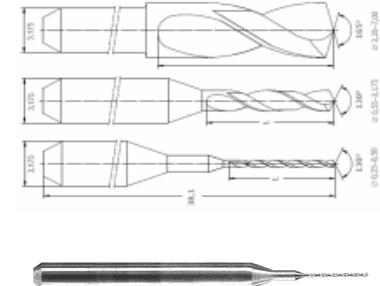


Mechanical drilling

Mechanical drilling of through holes with diameters from 0.10mm to 6.35mm

Deburring

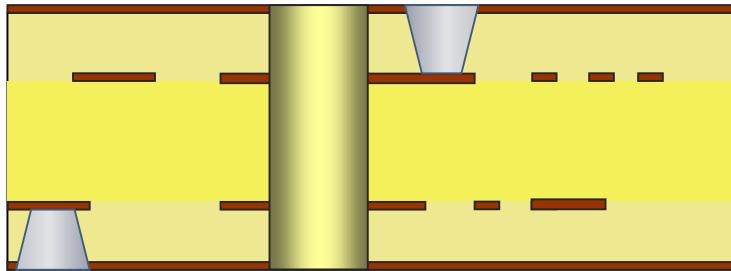
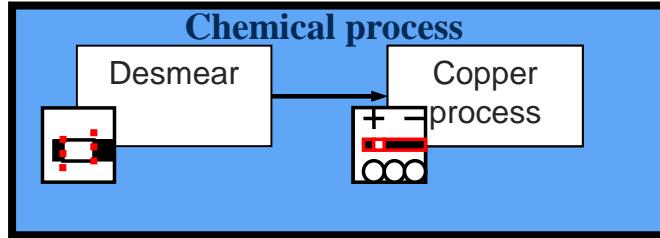
Removing the burr around the holes





COPPER PROCESS

COPPER PROCESS



Desmear

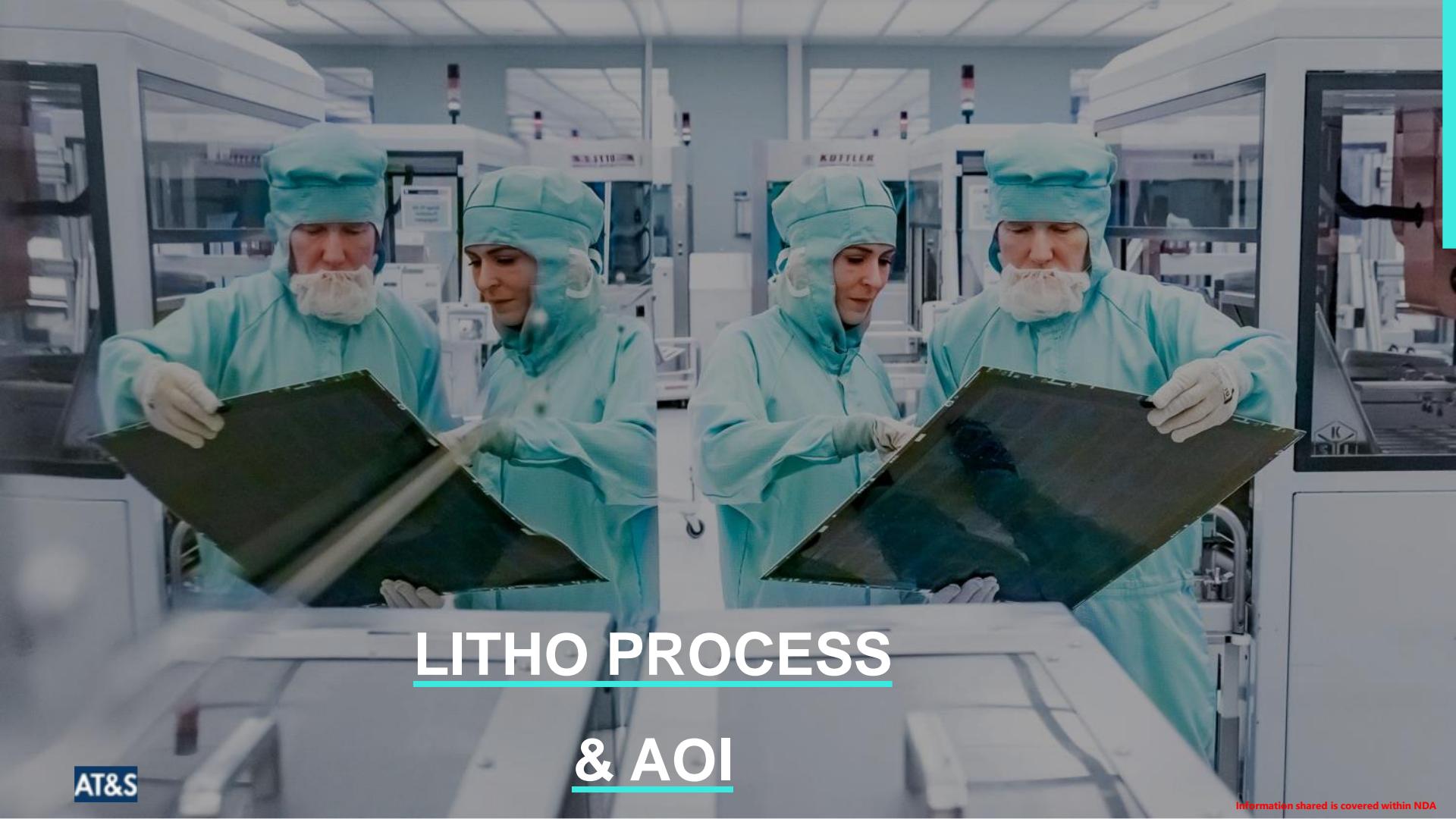
Cleaning the holes from resin residues and dust particles.

E'less copper

Here, an extremely thin copper layer ($\sim 0.5\mu\text{m}$) is applied to establish an electrical connection in the drill hole.

Copper plating

With the help of high power, the printed circuit board is plated up to the desired copper height.

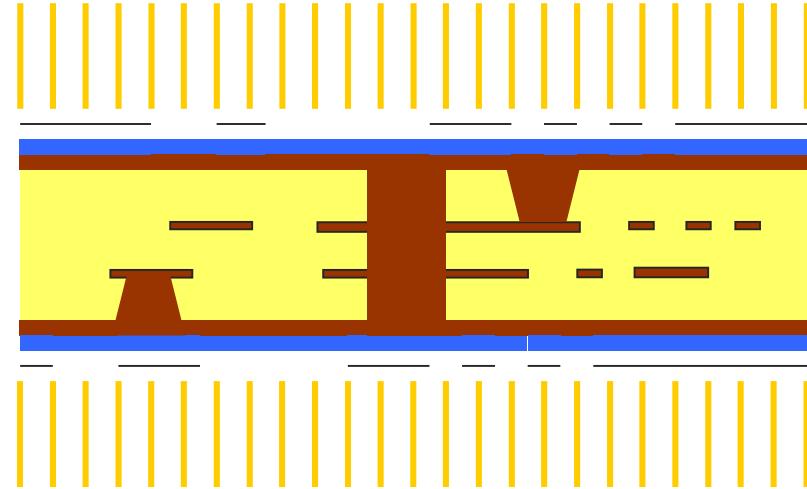
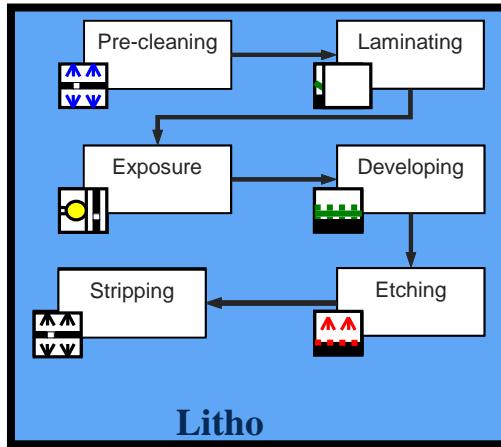


A photograph showing two technicians in full-body blue protective suits and hairnets working in a cleanroom. They are holding up large, dark rectangular panels, likely wafers or substrates, and examining them closely. The background shows various pieces of industrial equipment and monitors. The overall lighting is bright and clinical.

LITHO PROCESS

& AOI

LITHO PROCESS



Pre-cleaning

Removal of oxidation and residues, as well as light roughening of the surface

Laminating

Photosensitive dry film is applied to the panels

Exposure

UV light is used to expose the layout onto the film. For this purpose, either a plotted template is used, or directly exposed with laser (LDI).

Developing

All resist that has not been exposed to UV light is washed off. => exposed copper and areas with resist are equally present on the panel

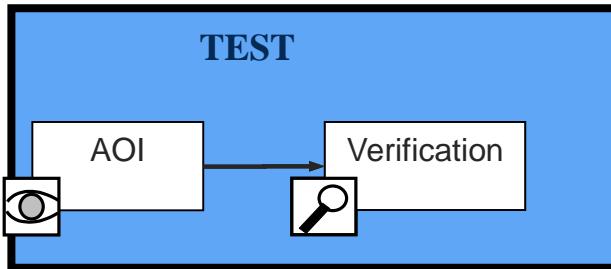
Etching

All areas with exposed copper are etched away

Stripping

The remaining resist, which is still on the panels, is stripped down => finished layout

AOI & VERIFICATION



In AOI (Automatic Optical Inspection), the entire panel is scanned. During verification, the scanned image is compared with the original customer data. The camera automatically moves to all the places where it has detected a deviation. However, the employee decides whether this is actually a defect or a pseudo-defect (dust, etc.).

Scanning Front

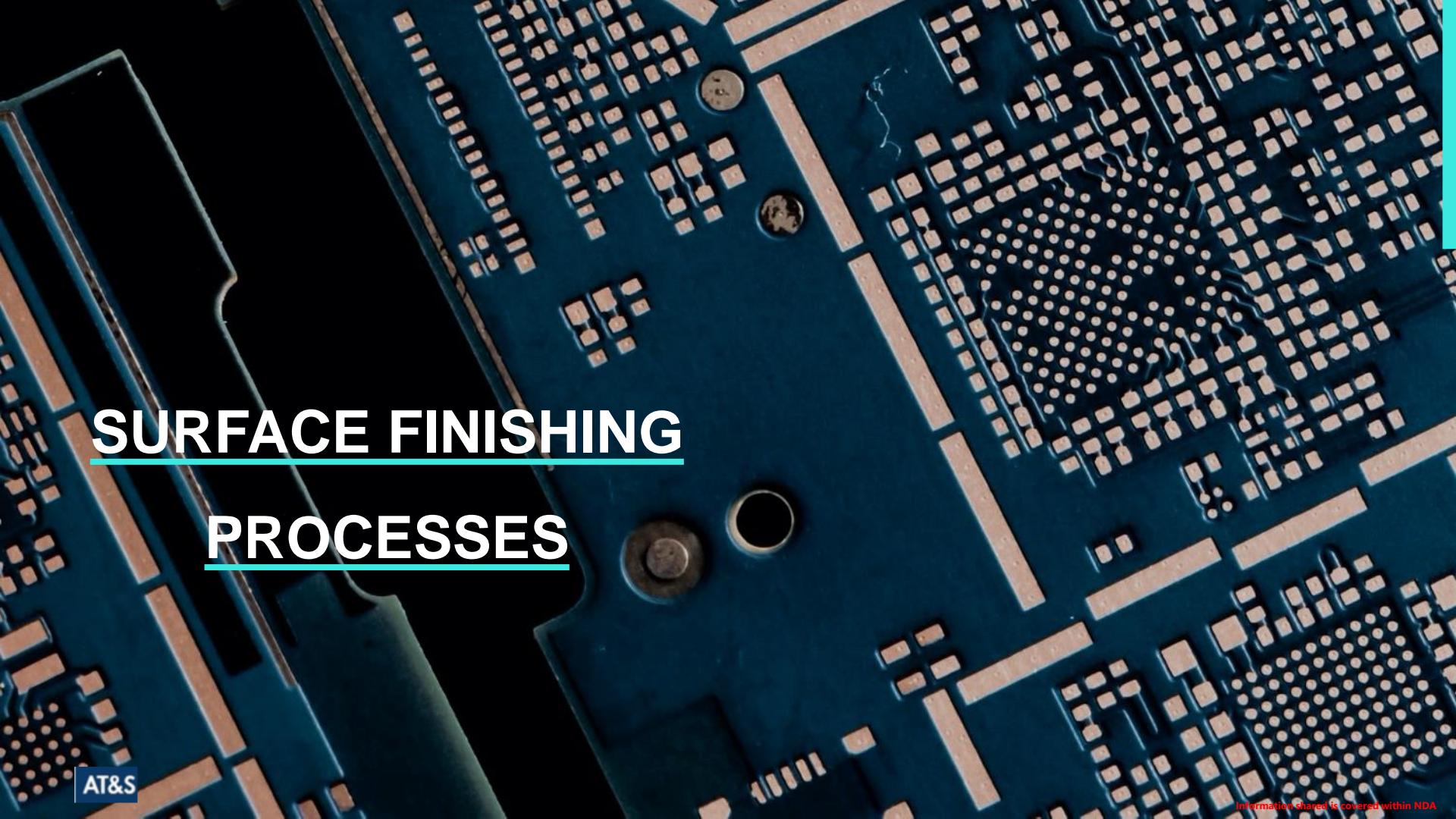
Front side of the panel is scanned

Scanning Back

Back side of the panel is scanned

Verification

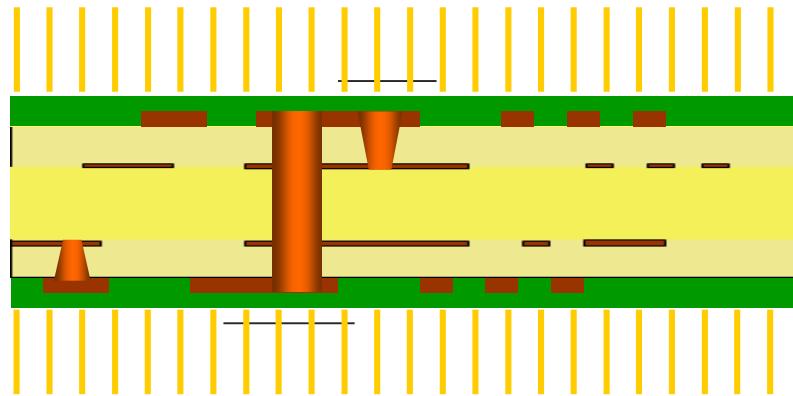
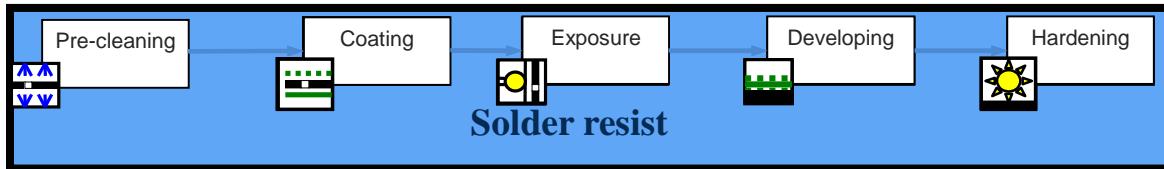
Comparison of the scanned image with the original data. Checking all places where a deviation was found



SURFACE FINISHING

PROCESSES

SOLDERMASK PROCESS



Pre-cleaning

Removal of oxidation and residues, as well as light roughening of the surface.

Coating

The complete panel is coated with solder mask resin. This is done either by curtain coating or screen printing.

Exposure

UV light is used to expose all areas that are to be covered with laquer (film template or laser).

Developing

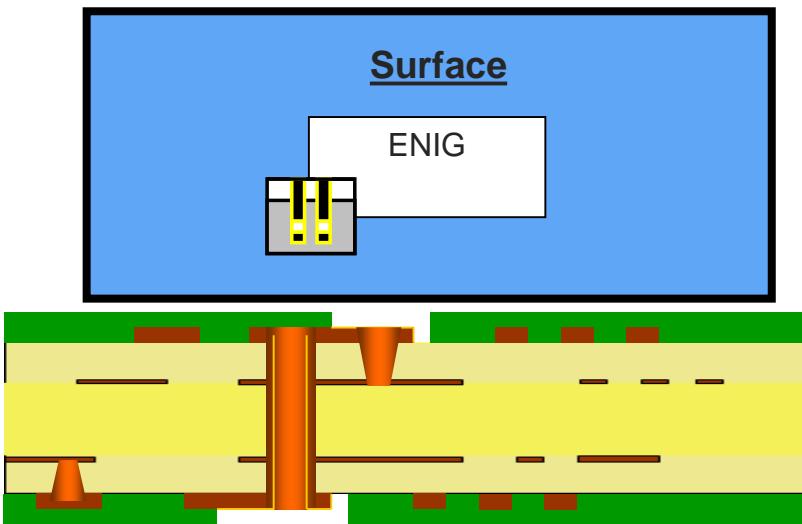
Non-exposed parts are washed off.

Hardening

Thermal curing of the soldermask.

ENIG PROCESS

E'less Nickel Immersion Gold



Pre-cleaning

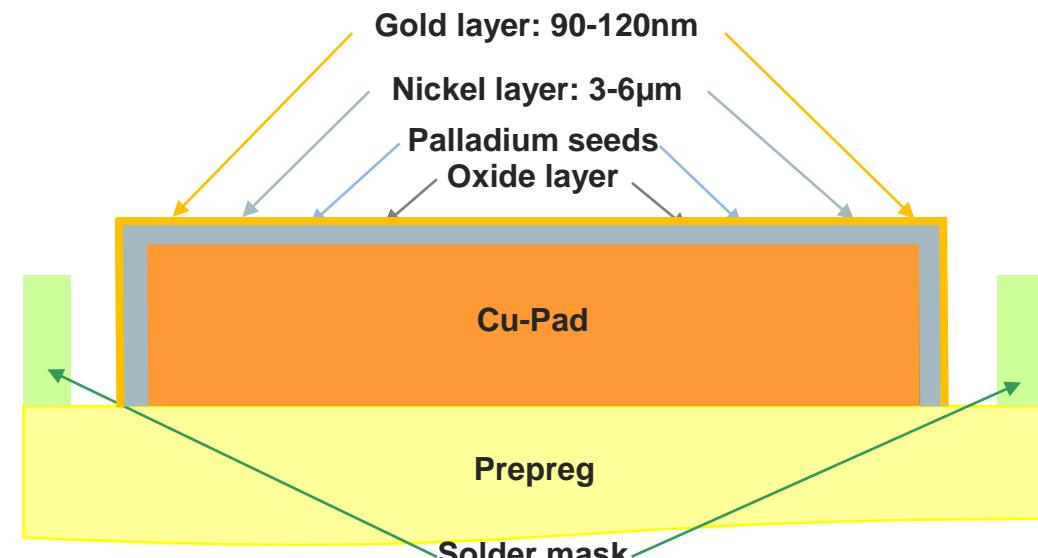
Cleaning the surface, removing oxidation.

E'less Nickel

Chemical deposition of the nickel layer on the copper surface ($> 3\mu\text{m}$).

Immersion Gold

Deposition of an ultra-thin layer of pure gold (99.999% Au) on the nickel layer ($> 0.05\mu\text{m}$).



Palladium = catalyst

E'less Nickel process = reduction reaction
Nickel = diffusion barrier layer between Cu & Au

Gold process = chemical catalytic deposition



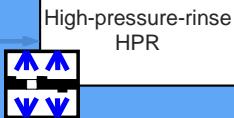
ROUTING & SCORING

ROUTING & SCORING

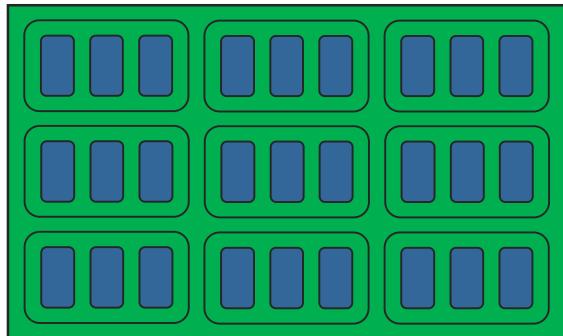
Mechanical



AT&S production format



Delivery format customer



Scoring

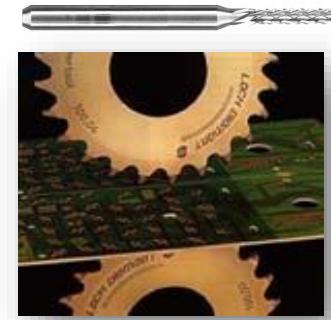
If required, the panel can be scored first (make a notch)

Routing

During routing, the PCBs are cut out of the panel and the desired contour is produced

HPR

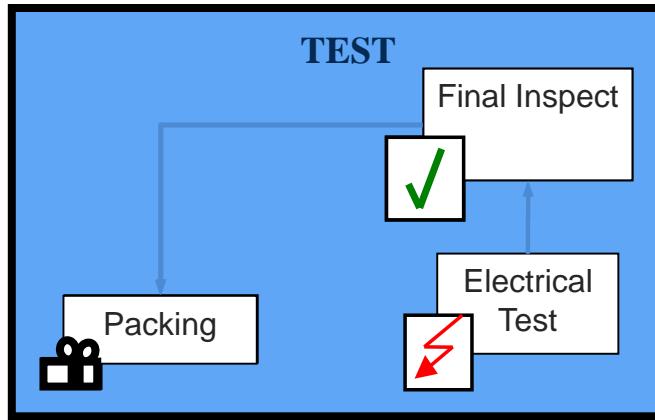
Remaining milling dust is washed off during high-pressure rinsing (HPR)



ELECTRICAL TEST & FINAL INSPECT



ELECTRICAL TEST & FINAL INSPECT



E-Test

All connections are tested for interruptions and shorts.
Finger tester for smaller quantities
Adapter tester for higher quantities

FI (Final Inspect)

100% visual inspection, checking of the surface finishes, reflow test, creating the customer certificates...

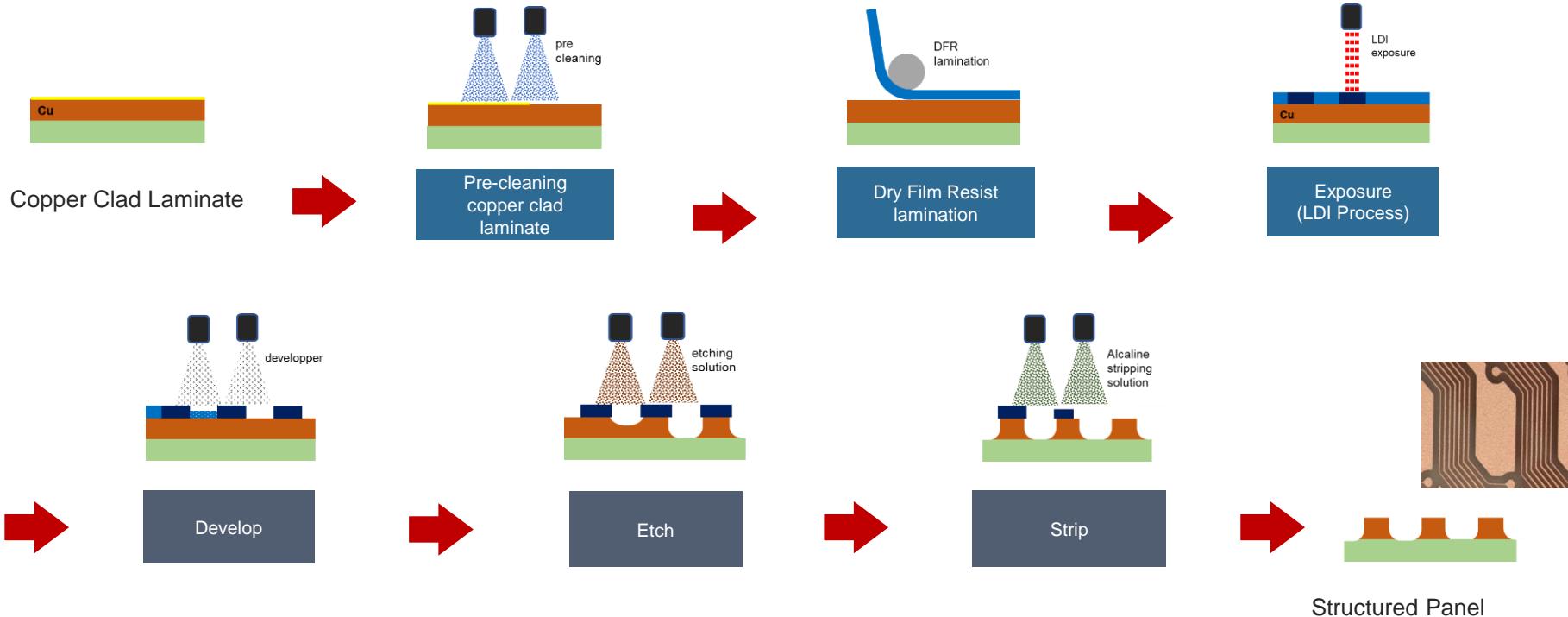
Packing

Packing of the printed circuit boards according to customer requirements

PROCESS OVERVIEW

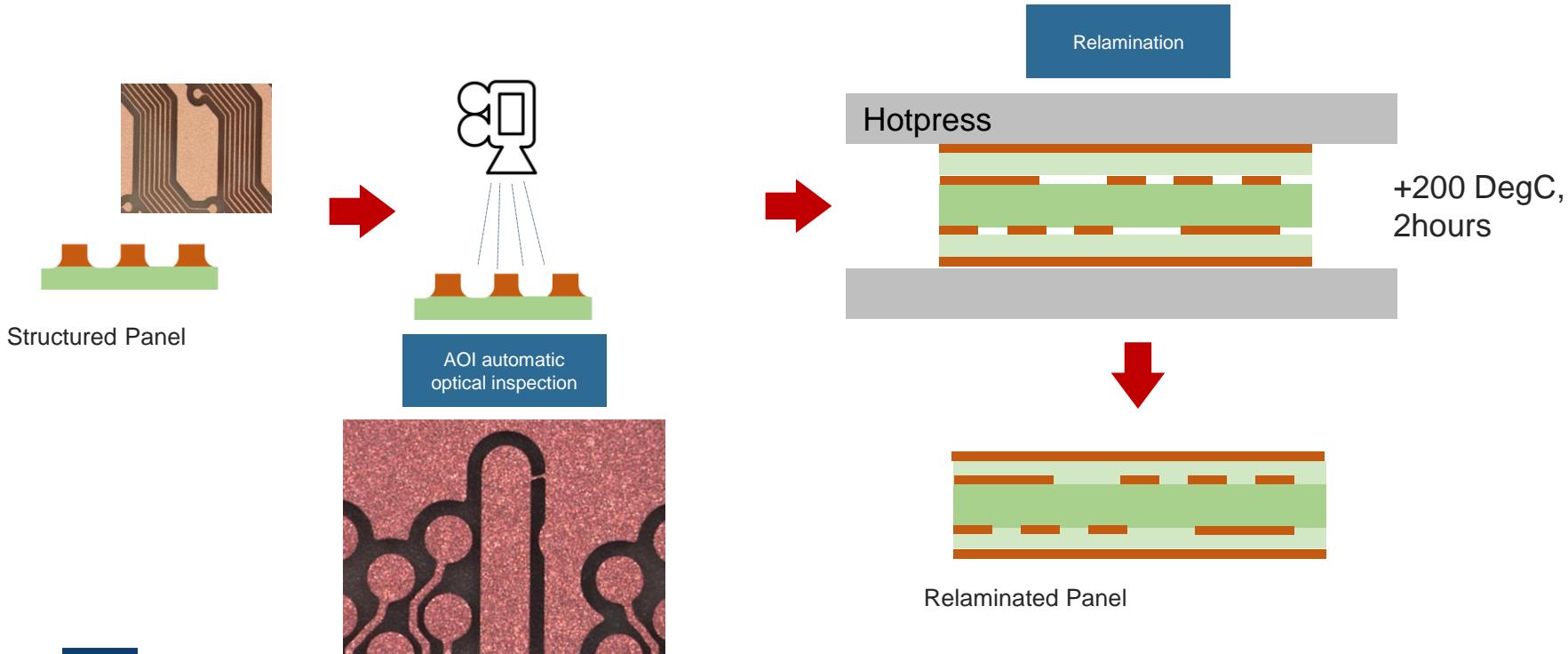
PCB MANUFACTURING SCHEMATICS

Fotolithographic Structuring



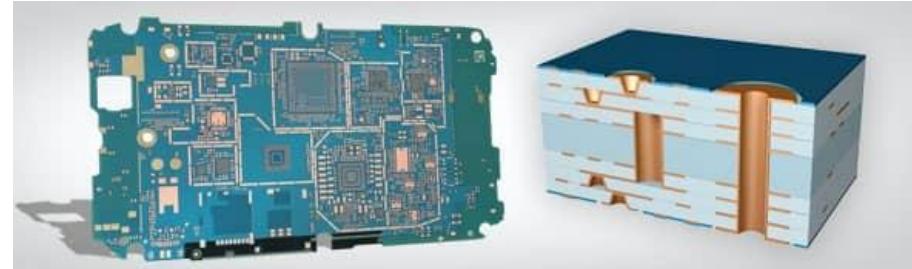
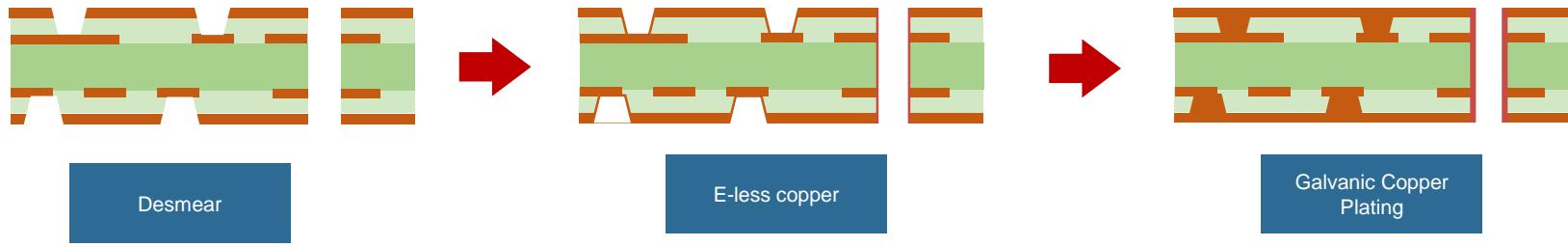
PCB MANUFACTURING SCHEMATICS

Relamination



PCB MANUFACTURING SCHEMATICS

Copper Plating



Source: www.ats.net, © AT&S

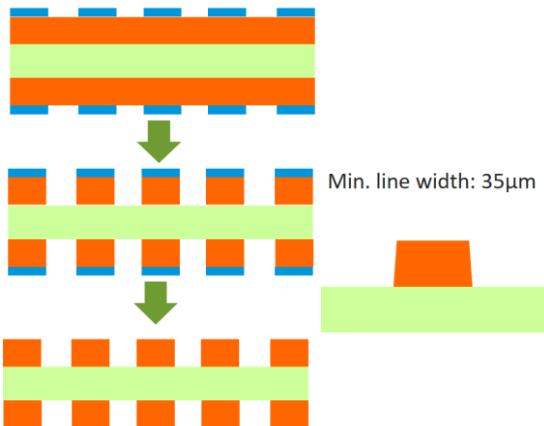
DIFFERENT STRUCTURING PROCESSES

➤ subtractive process

Cu thickness = final thickness



Every Cu, which is not needed is removed by an etching step

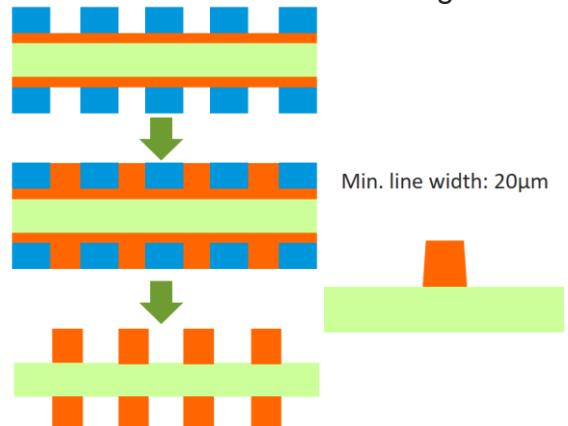


mSAP

2-5µm Cu foil



Lines/ structures are plated, where they are needed, Cu foil is removed with flash etching

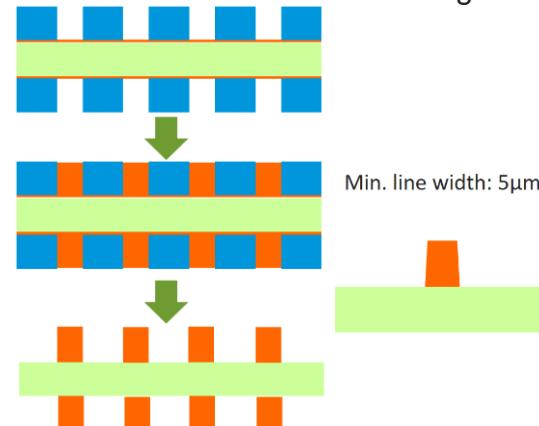


SAP

0,5-1µm e'less copper layer



Lines/ structures are plated, where they are needed, Cu seed layer is removed with flash etching



PCB & RELIABILITY @ AT&S

01 Introduction Round & Agenda

02 AT&S at a Glance

03 PCBs?

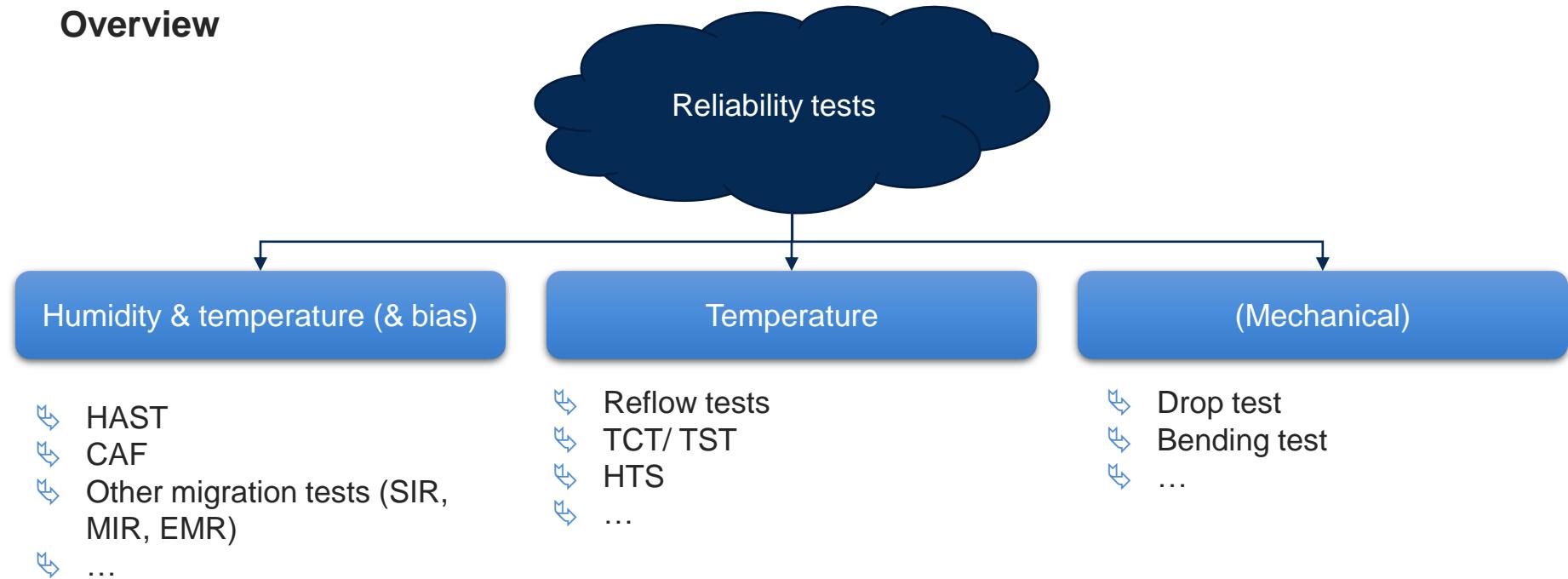
04 Materials

05 Process Flow

06 Reliability

RELIABILITY TESTS

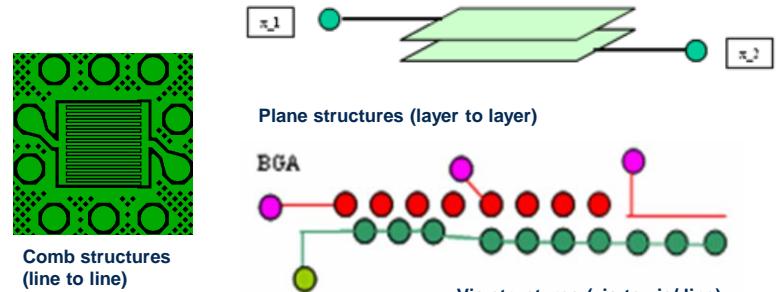
Overview



RELIABILITY TESTS

Humidity & temperature (& bias) test characteristics

- Testing for: electro(chemical) migration
- Test structures: high-ohmic/ high resistance
- Influencing parameters: Temperature
Humidity
(Bias)
- Typical failure modes: Shorts created by copper migration, dendrites, CAF, haloing,...
- Typical tests (+norm):



Reliability Test	Preference Specs	Stress Parameter	Purpose	Structures	Failure Modes
Highly Accelerated Stress Test (HAST)	JESD22-A110	<ul style="list-style-type: none">• Temperature• Humidity• Bias• Pressure	PCB resistance against Electrochemical Migration	High resistance structures	Electrochemical migration e.g.: CAF, dendrites, haloing
Temp Humidity Bias Test (SIR, CAF, MIR, EMR)	IPC-TM-650 2.6.(X) JSD22-A101	<ul style="list-style-type: none">• Temperature• Humidity• Bias	degradation of solder mask and insulation materials, quantifying of residues	High resistance structures	Electrochemical migration e.g.: CAF, dendrites, haloing

RELIABILITY TESTS

Mechanical test characteristics

- Testing for: mechanical fatigue
- Test structures: low-ohmic/ low resistance
- Influencing parameters: mechanical stress
- Typical failure modes: Opens created by broken structures
- Typical tests (+norm): ! Very seldom done in the mean time & only for specific products!



Drop test board

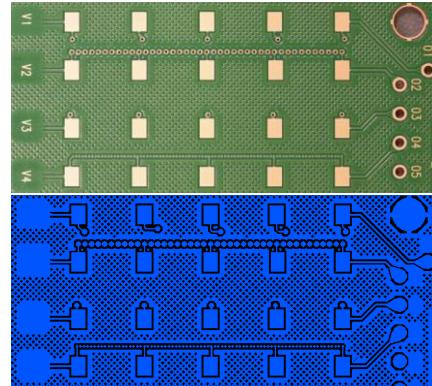
Reliability Test	Preference Specs	Stress Parameter	Purpose	Structures	Failure Modes
Drop Test	JESD22-B111&B104C	• Mechanical stress	the compatibility of components to withstand moderately shocks	Low resistance structures	Cracks in via structure, material defects, cracks in solder
Bending Test	NA	• Mechanical stress	check flexible PCBs how often they can withstand bending	Low resistance structures	Cracks in copper lines and other material defects

RELIABILITY TESTS

Temperature test characteristics

- Testing for: thermo-mechanical fatigue
- Test structures: low-ohmic/ low resistance
- Influencing parameters: Temperature
(Bias)
- Typical failure modes: Opens/ Failures created by cracks/ defects in the materials
- Typical tests (+norm):

Daisy chains (laser and/ or mechanical via stacks)

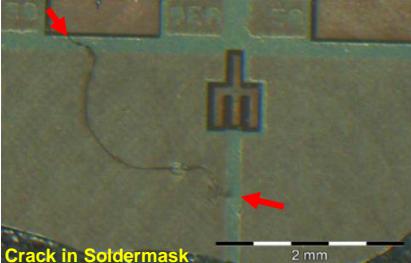
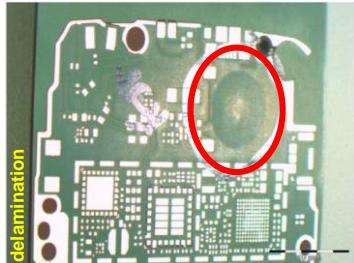


Reliability Test	Preference Specs	Stress Parameter	Purpose	Structures	Failure Modes
Reflow Sensitivity	J-STD-020	• Soak • Temperature	ability of PCBs to withstand the assembly process	All structures	Delaminations, cracks in solder mask
High Temperature Storage	Hella-N67036-02.8.6	• Temperature	degradation of solder mask and insulation materials	All structures	Cracks in solder mask, material defects, cracks in via structure
Temperature Cycle Test	JESD22-A104	• Repeated temperature changes	physical endurance of PCB to repeated changes of temperature	Low resistance structures	Cracks in via structure, material defects
Thermal Shock Test	IPC-TM-650 2.6.7.2B	• Sudden temperature changes	the physical endurance of PCB to sudden changes of temperature	Low resistance structures	Cracks in via structure, material defects

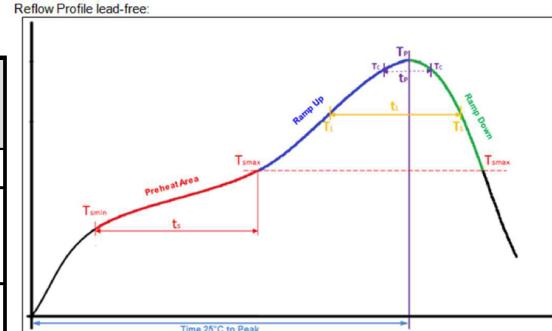
TEMPERATURE TESTS

Reflow Sensitivity

- Testing for: material defects, delaminations caused by humidity uptake, ability of PCBs to withstand the assembly process
- Test structures: all kind of PCBs
- Influencing parameters: Humidity & Temperature
- Typical failure modes: Delaminations
Cracks in SM
- Specification: J-STD-020



Moisture sensitivity level	MSL 1	MSL 2	MSL 3	MSL 3 acc
Pretreatment	24hrs/125°C			
Temperature	85°C	85°C	30°C	60°C
Humidity	85%RH	60%RH	60%RH	60%RH
Moisture duration	168hrs	168hrs	192hrs	40hrs
Reflow Cycles	8 – 15 x Reflow lead-free			



Reflow Profile lead-free:

Time 25°C to peak temperature: max. 8 minutes

Preheat Area:

- T_{min} (minimum Temperature): 150°C
- T_{max} (maximal Temperature): 200°C
- t_s (time from $T_{\text{min}} - T_{\text{max}}$): 60-120 seconds

Ramp up:

- $\bar{T}_{\text{max}} - T_s$ (Average ramp - up rate): max. 3°C/sec

Liquidus Area:

- T_L (Liquidus temperature): 217°C
- t_L (Time at liquidus): 60-150 seconds

Peak:

- T_p (Peak temperature): 260°C
- t_p (time above T_L): 30 seconds
- T_c (classification temperature = $T_p - 5^\circ\text{C}$): 255°C

Ramp down:

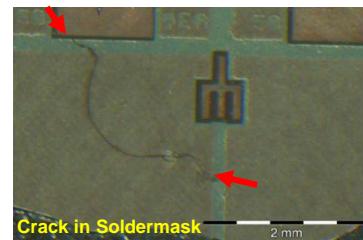
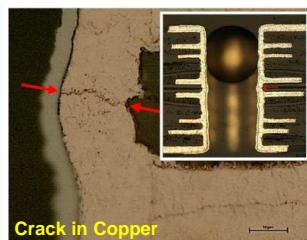
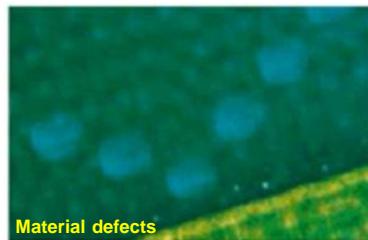
- $\bar{T}_s - T_{\text{max}}$ (Average ramp - down rate): max. 6°C/sec

TEMPERATURE TESTS

High Temperature Storage

- Testing for: degradation of dielectric materials & solder masks
- Test structures: all kind of PCBs
- Influencing parameters: Temperature
- Typical failure modes: Cracks in SM
Cracks in copper
Other material defects
- Specification: N67036-02.8.6

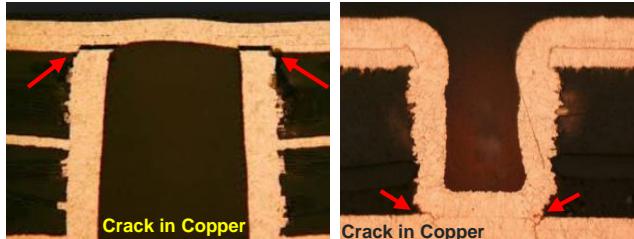
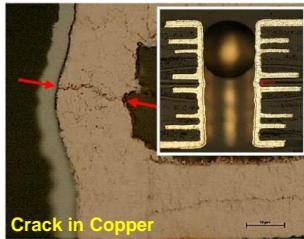
High Temperature Storage	
Temperature	125°C
Test duration	1000hrs



TEMPERATURE TESTS

Temperature Cycling Test (TCT) & Thermal Shock Test (TST)

- Testing for: physical endurance of PCBs to repeated changes of temperature
- Test structures: low ohmic/ low resistance
- Influencing parameters: Repeated temperature changes
- Typical failure modes: Cracks in copper
Other material defects
- Specification:
TCT: JEDEC JESD 22-A104C
TST: IPC-TM-650 2.6.7.2B



TCT:

Step per cycle	Chamber	Sample Temperature	Min. Soak Time	Cycle count ³
1	Cold	-40 +0/-10°C	5min	1000
2	Heat-up	-	-	
3	Hot	+125 +15/-0°C	5min	
4	Cool-down	-	-	

The heating and cooling rate has to be set in such a way that in total 2 cycles per hour are achieved.

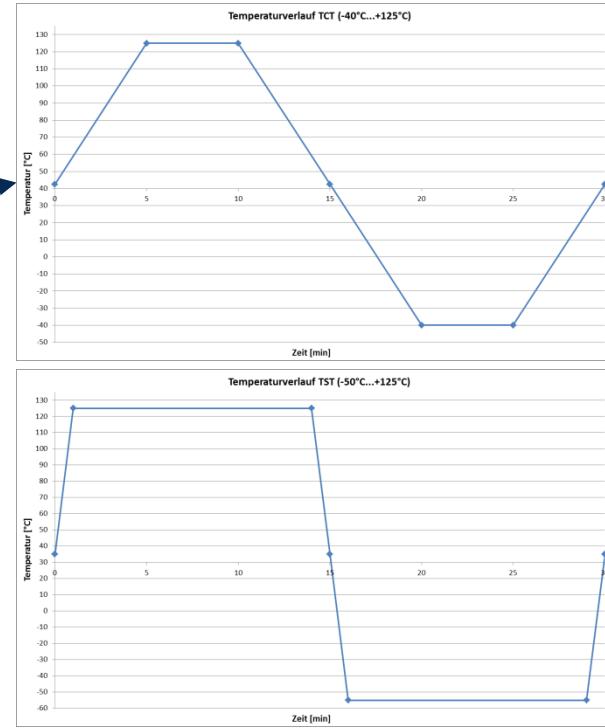
TST:

Step per cycle	Chamber	Sample Temperature	Time	Cycle count
1	Cold	-55 +0/-5°C	15min	1000
2	Transfer Recovery	-	<2min	
3	Hot	+125 +5/-0°C	15min	
4	Transfer Recovery	-	<2min	

Information shared is covered within NDA

TEMPERATURE TESTS

Temperature Cycling Test (TCT) & Thermal Shock Test (TST)



One-chamber test tool for TCT

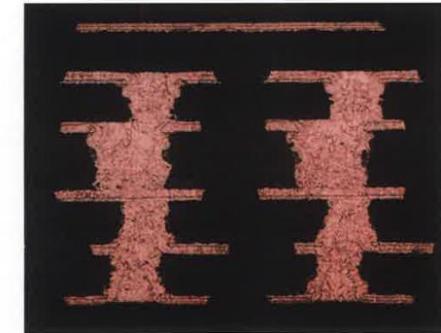
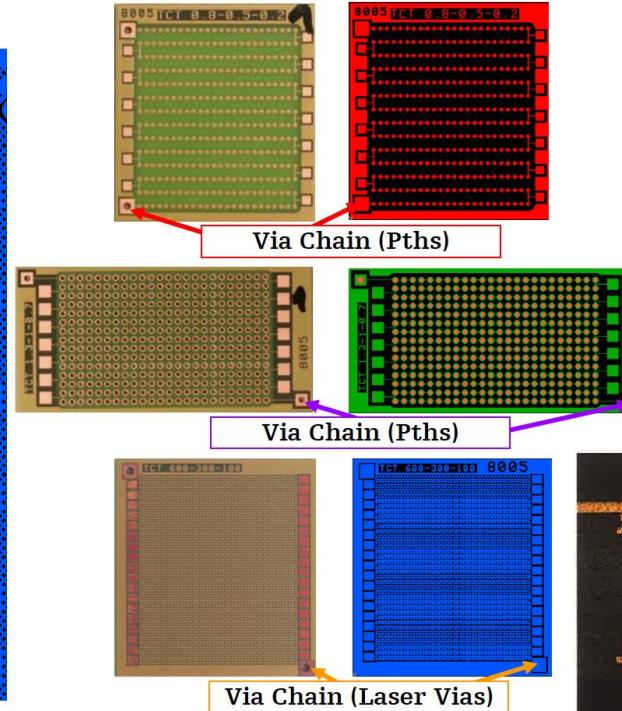
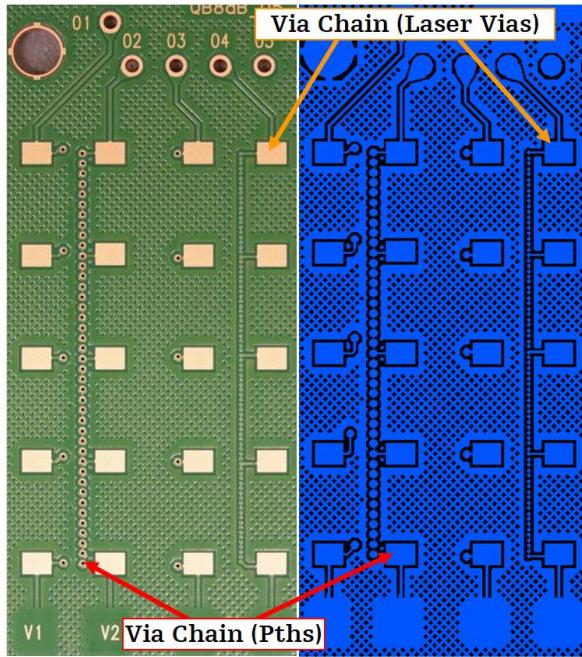


Two-chamber test tool for TST

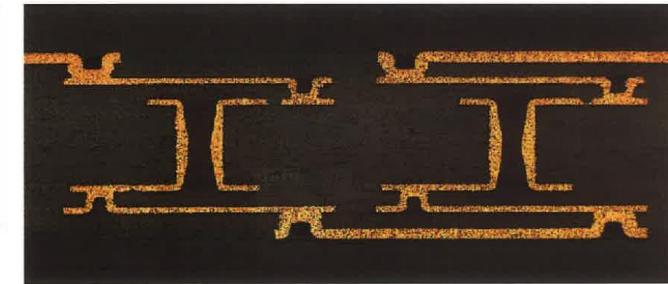
TEMPERATURE TESTS

Temperature Cycling Test (TCT) & Thermal Shock Test (TST)

→ Low Resistance Test Structures



Stacked vias



Staggered vias

PCB & RELIABILITY @ AT&S

- 01** Introduction Round & Agenda
- 02** AT&S at a Glance
- 03** PCBs?
- 04** Materials
- 05** Process Flow
- 06** Reliability



Influencing
processes on
reliability?



THANK YOU FOR YOUR ATTENTION!