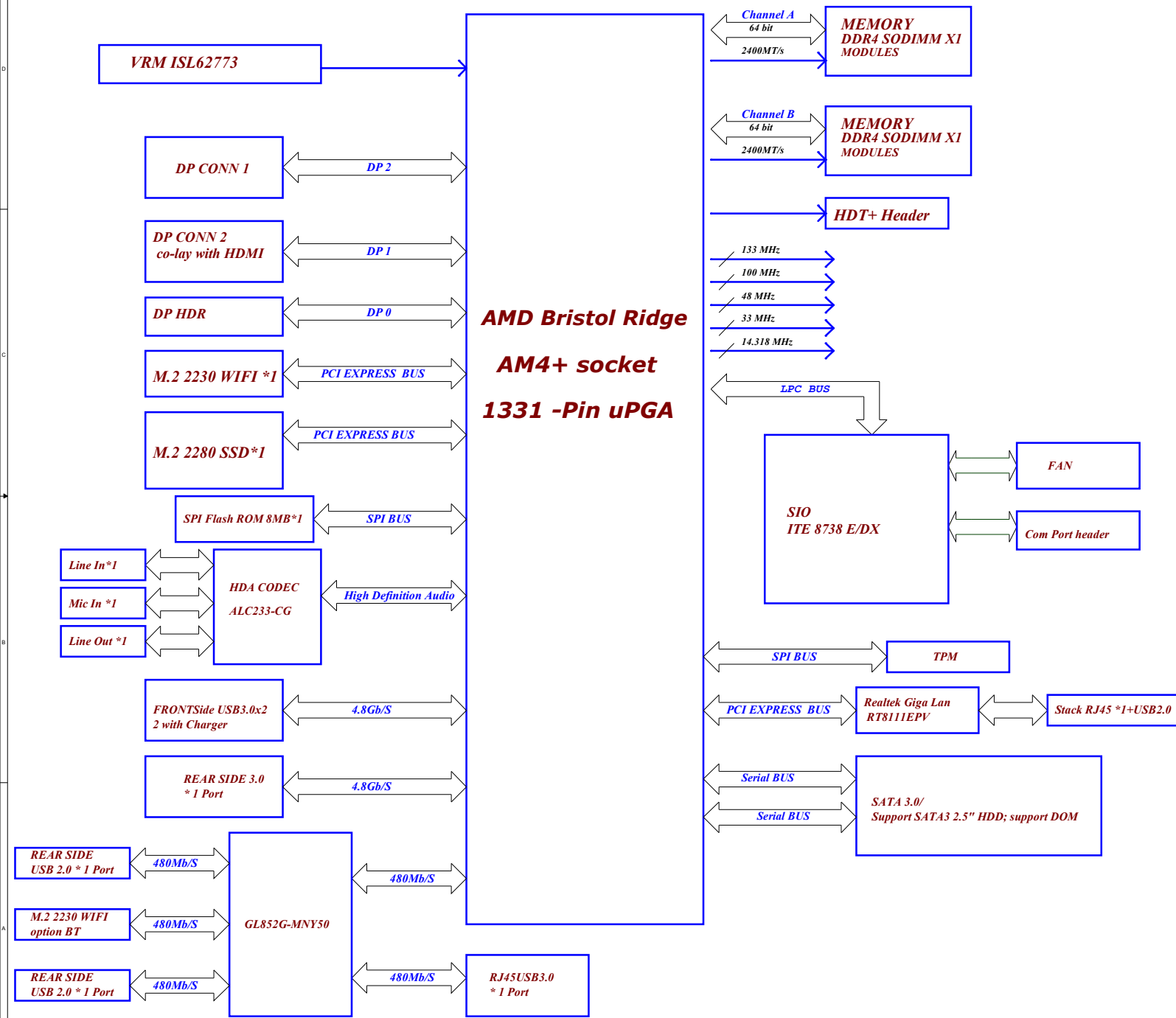


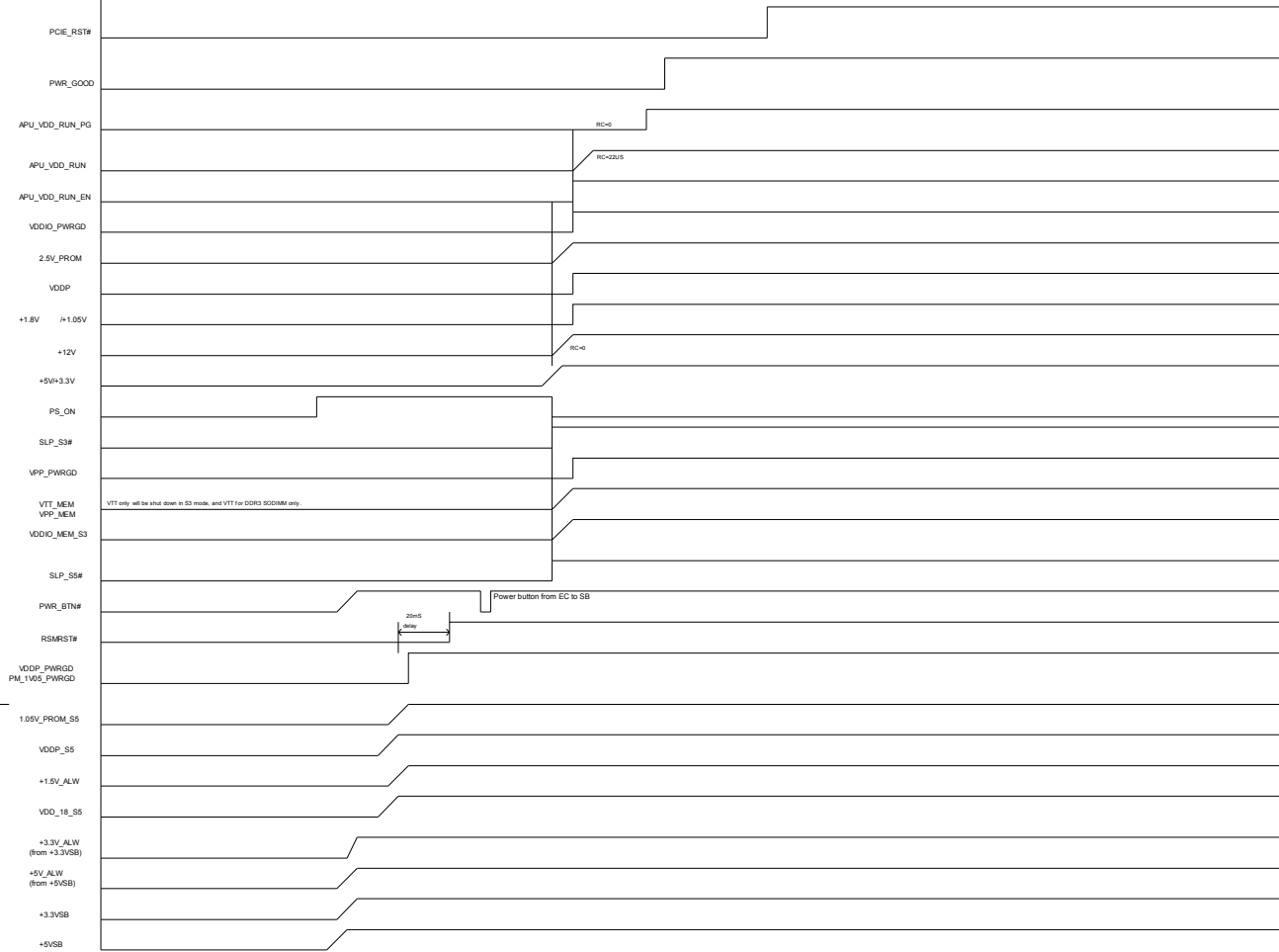
Project: **KC790**
PCB Size : 174*175 mm



Project
Document No :
X03 : 04/29/2016Y

PAGE	TITLE
01	Block Diagram
02	Power Sequence
03	Power Delivery Map
04	AM4 PCIE I/F
05	AM4 MEM
06	AM4 DISPLAY/MISC
07	AM4 ACPI/AZ/SD/I2C/GPIO/FCH
08	AM4 CLK/LPC/SPI/USB
09	AM4 POWER AND DECOUPLING
10	AM4 GND
11	DDR4 CHA SO-DIMM1 -8H
12	DDR4 CHB SO-DIMM3 -4H
13	Knoll &Asset ID&SPI ROM
14	CMOS Clear / Battery/ HDR
15	USB Hub2.0 GL852G
16	Display Port 1
17	Display Port 2
18	Display Port HDR
19	Audio Codec - ALC233-CG
20	Audio Jack Line I-O/ Mic in
21	SuperI/O IT8738E
22	COM Port/ PS/2/ FAN CTRL
23	TPM - TCG 2.0
24	LAN RTL8111EPV
25	RJ45 + USB3 Stack
26	Rear USB2 x 3
27	Front USB3 Charger x2
28	M.2 2230-E WIFI/ BT
29	M.2 2280-M SSD
30	Buzzer &debug card
31	SATA-Express DOM
32	PWRGD & Bleed Off
33	Button/ LED
34	SM BUS/Thermal Sensing/APS
35	Debug Port
36	Mounting Hole/ PCB/ Metal
37	Blank
38	APU VDD RUN/APU VDDCR SOC
39	APU VDD RUN OUTPUT
40	APU VDDCR SOC OUTPUT
41	+20V S5 ADP
42	VDDCR ALW
43	+12V
44	+3V3 DSW / +1.5V ALW
45	+5V S5/+3V3 S5
46	VDDIO MEM S3/VTT MEM
47	VPP MEN
48	+5V RUN/+3V3 RUN
49	APP VDDP RUN/+1.8V RUN
50	VDDCR SOC S5
51	VDDP S5
52	VDD I8 S5
53	+5V USB
54	STRAPPING PIN
55	AM4 GPIO TABLE
56	SIO GPIO TABLE
57	RESET MAP-CLOCK DIAGRAM
58	SMBUS Block Diagram
59	INA300
60	Change List2

Power on Sequence required:



POWER CONN

+20V_S5_ADP
Imax= 3.25A (65W)
Imax= 4.5A (90W)

CPU: 4+2

PWM
RT8296A

+3V3_DSW
Imax= 0.1A

PWM
ISL62773A

2 Phase Design

CPU Cores

APU_VDD_RUN
TDC= 39A
Imax= 55A

2 Phase Design

GFX & NB

APU_VDDCR_SOC
TDC= 40A
Imax= 60A

VDDCR_ALW

MOS

FCH & USB

VDDCR_SOC_S5
Imax=20A

PWM
NCP1589L

MEM PHY

VDDIO_MEM_S3
Imax= 7A

LDO

NCP51200

GFX & NB

VTT_MEM
Imax=1.5A

PWM
RT8296A

GFX & NB

+VPP_DDR
Imax= 1A

PWM
RT8068A

VDDCR_ALW
Imax= 1A

PWM
NCP1589L

USB PHYs

VDDP_S5
Imax= 9.5A

MOS

PCIe & DISPLAY PHYs

APU_VDDP_RUN
Imax= 8.5A

PWM
RT6576

+5V_S5
Imax=13.77A

MOS

+5V_RUN
Imax=2.6A

+3.3V_S5
Imax=10A

MOS

+3.3V_RUN
Imax=5.76A

PWM
RT8296A

+12V
Imax= 1A

PWM
RT8296A

RTC, USB2, USB3

VDD_18_S5
Imax= 2.75A

LDO

APL5932

AZ

+1.5V_ALW
Imax=0.25A

MOS

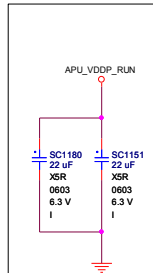
+1.8V_RUN
Imax=2A

BATTERY

+3V3_DSW

DIODE
BAT54C

+3V_BATT
Imax=6uA



SATA CONN-7P+15P

WLAN M.2 2230 Key-E

LAN PHY

SSD Card PCIE
M.2 2280 Key-M

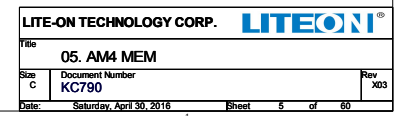
CAD NOTE: PLACE CAPS NEAR SLOT

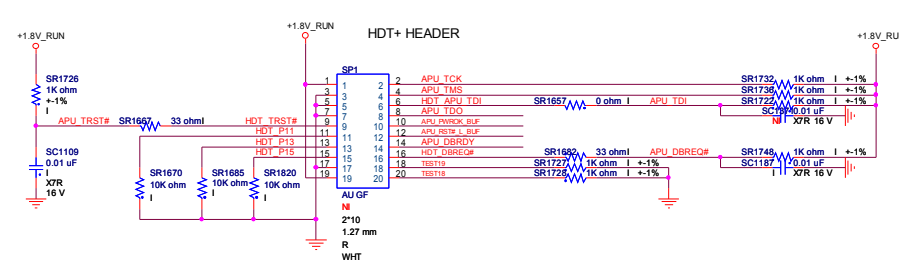
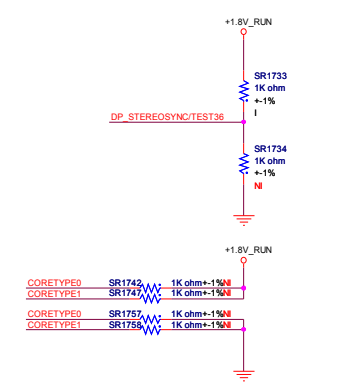
SATA CONN-7P+15P

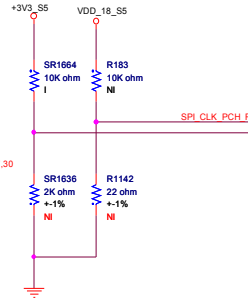
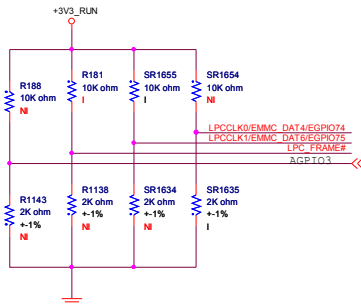
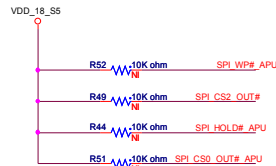
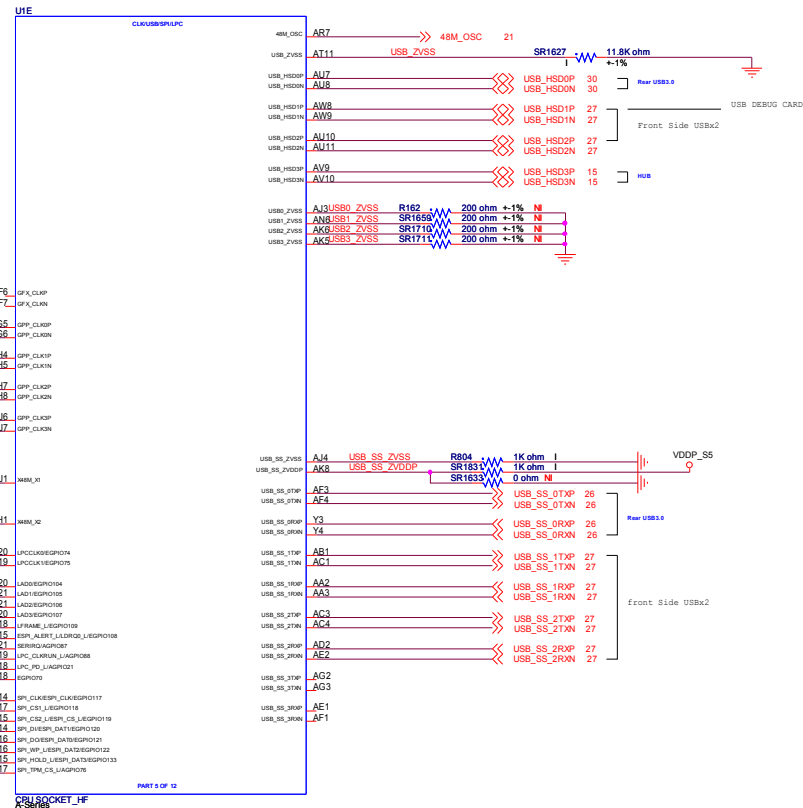
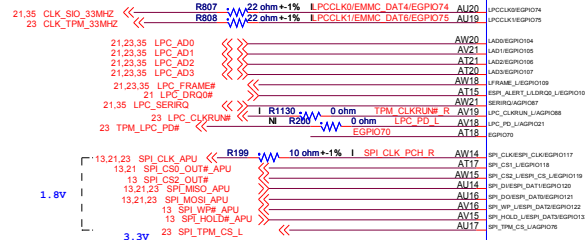
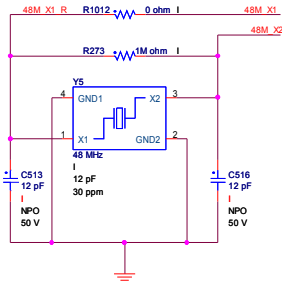
WLAN M.2 2230 Key-E

LAN PHY

SSD Card PCIE
M.2 2280 Key-M

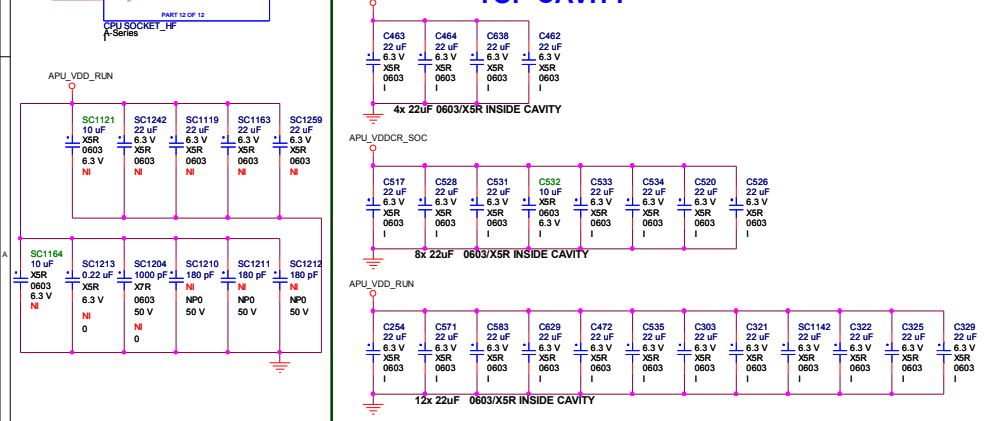


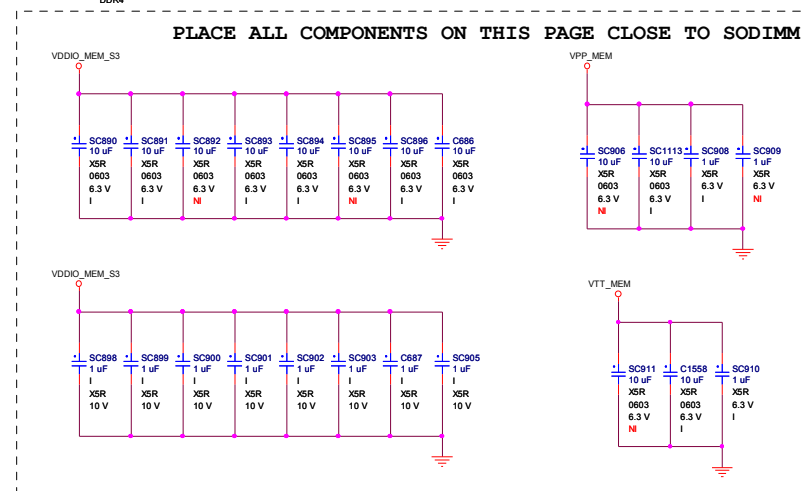
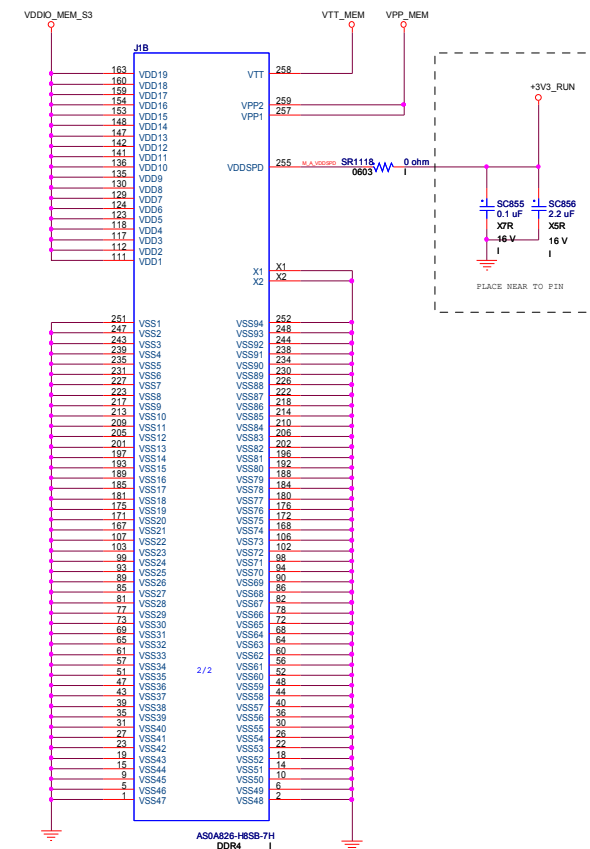
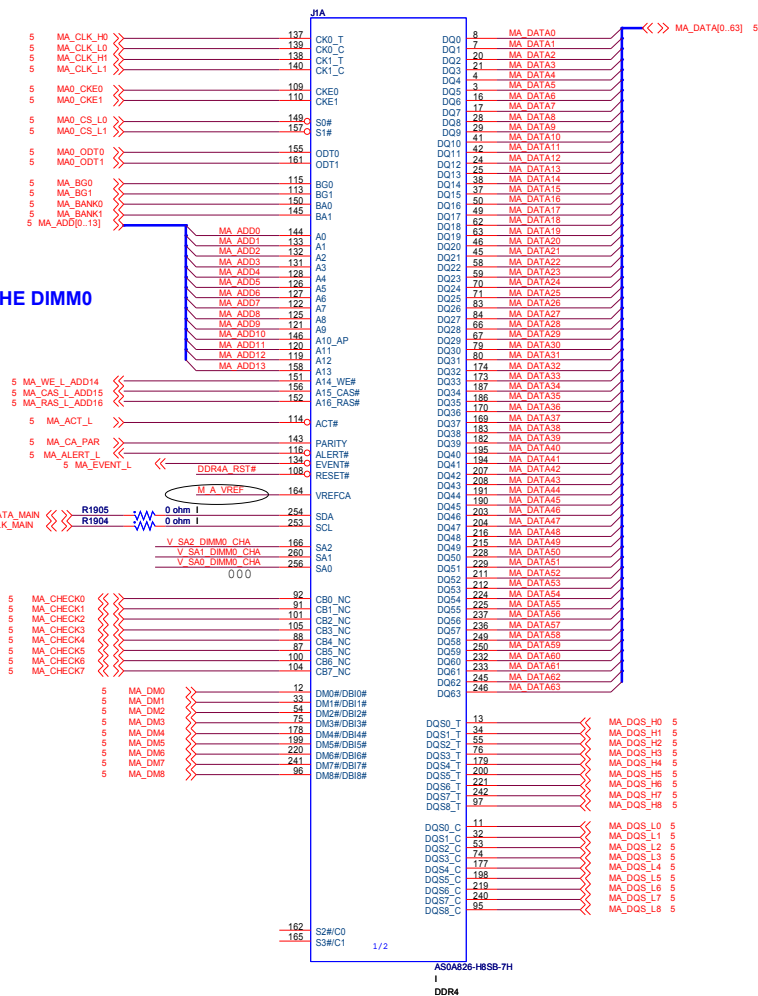
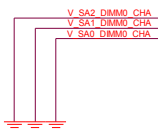
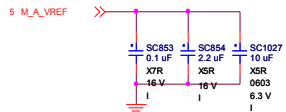
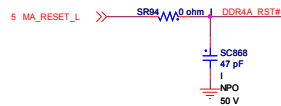


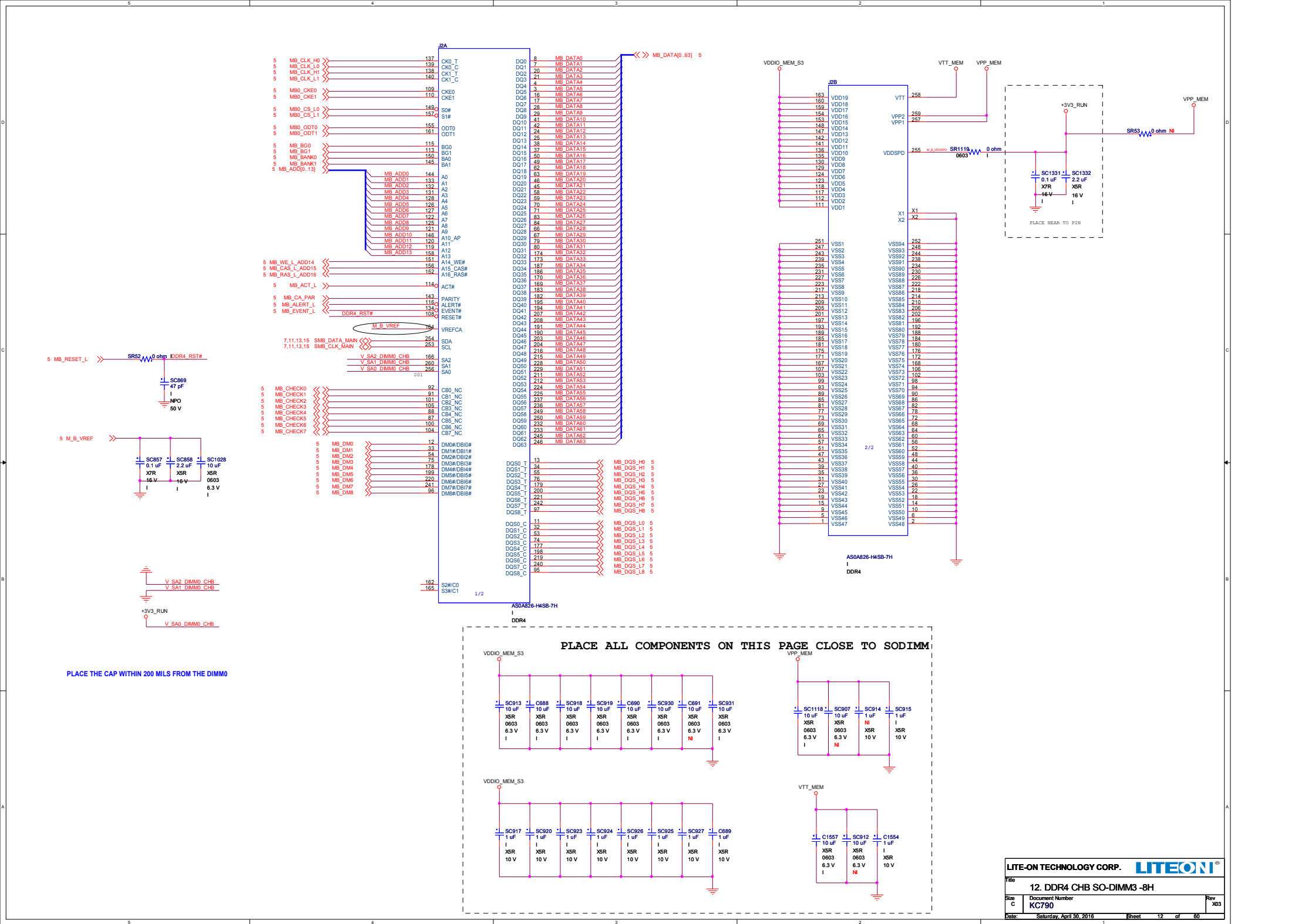


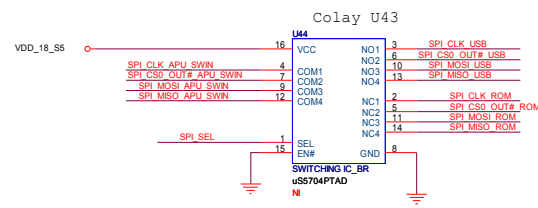
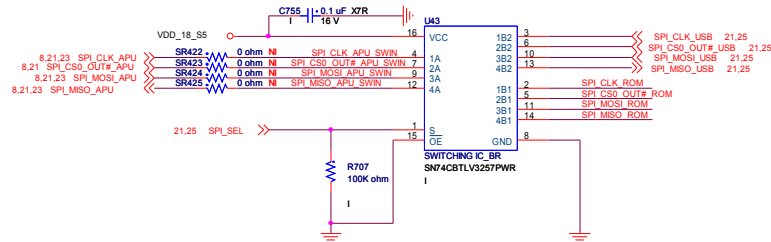
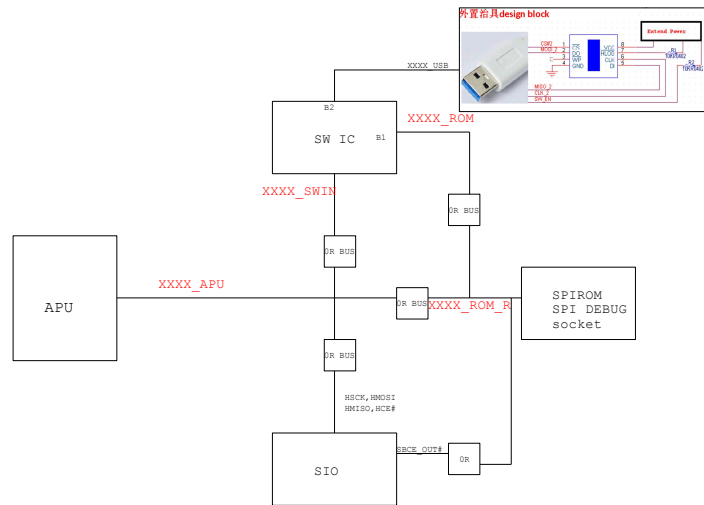
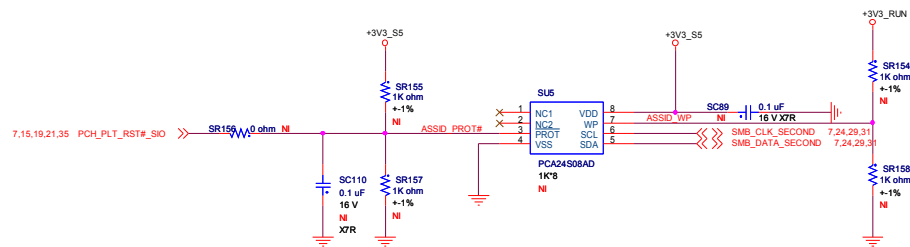
RTCLK 7.38
Type 0 APU: Pull-up resistor to VDD_33_s5
Type 2/3 APU: Pull-up resistor to VDD_18_s5

	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI CLK (ZF)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5\ resume) (DEFAULT)	SPI ROM (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLE (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic	LPC ROM	LPC ROM	short reset mode	Use 100Mhz PCIE clock as reference clock and generate internal clocks only
CZ/ST DIE ONLY							ZP DIE ONLY

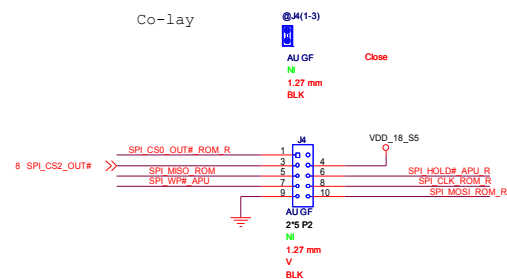
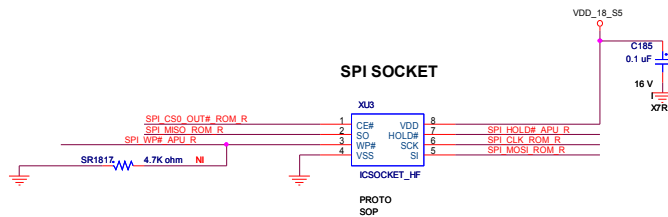
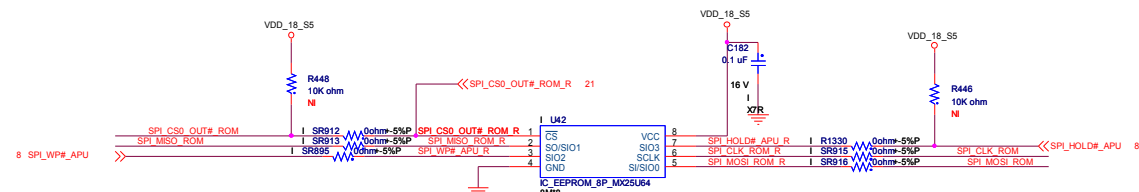
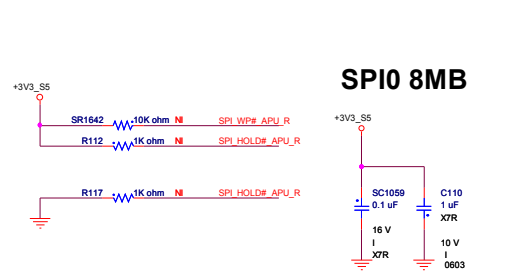
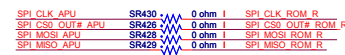


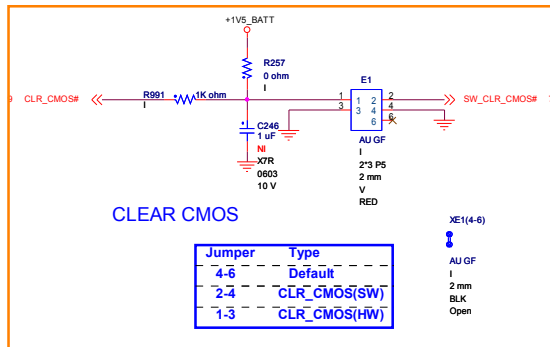




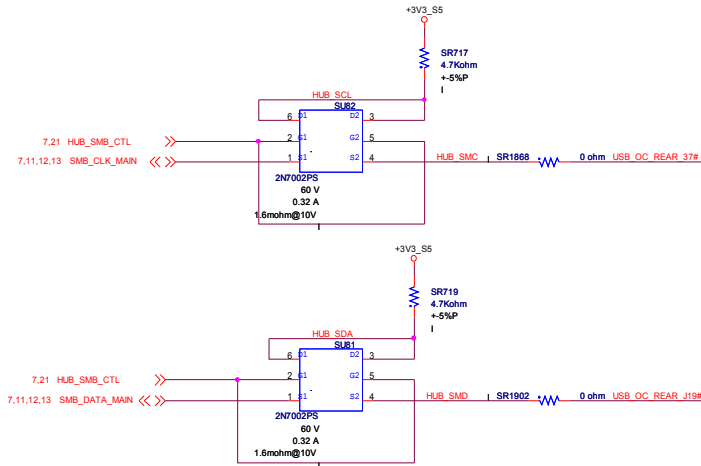
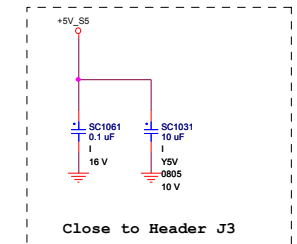
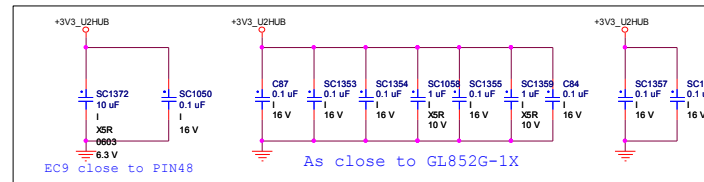
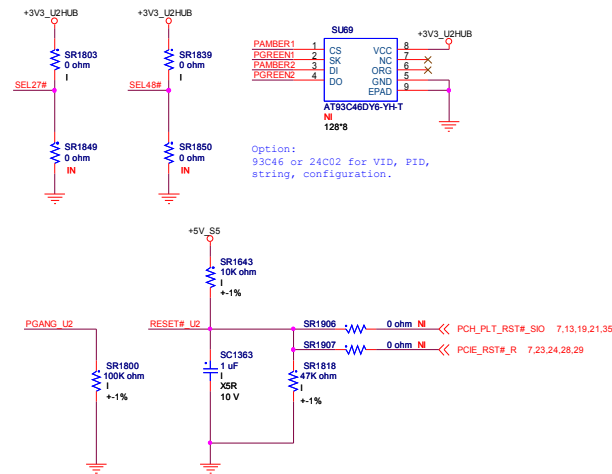
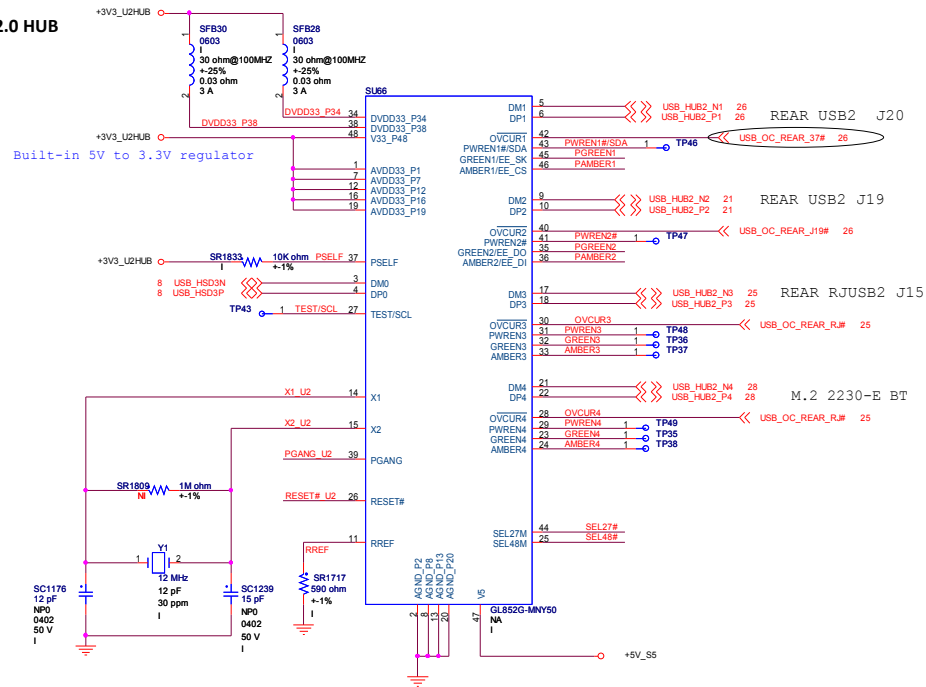


INPUT		Function
OE	S	
L	L	B1 Port
L	H	B2 Port
H	X	Disconnect



[illegible]

USB2.0 HUB



HDMI high speed signal level shift

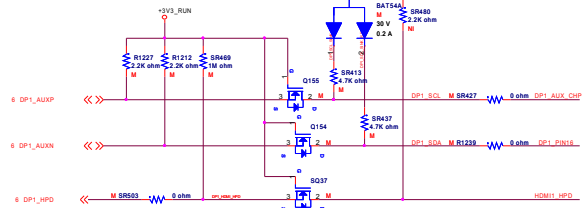
IF U7 NI below item INSTALL 0 ohm



CAD Note : Please place 470 ohm component as short as possible (to bridge the antenna effect)

HDMI other signal level shift

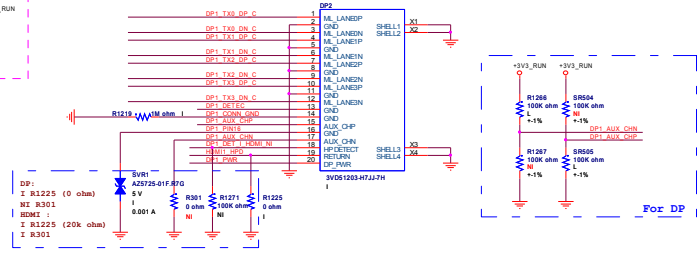
For HDMI



BOM --> L -DP ; M -HDMI

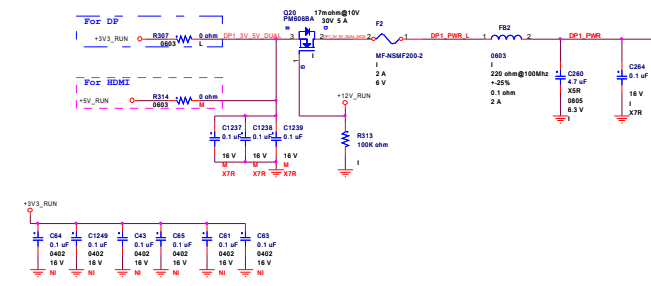


DP & HDMI co-lay Connector



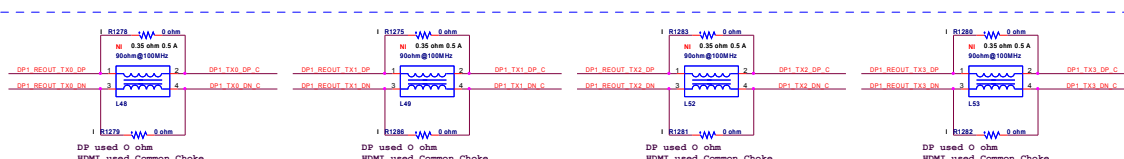
option for layout length not enough

DisplayPort Interoperability



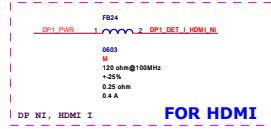
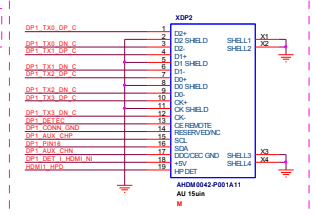
DP++(SUPPORT DONGLE)

CAD Note : Please place ESD component close to DP connector

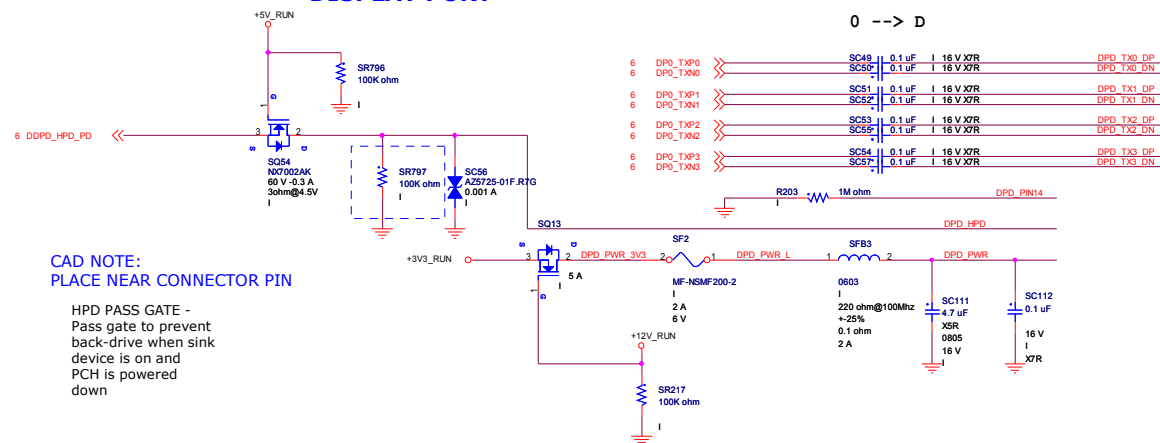


CAD Note : Please place Common Choke component close to DP & HDMI connector

Option for HDMI

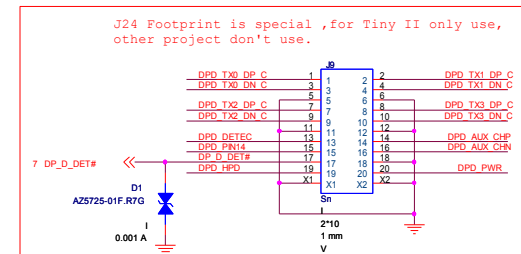


DISPLAY PORT



CAD NOTE:
PLACE NEAR CONNECTOR PIN

HPD PASS GATE -
Pass gate to prevent
back-drive when sink
device is on and
PCH is powered
down

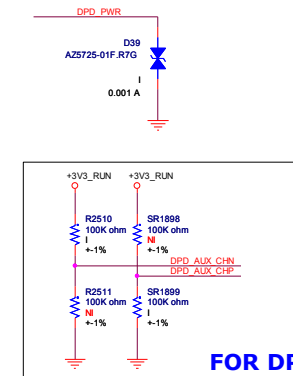


On Cable side Pin17 & Pin 18 need short

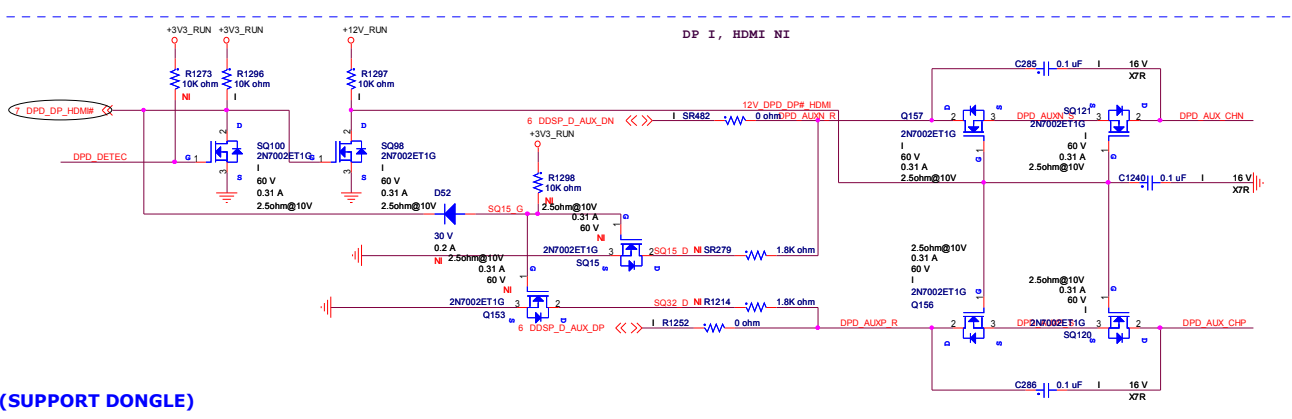
DPC_DETEC

L : Connect to Display Port or No Connection

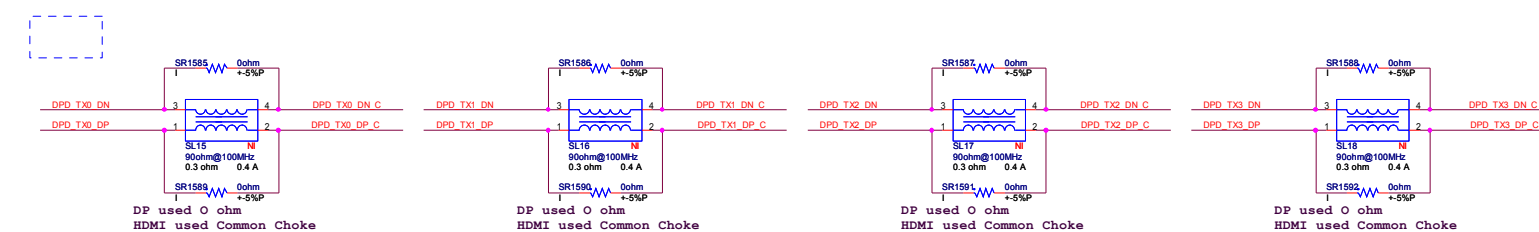
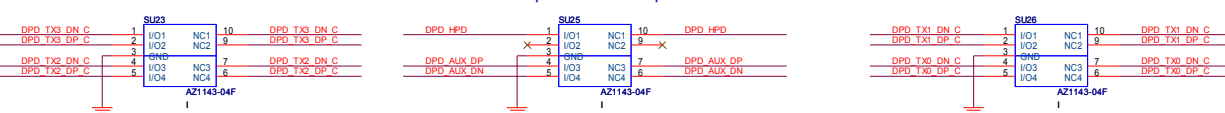
H : Connect to Dounge



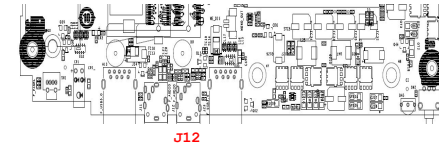
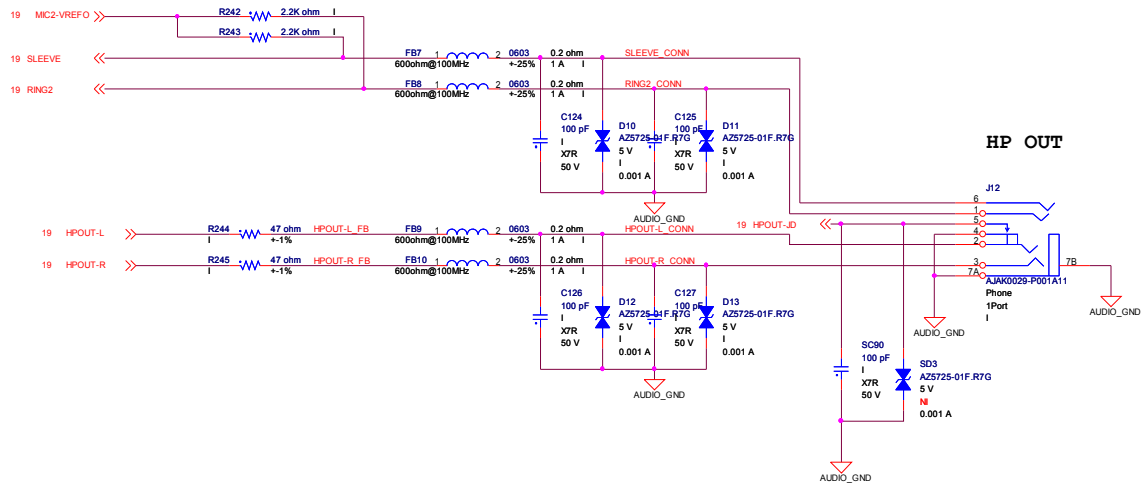
FOR DP



CAD Note : Please place ESD component close to DP connector

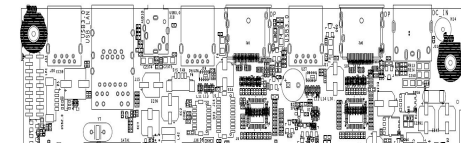
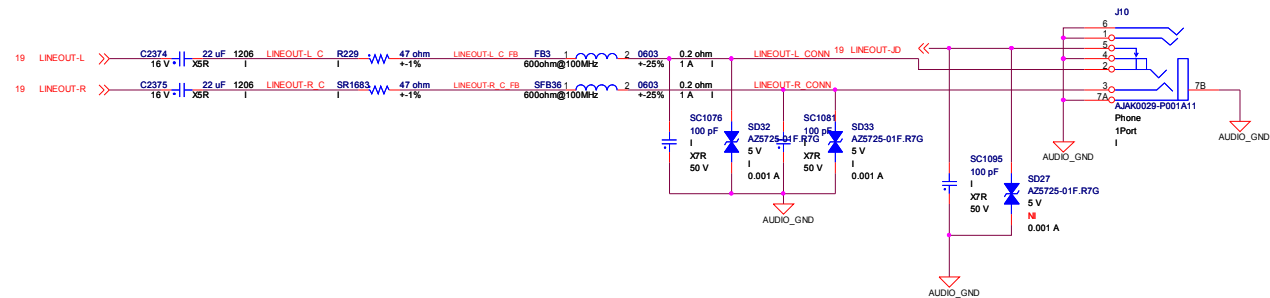


CAD Note : Please place Common Choke component close to J9 pinheader

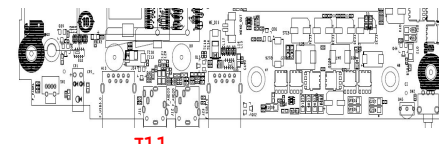
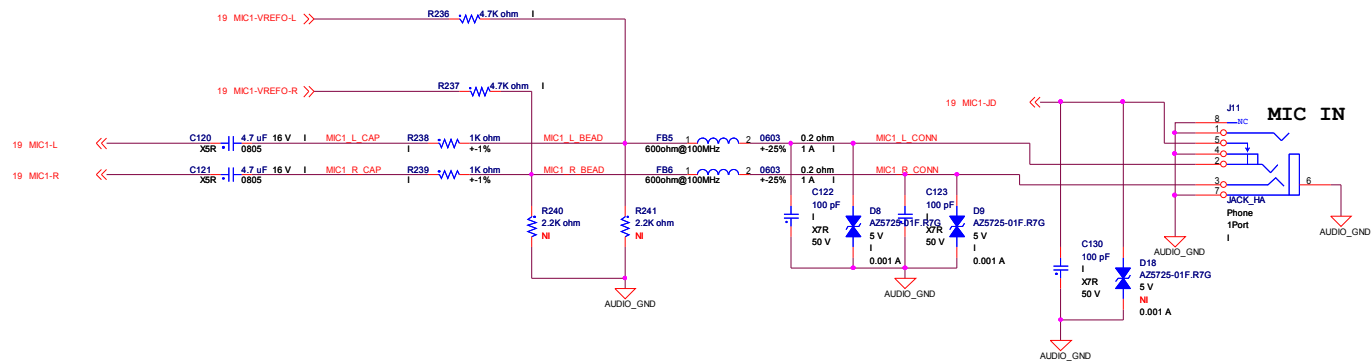


J12

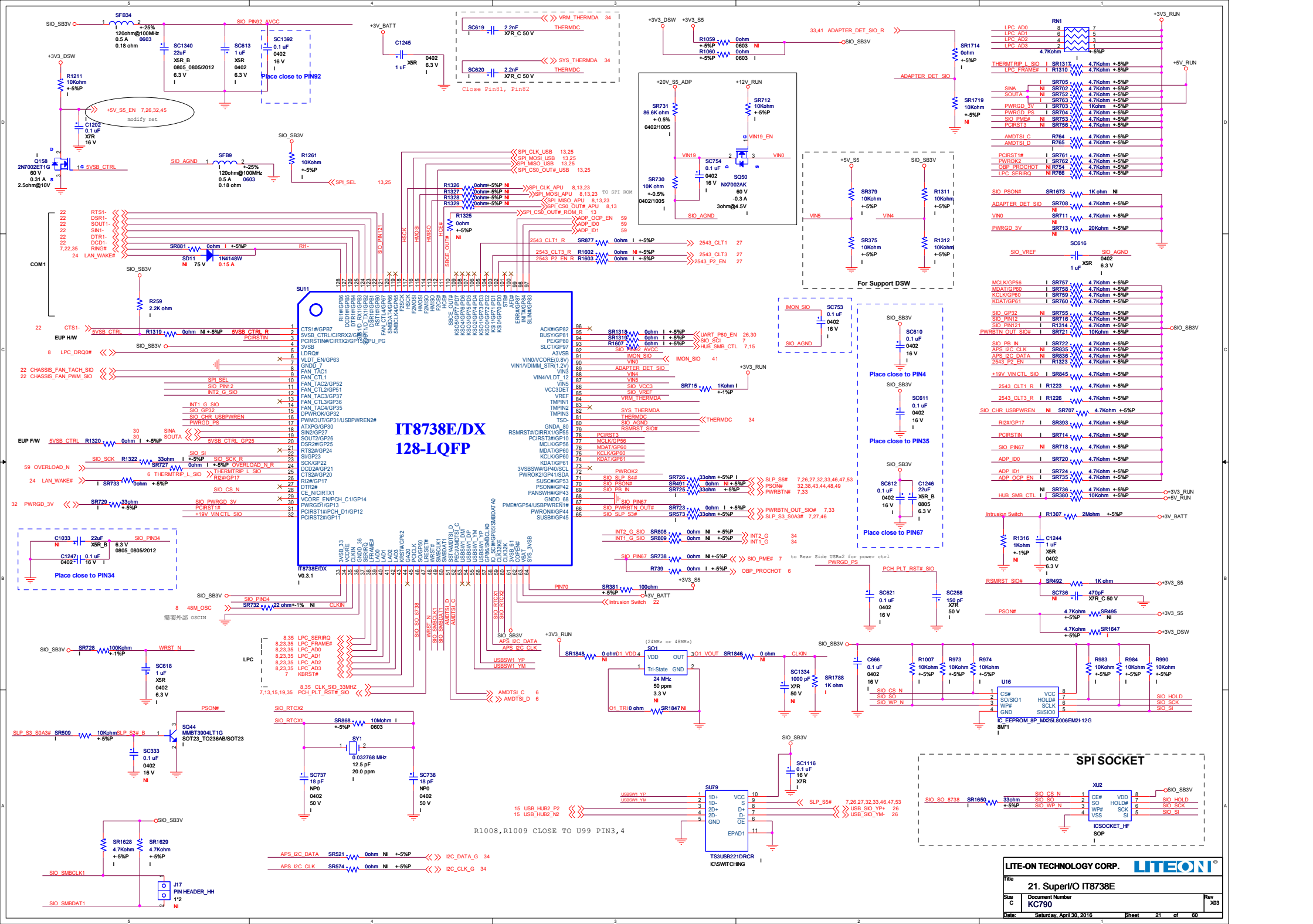
Rear - LINE OUT



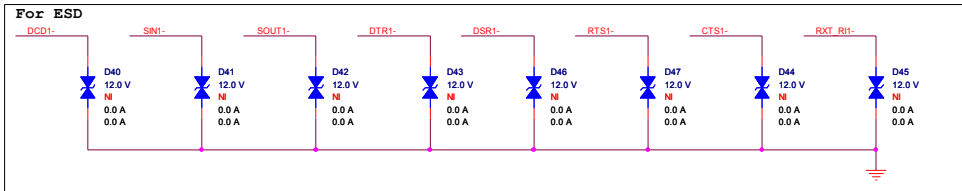
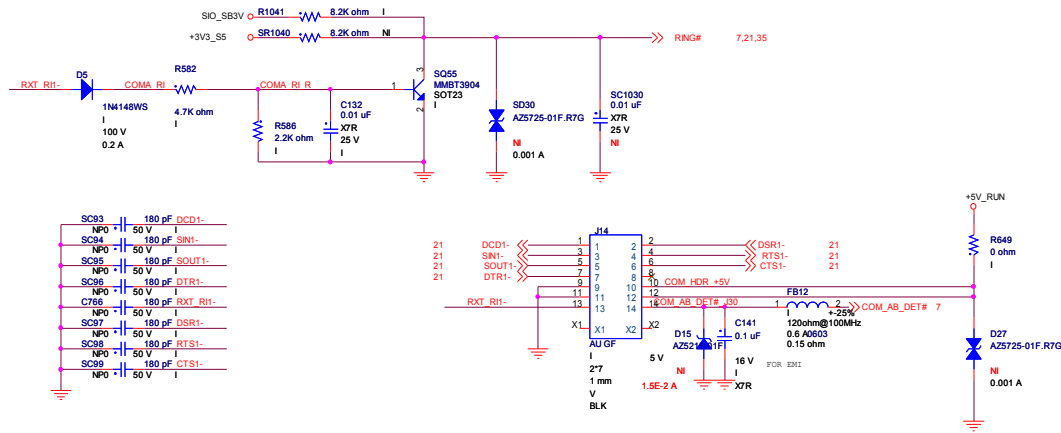
J10



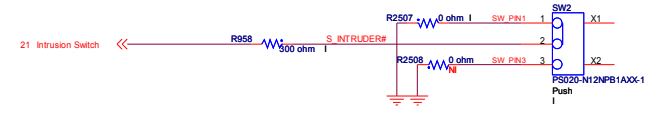
J11



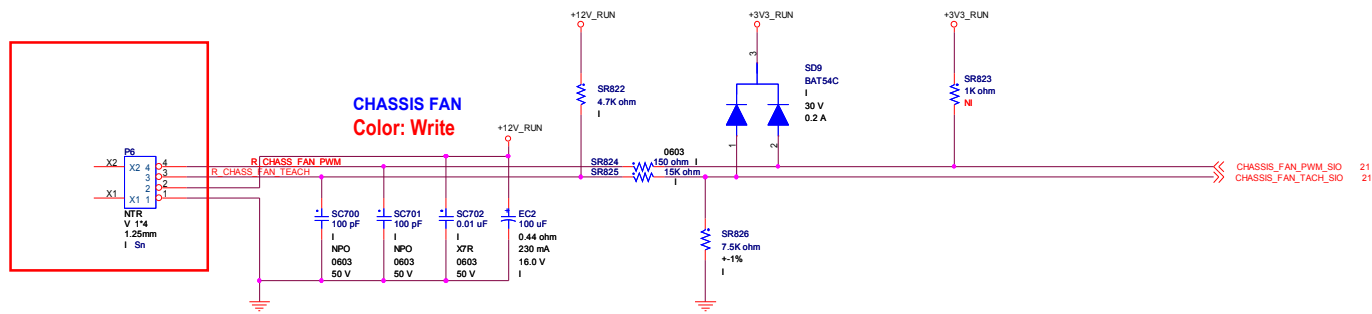
COM PORT HDR

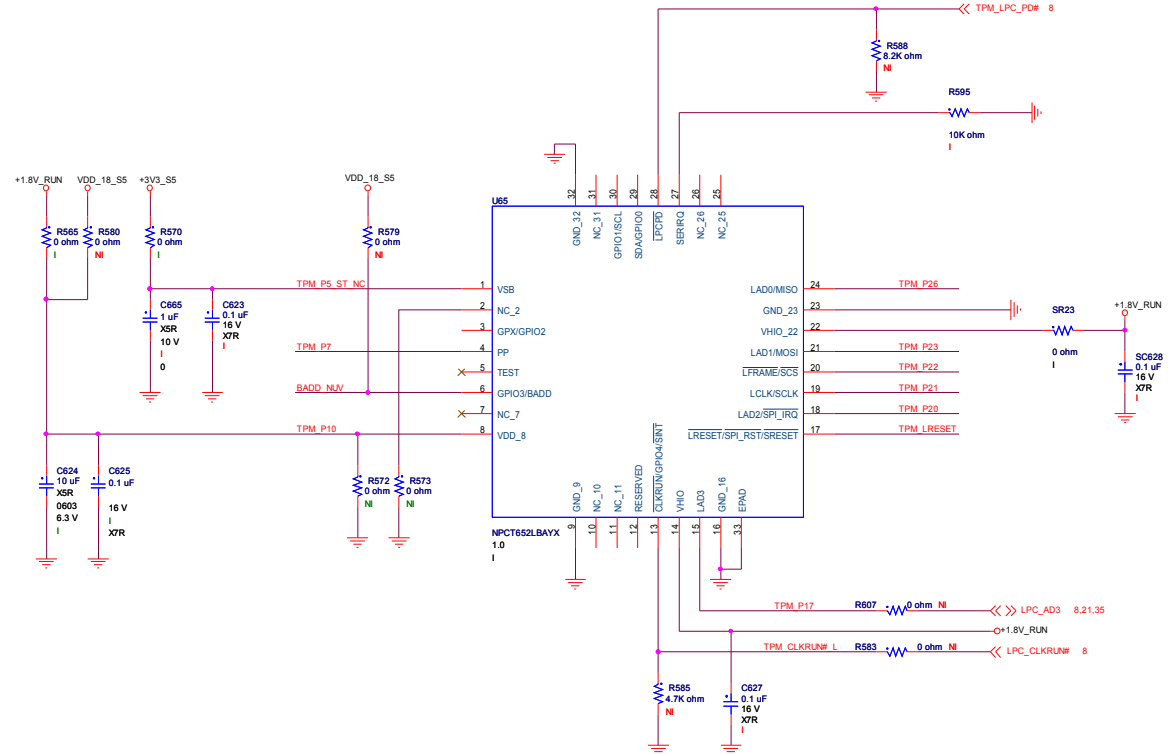


Intrusion Switch



CHASSIS/CPU/PSU FAN





CHANGE FROM NUVTION

R601

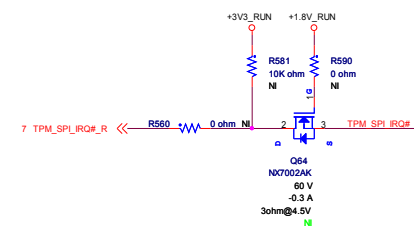
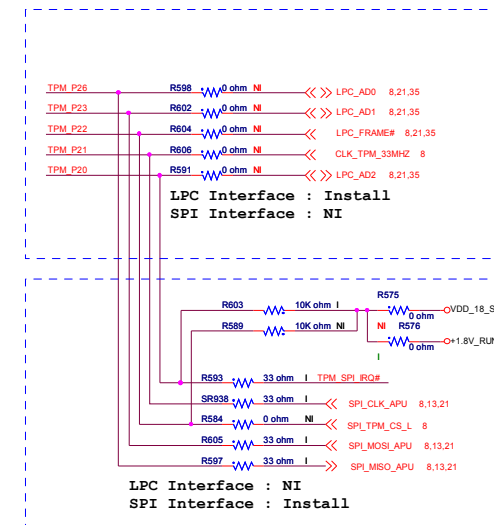
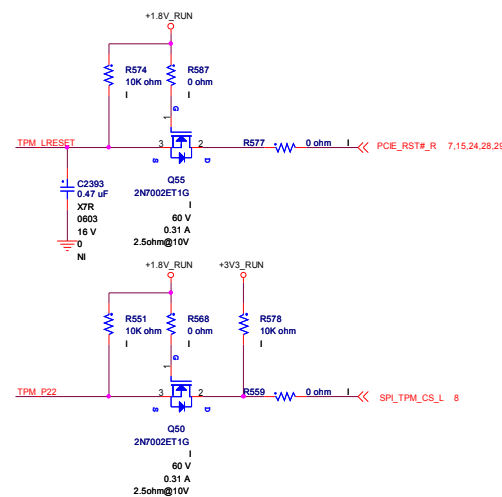
10K ohm

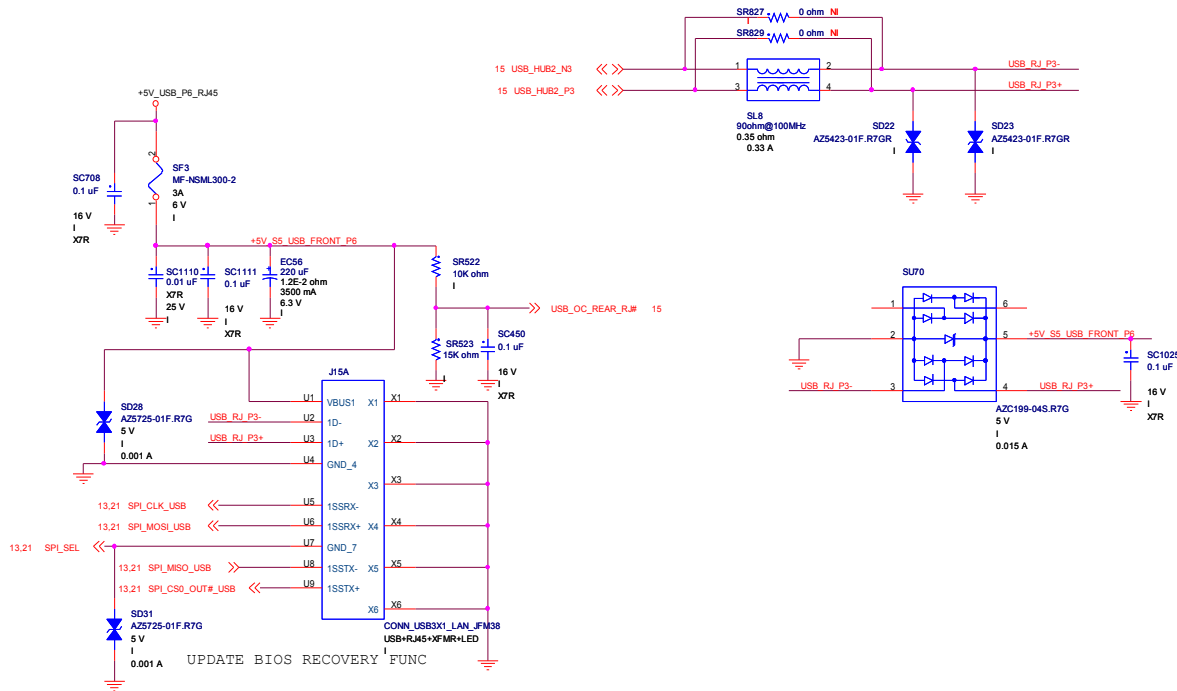
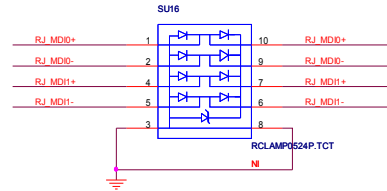
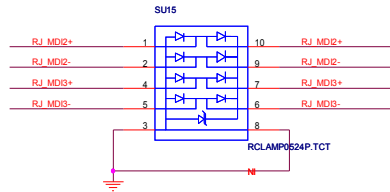
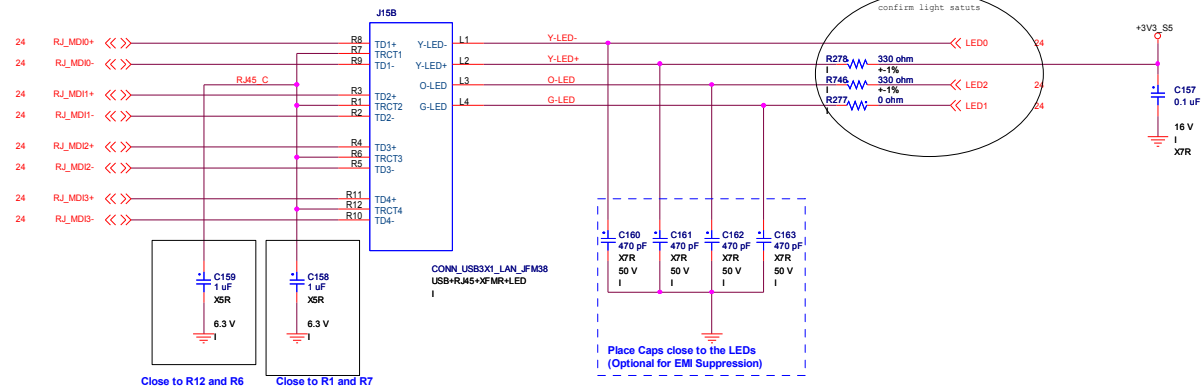
N

BADD	SELECTION
0	EEh - EFh
1	7Eh - 7Fh

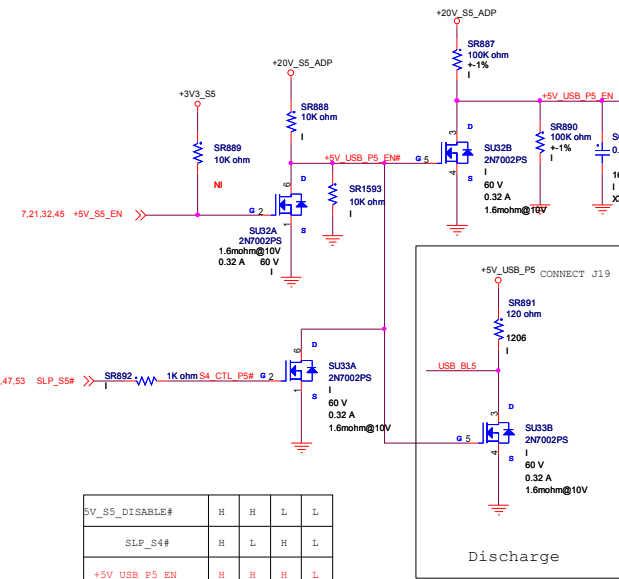
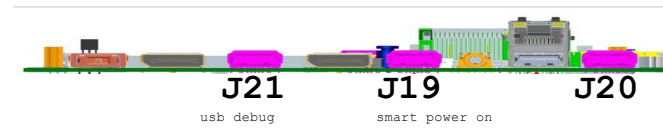
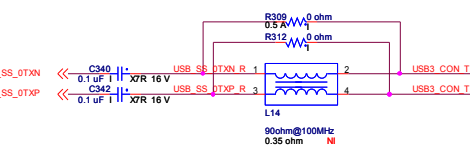
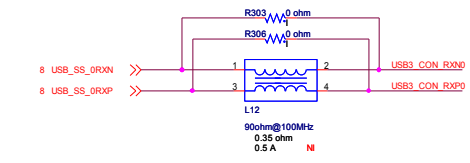
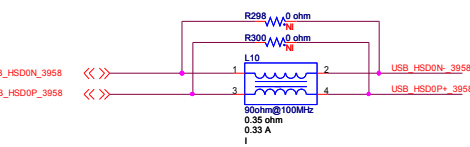
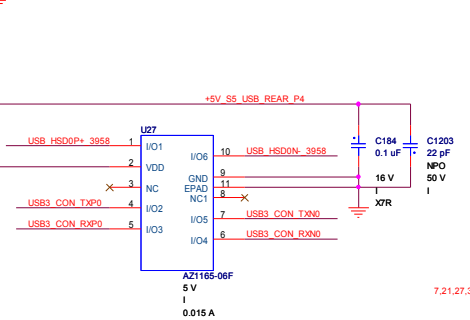
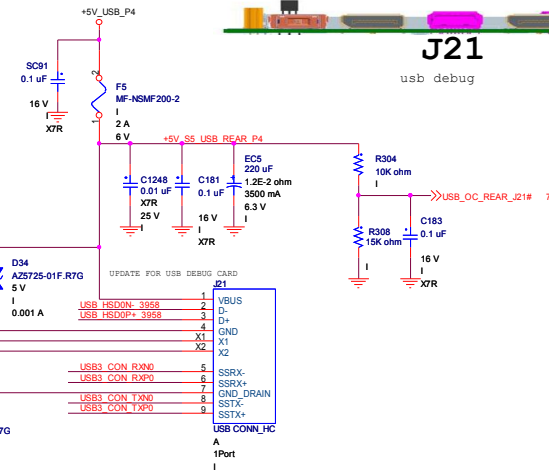
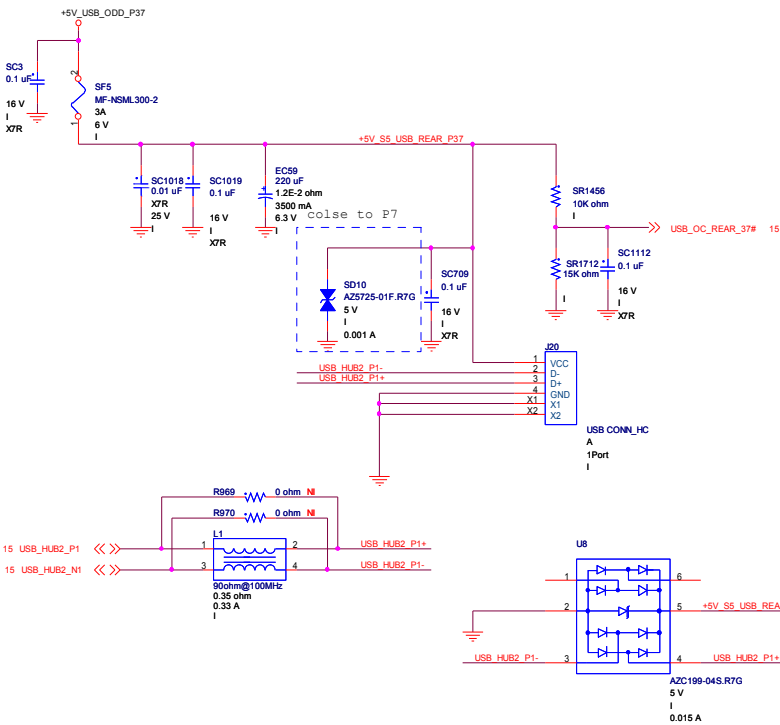
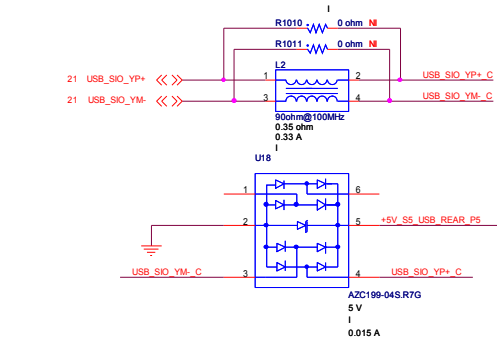
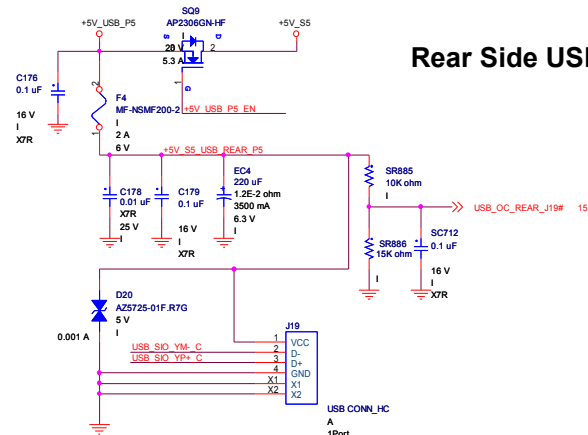
'1' - Pin is left open.
'0' - pin is pulled down.

Base Address
EE / EF

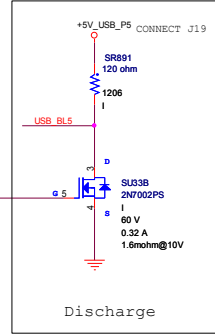




Rear Side USB2X2 USB3X1



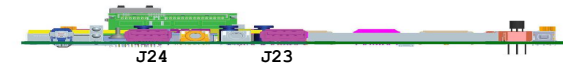
5V_SS_DISABLE#	H	H	L	L
SLP_S4#	H	L	H	L
+5V_USB_P5_EN	H	H	H	L



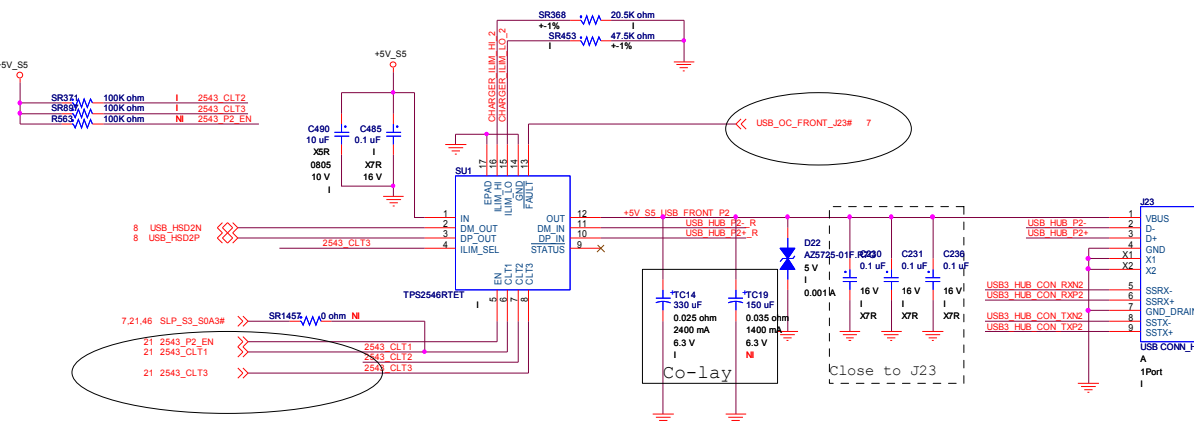
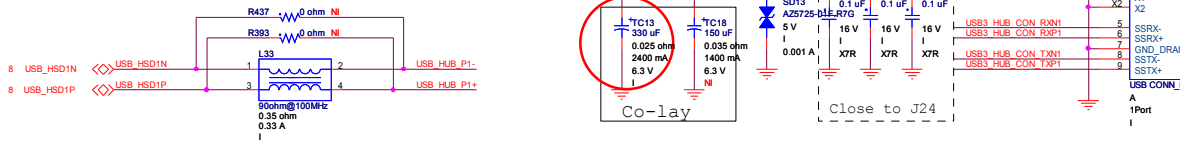
FRONT USB3.0 Charger x 1

ILIM_HI	20.5K	2.5A	DCP	Tiny S3/S4/S5
			CDP	Tiny S0
ILIM_LO	47.5K	1.1A	SDP	Tiny not support

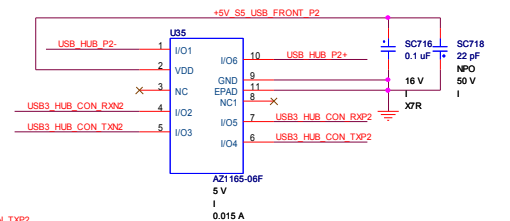
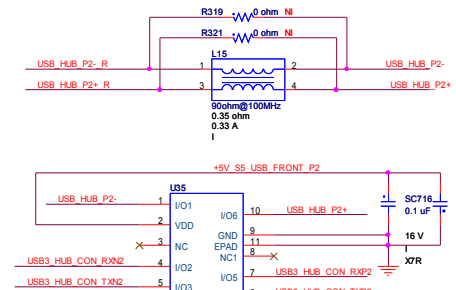
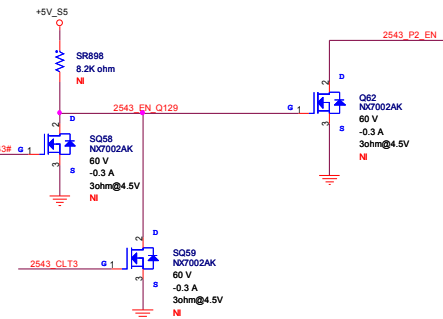
CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	0	Discharge	NA	off
0	0	0	1	Discharge	NA	off
0	0	0	0	DCP / auto	ILIM_HI	off
0	0	1	1	DCP / auto	I_{L2_reg} & ILIM_HI ⁽¹⁾	DCP load present ⁽²⁾
0	1	0	0	SDP	ILIM_LO	off
0	1	0	1	SDP	ILIM_HI	off
0	1	1	0	DCP / auto	ILIM_HI	off
0	1	1	1	DCP / auto	ILIM_HI	DCP load present ⁽³⁾
1	0	0	0	DCP / Shorted	ILIM_LO	off
1	0	0	1	DCP / Shorted	ILIM_HI	off
1	0	1	0	DCP / Divider1	ILIM_LO	off
1	0	1	1	DCP / Divider1	ILIM_HI	off
1	1	0	0	SDP	ILIM_LO	off
1	1	0	1	SDP	ILIM_HI	off
1	1	1	0	SDP ⁽⁴⁾	ILIM_LO	off
1	1	1	1	CDP ⁽⁴⁾	ILIM_HI	CDP load present ⁽⁵⁾



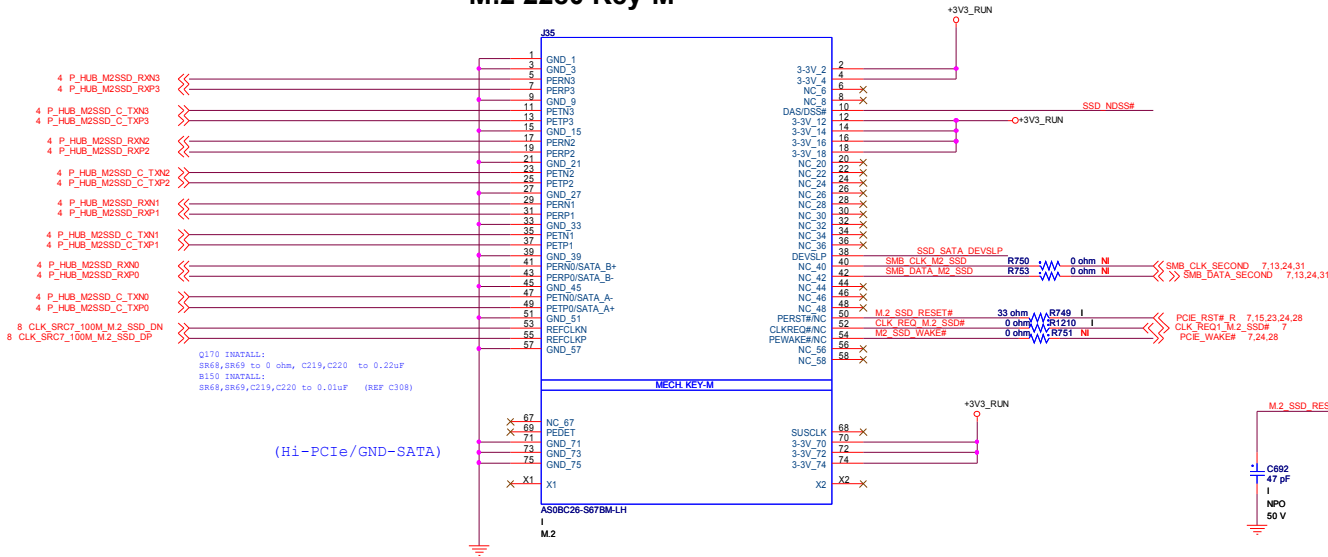
Follow BOM With J24



2543_CLT3	H	H	L	L
SLP_S4#	H	L	H	L
2543_EN	H	H	H	L



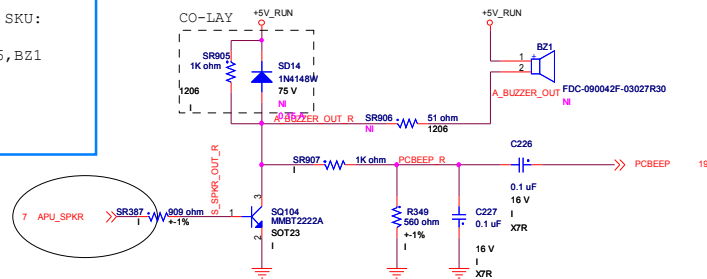
SSD Card PCIe M.2 2280 Key-M



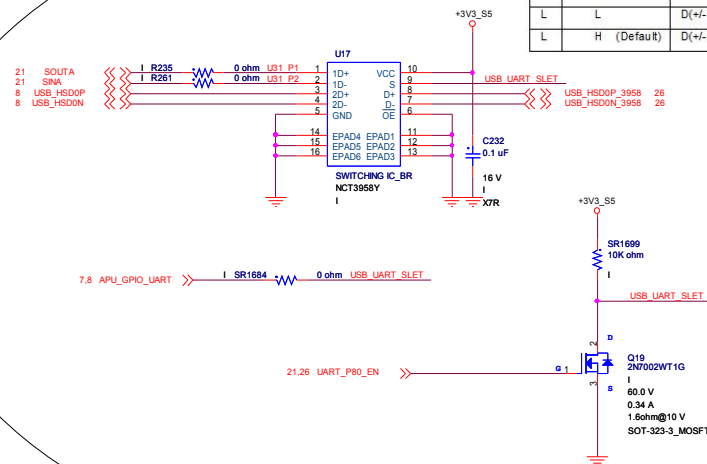
SATA_LED Circuit

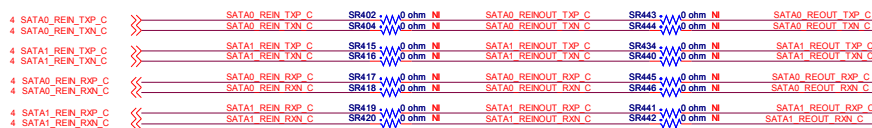
For Google SKU:
Install
SD14 ,SR906,BZ1

Remove
SR905

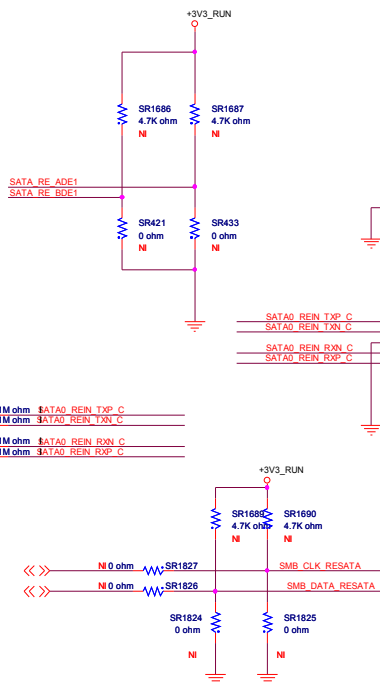
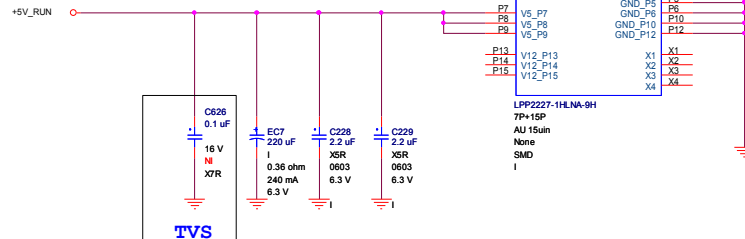


OE#	S	Function
H	X	Disable
L	L	D(+/-) to 1D(+/-)
L	H (Default)	D(+/-) to 2D(+/-)

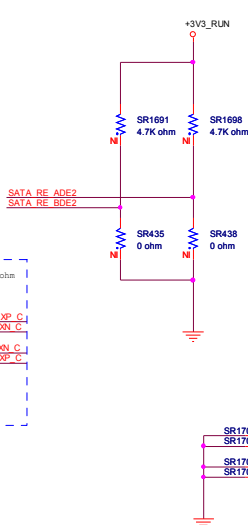




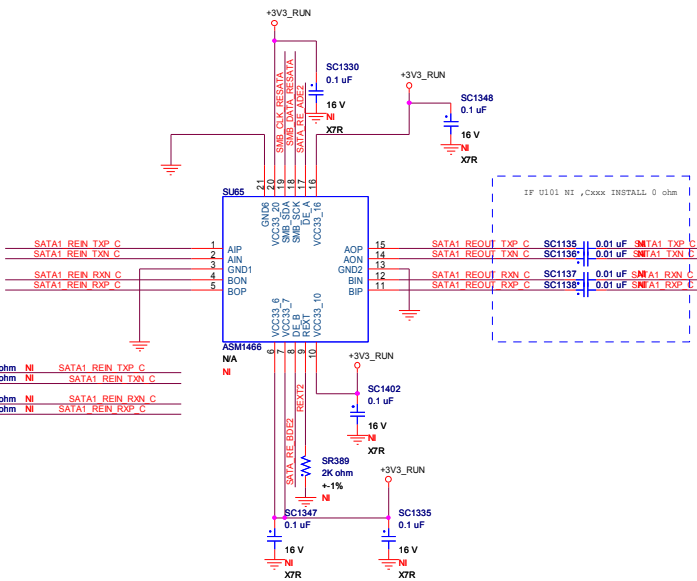
SATA-CONN



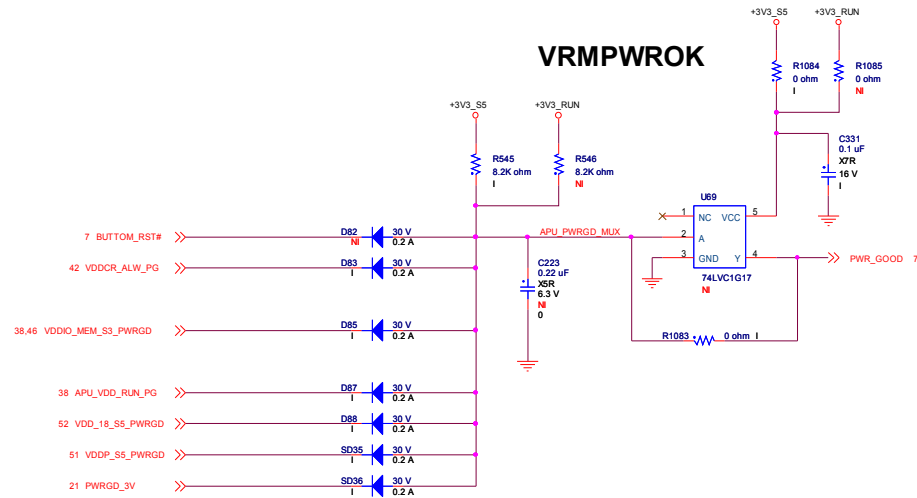
SATA0 REDIRVER



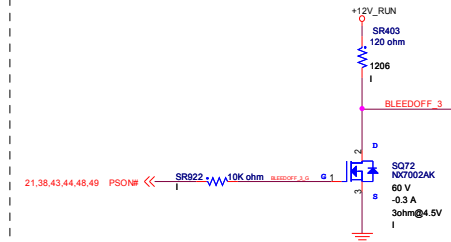
SATA1 REDIRVER



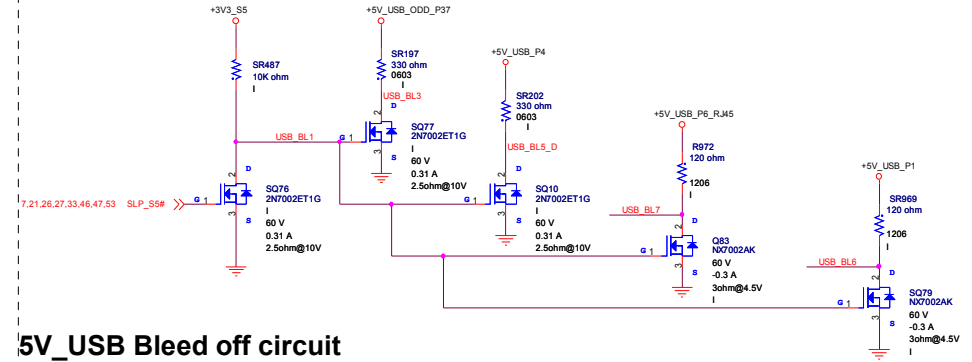
VRMPWROK



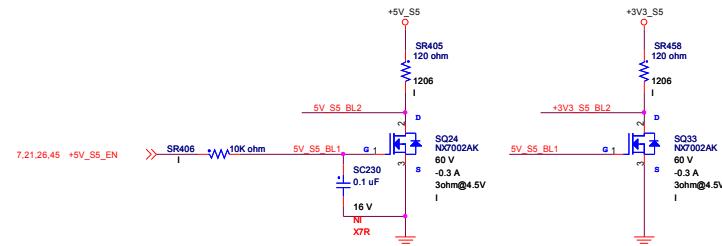
+12V Bleed off circuit



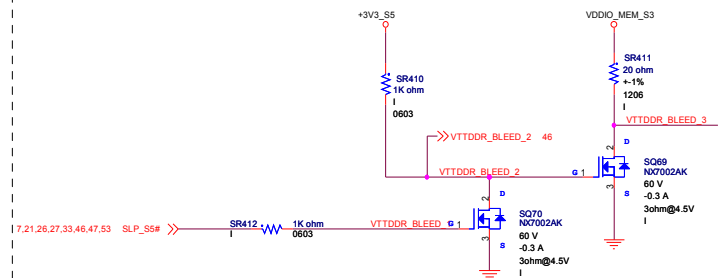
5V_USB Bleed off circuit



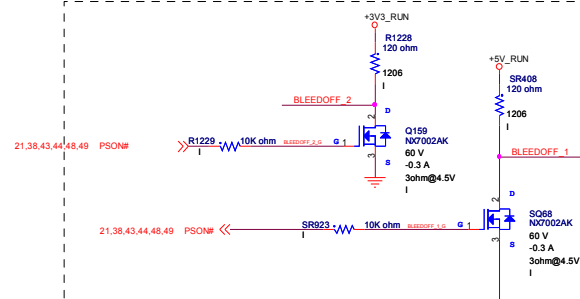
5V_S5 and 3V_S5 Bleed off circuit



DESIGN NOTE: THESE CIRCUITS ARE USED TO BLEED OFF 1.5V DDR



+1V2_MEM Bleed off circuit



5V & 3.3V Bleed off circuit

CONTROL PANEL / LED CIRCUITRY

POWER BUTTON & LED

Color	Functoin
G	HDD
G	WiFi
G	BT

Id = 25mA @ 2.8V (SPEC)
 Id = (5V-2.8V) / 330ohm = 5mA
 5m * 3.2 V = 16 mW
 0.1W (For Current limit R)

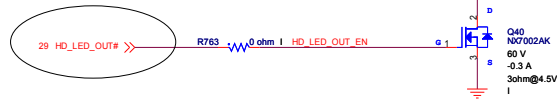
For NEC SKU:
Remove:
R765Q,Q42,R762
SW1
CR1

Install :
R779
SW1_
CR1_

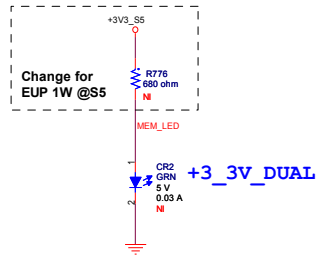
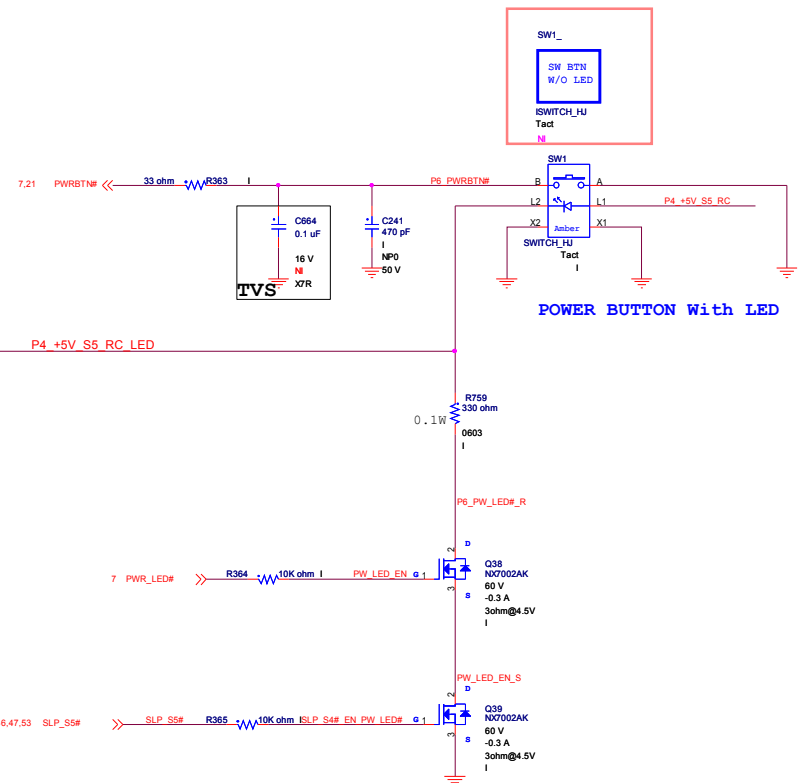
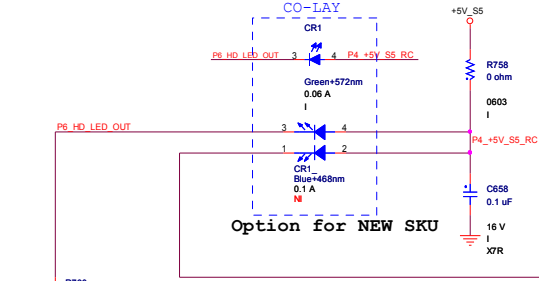
WLAN LED

HDD LED

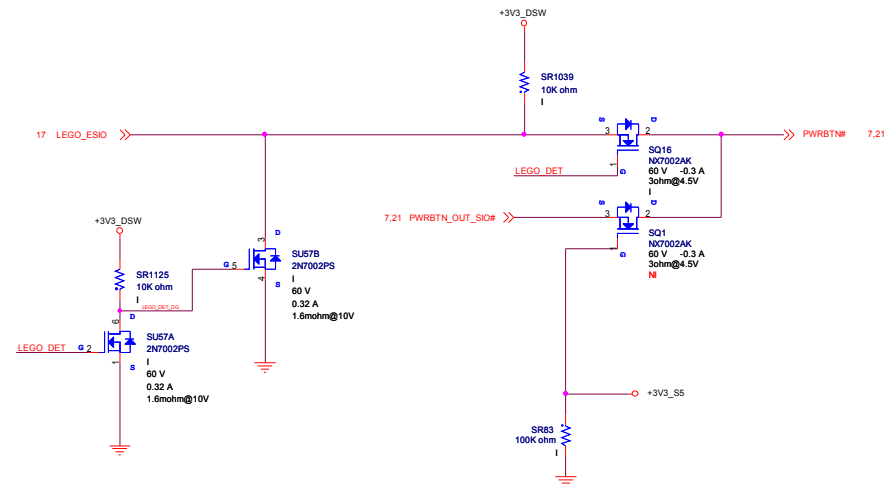
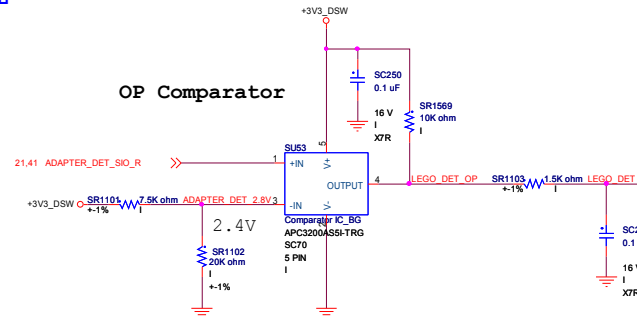
BT LED



Stack LED



PCA LED CIRCUITS



[illegible]

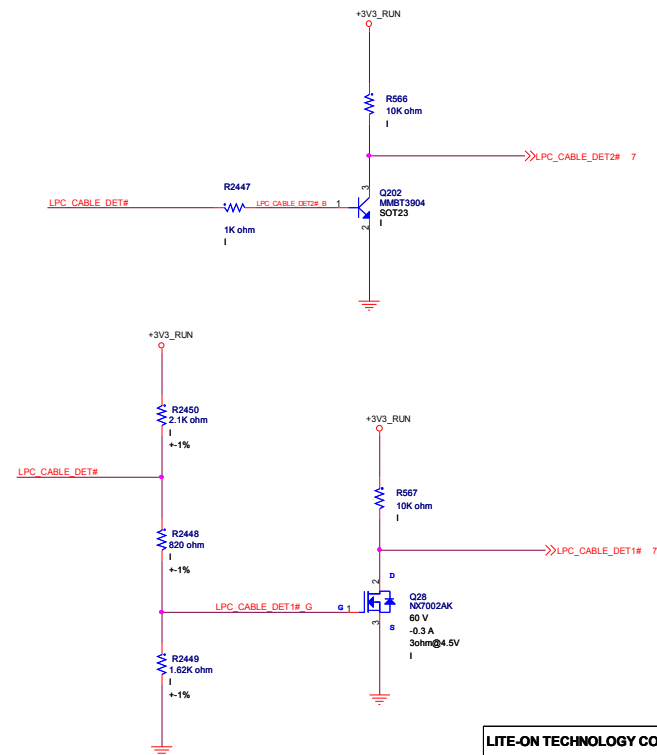
Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconductor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

The schematic diagram illustrates the power and signal connections for the SC1029 module. The module's pins are numbered 1 through 16. The connections are as follows:

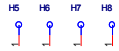
- Pin 1:** Connected to +3V3_RUN.
- Pin 2:** Connected to RING#.
- Pin 3:** Connected to CLK.
- Pin 4:** Connected to FRAME#.
- Pin 5:** Connected to PCH_PLT_RST# SIO.
- Pin 6:** Connected to LPC_SERIRQ.
- Pin 7:** Connected to LPC_ADI.
- Pin 8:** Connected to LPC_ADI.
- Pin 9:** Connected to LPC_ADI.
- Pin 10:** Connected to LPC_ADI.
- Pin 11:** Connected to LPC_ADI.
- Pin 12:** Connected to LPC_ADI.
- Pin 13:** Connected to LPC_ADI.
- Pin 14:** Connected to LPC_ADI.
- Pin 15:** Connected to LPC_ADI.
- Pin 16:** Connected to +12V_RUN.
- Pin 17:** Connected to PCH_PLT_RST# SIO.

Power connections include +3V3_RUN, +5V_S5, and +12V_RUN. Signal connections include CLK, FRAME#, PCH_PLT_RST# SIO, LPC_ADI, LPC_DET#, and RING#. A dashed box highlights the PCH_PLT_RST# SIO connection to pin 17. Component values are specified for capacitors (SC1020, SC1029, C492) and resistors (SR1574).

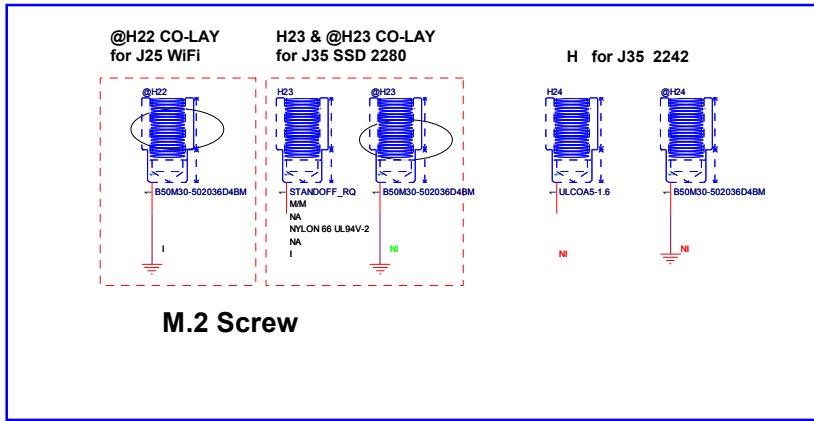
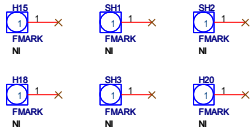
	LPC_CARD_DET#	LPC_CABLE_DET2#	LPC_CABLE_DET1#
No Card	Float (1.2V)	L	H
Card A	0V	H	H
Card B	3.3V	L	L



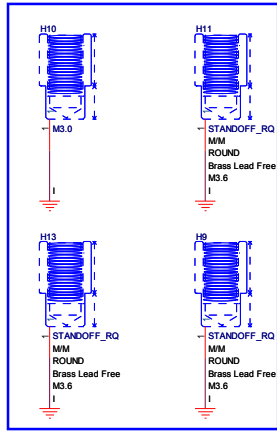
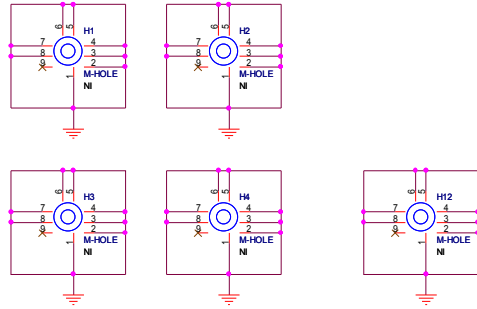
CPU HEATSINK_HOLE



FAN DUCT



M.2 Screw



HDD Cage



LABEL
10*10 mm
BIOS
LABEL-BIOS-AM 686 PLCC-RoHS



11S_LABEL
28*5.5 mm



PCB1
X01
174*175*1.6mm
OSP



Housing
9*5.7*3.5mm



LABEL
17*7mm

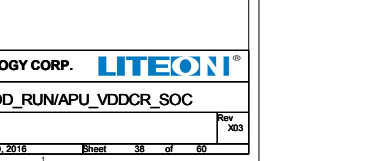
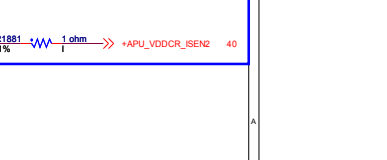
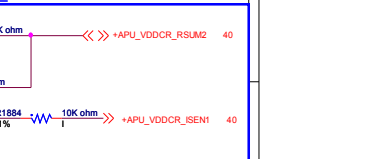
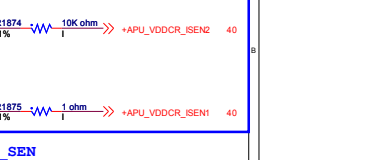
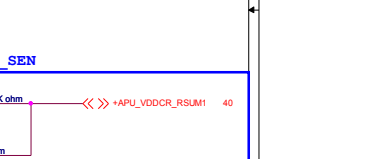
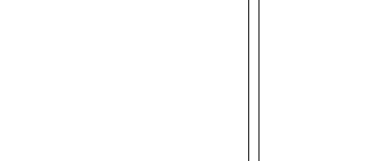
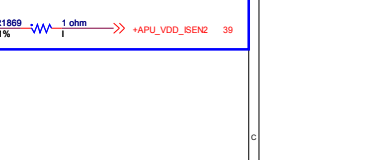
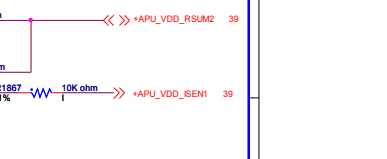
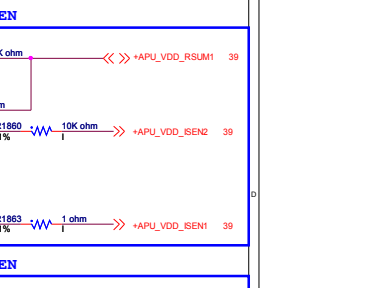
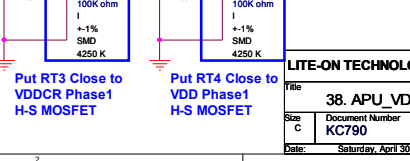
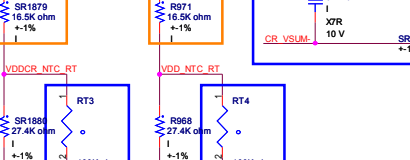
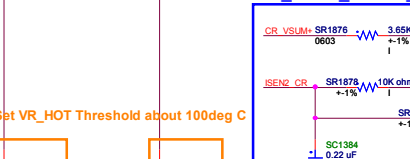
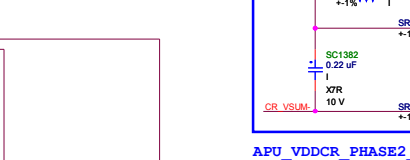
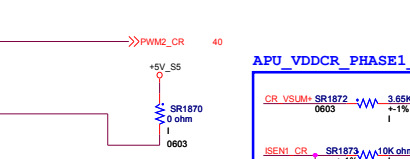
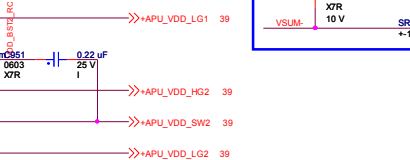
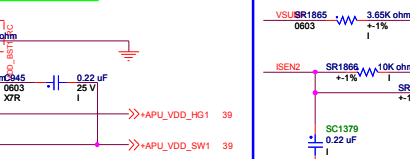
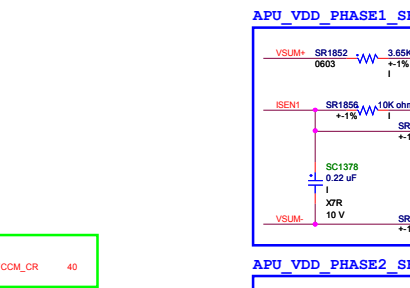
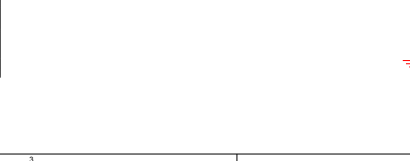
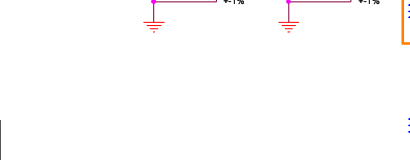
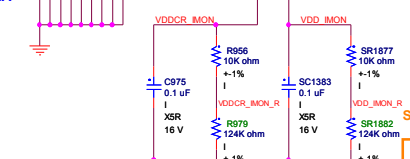
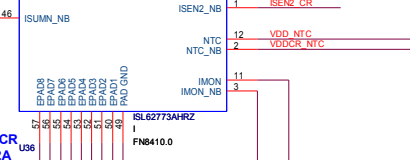
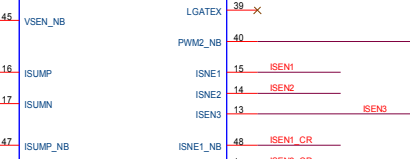
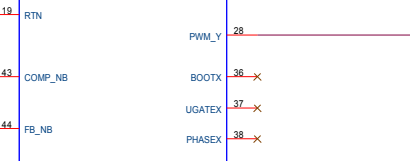
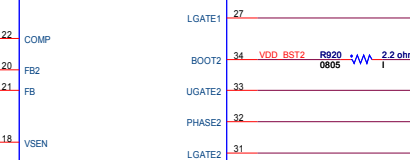
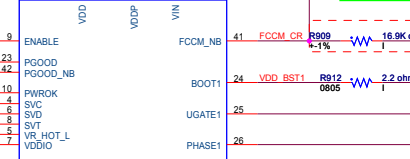
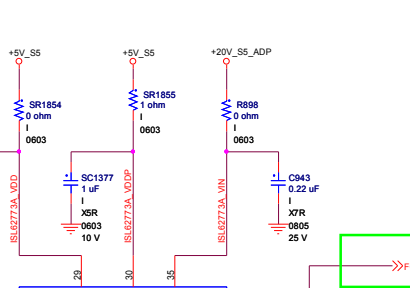
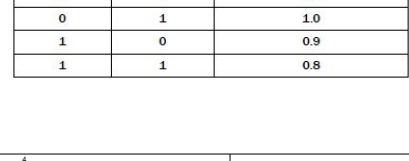
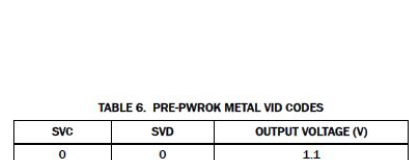
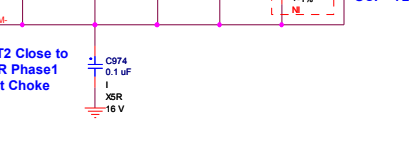
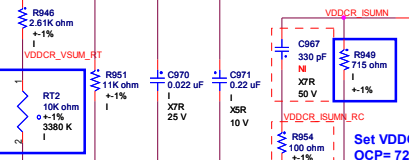
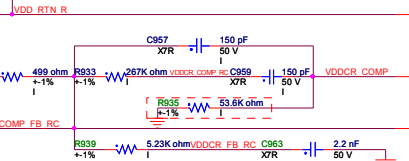
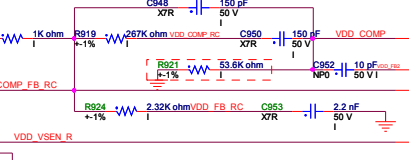
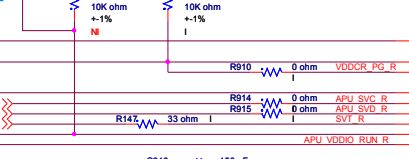
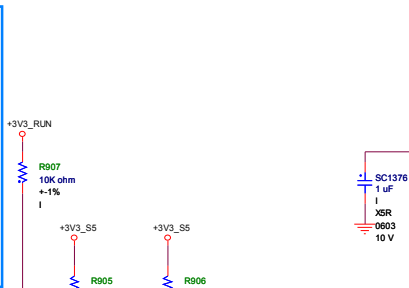
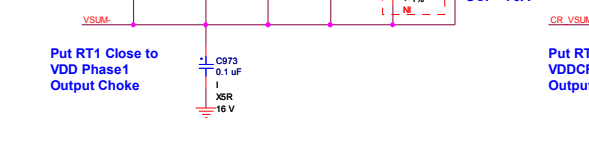
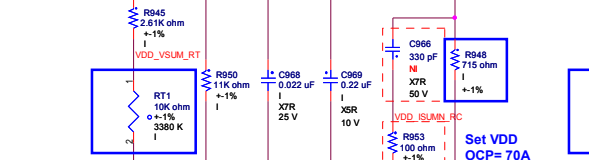
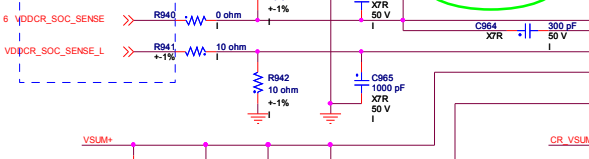
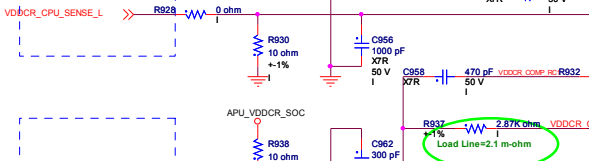
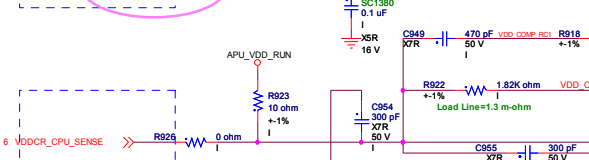
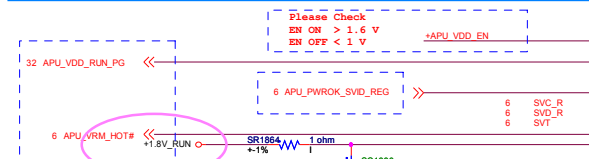
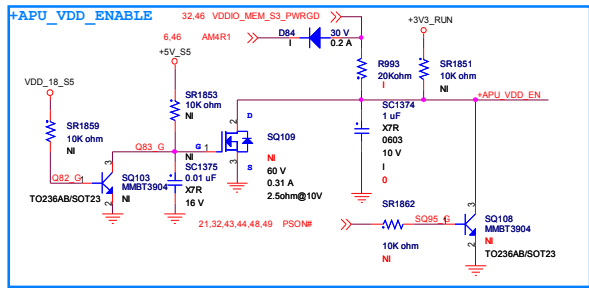
LITE-ON TECHNOLOGY CORP. LITEON®

File 36. Mounting Hole/ PCB/ Metal

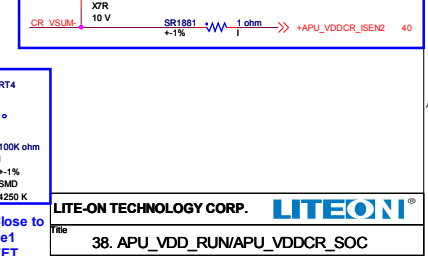
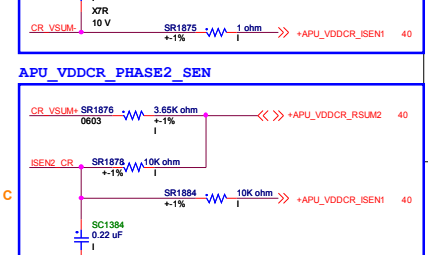
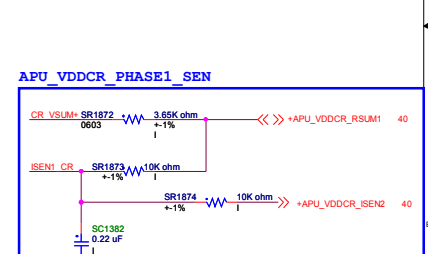
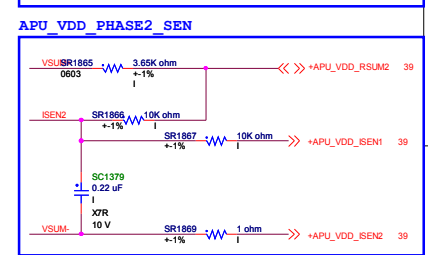
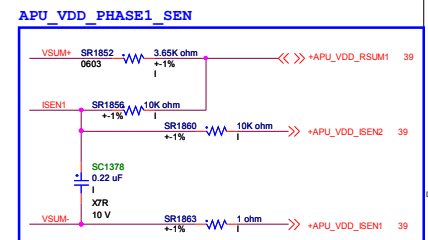
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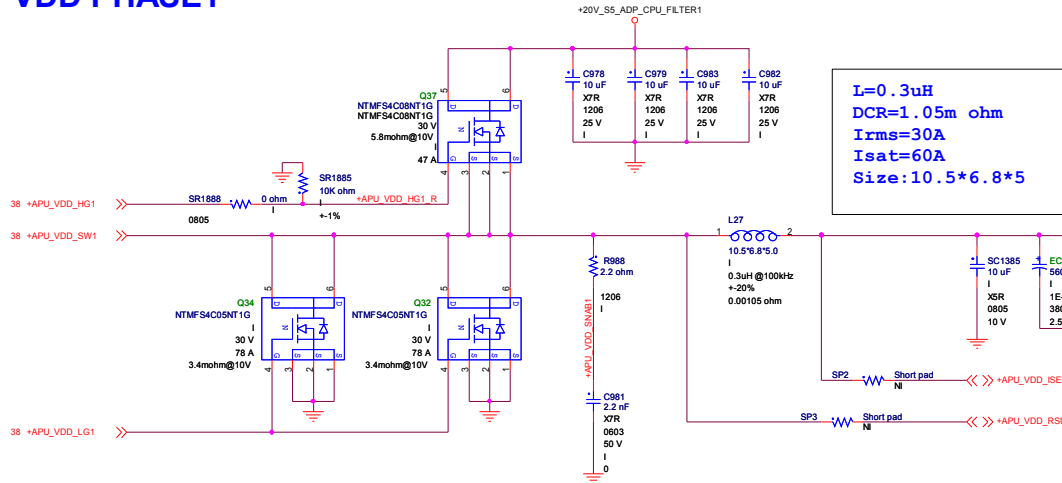
[illegible]



SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



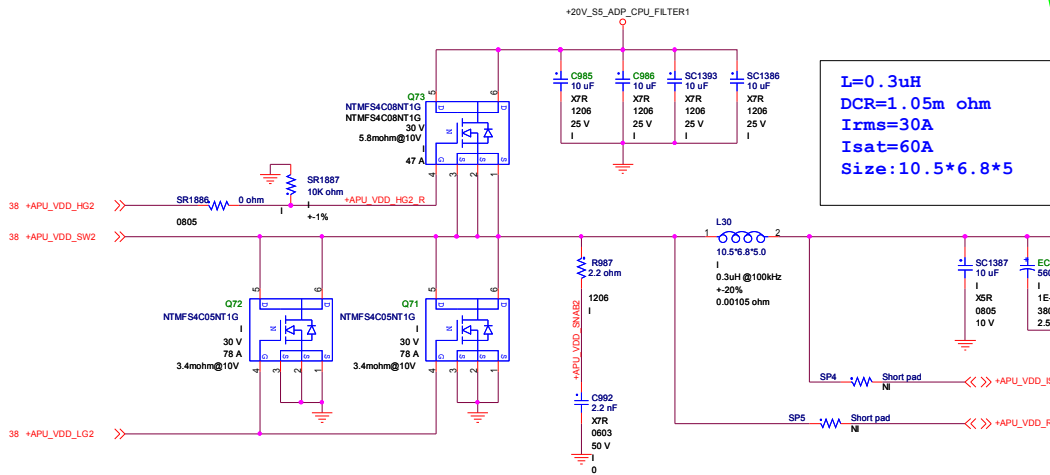
VDD PHASE1



APU_VDD_RUN

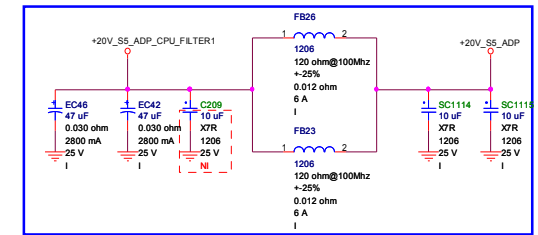
TDC:39A
 I_{max}:55A
 OCP:70A
 DC Load Line:1.3 mohm
 F_{sw}:300KHz

VDD PHASE2

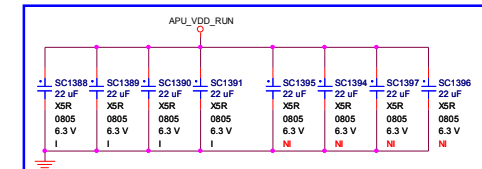


$C_{\text{in}}=127\mu\text{F}(\text{EC}+\text{MLCC})$
 ripple current: 9.82A
 $C_{\text{out}}=3288\mu\text{F}(\text{EC}+\text{POSCAP}+\text{MLCC})$
 ripple current:14.17A

APU_VDD_RUN_VIN_POWER

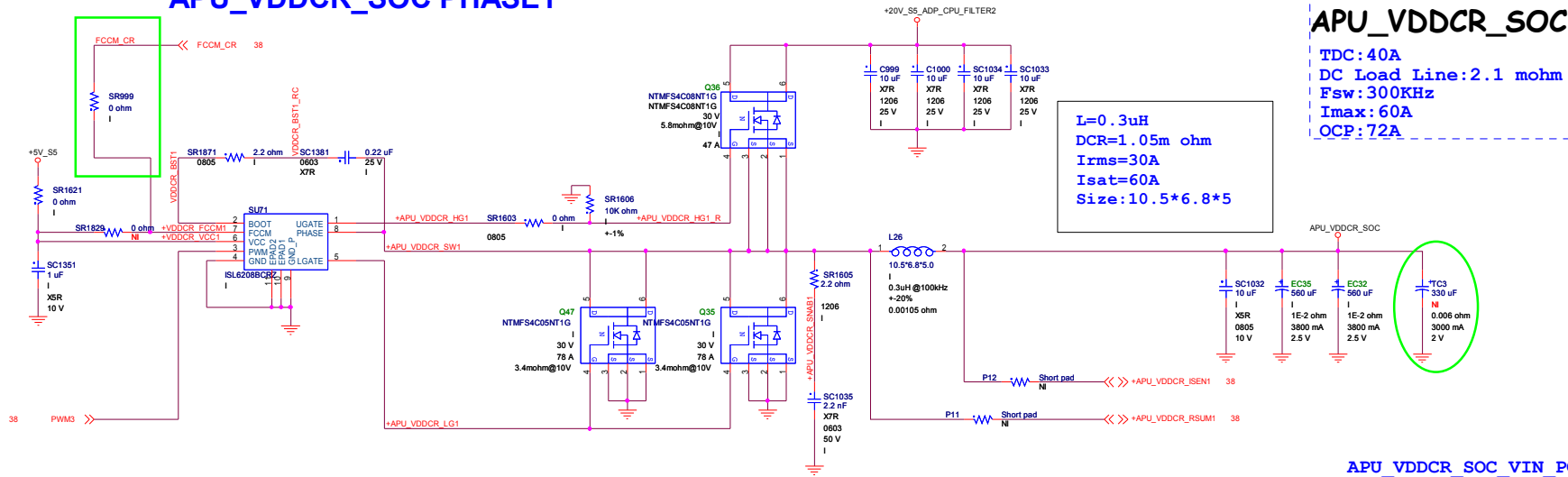


APU_VDD_RUN_Output_MLCC

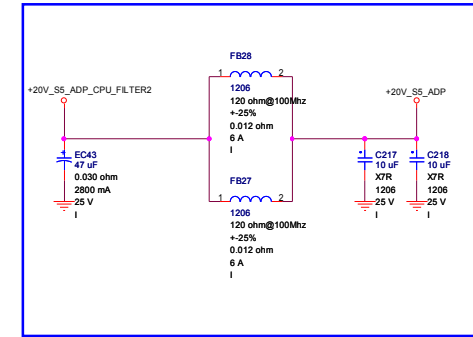


MLCC ripple current(at 5 degree)= 2.49A, ESR= 4 mohm

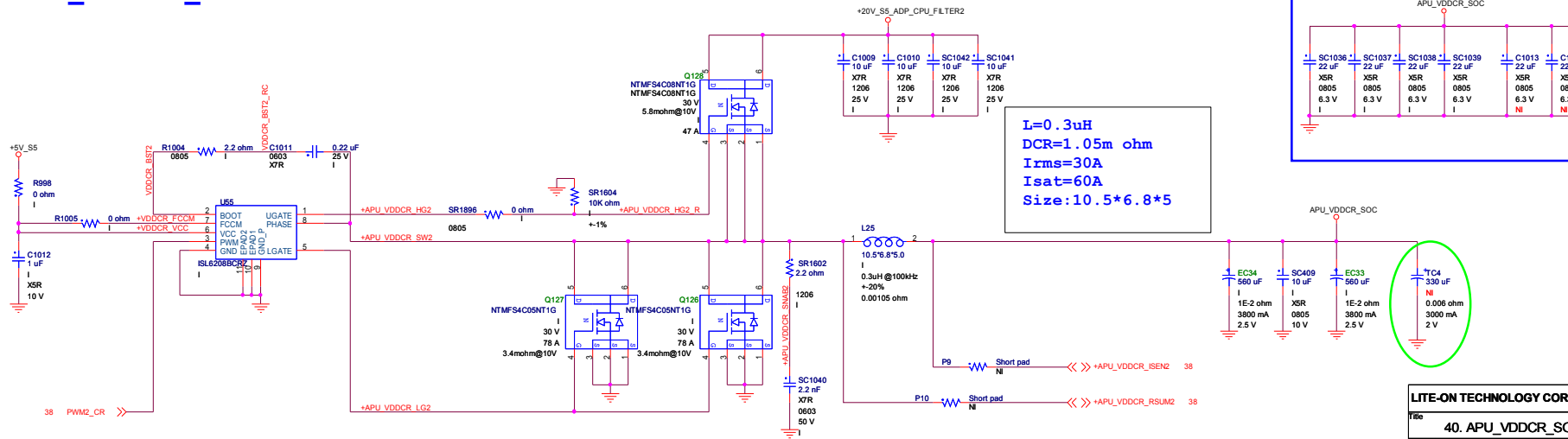
APU_VDDCR_SOC PHASE1



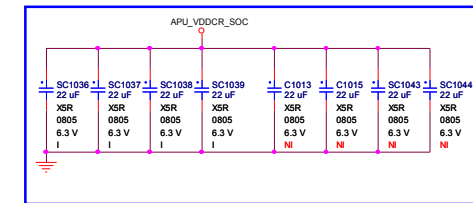
APU_VDDCR_SOC_VIN_POWER

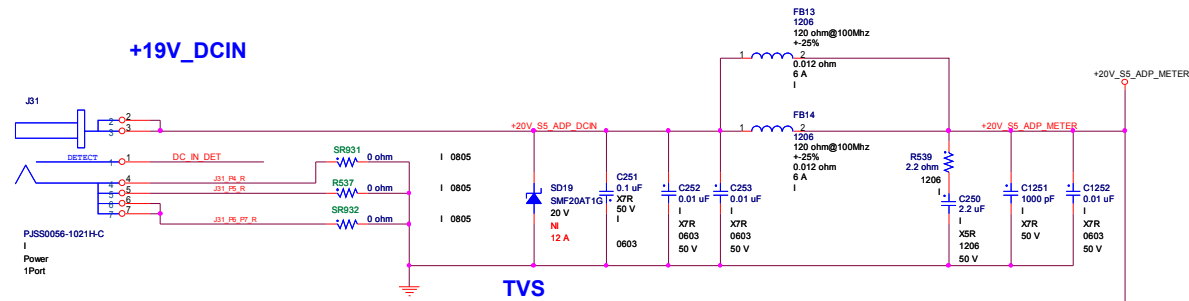


APU_VDDCR_SOC PHASE2

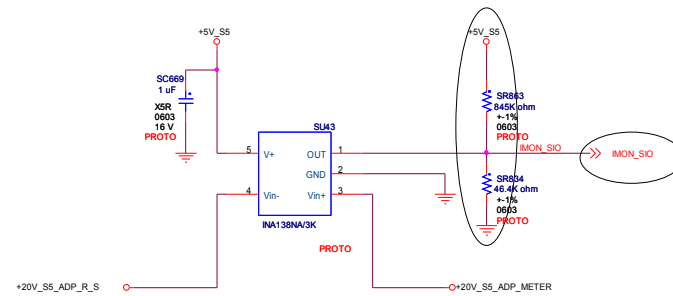
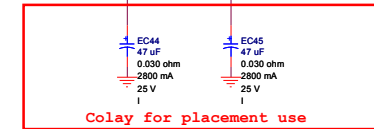
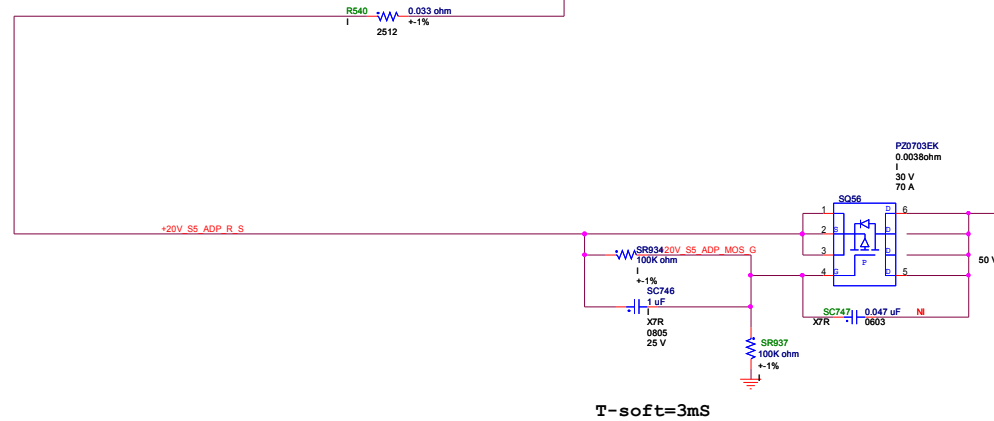
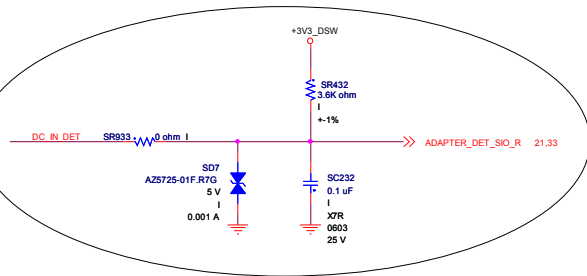
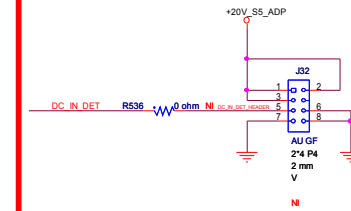


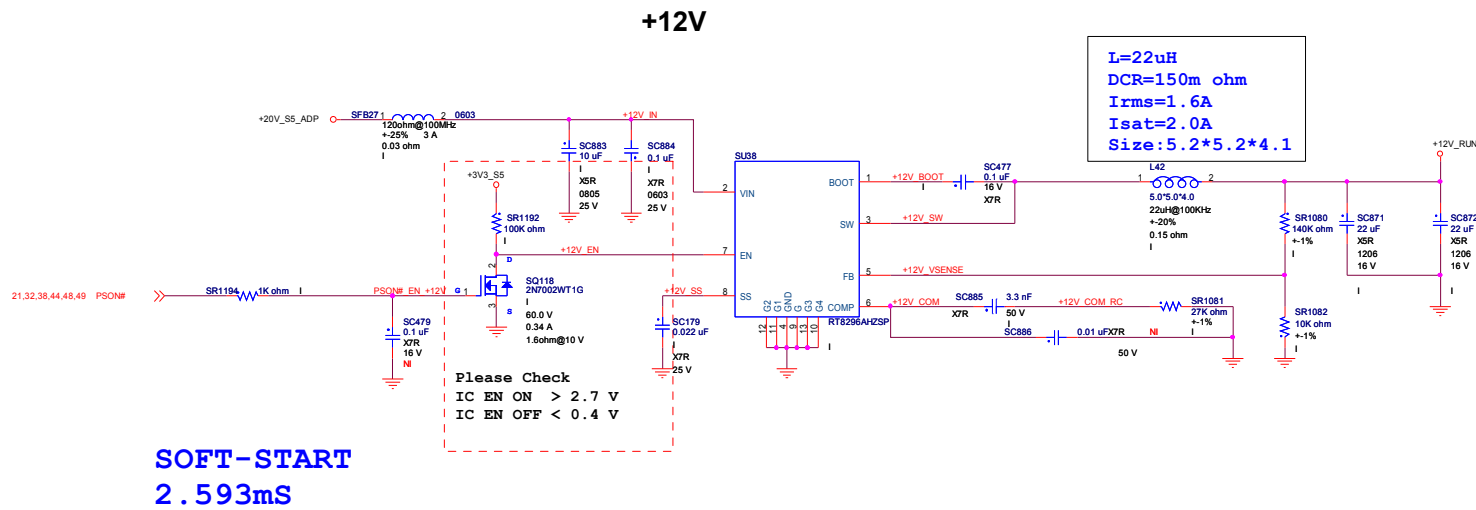
APU_VDDCR_SOC_Output_MLCC

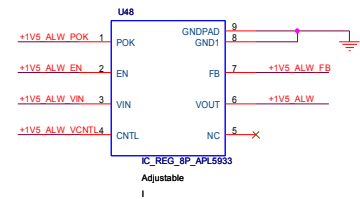
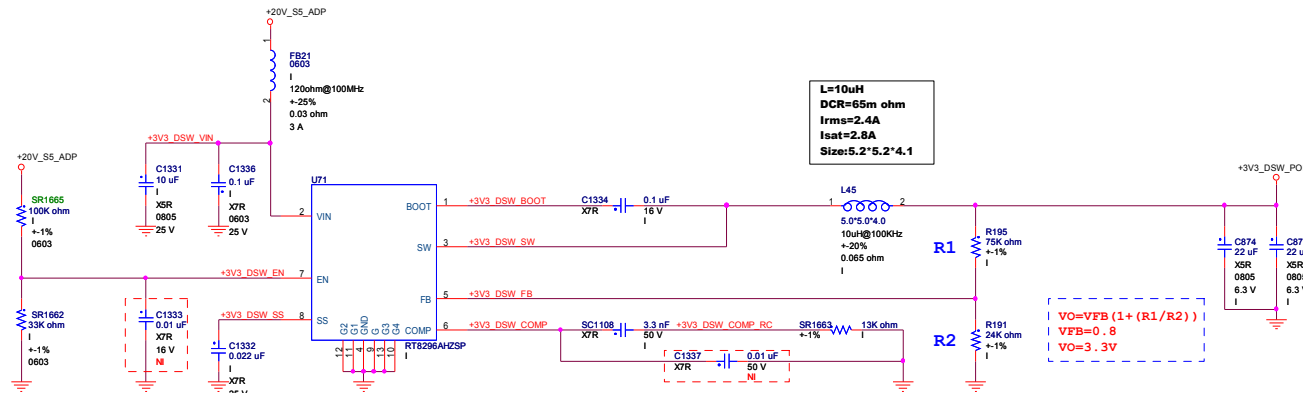




Power Header For 2L Box

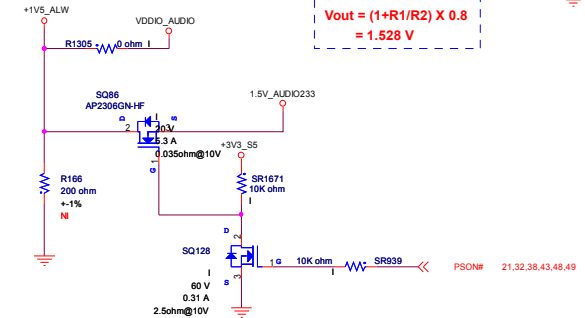






Please Check
 EN ON < 2.5 V
 EN OFF > 1 V

$$V_{out} = (1 + R1/R2) \times 0.8 = 1.528 V$$

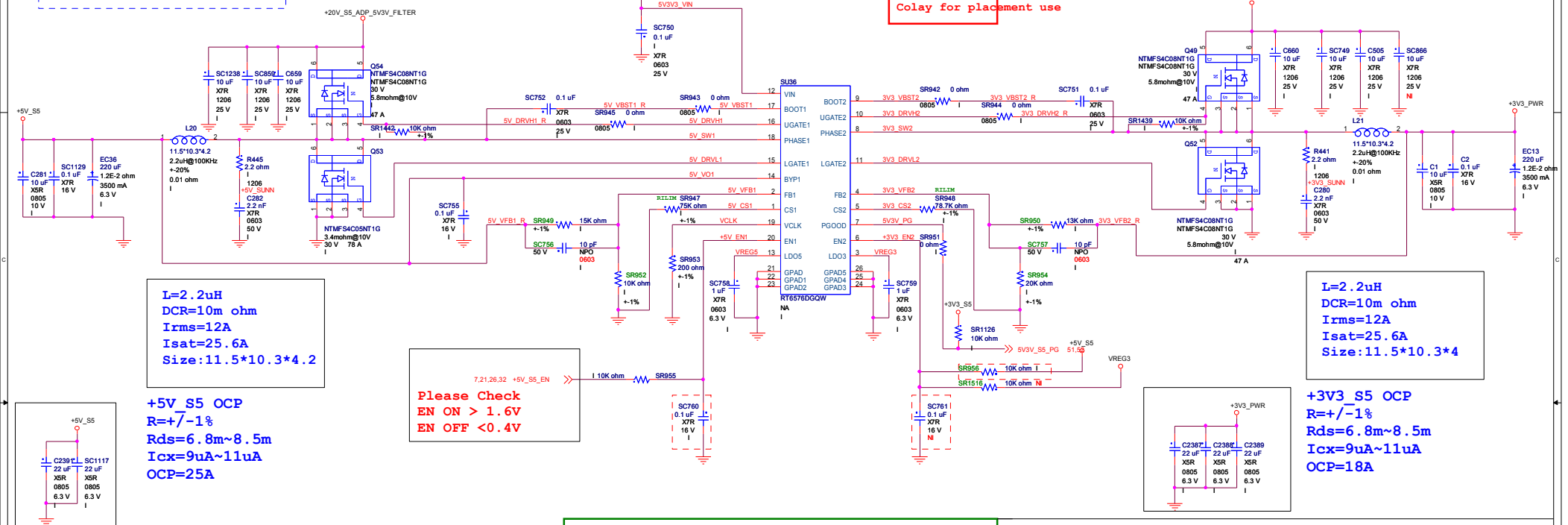


+5V_S5

Vin:+20V_S5_ADP_5V3V_FILTER
Vout:+5V
Imax: 13.77A
OCP: 25A
EN ON > 1.6V
EN OFF <0.4V
Fsw:300KHz (typ)

+3V3_PWR

Vin:+20V_S5_ADP_5V3V_FILTER
Vout:+3V3_S5
Imax:10A
OCP:18A
EN ON > 1.6V
EN OFF <0.4V
Fsw:355KHz (typ)



L=2.2uH
DCR=10m ohm
Irms=12A
Isat=25.6A
Size:11.5*10.3*4.2

+5V_S5 OCP
R=+/-1%
Rds=6.8m~8.5m
Icx=9uA~11uA
OCP=25A

L=2.2uH
DCR=10m ohm
Irms=12A
Isat=25.6A
Size:11.5*10.3*4

+3V3_S5 OCP
R=+/-1%
Rds=6.8m~8.5m
Icx=9uA~11uA
OCP=18A

Please Check
EN ON > 1.6V
EN OFF <0.4V

OCP
+3V3_S5
 $R_{limit} = (I_{limit} - \Delta I_L / 2) * R_{on} * 8 / 9uA = 137K$
+5V_S5
 $R_{limit} = (I_{limit} - \Delta I_L / 2) * R_{on} * 8 / 9uA = 147K$
 $R_{on} = 8.5m$ $I_{cx} = 9uA$ $R = -1\%$

+3V3_S5
 $\Delta I_L / 2 = 5.43 / 2 = 2.715$

+5V_S5
 $\Delta I_L / 2 = 5.82 / 2 = 2.91$

使用RT6576 (+3V3_DSW)

1. FB22-->NI
2. FB40-->NI
3. SR956-->NI
4. SR1516; SR1573, Q151; FB41-->Add

使用RT8296A (+3V3_DSW)

1. SR1516-->NI
2. FB41-->NI
3. SR1573-->NI
4. Q151-->NI
5. FB22; FB40; SR956 --> add

Cin=116uF
ripple current:11.8A
+5V_S5:
Cout=220uF
ripple current:3.5A
+3V3_S5:
Cout=220uF
ripple current:3.5A

+3V3_S5

Soft start:2.519ms
Inrush current:166.6mA

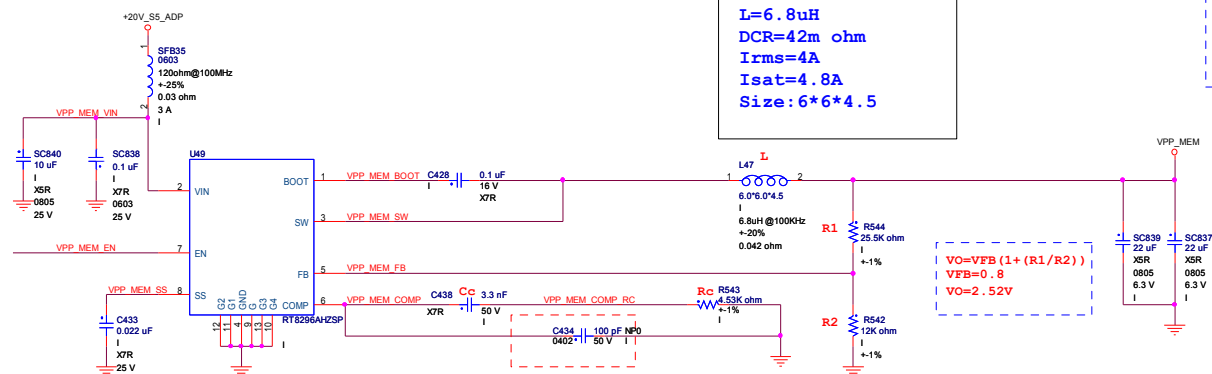
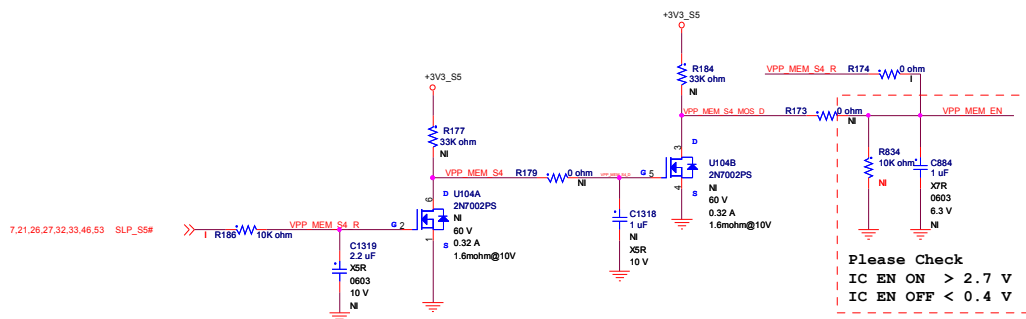
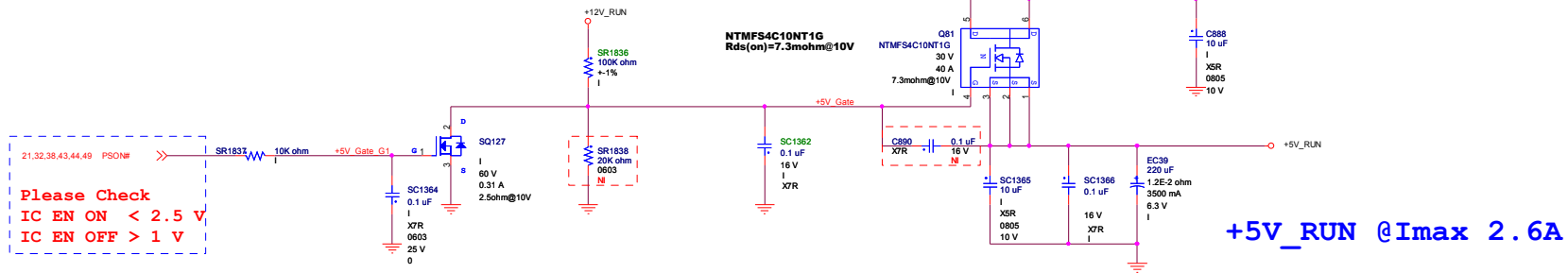


Table 1. Recommended Component Selection

VOUT (V)	R1 (kΩ)	R2 (kΩ)	RC (kΩ)	CC (nF)	L (μH)	COUT (μF)
8	27	3	33	3.3	22	22 x 2
5	62	11.8	20	3.3	15	22 x 2
3.3	75	24	13	3.3	10	22 x 2
2.5	25.5	12	9.1	3.3	6.8	22 x 2
1.5	10.5	12	5.6	3.3	3.6	22 x 2
1.2	12	24	4.3	3.3	3.6	22 x 2
1	3	12	3.6	3.3	2	22 x 2

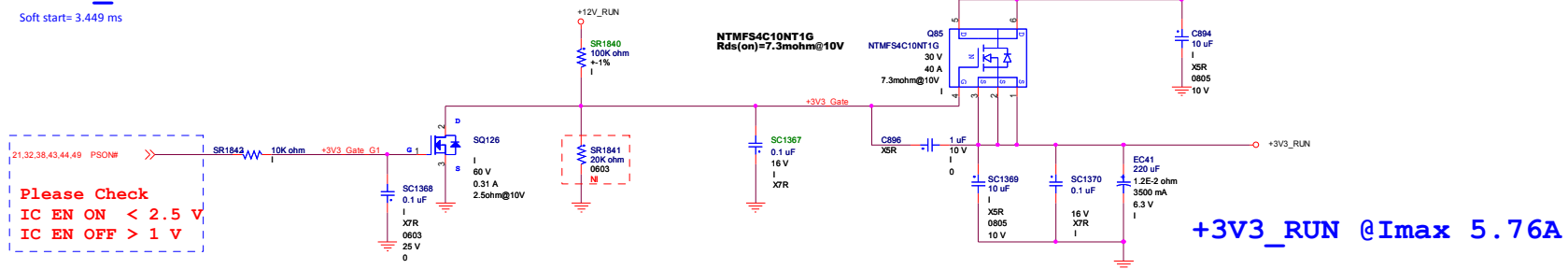
+5V_RUN

Soft start= 5.835 ms



+3V3_RUN

Soft start= 3.449 ms



APU_VDDP_RUN

Soft start= 3.449 ms

Please Check
IC EN ON < 2.5 V
IC EN OFF > 1 V

APU_VDDP_RUN @Imax 8.5A

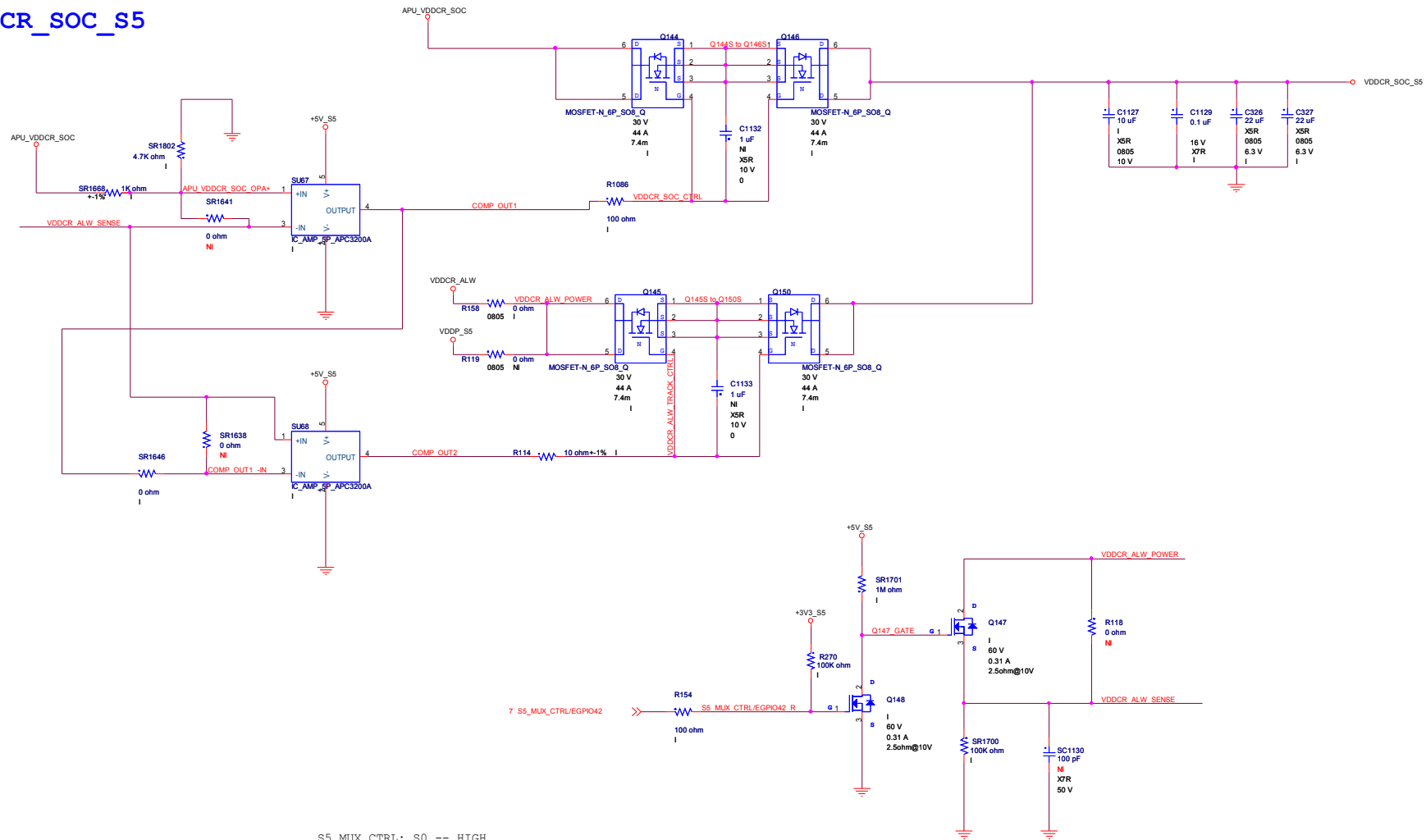
+1.8V_RUN

Soft start= 3.449 ms

Please Check
IC EN ON < 2.5 V
IC EN OFF > 1 V

+1.8V_RUN @Imax 2A

VDDCR_SOC_S5



```
S5_MUX_CTRL: S0 -- HIGH
               S3/S5 -- LOW
```

```
H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB
```


VDD_18_S5

VDD_18_S5

Temp. Max. DC: 2.75A

OCP: 5.1A

```
| IC EN ON > 2.7V
```

```
| IC EN OFF <0.4V
```

L=3.3uH
DCR=30m ohm
Irms=6A
Isat=10A
Size:7.6*6.8*3.2

+APU_VDDR_ENABLE

```
45,51 | 5V3V_S5_PG      >> R87U
|
| Please Check
| IC EN ON  > 2.5 V
| IC EN OFF < 1 V
|-----|
```

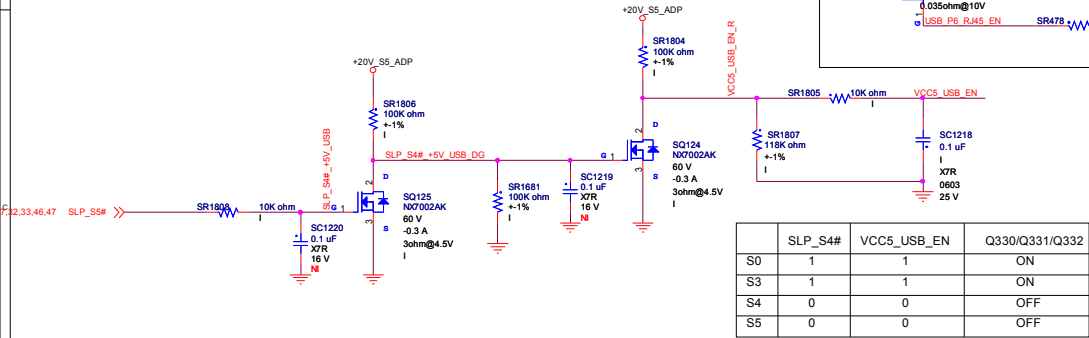
```
Please Check
IC EN ON  > 2.7 V
IC EN OFF < 0.4 V
```

```
| VO=VFB (1+ (R1/R2) )
| VFB=0.8
| VO=1.794V
|
```

SOFT-START
2.593mS

For Goolge SKU
Keep Q79 ,Q80 ,SQ85 then remove Others

+5V_USB



	SLP_S4#	VCC5_USB_EN	Q330/Q331/Q332
S0	1	1	ON
S3	1	1	ON
S4	0	0	OFF
S5	0	0	OFF

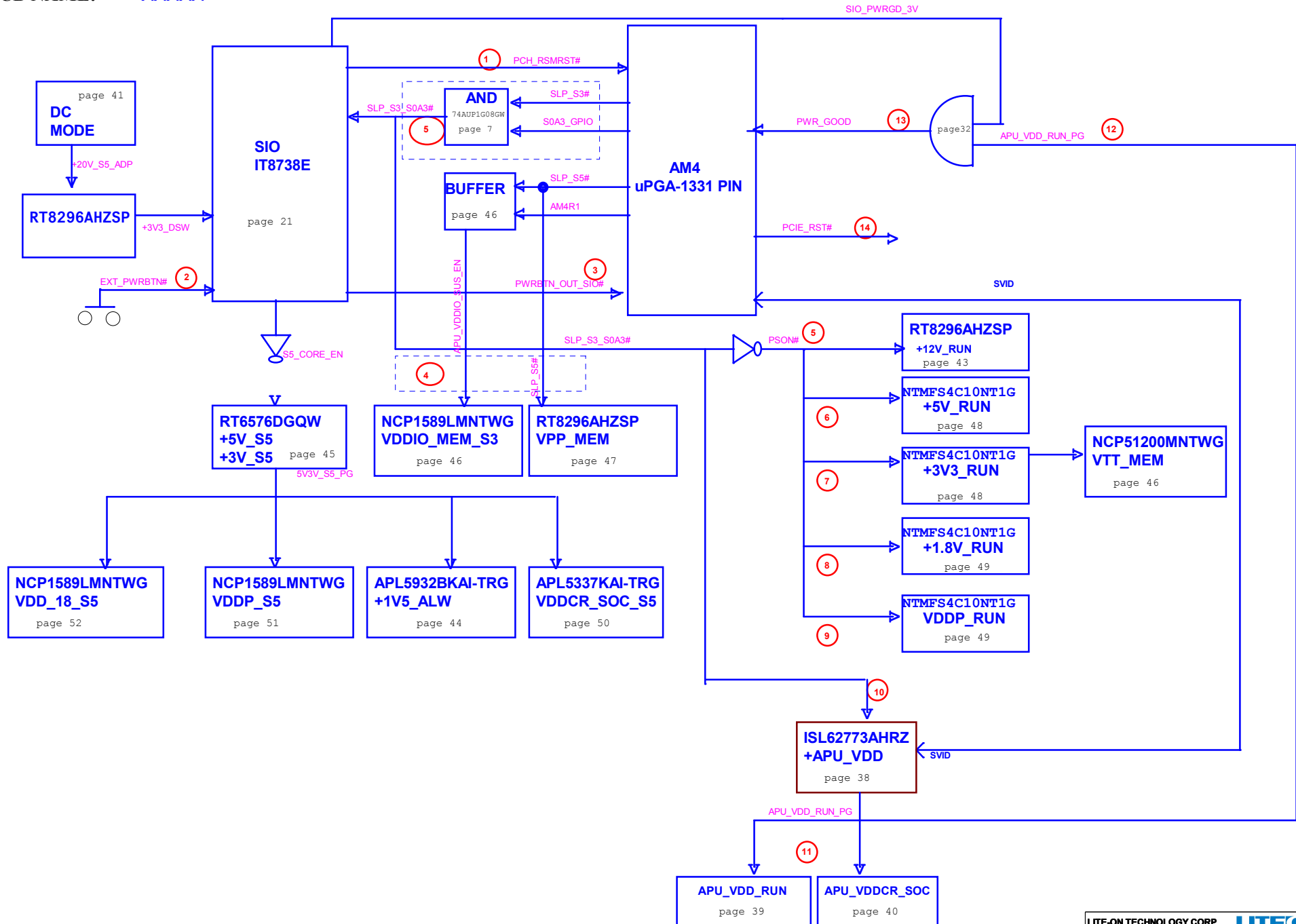
	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5\ resume) (DEFAULT)	SPI ROM (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLE (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic	LPC ROM	LPC ROM	short reset mode	Use 100Mhz PCIE clock as reference clock and generate internal clocks only
	CZ/ST DIE ONLY						ZP DIE ONLY

AM4 GPIO TABLE								
GPIO	Signal Name	Power Domain	Pin Type	Default State at Power-Up	ACTIVE/H/L	Integrated Resistor	Default Function at Power-Up	KC790
AGPIO8	PWR_BTN_L/AGPIO8	S5	IN/OUT	Input	---	INT / HIGH	PWR_BTN_L	PWR_BTN#
AGPIO1	SYS_RESET_L/AGPIO1	S5	IN/OUT	Input	---	INT / HIGH	SYS_RESET_L	SYS_RESET_L
AGPIO2	WAKE_L/AGPIO2	S5	IN/OUT	Input	---	INT / HIGH	WAKE_L	PCIE_WAKE#
AGPIO3	AGPIO3	S5	IN/OUT	Input	---	INT / HIGH	AGPIO3	APU_GPIO_UART
AGPIO6	AGPIO6	S5	IN/OUT	Input	---	INT / HIGH	AGPIO6	M2_VLAN_DISABLE#
AGPIO10	SOA3_GPIO/AGPIO10/ SGPIO0_CLK	S5	IN/OUT	Output	---	INT / HIGH	SOA3_GPIO	SOA3_GPIO
AGPIO11	BLINK/AGPIO11	S5	IN/OUT	Input	---	INT / HIGH	AGPIO11	PWR_LED#
AGPIO40	AGPIO40/ SGPIO0_DATAIN/ MDIO0_SDA	S5	IN/OUT	Input	---	INT / HIGH	AGPIO40	SW_CLR_CMOS#
AGPIO9	AGPIO9/ SGPIO0_DATAOUT	S5	IN/OUT	Input	---	INT / HIGH	AGPIO9	AGPIO9/SGPIO0
AGPIO4	AGPIO4	S5	IN/OUT	Input	---	INT / HIGH	AGPIO4	GPIO4
AGPIO16	USB_OC0_L/AGPIO16	S5	IN/OUT	Input	---	INT / HIGH	USB_OC0_L	USB_OC_REAR_J21#
AGPIO17	USB_OC1_L/UTDI/ AGPIO17	S5	IN/OUT	Input	---	INT / HIGH	USB_OC1_L	USB_OC_FRONT_12#
AGPIO18	USB_OC2_L/CLK/ AGPIO18	S5	IN/OUT	Input	---	INT / HIGH	USB_OC2_L	USB_OC_FRONT_J23#
AGPIO19	SCL1/SC2_SCL/ AGPIO19	S5	Open-Drain	Input	---	-	SCL1	SMB_CLK_SECOND
AGPIO21	LPC_PD_L/AGPIO21	S5	In/Out	Output	---	-	LPC_PD_L	TPM_LPC_PD#
AGPIO22	LPC_PME_L/AGPIO22	S5	In/Out	Input	---	INT / HIGH	LPC_PME	SIO_PME#
AGPIO23	AGPIO23/ SGPIO0_LOAD	S5	In/Out	Input	---	INT / HIGH	AGPIO23	DP_D_DET#_R
AGPIO24	USB_OC3_L/UTDO/ AGPIO24	S5	In/Out	Input	---	INT / HIGH	-	NA
AGPIO76	SPI_TPM_CS_L/ AGPIO76	S0	In/Out	Input	---	-	SPI_TPM_CS_L	SPI_TPM_CS_L
AGPIO84	FANIN0/AGPIO84	S0	In/Out	Input	---	INT / HIGH	FANIN0	HUB2_AMBER3_R
AGPIO85	FANOUT0/AGPIO85	S0	In/Out	Input	---	INT / HIGH	AGPIO85	HUB2_AMBER4_R
AGPIO86	AGPIO86	S0	In/Out	Input	---	INT / HIGH	AGPIO86	LPC_CABLE_DET2#
AGPIO87	SERIR0/AGPIO87	S0	In/Out	Input	---	INT / HIGH	SERIR0	LPC_SERIR0
AGPIO88	LPC_CLKRUN_L/ AGPIO88	S0	In/Out	Output	---	INT / HIGH	LPC_CLKRUN_L	LPC_CLKRUN#
AGPIO90	GENINT2_L/AGPIO90	S0	In/Out	Input	---	INT / HIGH	GENINT2_L	TPM_SPI_IRO#
AGPIO91	SPKR/AGPIO91	S0	In/Out	Input	---	INT / LOW	AGPIO91	APU_SPKR
AGPIO92	CLK_REQ0_L/ SATA_150_L/ SATA_ZP0_L/AGPIO92	S0	In/Out	Input	---	-	CLK_REQ0_L	CLK_REQ0_M2_VLAN#
AGPIO115	CLK_REQ1_L/ AGPIO115	S0	In/Out	Input	---	INT / HIGH	CLK_REQ1_L	CLK_REQ1_M2_SSD#
AGPIO116	CLK_REQ2_L/ AGPIO116	S0	In/Out	Input	---	INT / HIGH	CLK_REQ2_L	LOM_CLK_REQ#
AGPIO130	SATA_ACT_L/ AGPIO130	S0	Open-Drain	Input	---	-	SATA_ACT_L	APU_HD_LED_OUT#
EGPIO								
EGPIO26	PCIE_RST_L/EGPIO26	S5	In/Out	Output	---	-	PCIE_RST_L	PCIE_RST#_R
EGPIO42	S5_MUX_CTRL/ EGPIO42	S5	In/Out	Output	---	-	S5_MUX_CTRL	S5_MUX_CTRL/EGPIO42
AGPIO5	AGPIO5/DEVSLP0	S0	In/Out	Input	---	-	AGPIO5	AGPIO5/DEVSLP0
EGPIO74	LPCCLK0/EGPIO74	S0	In/Out	Output	---	-	LPCCLK0	CLK_SIO_33MHZ
EGPIO75	LPCCLK1/EGPIO75	S0	In/Out	Output	---	-	LPCCLK1	CLK_TPM_33MHZ
EGPIO70	EGPIO70	S0	In/Out	Input	---	INT / LOW	EGPIO70	EGPIO70
EGPIO95	EGPIO95	S0	In/Out	Input	---	INT / LOW	EGPIO95	EGPIO95
EGPIO96	EGPIO96	S0	In/Out	Input	---	INT / LOW	EGPIO96	NA
EGPIO97	EGPIO97	S0	In/Out	Input	---	INT / LOW	EGPIO97	DP1_DP_HDMI#
EGPIO98	EGPIO98	S0	In/Out	Input	---	INT / LOW	EGPIO98	DP2_DP_HDMI#
EGPIO99	EGPIO99	S0	In/Out	Input	---	INT / LOW	EGPIO99	DPD_DP_HDMI#
EGPIO100	EGPIO100	S0	In/Out	Input	---	INT / LOW	EGPIO100	COM_AB_DET#
AGPIO8	AGPIO8	S0	In/Out	Input	---	INT / LOW	AGPIO8	LPC_CABLE_DET2#
EGPIO113	SCL0/SC2_SCL/ EGPIO113	S0	Open-Drain	Input	---	INT / HIGH	SCL0	SMB_CLK_MAIN
EGPIO114	SDA0/SC2_SDA/ EGPIO114	S0	Open-Drain	Input	---	INT / HIGH	SDA0	SMB_DATA_MAIN
EGPIO117	SPI_CLK/ESPI_CLK/ EGPIO117	S0	In/Out	Input	---	INT / LOW	ESPI_CLK	SPI_CLK_APU
EGPIO118	SPI_CS1_L/EGPIO118	S0	In/Out	Input	---	-	SPI_CS1_L	SPI_CS0_OUT#_APU
EGPIO119	SPI_CS2_L/ESPI_CS_L/ EGPIO119	S0	In/Out	Input	---	-	SPI_CS2_L	SPI_CS2_OUT#
EGPIO120	SPI_DIVESPI_DAT1/ EGPIO120	S0	In/Out	Input	---	INT / LOW	SPI_DI	SPI_MISO_APU
EGPIO121	SPI_DOESPI_DAT0/ EGPIO121	S0	In/Out	Input	---	INT / LOW	SPI_DO	SPI_MOSI_APU
EGPIO122	SPI_WP_L/ESPI_DAT2/ EGPIO122	S0	In/Out	Input	---	INT / HIGH	EGPIO122	SPI_WP#_APU
EGPIO131	CLK_REQ3_L/ SATA_151_L/ SATA_ZP1_L/EGPIO131	S0	In/Out	Input	---	-	CLK_REQ3_L	LPC_CABLE_DET1#
EGPIO132	CLK_REQ5_L/OSCIN/ EGPIO132	S0	Input	Input	---	-	CLK_REQ5_L	NA
EGPIO133	SPI_HOLD_L/ ESPI_DAT3/EGPIO133	S0	In/Out	Input	---	INT / HIGH	EGPIO133	SPI_HOLD#_APU
EGPIO104	LAD0/EGPIO104	S0	In/Out	Input	---	INT / LOW	LAD0	LPC_AD0
EGPIO105	LAD1/EGPIO105	S0	In/Out	Input	---	INT / LOW	LAD1	LPC_AD1
EGPIO106	LAD2/EGPIO106	S0	In/Out	Input	---	INT / LOW	LAD2	LPC_AD2
EGPIO107	LAD3/EGPIO107	S0	In/Out	Input	---	INT / LOW	LAD3	LPC_AD3
ESPIO108	ESPI_ALERT_L/ LDREQ0_L/EGPIO108	S0	Input	Input	---	INT / LOW	LDREQ0_L	LPC_DRQ0#
EGPIO109	LFRAME_L/EGPIO109	S0	In/Out	Output	---	-	LFRAME_L	LPC_FRAME#

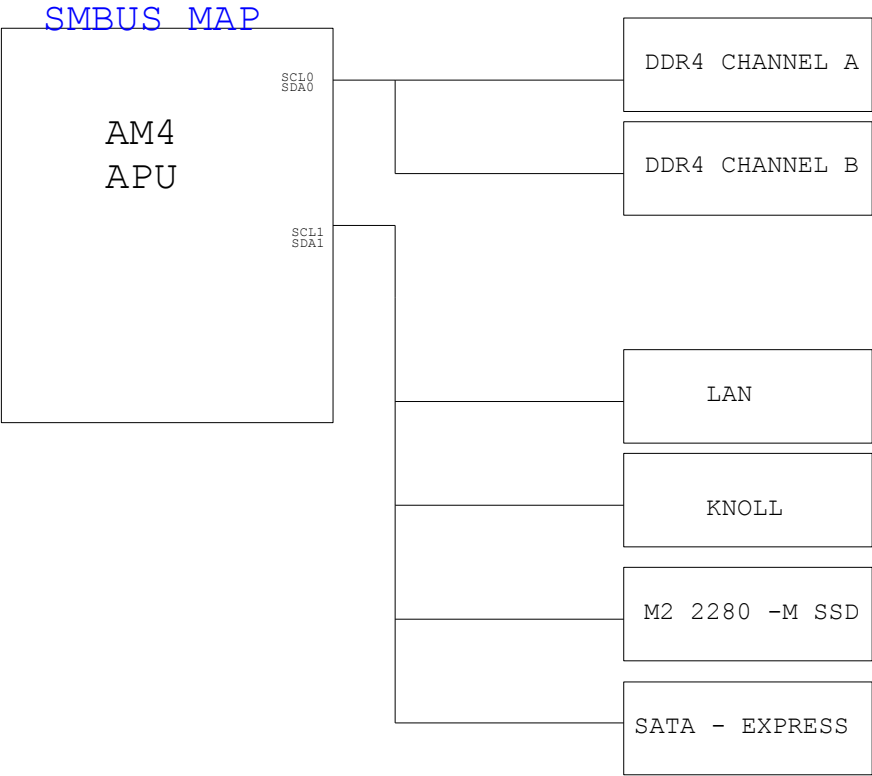
ITS738E/DX								
GRD(Pin Num)	Signal Name	KC790	Function_1	Function_2	Function_3	Function_4	Function_5	
GRD0(1078)	PCIRST3M/GP10	PCIRST3	PCIRST3M(D08/VCC3)	GP10(D008/V5B)				
GRD1(132)	PCIRST2M/GP11	+10V_VIN_CTL_SIO	PCIRST2M(D08/VCC3)	GP11(D008/V5B)				
GRD12(31)	PCIRST1M/PC_H_D1/GP12	NA	PCIRST1M(D08/VCC3)	PC_H_D1(D008/VCC3)	GP12(D008/V5B)			
GRD13(30)	PWR0K1/GP13	SIO_PWRGD_3V	PWR0K1(D008/VCC3)	GP13(D008/V5B)				
GRD14(29)	VCORE_EN/PC_H_C1/GP14	NA	VCORE_EN(D008/VCC3)	PC_H_C1(D008/VCC3)	GP14(D008/V5B)			
GRD15(3)	PCIRSTM/CRT2/GP15/CPU_PG	PCIRSTM	PCIRSTM(DI)	CRT2(D008)	GP15(D008)	CPU_PG(D008)		
GRD16(2)	SV5B_CTLR#/CRR2/GP16	SV5B_CTLR	SV5B_CTLR#/D008/V5B)	OTR8M(DIVCC3)	GP16(D008/V5B)			
GRD17(26)	R2W/GP17	R2W/GP17	R2W(DIV3)	GP17(D008/V5B)				
GRD20(25)	CTS2M/GP20	NA	GP20(D008/V5B)	CTS2M(DIVCC3)				
GRD21(24)	OVERLOAD_N_R	OVERLOAD_N_R	GP21(D008/V5B)	DCD2M(DIVCC3)				
GRD22(23)	SOCK/GP22	SIO_SCK_R	SOCK(D08/V5B)	GP22(D008/V5B)				
GRD23(22)	SI/GP23	SIO_SI	SI(D08/V5B)	GP23(D008/V5B)				
GRD24(21)	RTS2M/GP24	NA	GP24(D008/V5B)	RTS2M(D08/VCC3)				
GRD25(20)	DSR2M/GP25	NA	GP25(D008/V5B)	DSR2M(DIVCC3)				
GRD26(19)	SOUT2/GP26	SOUTA	GP26(D008/V5B)	SOUT2M(D08/VCC3)				
GRD27(18)	SR2/GP24	SRA	GP27(D008/V5B)	SR2(DIVCC3)				
GRD30(17)	ATXPG/GP30	PWRGD_P5	ATXPG(DIVCC3)	GP30(D008/V5B)				
GRD31(16)	PWMOUT/GP31/USBPWRREN#	SIO_CHR_USBPWRREN	PWM_OUT(D08/V5B)	GP31(D008/V5)				
GRD32(15)	DRV0R0/GP32	SIO_GP32	DRV0R0(D008/V5B)	GP32(D008/V5B)				
GRD35(14)	FAH_TAC4/GP35	INT1_O_SIO	FAH_TAC4(DIV5B)	GP35(D008/V5B)				
GRD36(13)	FAH_CTL3/GP36	NA	FAH_CTL3(D008/V5B)	GP36(D008/V5B)				
GRD37(12)	FAH_TAC3/GP37	INT2_O_SIO	FAH_TAC3(DIV5B)	GP37(D008/V5B)				
GRD40(73)	3VSSB#/GP40/SCL	NA	3VSSB#/D08/V5B)	GP40(D008/V5B)	SCL(D008/VCC3)			
GRD41(72)	PWR0K2/GP41/SDA	NA	PWR0K2(D008/VCC3)	GP41(D008/V5B)	SDA(D008/VCC3)			
GRD42(70)	P50M/GP42	SIO_P50M#	P50M#/D008/V5B)	GP42(D008/V5B)				
GRD43(69)	PANSW/M/GP43	SIO_PB_IN	PANSW/M(DIV5B)	GP43(D008/V5B)				
GRD44(66)	PWR0M/GP44	SIO_PWRBTH_OUT#	PWR0M(D008/V5B)	GP44(D008/V5B)				
GRD45(65)	SUSB#/GP45	SIO_SLP_S#	SUSB#/DIV5B)	GP45(D008/V5B)				
GRD50(46)	SO/GP50	SIO_SO_8738	SO(DIV5B)	GP50(D008/V5B)				
GRD51(11)	FAH_CTL2/GP51	SIO_FH12	FAH_CTL2(D008/V5B)	GP51(D008/V5B)				
GRD52(10)	FAH_TAC2/GP52	SR_SEL	FAH_TAC2(DIV5B)	GP52(D008/V5B)				
GRD53(71)	SUSC#/GP53	SIO_SLP_S4#	SUSC#/DIV5B)	GP53(D008/V5B)				
GRD54(87)	PME#GP54/USBPWRREN#	SIO_FH67	PME#/D008/V5B)	GP54(D008/V5B)	USBPWRREN#(D008/V5B)			
GRD55(79)	RSMRST#/CRR1/GP55	RSMRST_SQ#	RSMRST#/D008/V5B)	CRR1(DIV5B)	GP55(D008/V5B)			
GRD56(77)	MCLK/GP56	MCLK/GP56	MCLK(DI024/V5B)	GP56(DI024/V5B)				
GRD57(76)	MDAT/GP57	MDAT/GP57	MDAT(DI024/V5B)	GP57(DI024/V5B)				
GRD60(75)	KCLK/GP60	KCLK/GP60	KCLK(DI024/V5B)	GP60(DI024/V5B)				
GRD61(74)	KDAT/GP61	KDAT/GP61	KDAT(DI024/V5B)	GP61(DI024/V5B)				
GRD62(43)	KRSTW/GP62	KBRST#	KRSTW(D08/VCC3)	GP62(D008/V5B)				
GRD63(8)	VLDT_EN/GP63	NA	VLDT_EN(D008/V5B)	GP63(D008/V5B)				
GRD65(119)	SMBCLK4/GP66	NA	SMBCLK4(DI024/V5B)	GP65(DI024/V5B)				
GRD66(120)	SMBDAT4/GP66	NA	SMBDAT4(DI024/V5B)	GP66(DI024/V5B)				
GRD67(121)	FAH_CTL4/GP67	SIO_FH121	FAH_CTL4(D008/V5B)	GP67(D008/V5B)				
GRD70(102)	KS0P05/GP70	2543_P2_EN	GP70(DI024/V5B)	KS0(DIV5B)				
GRD71(103)	KS1P01/GP71	2543_CLT3_R	GP71(DI024/V5B)	KS0(DIV5B)				
GRD72(104)	KS0P02/GP72	2543_EN_R	GP72(DI024/V5B)	KS0(DI024/V5B)				
GRD73(105)	KS01P03/GP73	2543_CLT1_R	GP73(DI024/V5B)	KS01(DI024/V5B)				
GRD74(106)	KS02P04/GP74	NA	GP74(DI024/V5B)	KS02(DI024/V5B)				
GRD75(107)	KS03P05/GP75	NA	GP75(DI024/V5B)	KS03(DI024/V5B)				
GRD76(108)	KS04P06/GP76	NA	GP76(DI024/V5B)	KS04(DI024/V5B)				
GRD77(109)	KS05P07/GP77	NA	GP77(DI024/V5B)	KS05(DI024/V5B)				
GRD80(94)	PE/GP80	NA	PE(DIVCC3)	GP80(DI024/V5B)				
GRD81(95)	BUSY/GP81	NA	BUSY(DIVCC3)	GP81(DI024/V5B)				
GRD82(96)	ACK#/GP82	NA	ACK#/DIVCC3)	GP82(DI024/V5B)				
GRD83(97)	SLN#/GP83	ADP_E1	SLN#/DI024/VCC3)	GP83(DI024/V5B)				
GRD84(98)	INT#/GP84	ADP_E0	INT#/DI024/VCC3)	GP84(DI024/V5B)				
GRD85(56)	ID_SC#/GP85/SMBDAT0	APS_DC_DATA	ID_SC#/DI024/V5B)	GP85(DI024/V5B)	SMBDAT(DI024/V5B)			
GRD86(57)	GP86/SMBCLK0	APS_DC_CLK	GP86(DI024/V5B)	SMBCLK0(DI024/V5B)				
GRD87(99)	ERR#/GP87	ADP_OCP_EN	ERR#/DIVCC3)	GP87(DI024/V5B)				
GRD87(93)	SLCT/GP87	NA	SLCT(DIVCC3)	GP87(DI024/V5B)				
GRD88(122)	RTS1#/GP88	RTS1-	RTS1#/D08/VCC3)	GP88(DI008/V5B)				
GRD89(123)	DSR1#/GP81	DSR1-	DSR1#/D08/VCC3)	GP81(DI008/V5B)				
GRD92(124)	SOUT1#/TX1/GP82	SOUT1-	SOUT1#/D08/VCC3)	D_TX1(DI08/V5B)	GP82(DI008/V5B)			
GRD93(125)	SND_RX1/GP83	SN1-	SN1#/DIVCC3)	D_RX1(DIV5B)	GP83(DI008/V5B)			
GRD94(126)	DTR1#/GP84	DTR1-	DTR1#/D08/VCC3)	GP84(DI008/V5B)				
GRD95(127)	DCD1#/GP85	DCD1-	DCD1#/D08/VCC3)	GP85(DI008/V5B)				
GRD96(128)	RI1#/GP86	RI1-	RI1#/DIV5B)	GP86(DI008/V5B)				
GRD97(1)	CTS1#/GP87	CTS1-	CTS1#/DIVCC3)	GP87(DI008/V5B)				

MODEL NAME: *Power Sequence Block Diagram*

PCB NAME: *XXXXXX*



SMBUS Block Diagram



P04
1. del SC1175, SC1151.
2. SC1060, SC1180 change to 22uF

P38
1. R905 change to I
2. +1.5V_ALW change to +1.8V_RUN

P39
1. L27, L29 重抓

P40
1. L26, L25 重抓

P42
1. VDDIO MEM S3 change to +5V_S5
2. del U59 circuit

P51
1. add EC24
2. EC52 change to 560uF

P52
1. add EC53

For SDV

P38
1. R921 change to 53.6K
2. R935 change to 53.6K
3. C953 change to 2.2nF
4. C963 change to 2.2nF
5. R909 change to I
6. R937 change to 2.87K

For SIT

P45
1. SC760 change to I

P46
1. R992 change to I, SR1666 change to NI
2. SC1090 change to 1nF

P47
1. C884 change to I

P52
1. R1200 change to 11K
2. R1201 change to 8.45K

P44
1. C1332 change to 0.022uF
2. SR1832 change to I

P40
1. add SR999 = 0R & connect to P38 R909

P51
1. C906 change to 1nF

P38
1. del SR1861, del SR1868
2. R909 change to 16.9K

For SIT (0421)

P39
1. add R907, R905 change to NI

For SIT (0427)

P45
1. R947 change to 75K

P44
1. U48 change to APL5933C

P42
1. add P5

For SIT (0429)

P39
1. TC2 => STC1
2. add EC46

P46
1. SU77 => GS7901TD
2. Q121 => NTTFS4C25NTAG
3. Q120 => NTTFS4C10NTAG