

Project: KC790

PCB Size : 174*175 mm



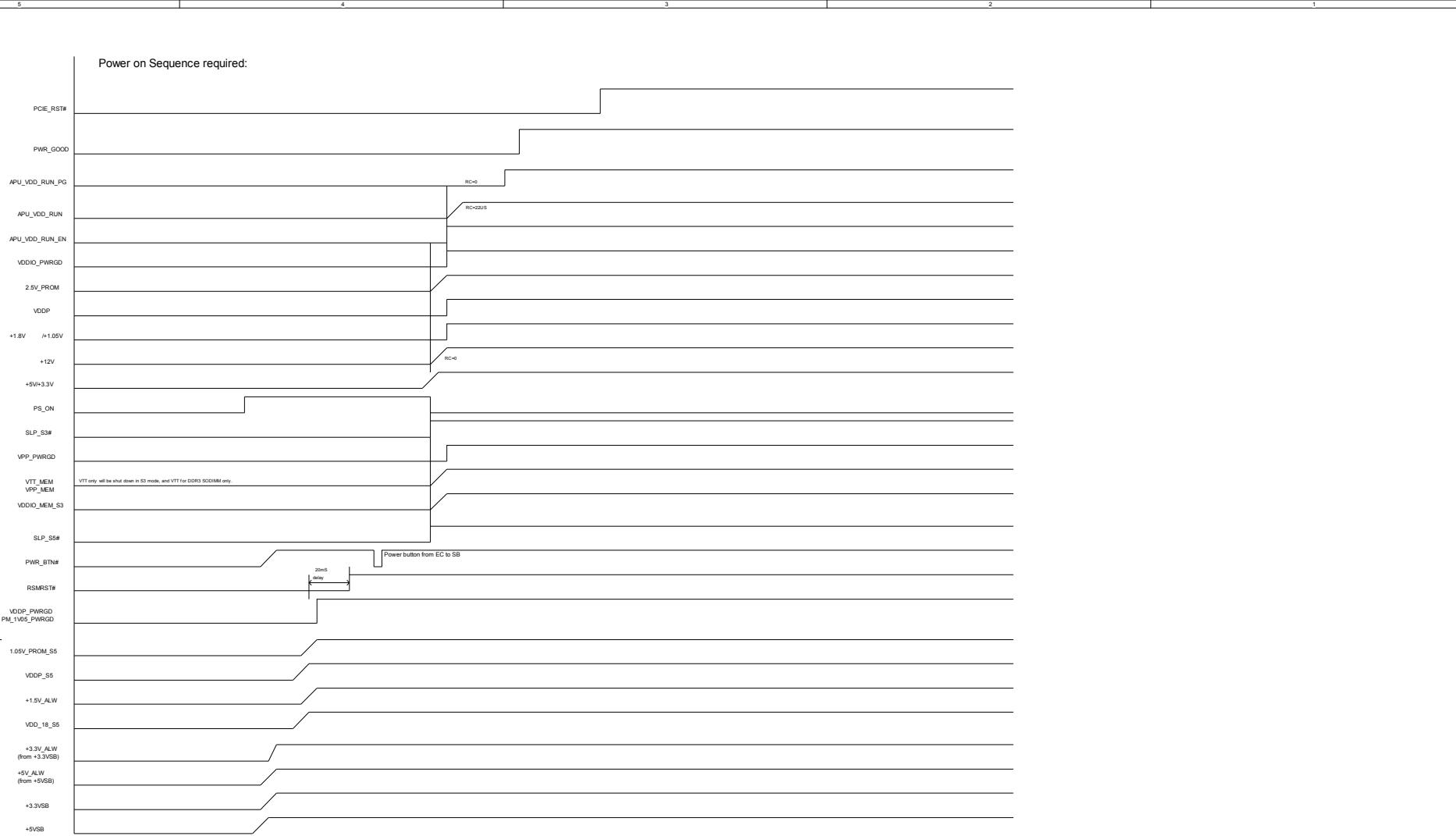
Project

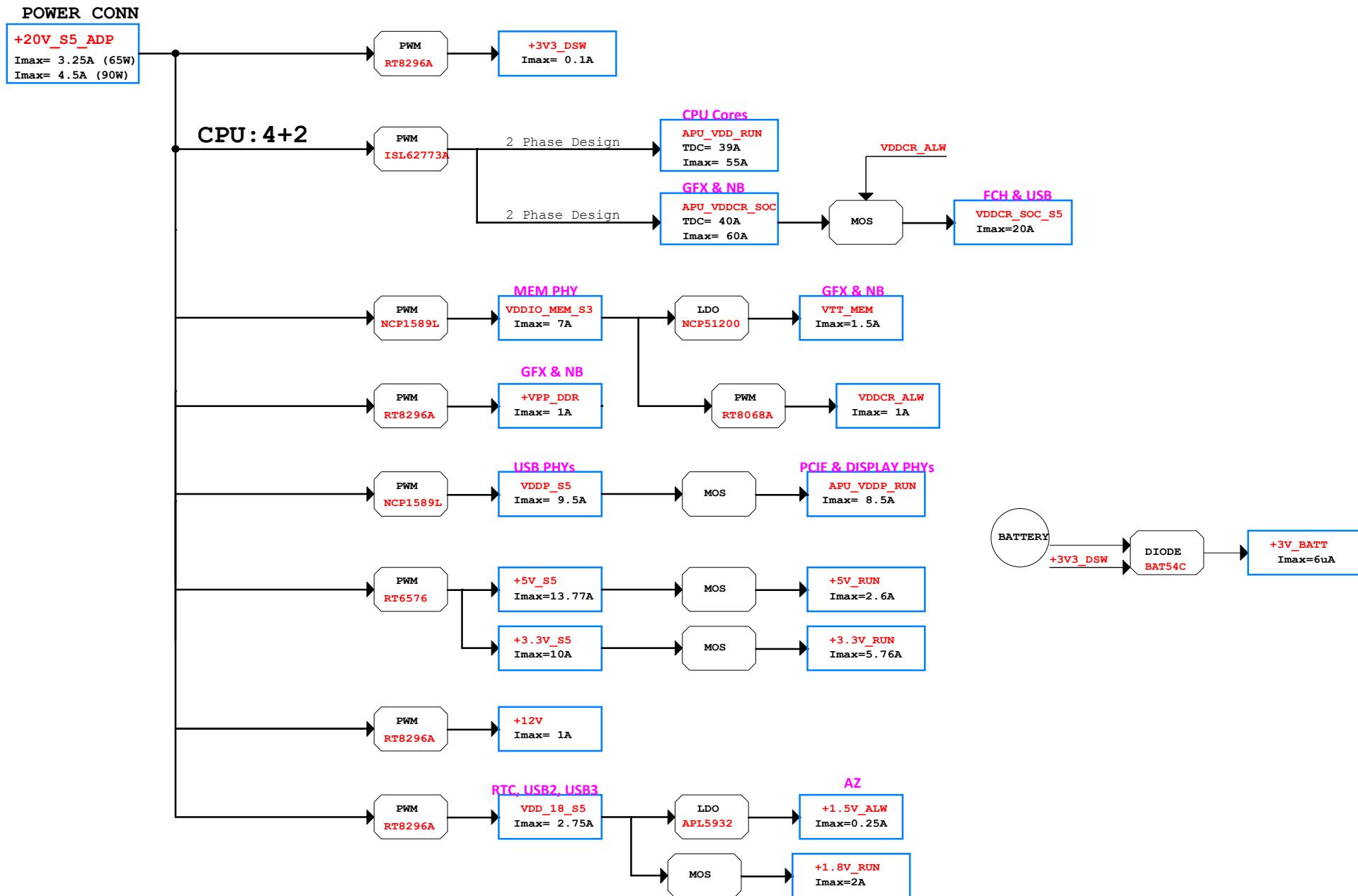
Document No :
X03 : 04/29/2016Y

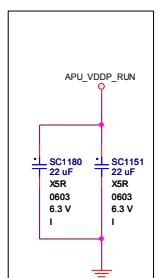
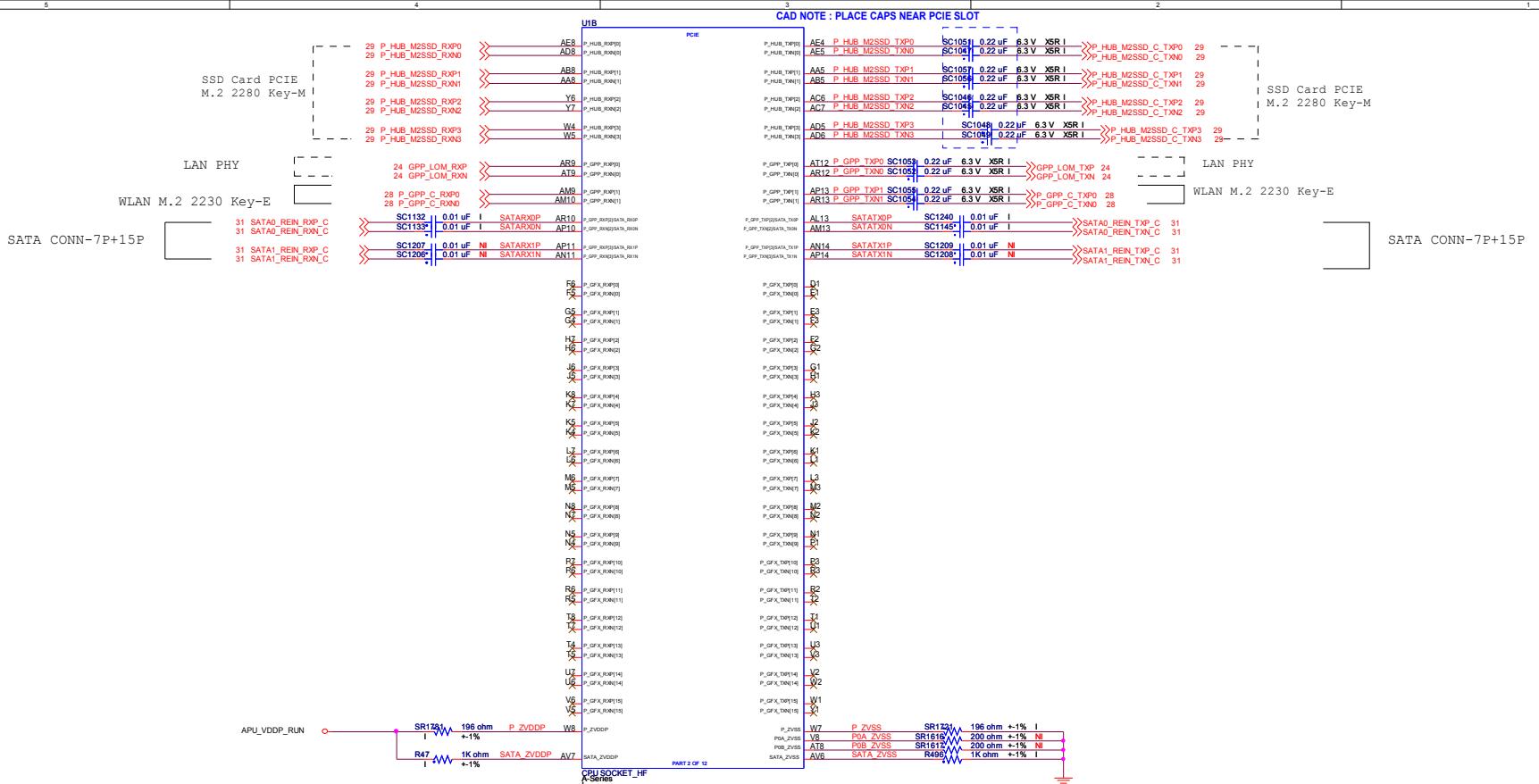
PAGE	TITLE
01	Block Diagram
02	Power Sequence
03	Power Delivery Map
04	AM4 PCIE I/F
05	AM4 MEM
06	AM4 DISPLAY/MISC
07	AM4 ACPI/AZ/SD/I2C/GPIO/FCH
08	AM4 CLK/LPC/SPI/USB
09	AM4 POWER AND DECOUPLING
10	AM4 GND
11	DDR4 CHA SO-DIMM1 -8H
12	DDR4 CHB SO-DIMM3 -4H
13	Knoll &Asset ID&SPI ROM
14	CMOS Clear / Battery/ HDR
15	USB Hub2.0 GL852G
16	Display Port 1
17	Display Port 2
18	Display Port HDR
19	Audio Codec - ALC233-CG
20	Audio Jack Line I-O/ Mic in
21	SuperI/O IT8738E
22	COM Port/ PS/2/ FAN CRTL
23	TPM - TCG 2.0
24	LAN RTL8111EPV
25	RJ45 + USB3 Stack
26	Rear USB2 x 3
27	Front USB3 Charger x2
28	M.2 2230-E WIFI/ BT
29	M.2 2280-M SSD
30	Buzzer &debug card
31	SATA-Express DOM
32	PWRGD & Bleed Off
33	Button/ LED
34	SM BUS/Thermal Sensing/APS
35	Debug Port
36	Mounting Hole/ PCB/ Metal
37	Blank
38	APU VDD RUN/APU_VDDCR SOC
39	APU VDD RUN OUTPUT
40	APU_VDDCR SOC OUTPUT
41	+20V S5 ADP
42	VDDCR ALW
43	+12V
44	+3V3 DSW / +1.5V ALW
45	+5V S5/+3V3 S5
46	VDDIO MEM S3/VTT MEM
47	VPP MEN
48	+5V_RUN/+3V3_RUN
49	APP_VDDP RUN/+1.8V RUN
50	VDDCR_SOC_S5
51	VDD_S5
52	VDD_18_S5
53	+5V USB
54	STRAPPING PIN
55	AM4 GPIO TABLE
56	SIO GPIO TABLE
57	RESET MAP-CLOCK DIAGRAM
58	SMBUS Block Diagram
59	INA300
60	Change List2

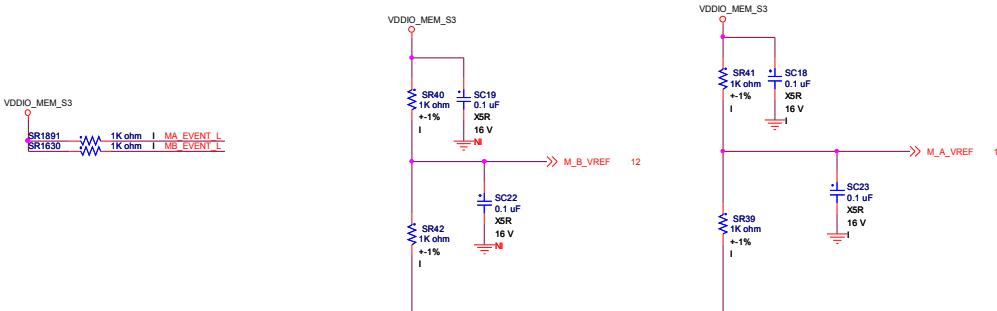
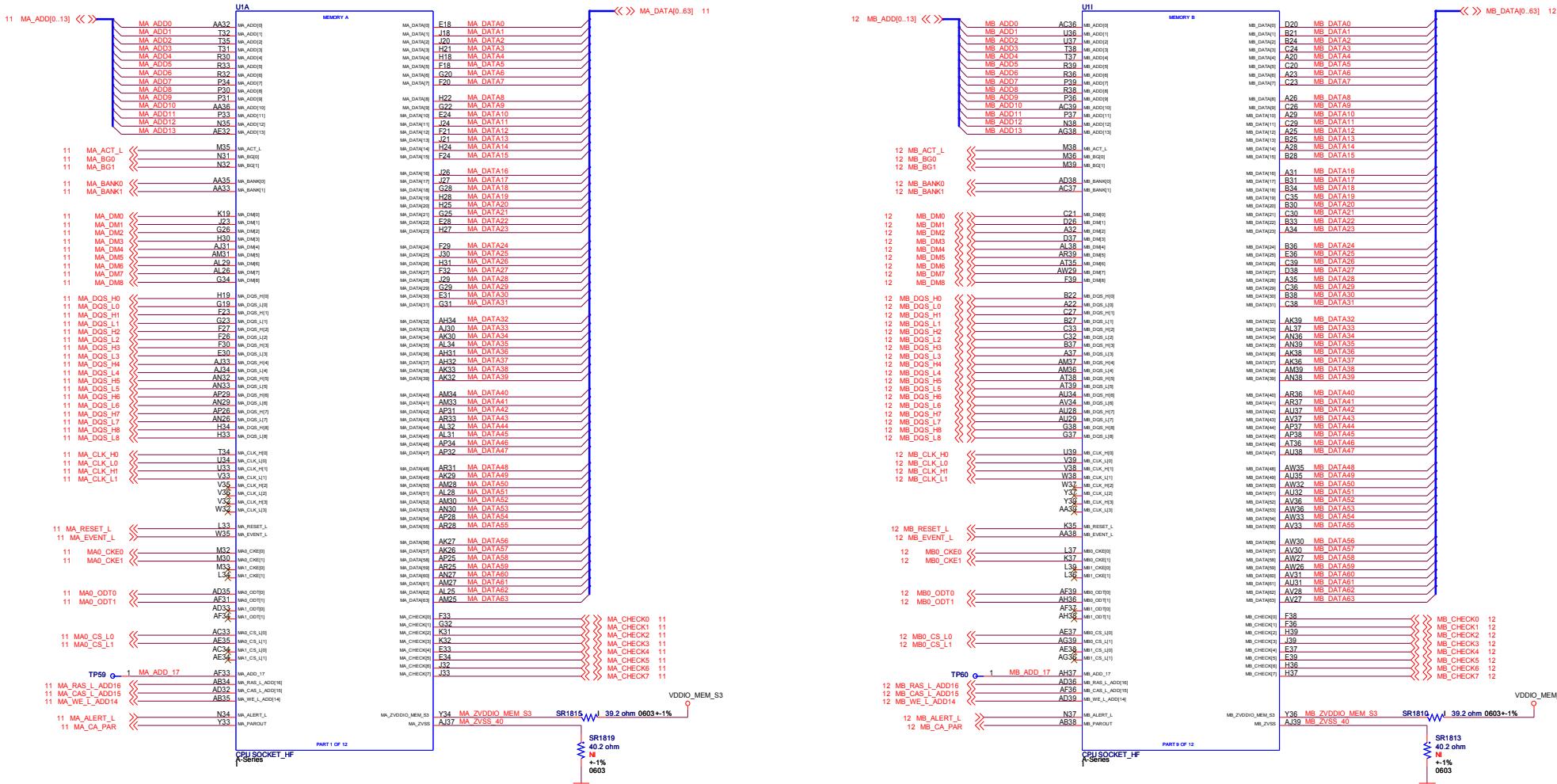
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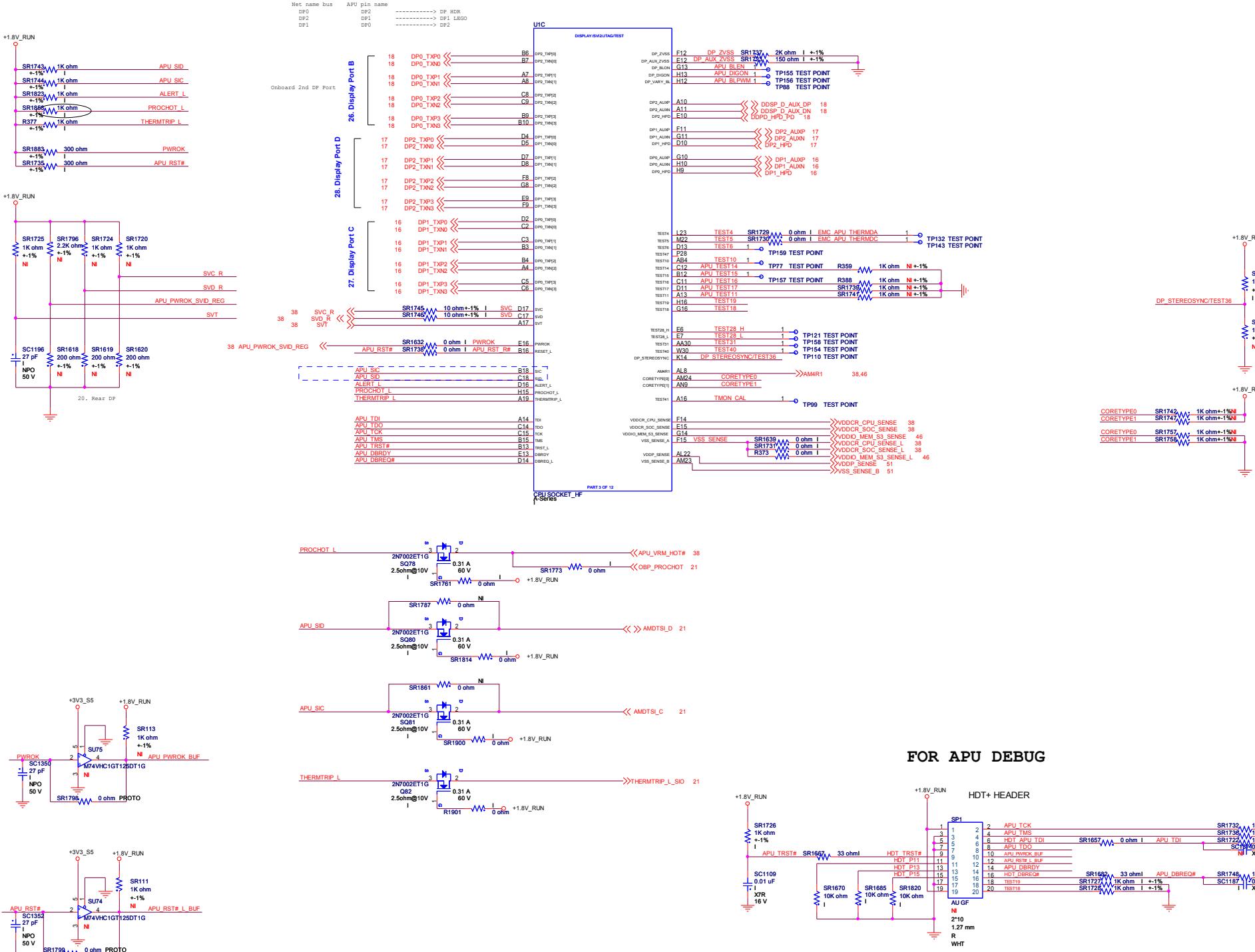
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01. Block Diagram	
Size	Document Number
C	KC790
Date:	Saturday, April 30, 2016
Rev	X03
Sheet	1 of 60

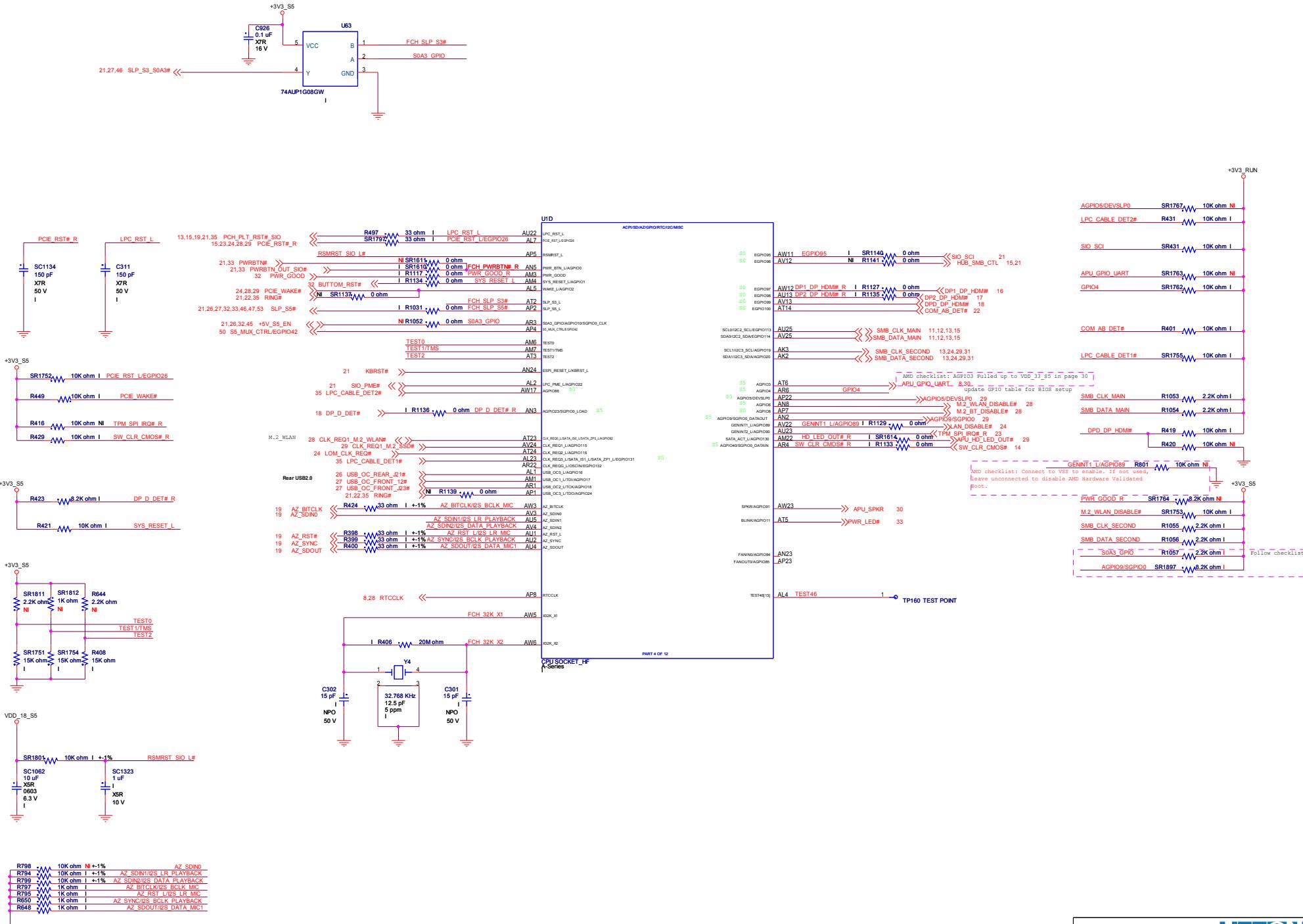


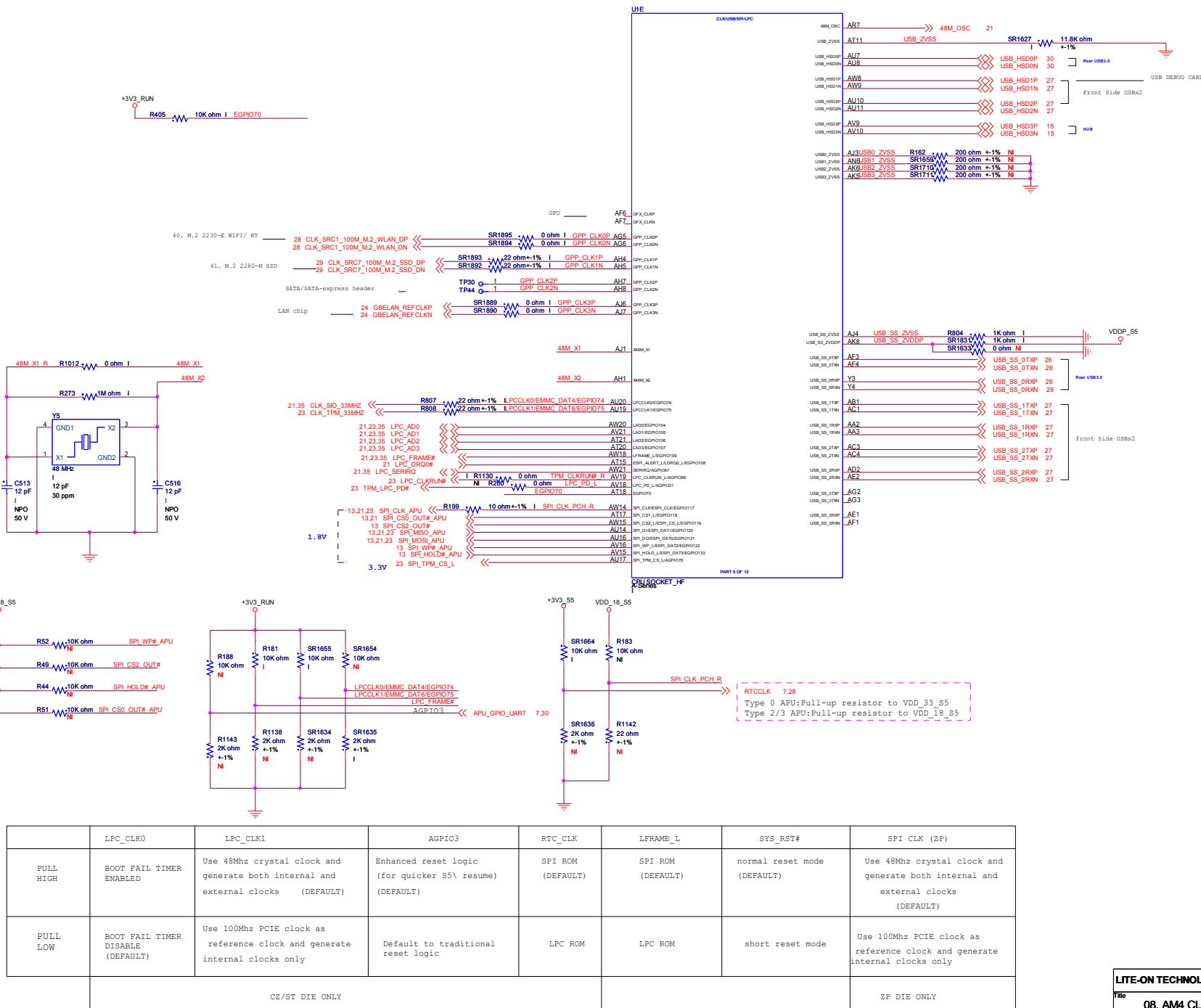


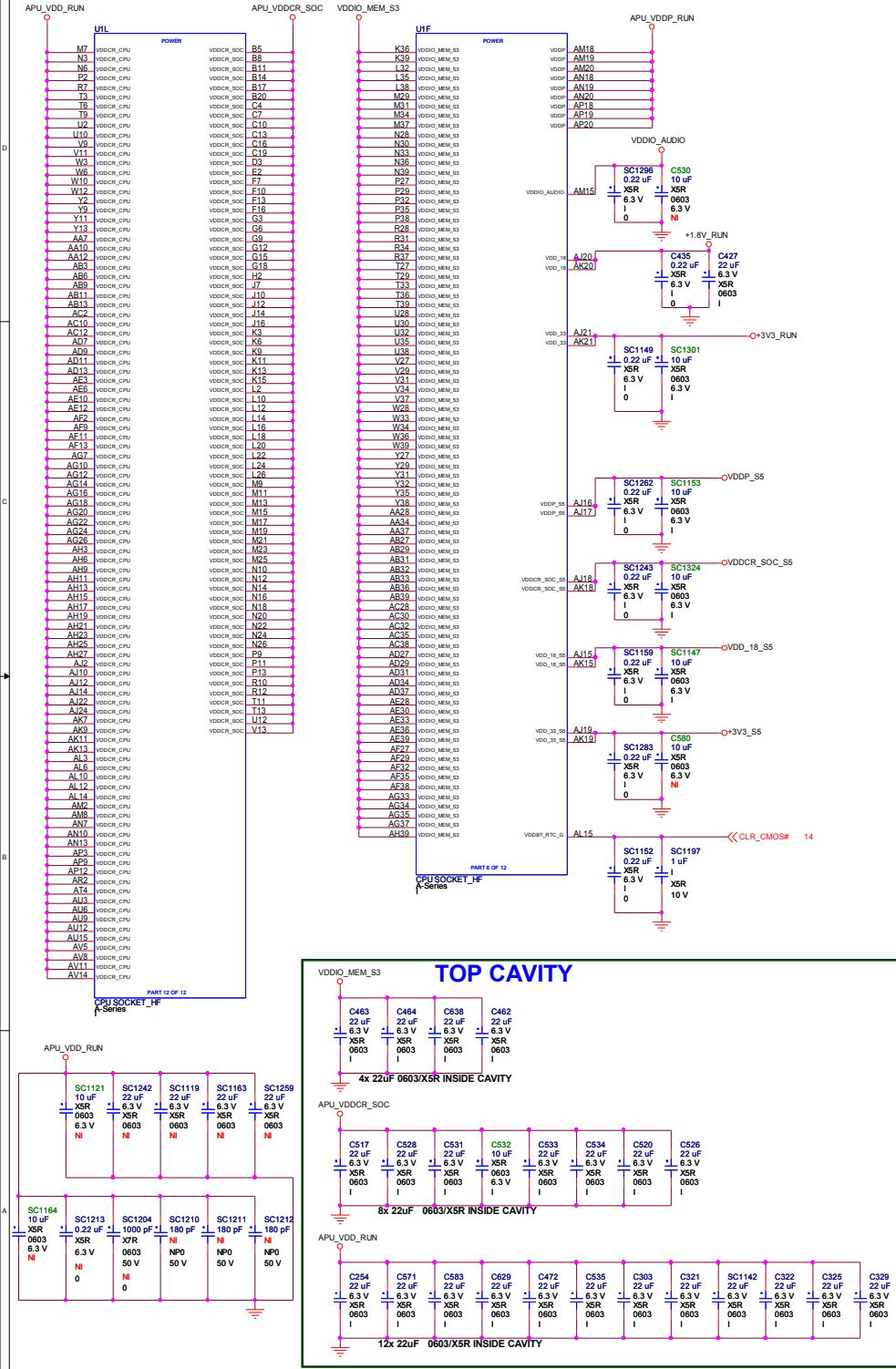






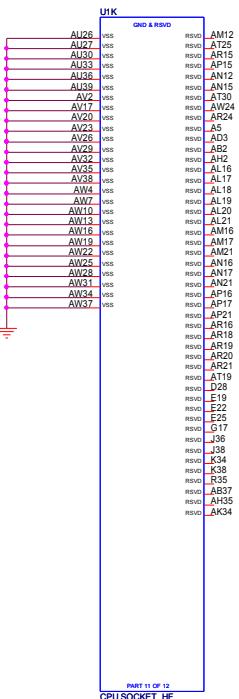
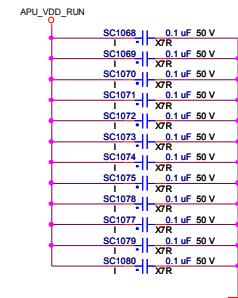
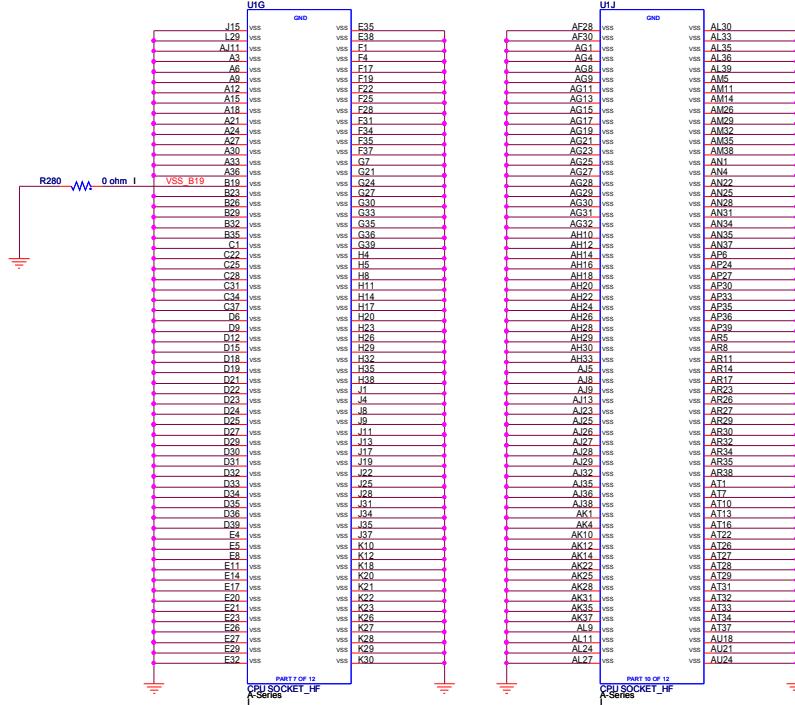


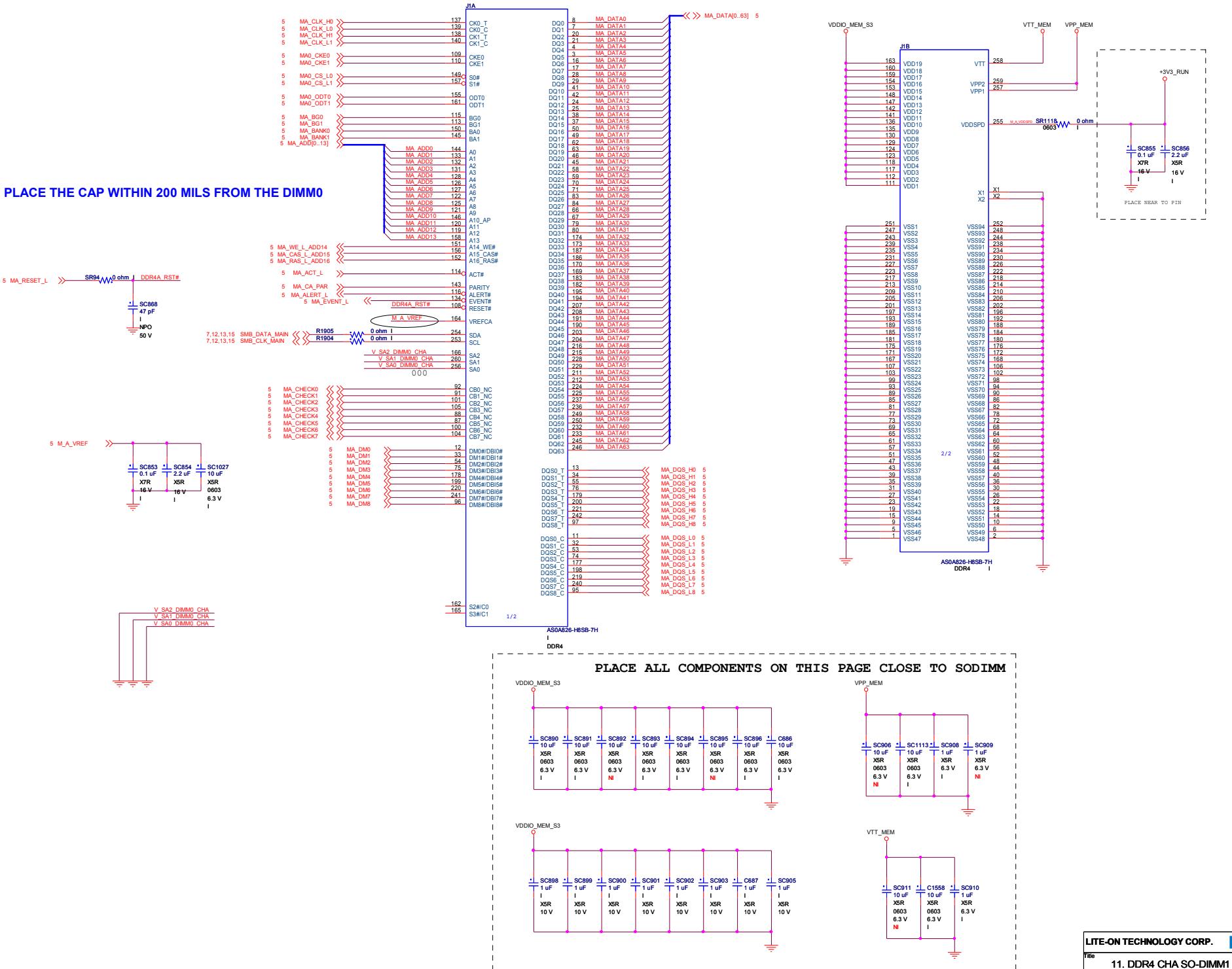


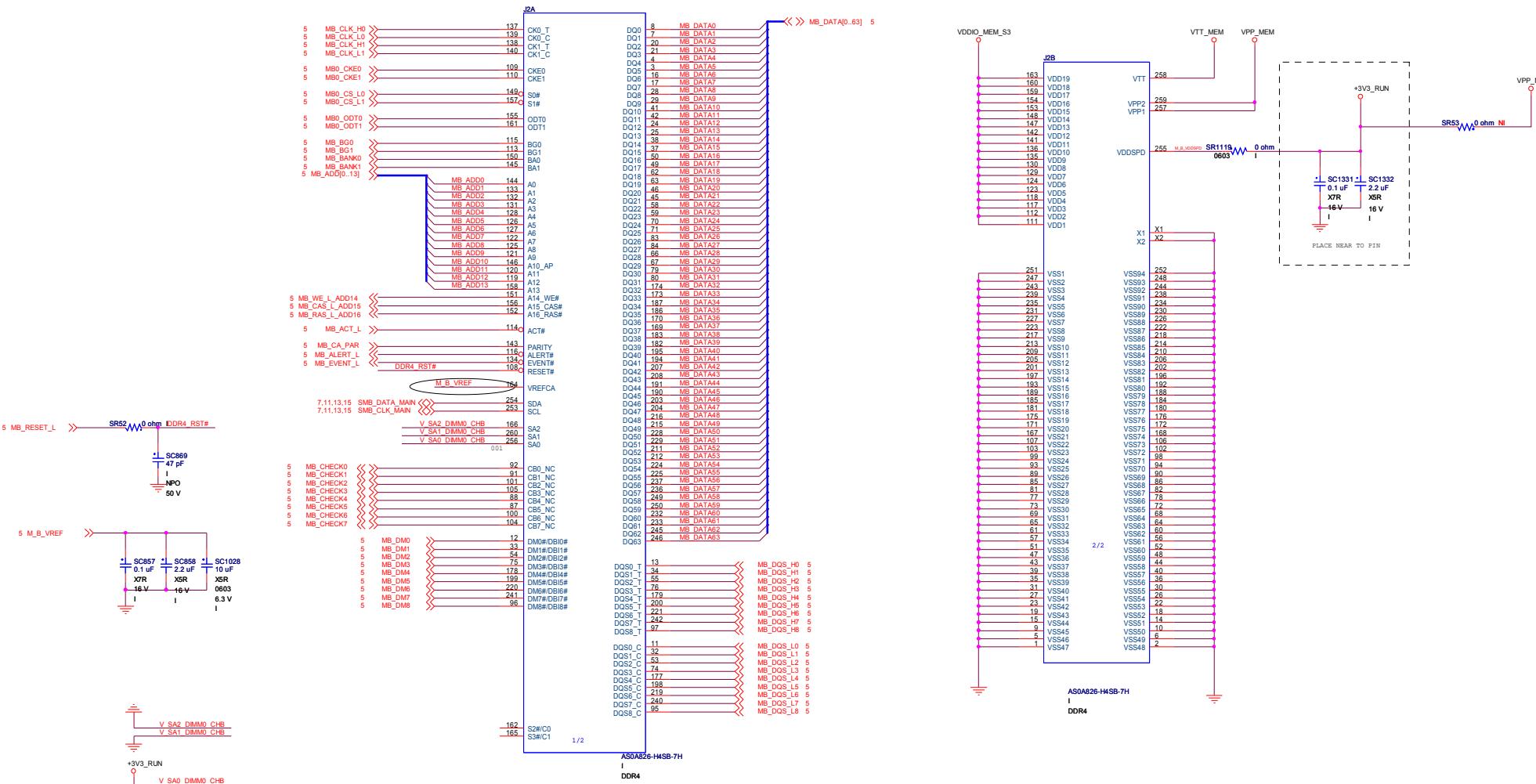


BOTTOM SIDE DECOUPLING

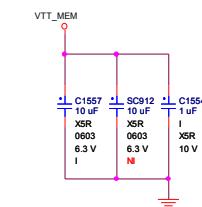
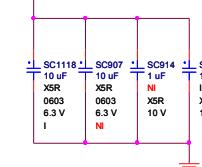
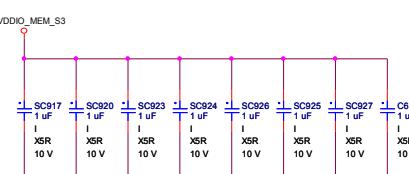
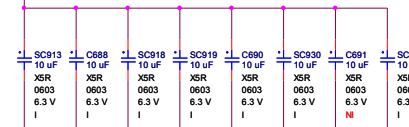


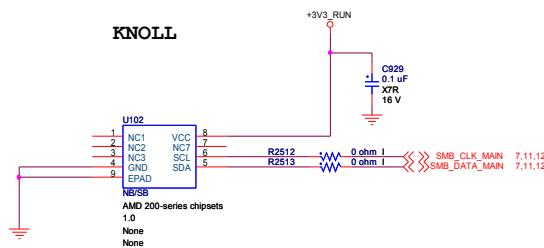




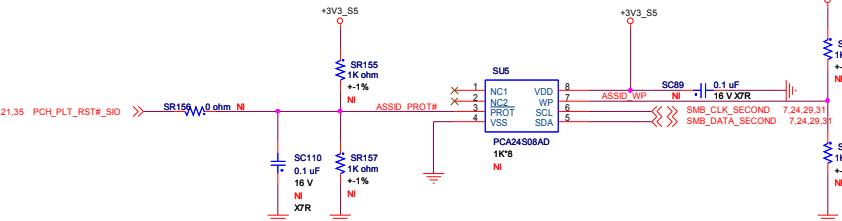
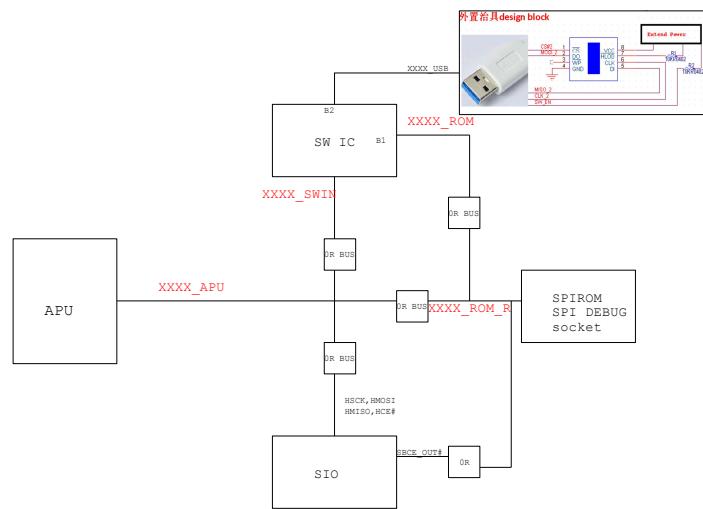


PLACE ALL COMPONENTS ON THIS PAGE CLOSE TO SODIMM

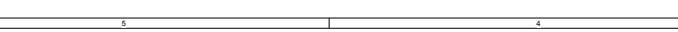
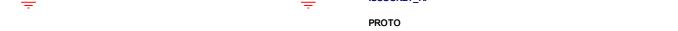
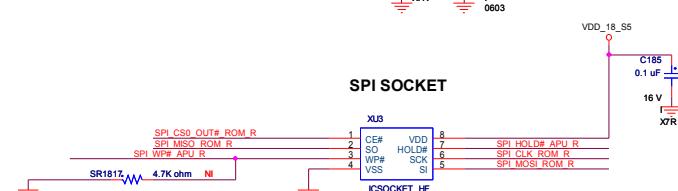
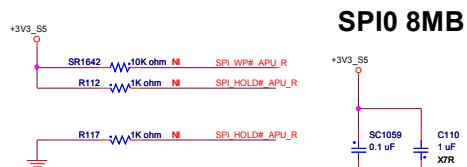




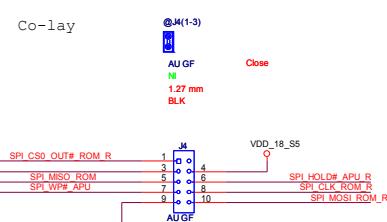
BIOS Recovery Function



INPUT		Function
OE	S	
L	L	B1 Port
L	H	B2 Port
H	X	Disconnect



SPI FLASH



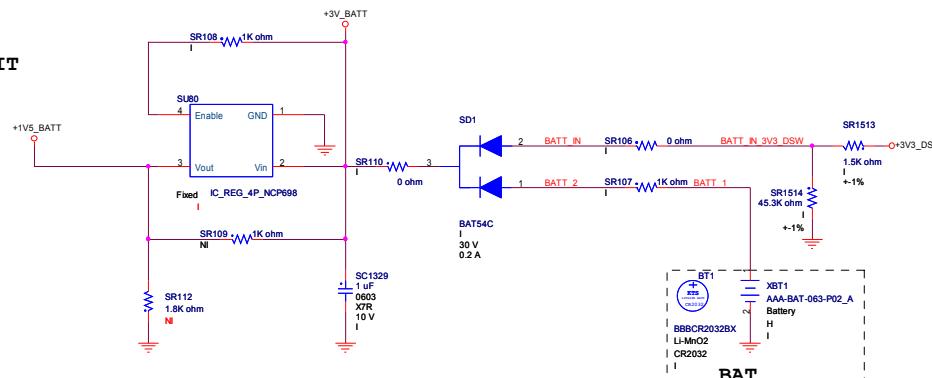
LITE-ON TECHNOLOGY CORP. LITEON

Title 13. Knoll & Asset ID&SPI ROM

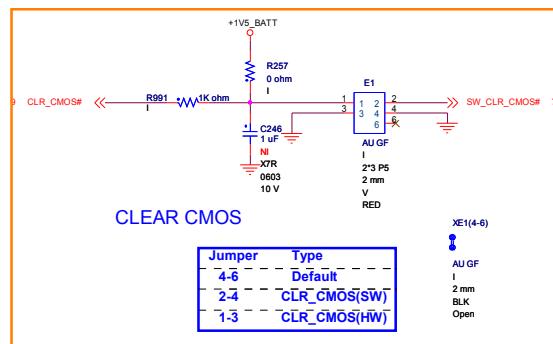
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KC790

Date: Saturday

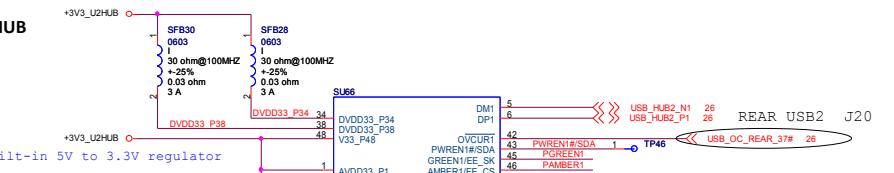
BATTERY CIRCUIT



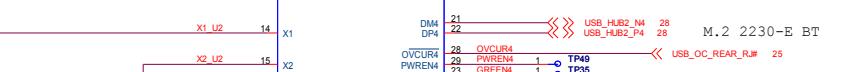
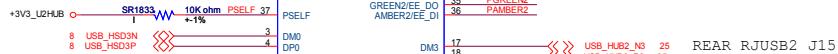
CLEAR CMOS



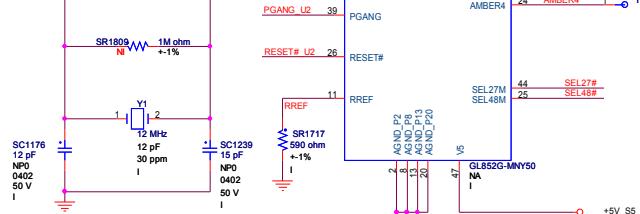
USB2.0 HUB



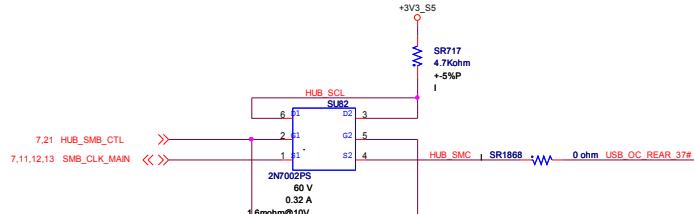
Built-in 5V to 3.3V regulator



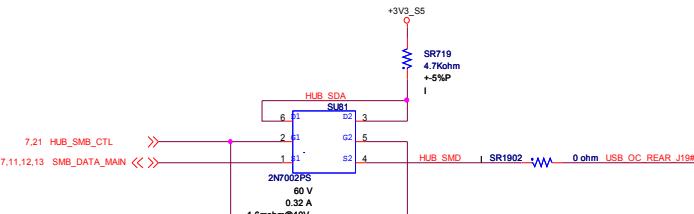
M.2 2230-E BT



Front Panel



SMBus Control



I2C Control

As close to GL852G-1X

As close to PIN48

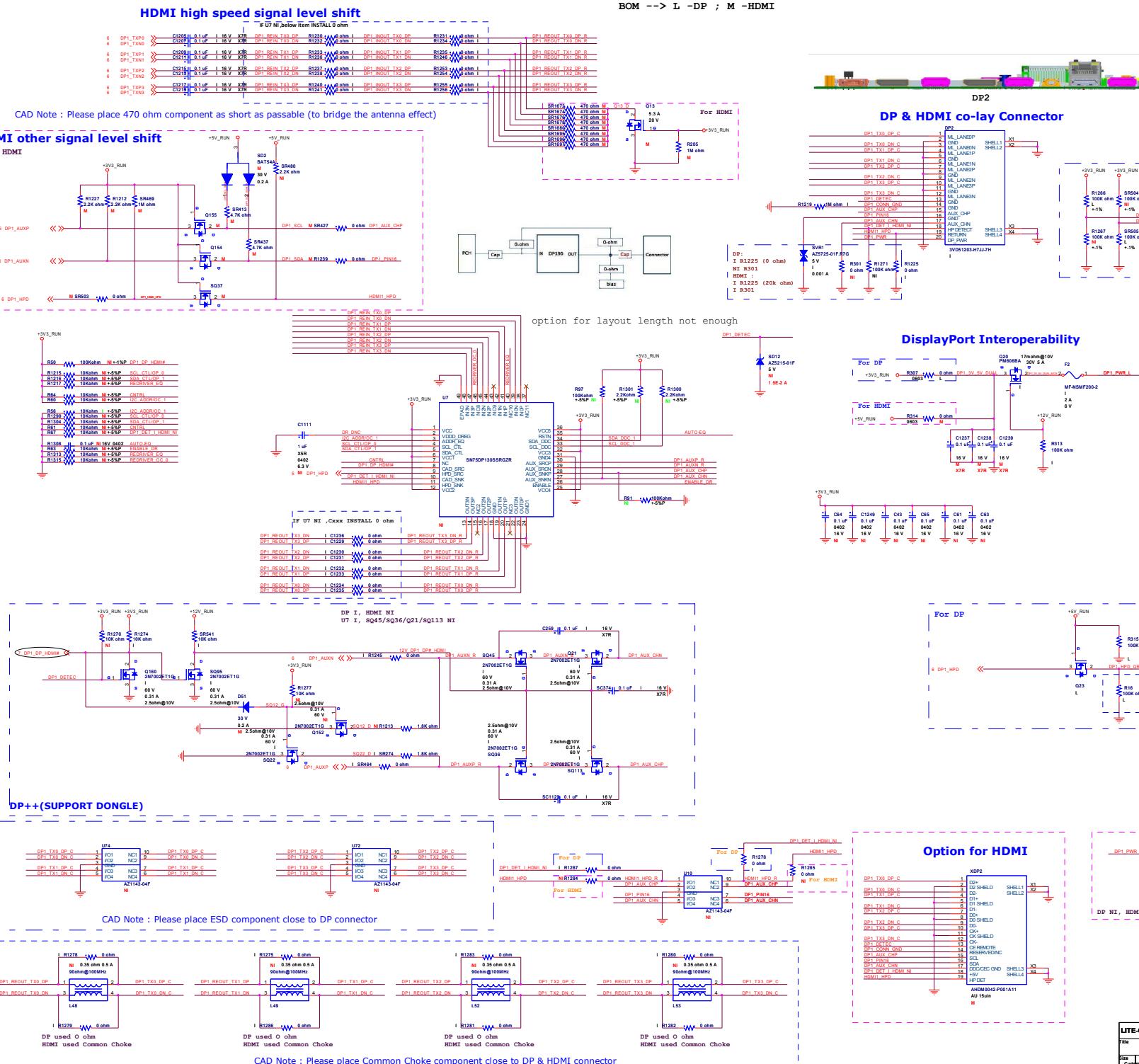
As close to Header J3

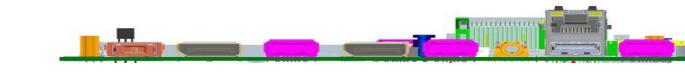
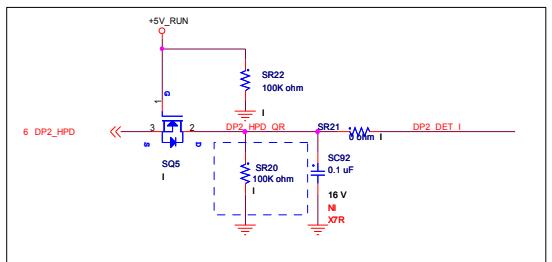
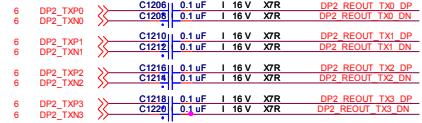
Close to Header J3

Close to 5V_S5

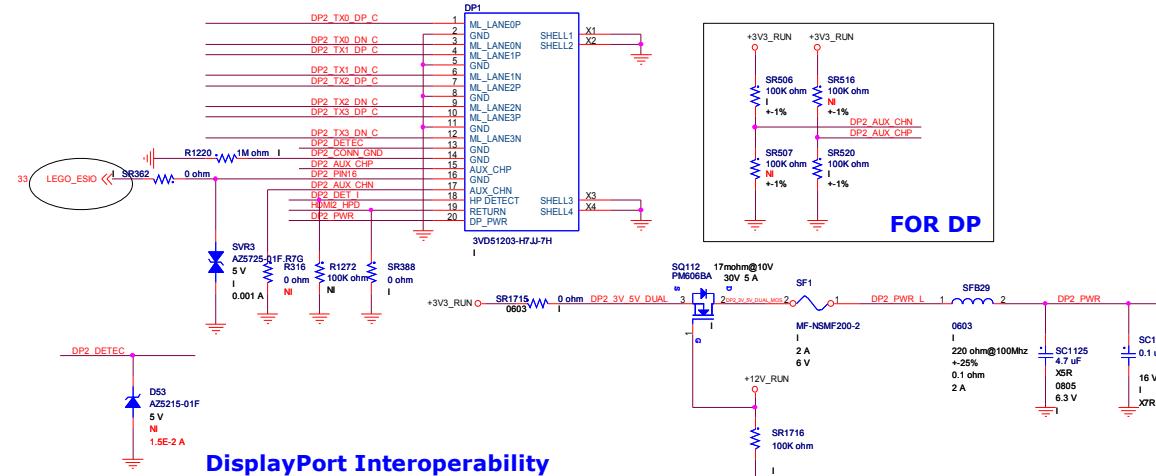
Close to 16V

Close to 10V

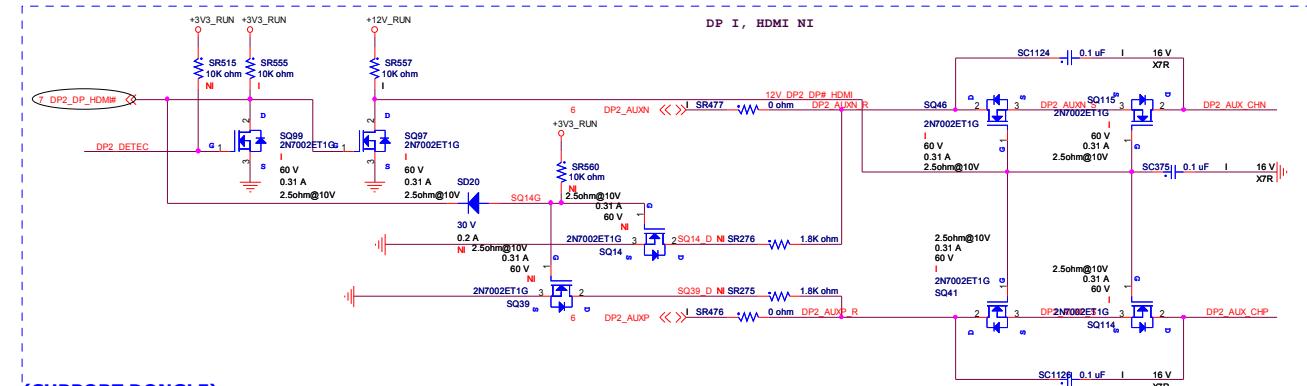




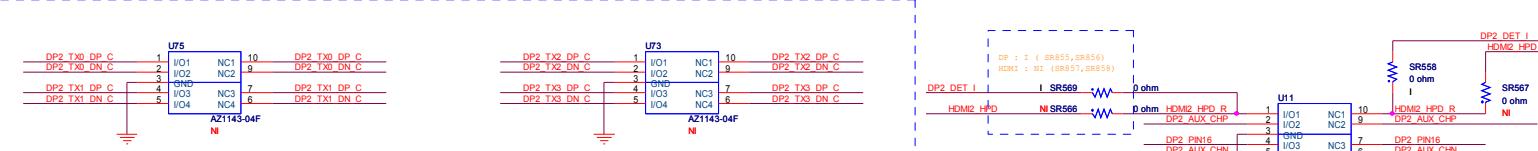
LEGO USE



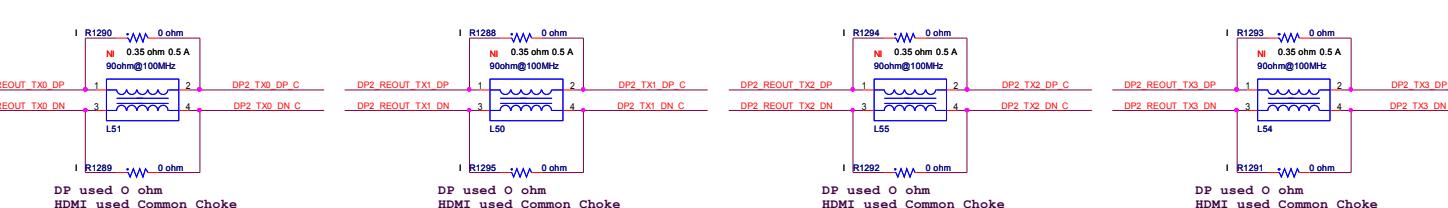
DisplayPort Interoperability



(SUPPORT DONGLE)



CAD Note : Please place ESD component close to DP connector



CAD Note : Please place Common Choke component close to DP & HDMI connector

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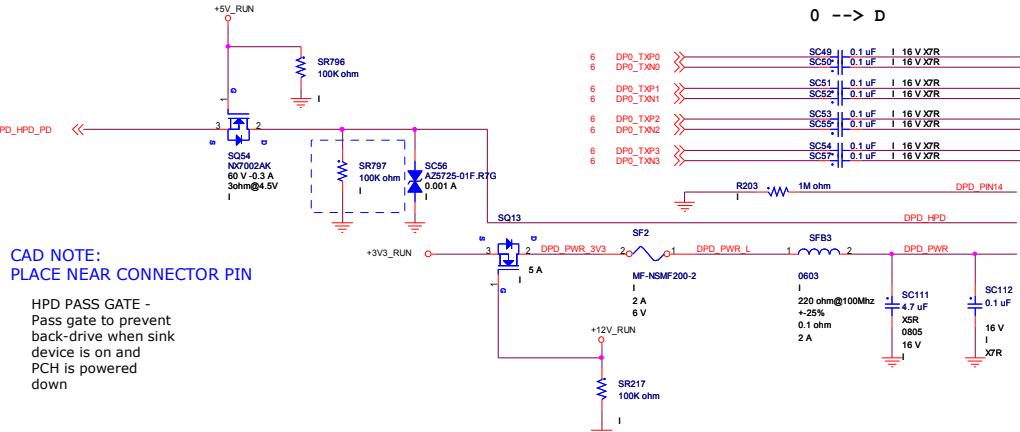
Title 17. Display Port & LEGO

Sheet C Document Number KC790 Rev X03

Date Tuesday, May 03, 2016

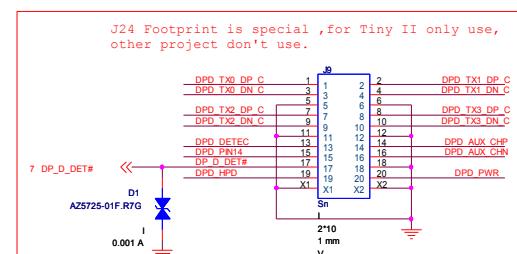
Page 17 of 60

DISPLAY PORT

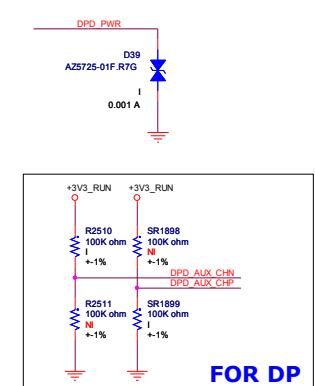
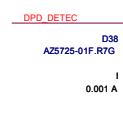


CAD NOTE:
PLACE NEAR CONNECTOR PIN

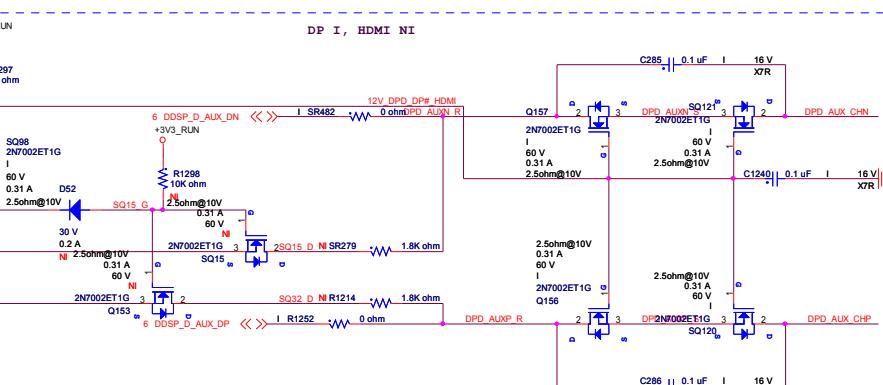
HPD PASS GATE -
Pass gate to prevent
back-drive when sink
device is on and
PCH is powered
down



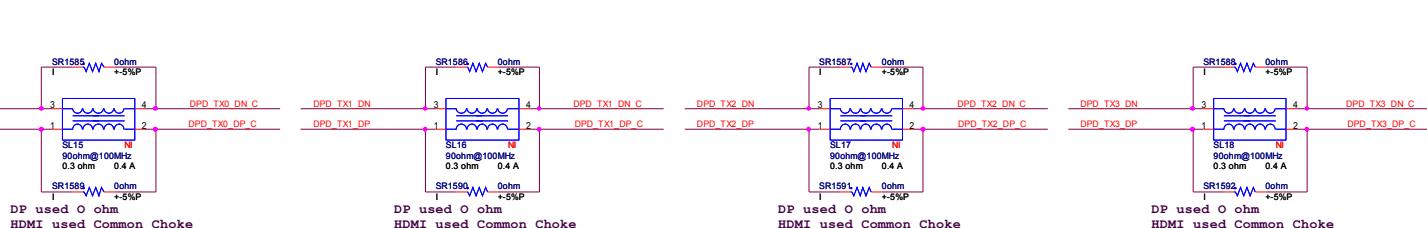
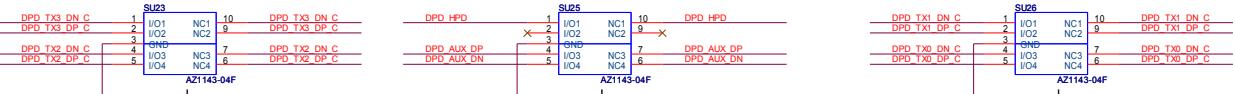
On Cable side Pin17 & Pin 18 need short
DPC_DETECT
L : Connect to Display Port or No Connection
H : Connect to Dangle



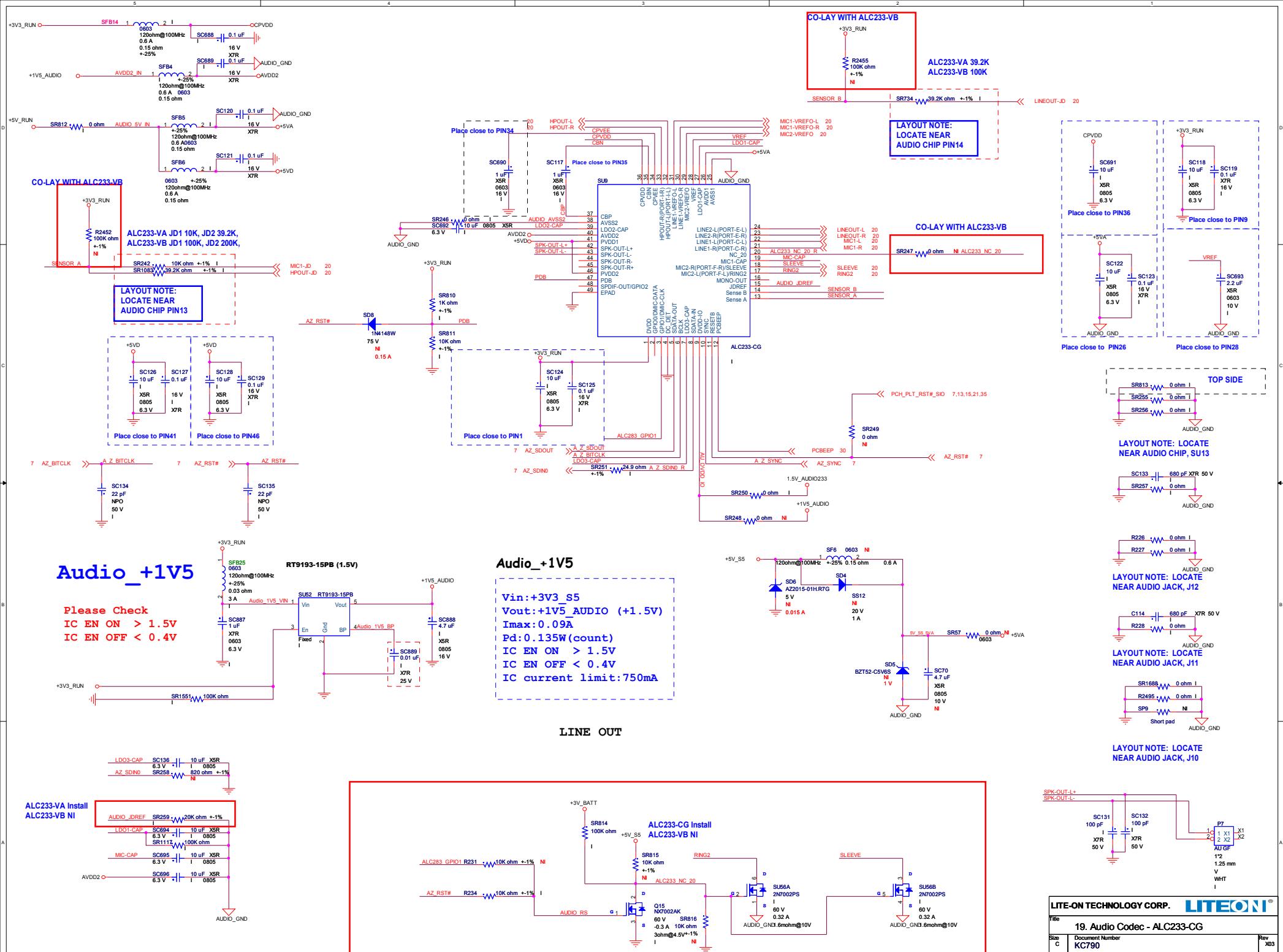
(SUPPORT DONGLE)

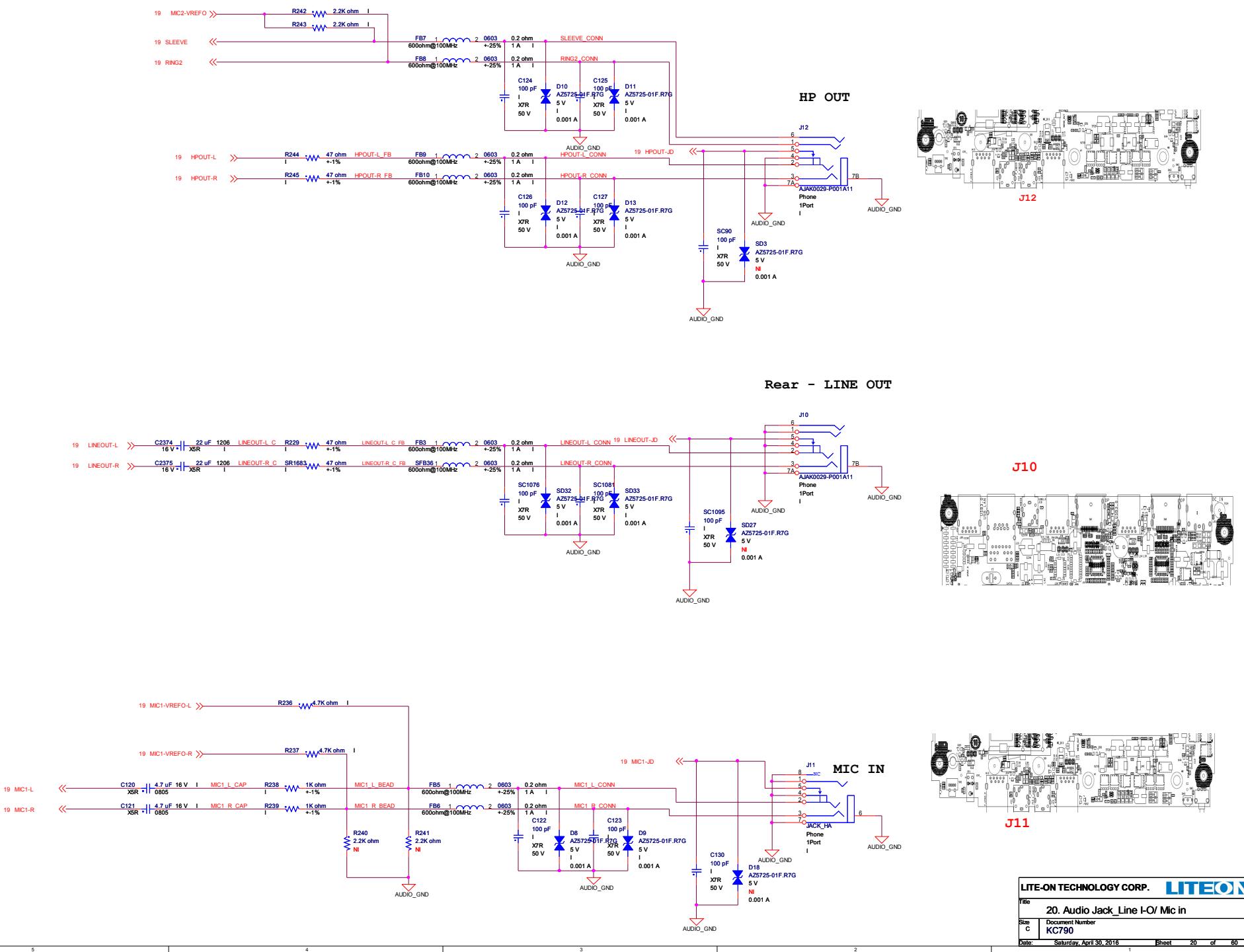


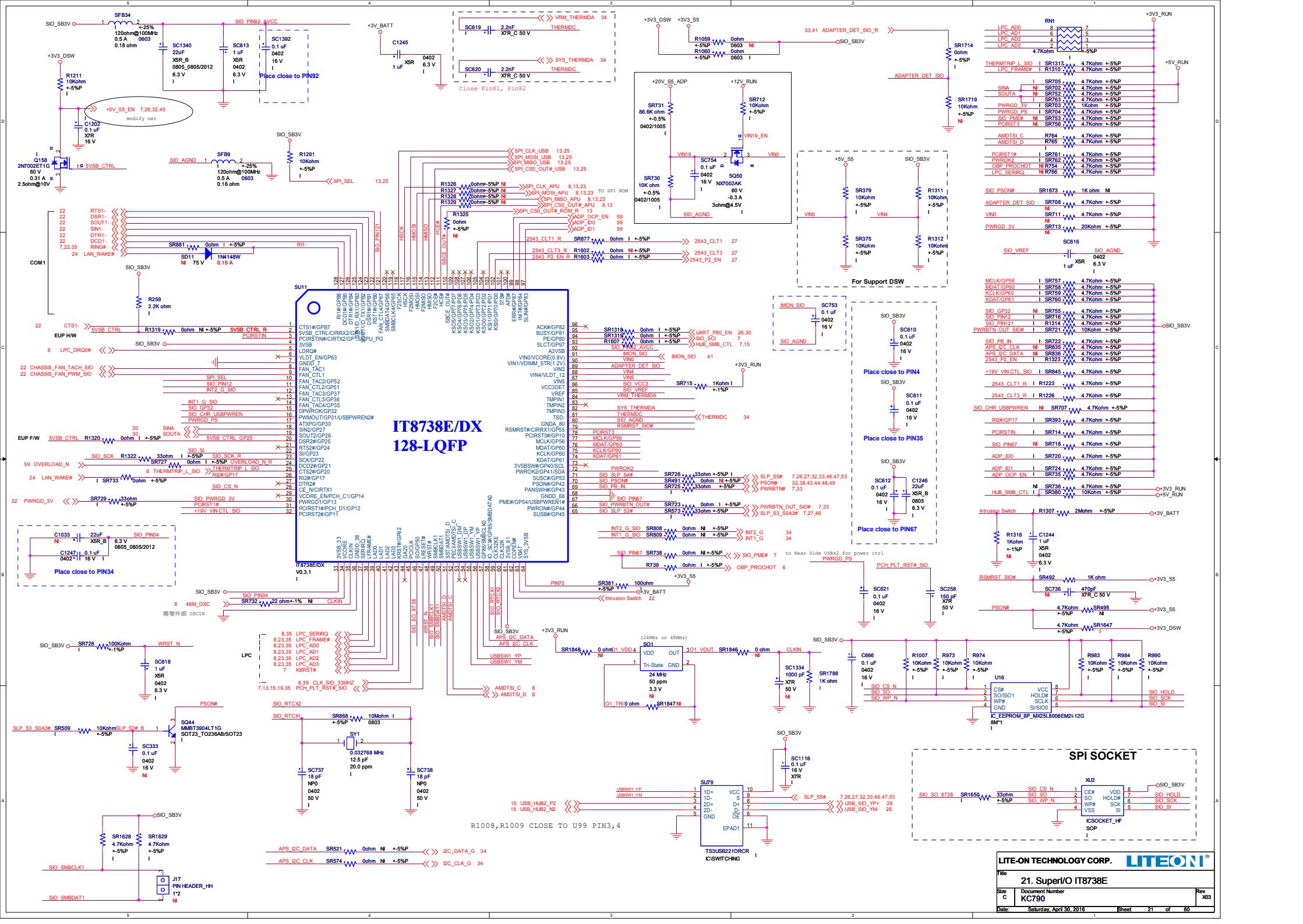
CAD Note : Please place ESD component close to DP connector



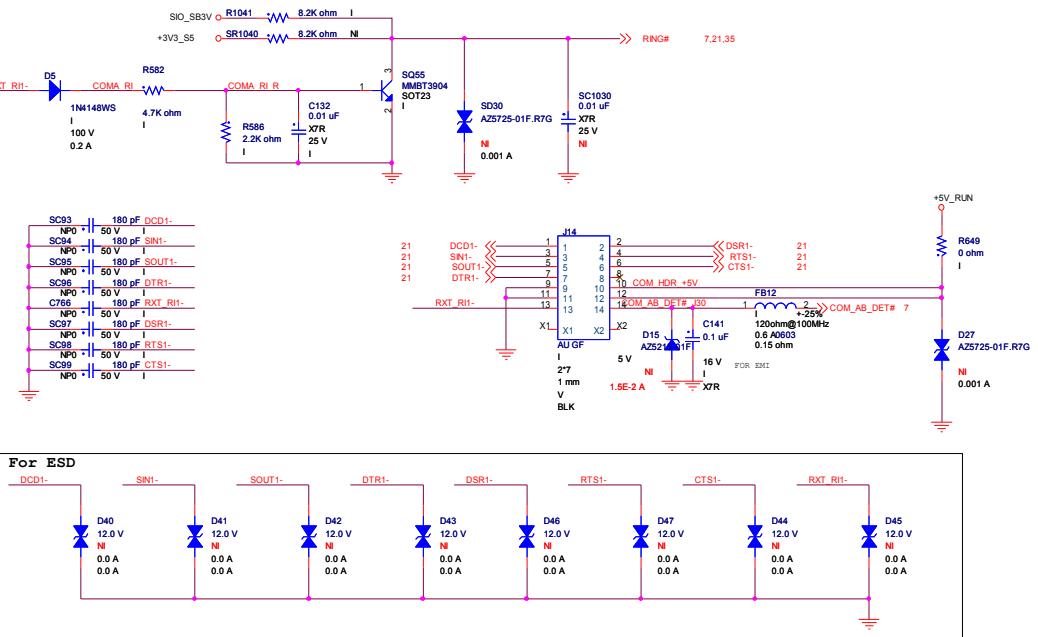
CAD Note : Please place Common Choke component close to J9 pinheader







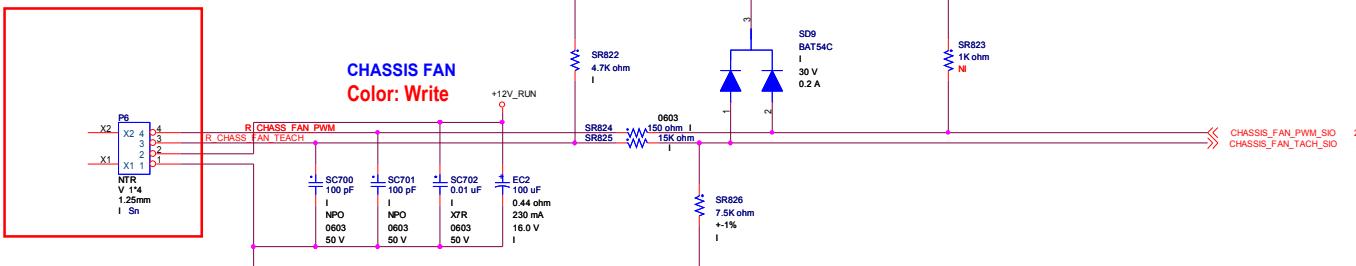
COM PORT HDR

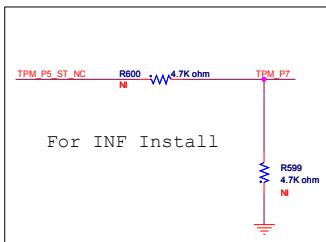


Intrusion Switch

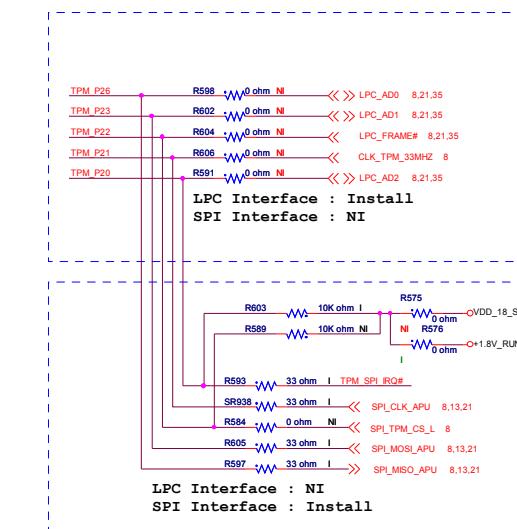
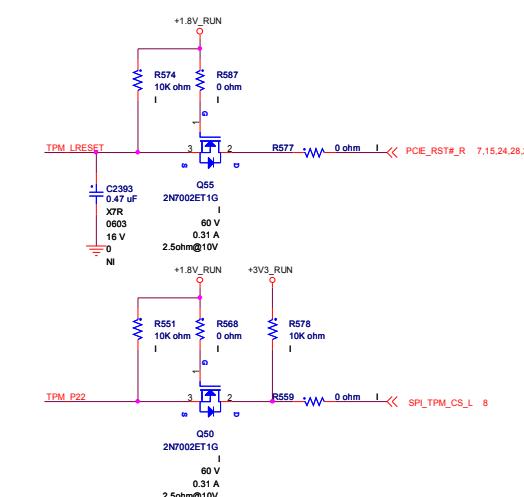
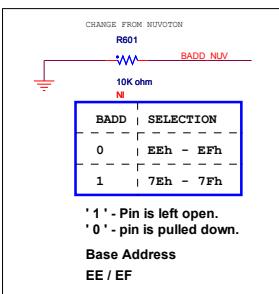
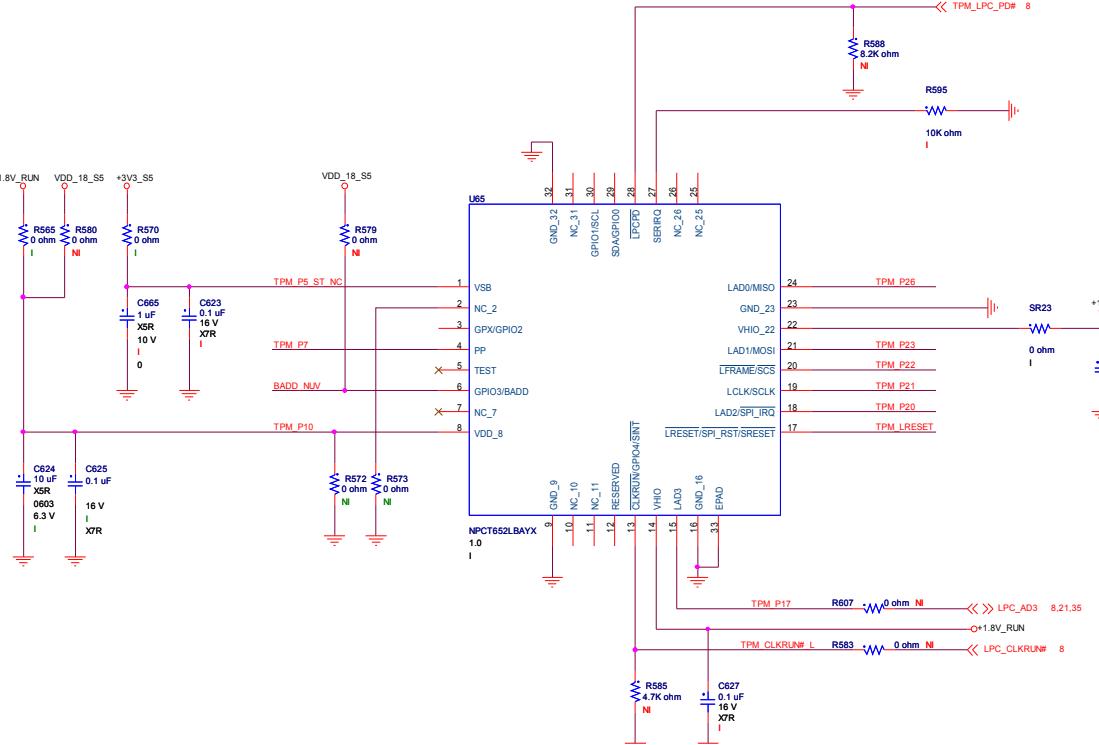


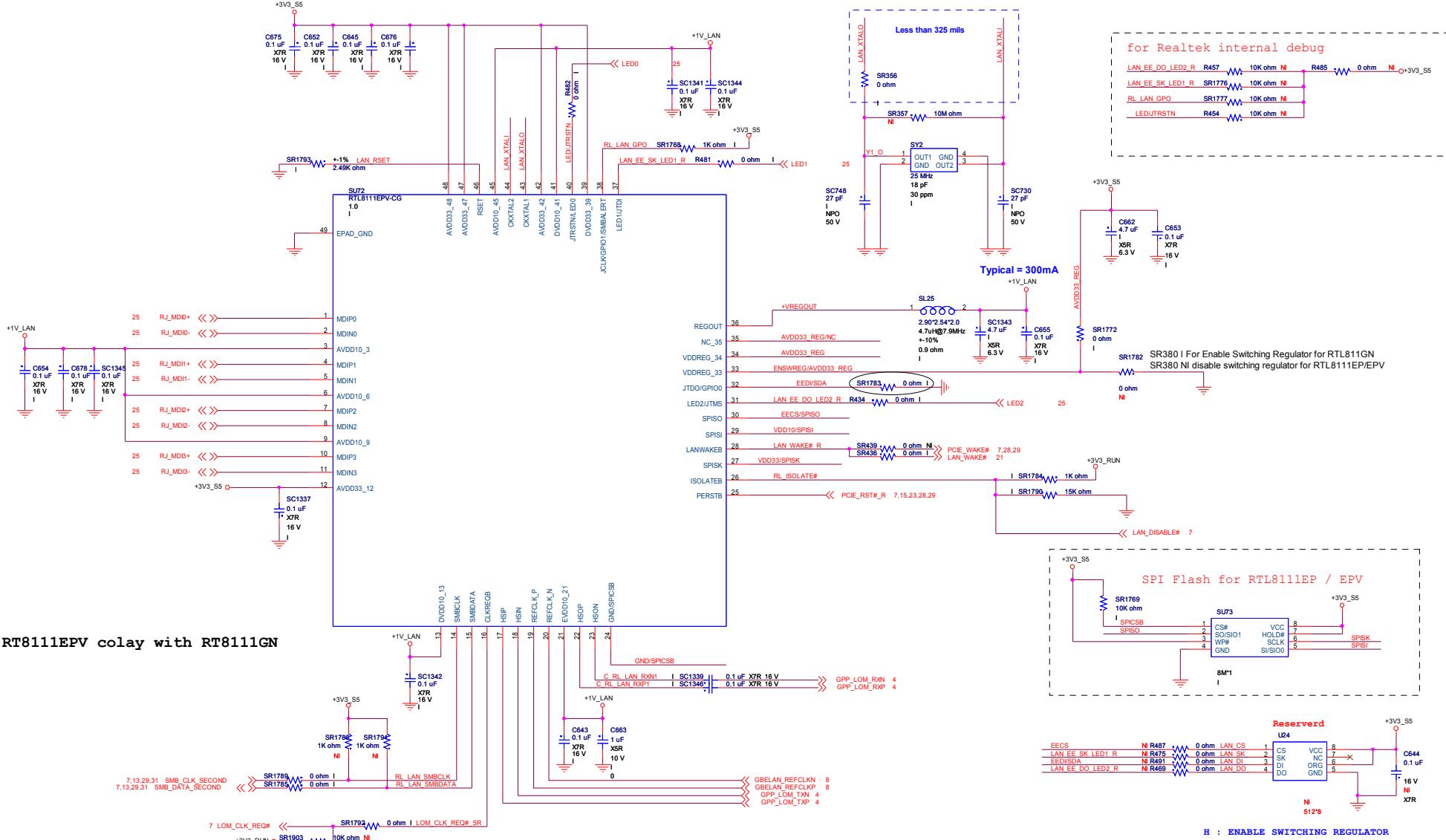
CHASSIS/CPU/PSU FAN



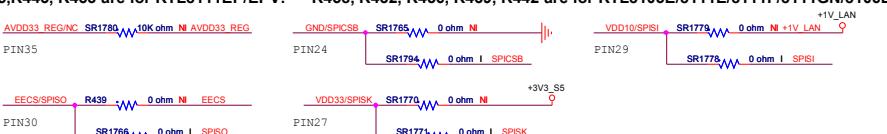


	INF	ST	NUVO
PIN1	VDD	NiC	VSB
PIN2	GND	GND	NC_2
PIN3	NC	NiC	GPX/GPIC2
PIN4	NC	NiC	PP
PIN5	NC	NiC	TEST
PIN6	GPIO	NC	GPIO3/BADD
PIN7	PP	PP	NC_7
PIN8	GND	NiC	VDD_8
PIN9	NC	NiC	GND_9
PIN10	NC	NiC	NC_9
PIN11	NC	NiC	NC_10
PIN12	NC	NiC	NC_11
PIN13	NC	NiC	CLKRUN/GPIO4/SINT
PIN14	NC	NiC	VHIO
PIN15	NC	NiC	LAD3
PIN16	NC	NiC	GND_16
PIN17	RST#	SPI_RST	SPI_RST
PIN18	PIRQ#	SPI_PIRQ	LAD2/SPI IRQ
PIN19	SCLK	SPI_CLK	LCLK/SCLK
PIN20	CS#	SPI_CS	LFRAME/SCS
PIN21	MOSI	MOSI	LAD1/MOSI
PIN22	VDD	VPS	VHIO_22
PIN23	GND	NiC	GND_23
PIN24	MISO	MISO	LADO/MISO
PIN25	NC	NiC	NC
PIN26	NC	NiC	NC
PIN27	NC	NiC	SERIRQ
PIN28	NC	NiC	LPCPCD
PIN29	NC	NiC	SDA/GPIO0
PIN30	NC	NiC	GPIO1/SCL
PIN31	NC	NiC	NC
PIN32	GND	NiC	GND





R493, R455, R443, R433 are for RTI 8111EP/EPV **R458, R432, R456, R439, R442** are for RTI 8105E/8111E/8111F/8111GN/8106EN



WOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off
Off	S3/S4/SS	Off	Off	Off
On	10Mb Inactive	On	Off	Off
On	10Mb Active	Blinking	Off	Off
On	100Mb Inactive	On	On	Off
On	100Mb Active	Blinking	On	Off
On	1Gb Inactive	On	Off	On
On	1Gb Active	Blinking	Off	On



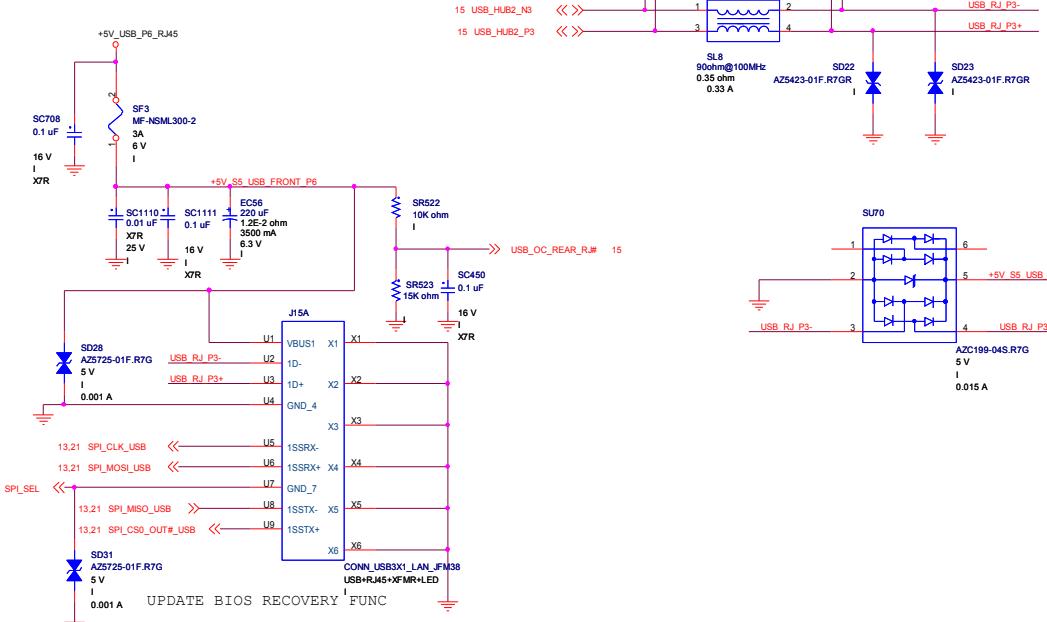
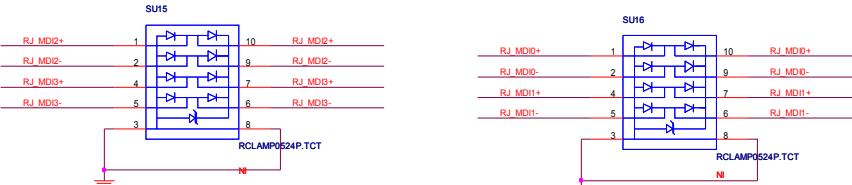
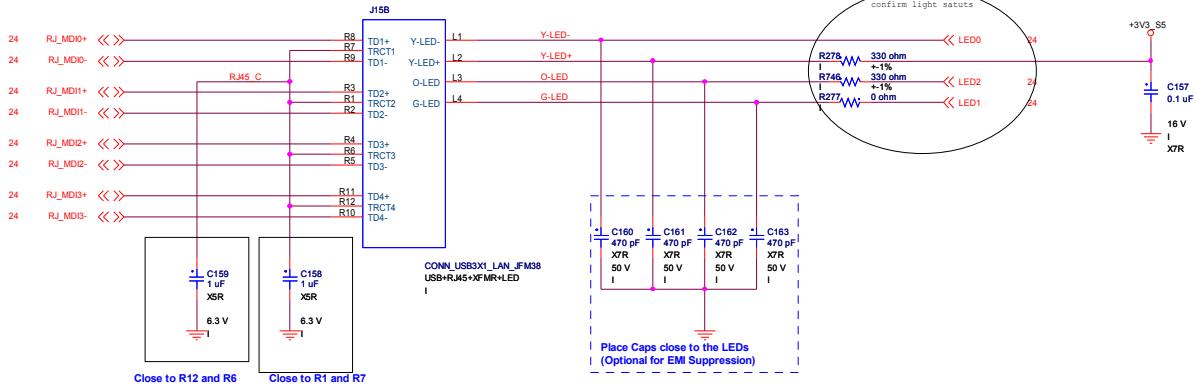
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Title

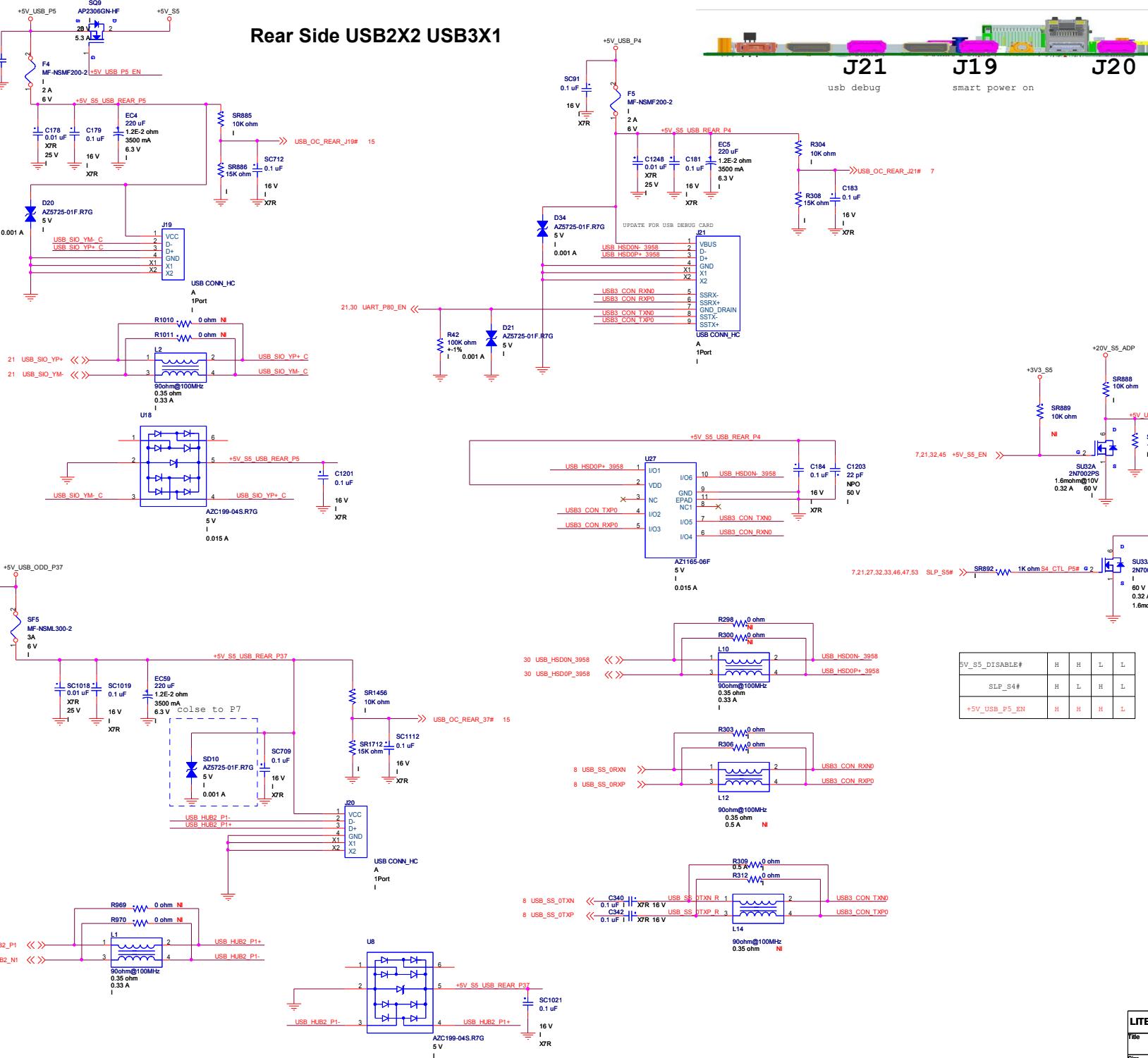
24. LAN RTL8111EPV

Size C Document Number KC790

Date: Saturday, April 30, 2016 Sheet 24 of 60



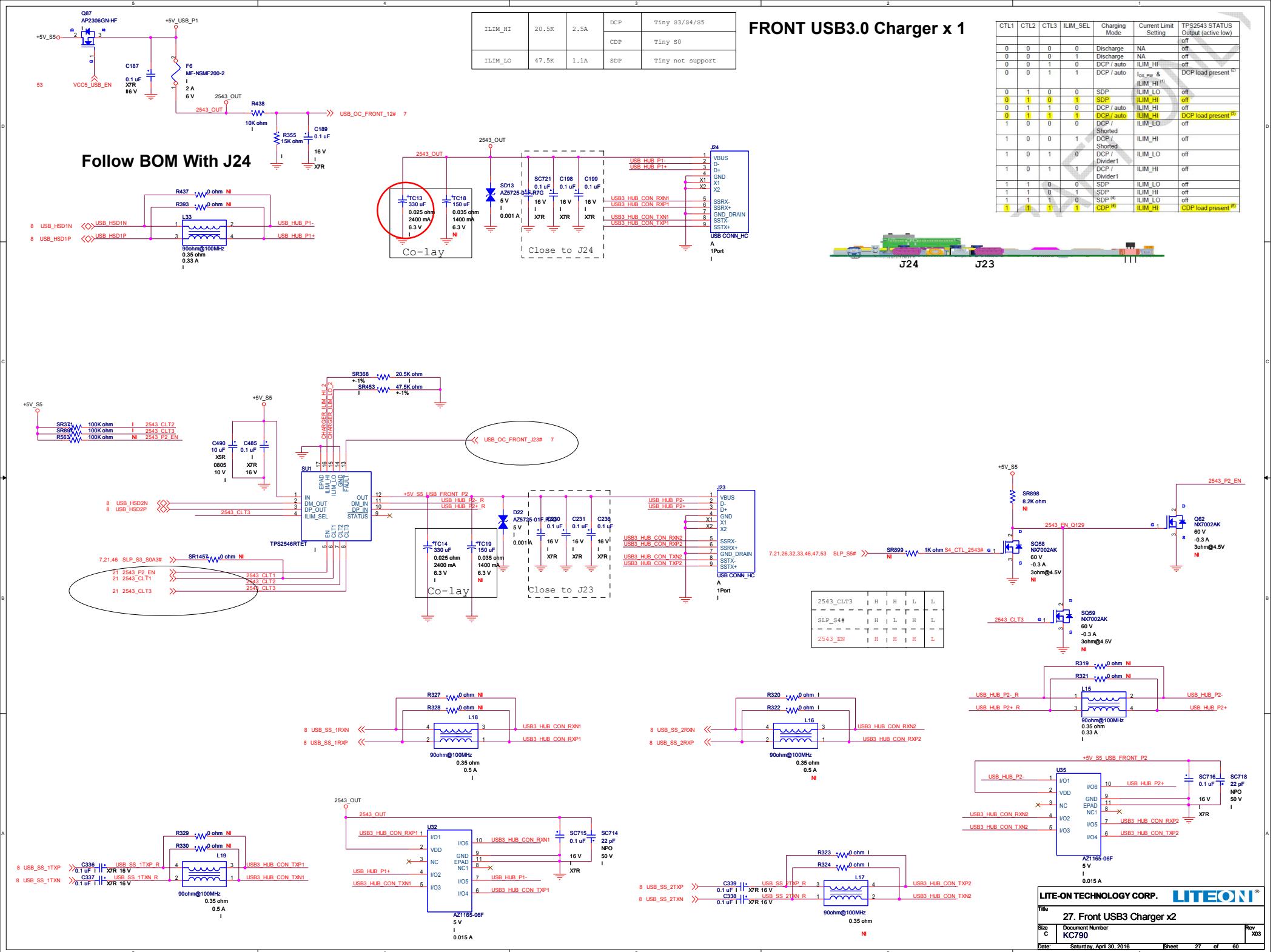
Rear Side USB2X2 USB3X1

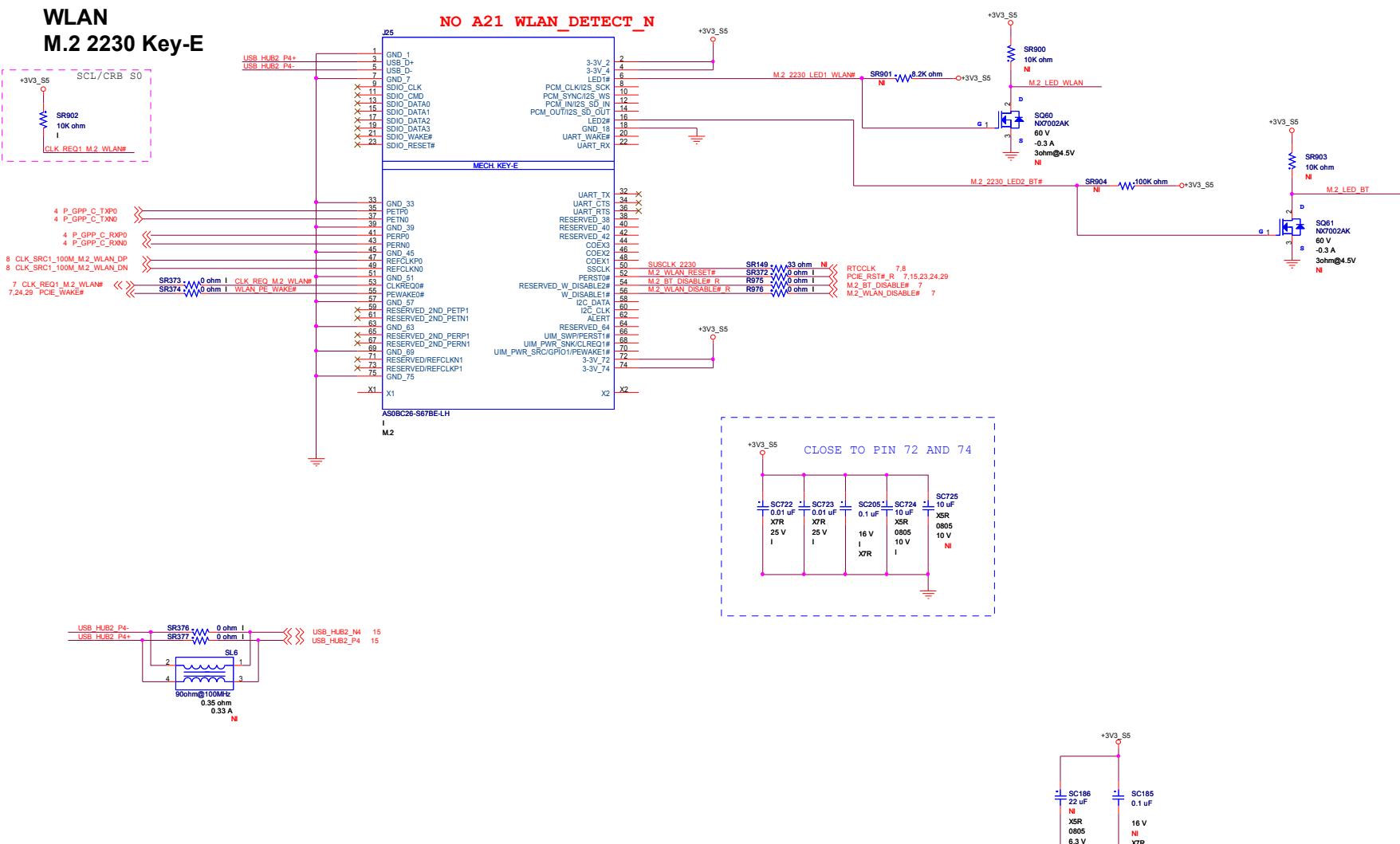


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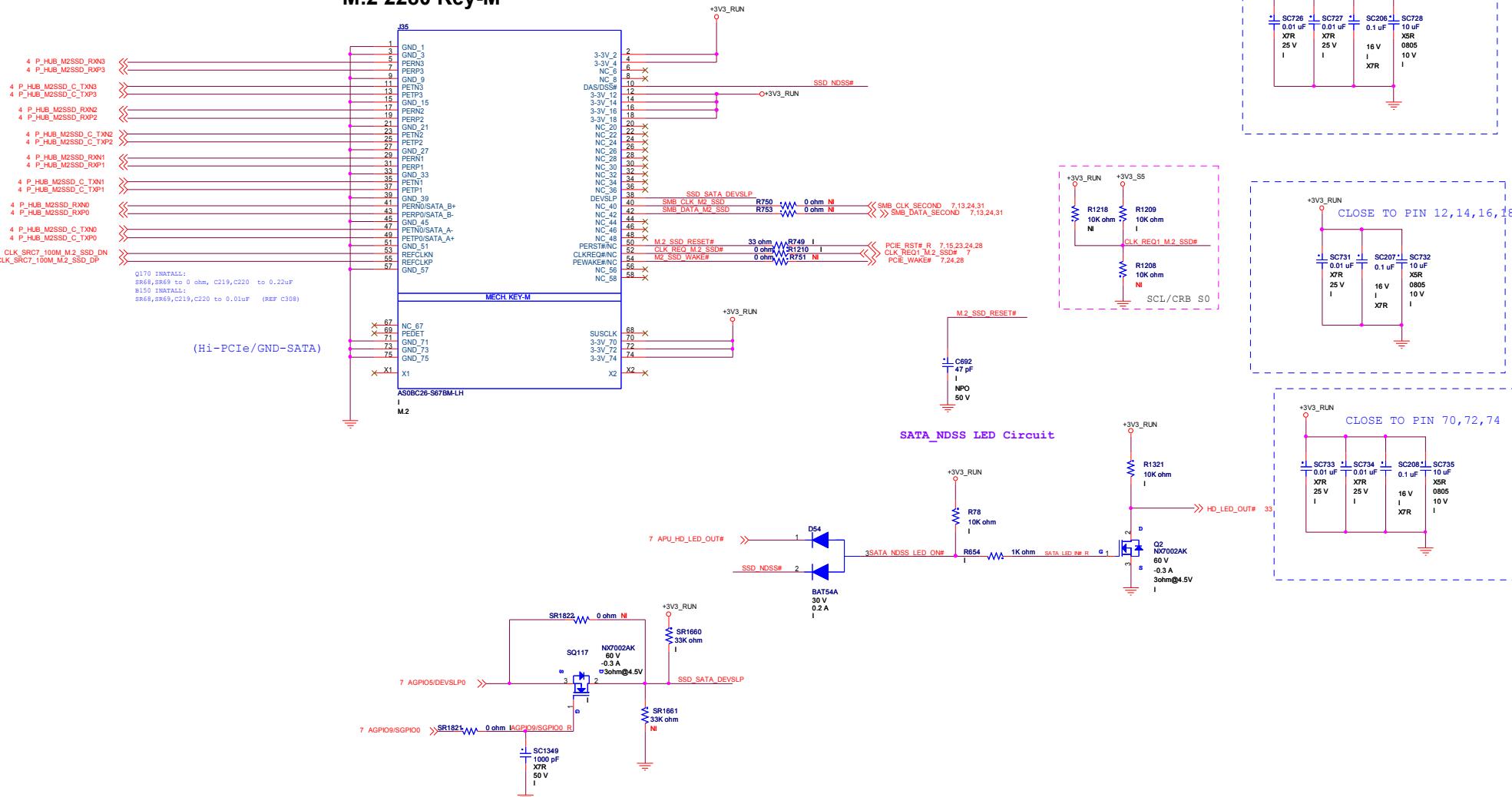
ELITE-ON TECHNOLOGY

26. Rear USB2
Size C Document Number K0700



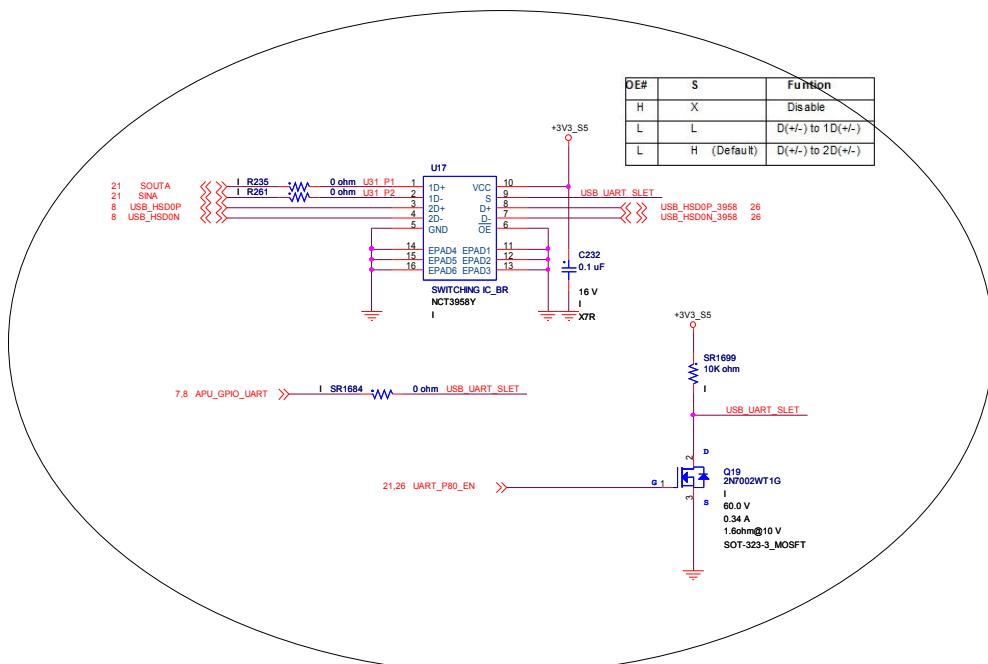
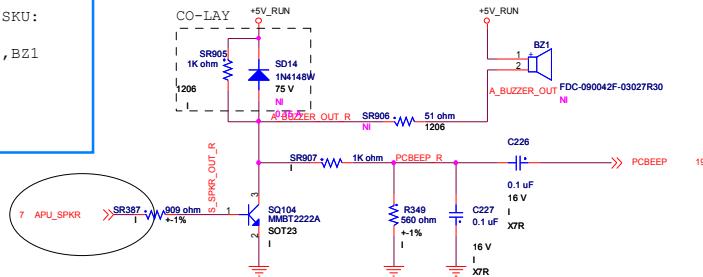


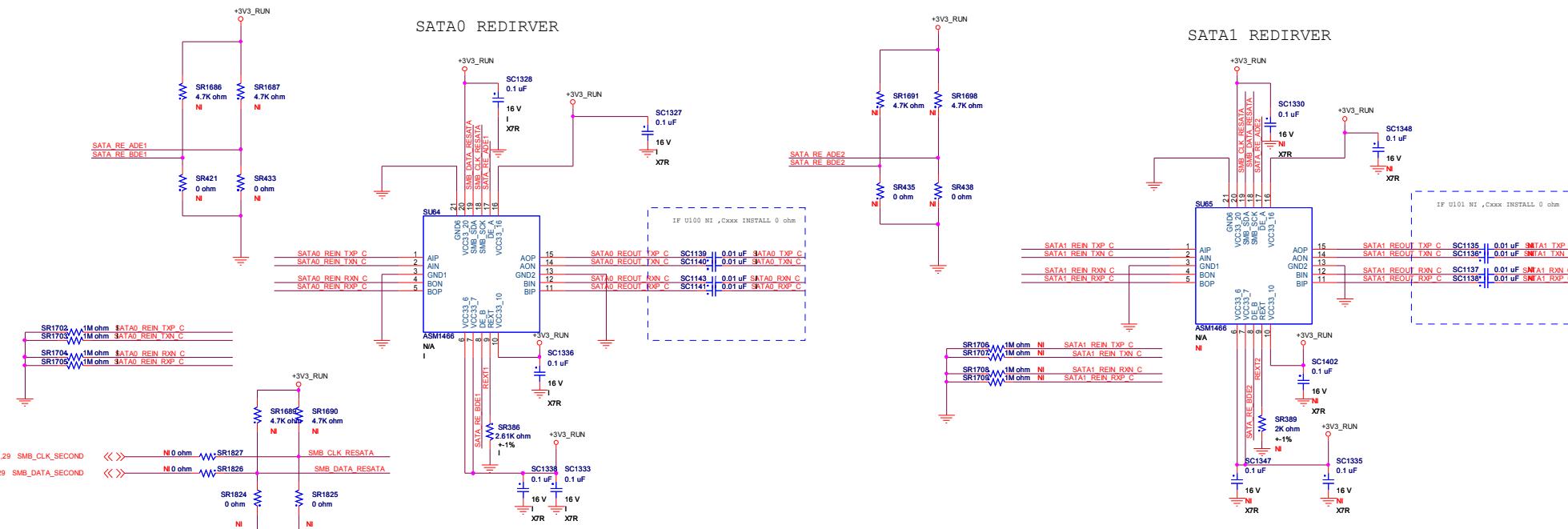
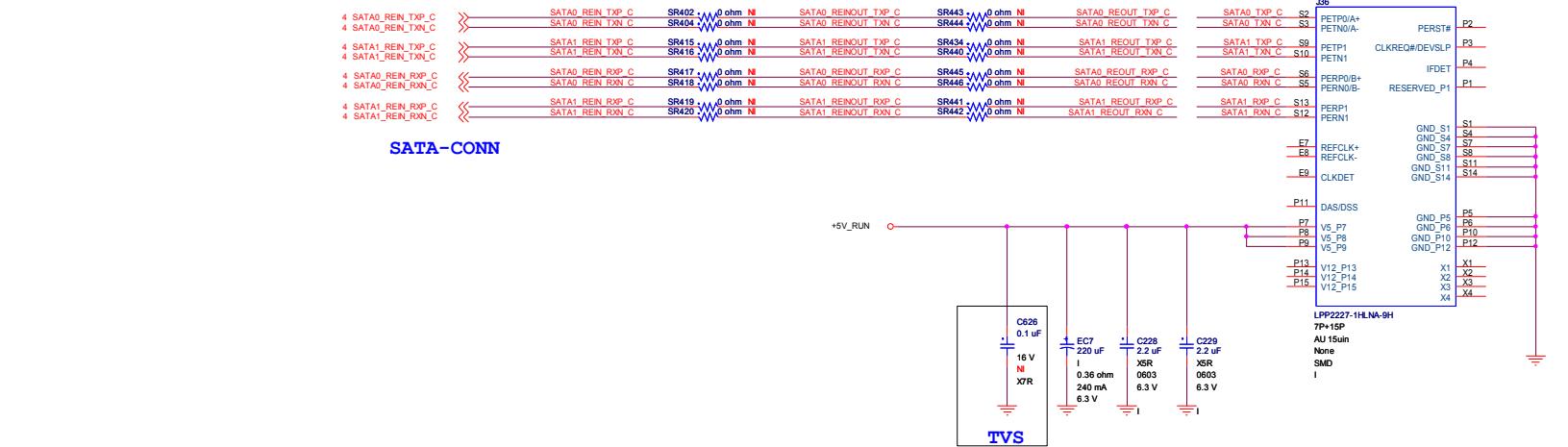
SSD Card PCIE M.2 2280 Key-M

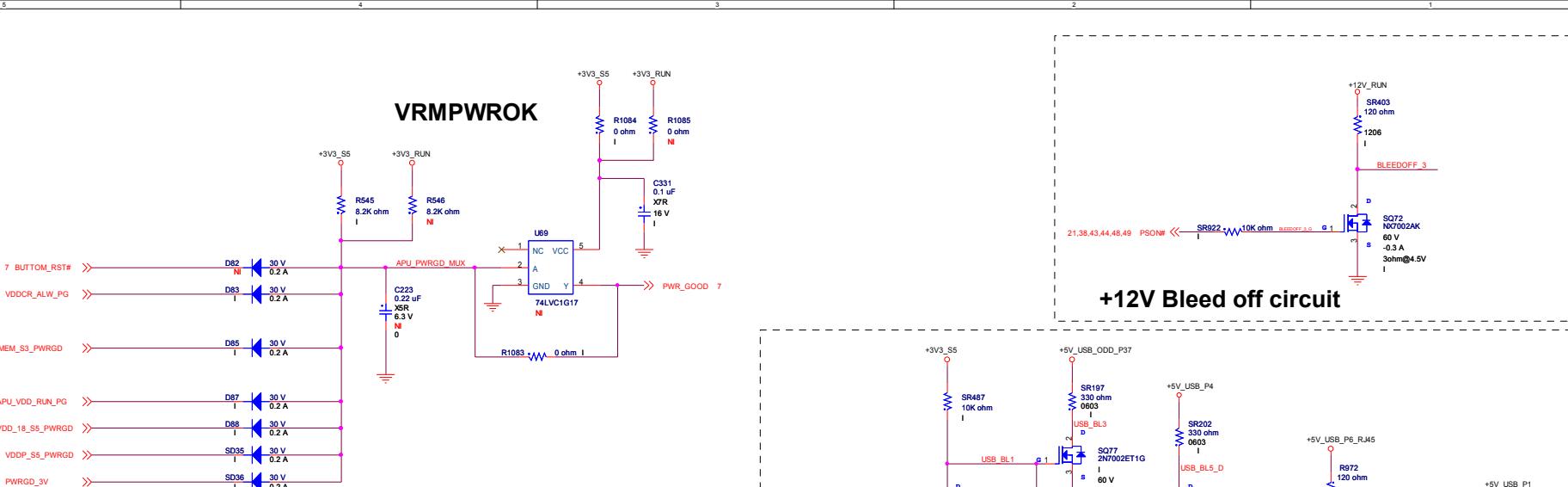


For Google SKU:
Install
SD14 ,SR906,BZ1

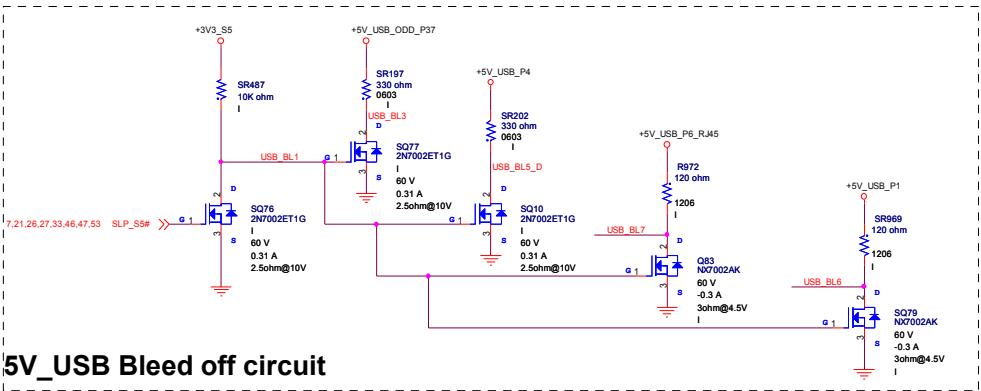
Remove
SR905



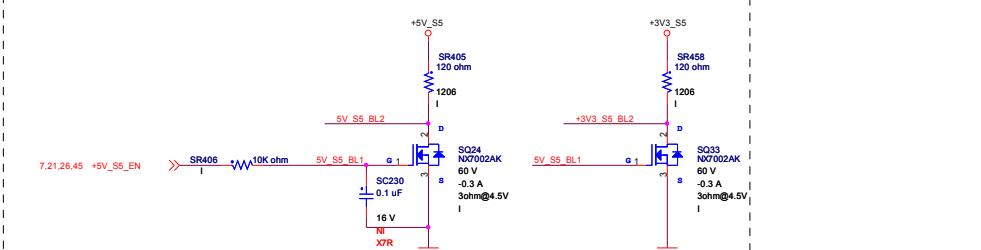




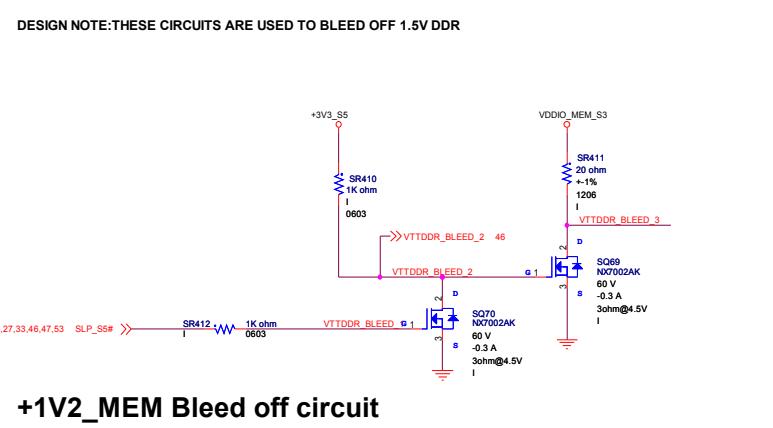
+12V Bleed off circuit



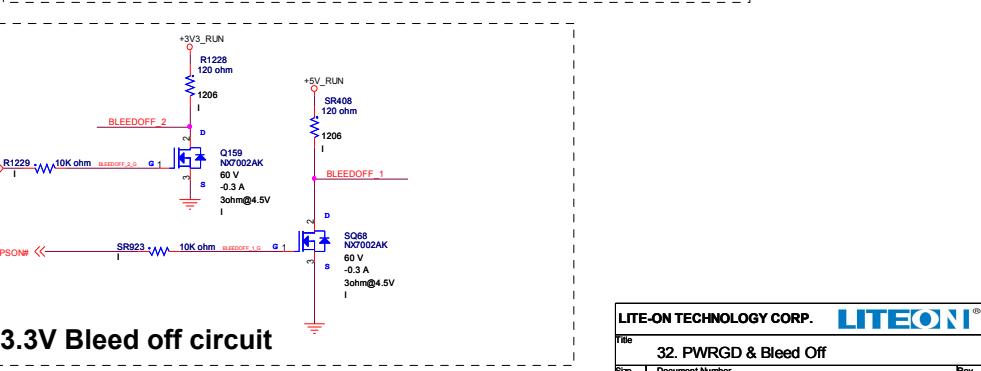
5V_USB Bleed off circuit



5V_S5 and 3V_S5 Bleed off circuit



+1V2_MEM Bleed off circuit



5V & 3.3V Bleed off circuit

CONTROL PANEL / LED CIRCUITY

POWER BUTTON & LED

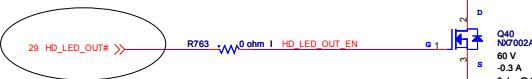
Color	Function
G	HDD
G	WiFi
G	BT

$I_d = 25mA @ 2.8V$ (SPEC)
 $I_d = (5V-2.8V) / 330\Omega = 5mA$
 $5m * 3.2 V = 16 mW$
 $0.1W$ (For Current limit R)

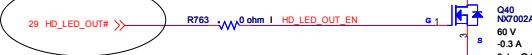
For NEC SKU:
 Remove:
 R765Q, Q42, R762
 SW1
 CR1

 Install :
 R779
 SW1_
 CR1_

WLAN LED



HDD LED

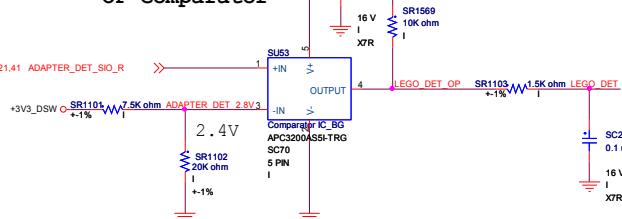


BT LED

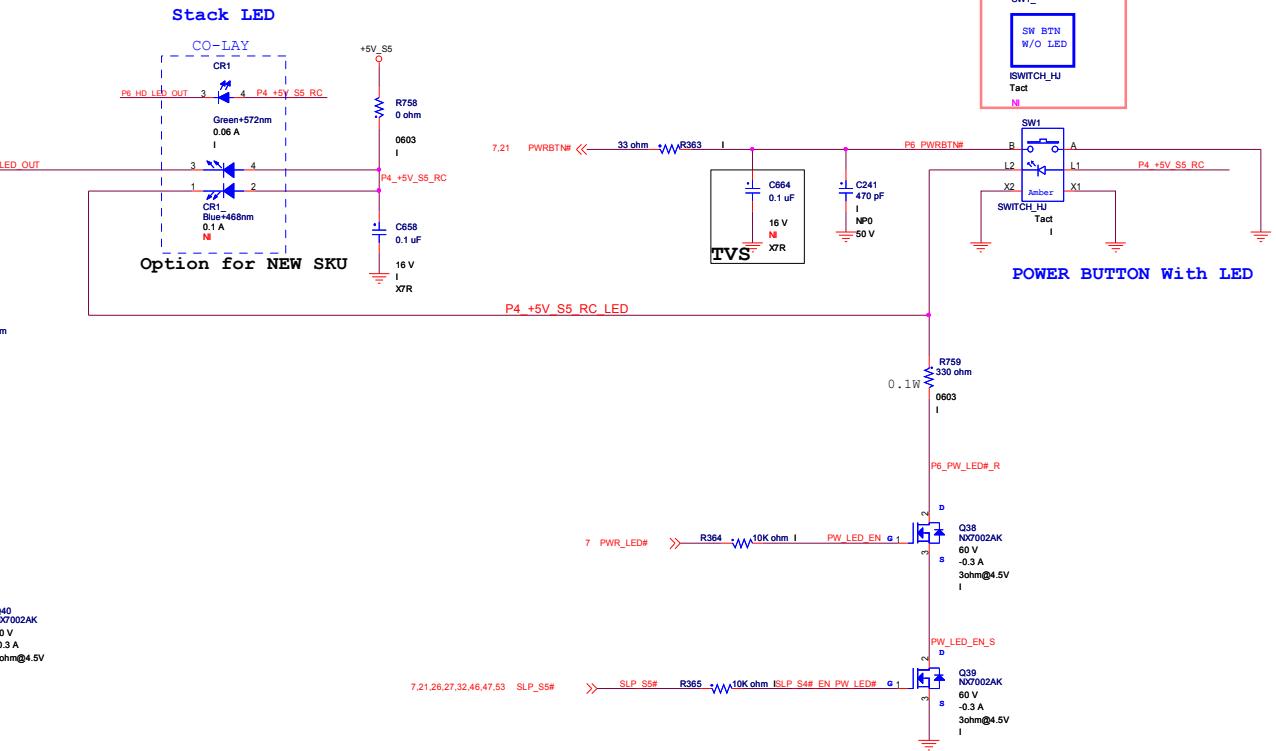
Change for EUP 1W @S5
 $+3V3_S5$
 R776 680 ohm
 MEM_LED

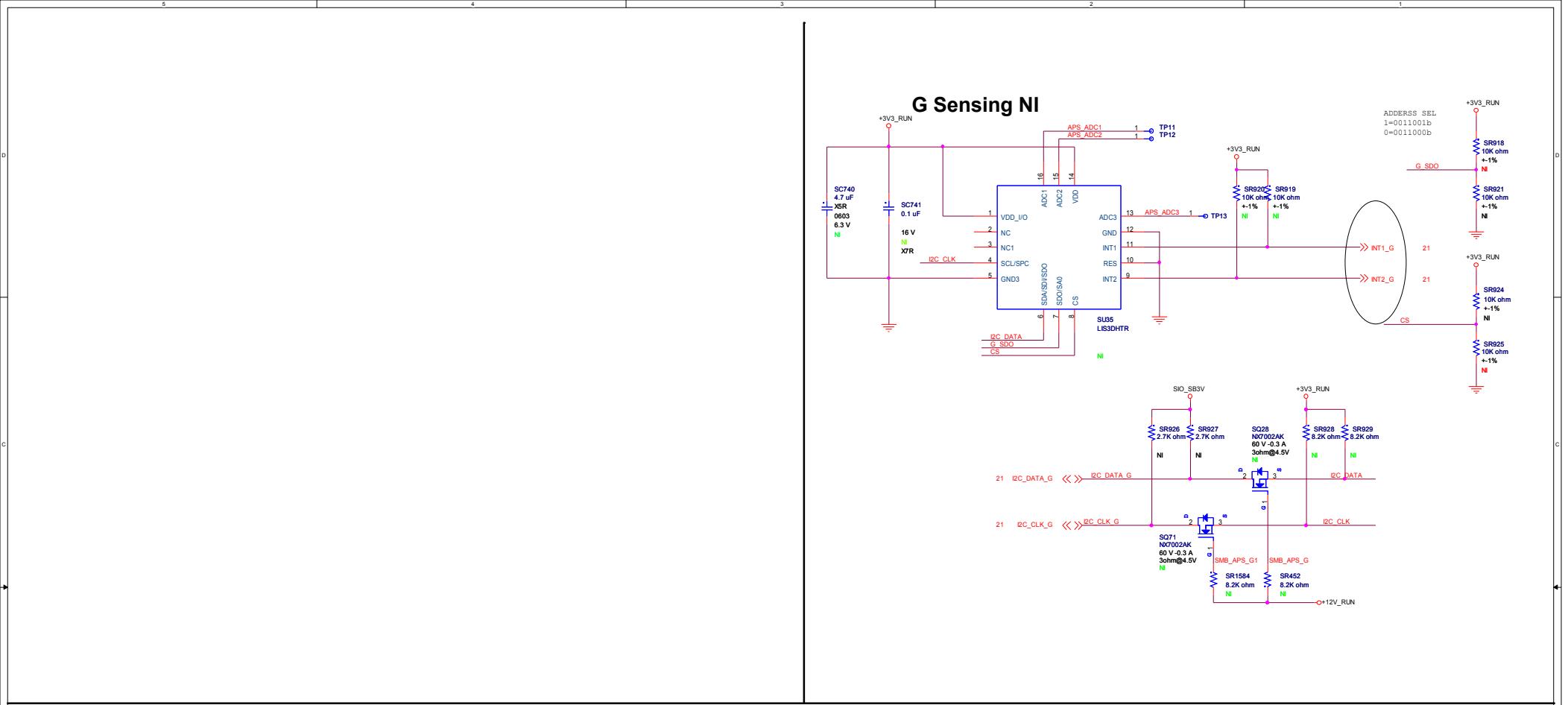
 C_{R2} GRN 5V 0.03 A
 +3_3V_DUAL

OP Comparator



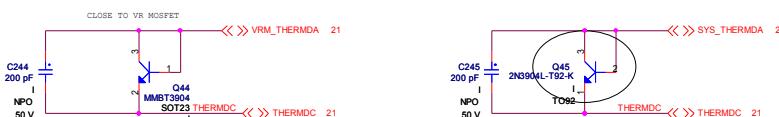
PCA LED CIRCUITS





Temperature Sensing

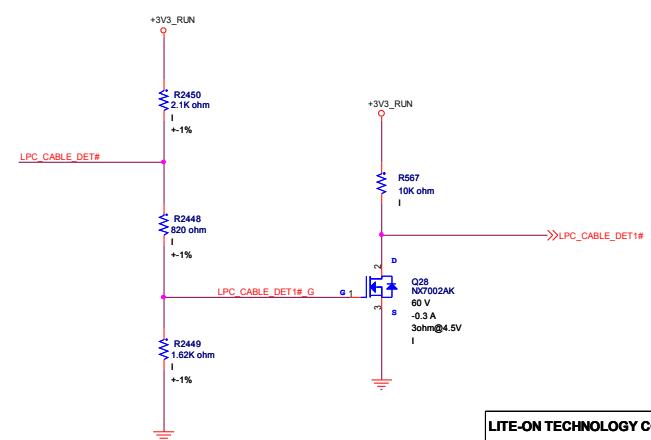
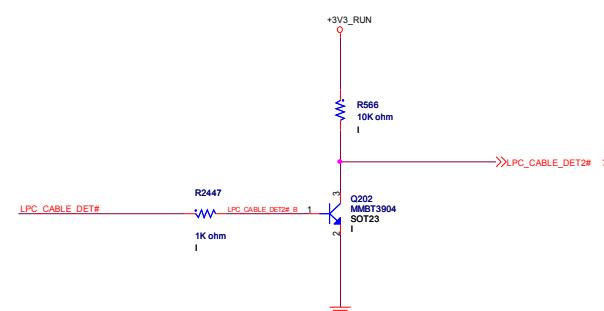
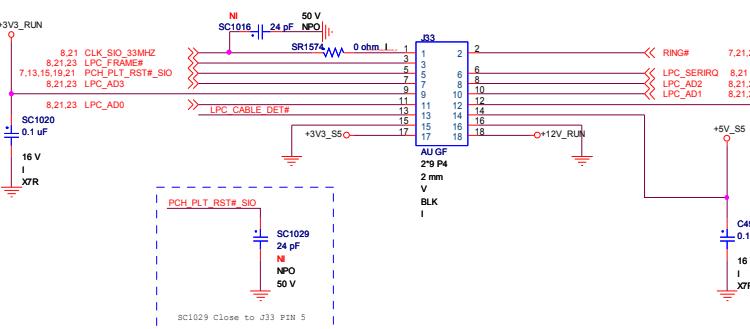
Current Mode

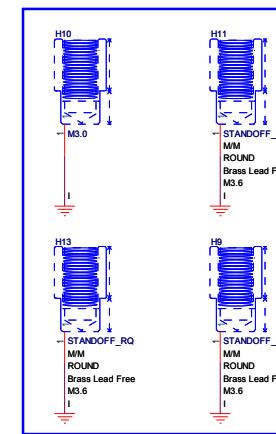
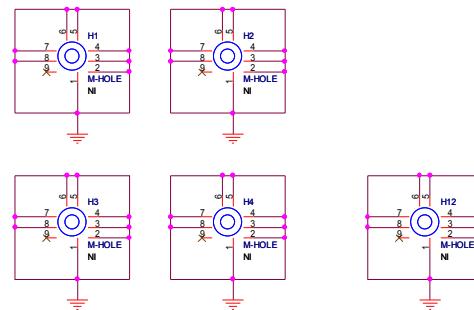
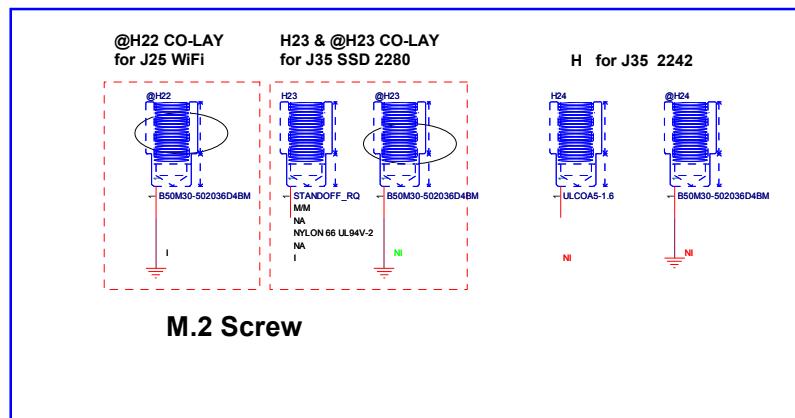
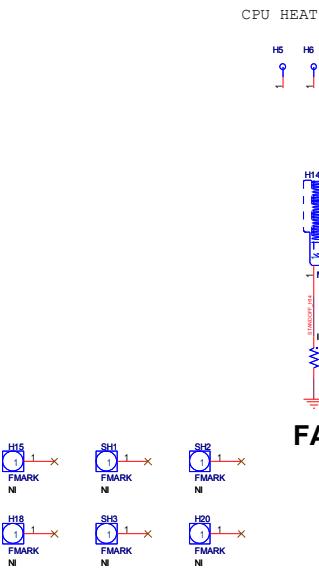


CAD NOTE : Place MLCC Close to Thermal Diode

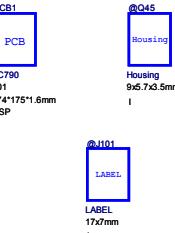
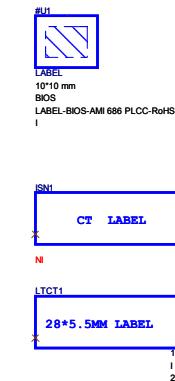
Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconductor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

Debug port





HDD Cage



Version Change List

Item	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	2016/04/20	Jasper	Source request to change	Change SU32,SU33,SU56,SU57,SU59,SU62,U104 from CA00065701NX-R to CA00082501NX-R	0.3
2.	2016/04/22	Jasper	iTE schematic review recommendation.	1.Populate SR1788. 2.Reserve LPC_SERIRQ pullup SR766. 3.SIO_PIN67 connect to OBP_PROCHOT for CPU process hot signal. 4.PSON# change pullup power from +3V3_S5 to +3V3_DSW. 5.Reserve SIO_PSON# pull-down 1K to GND. 6.Connect SIO pin25 to THERMTHIP_L_SIO for APU thermaltrip. 7.Connect SIO_SCI to APU GPIO. 8.Change LPC_FRAME RI310 to populate.	0.3
3.	2016/04/22	Jasper	USB HUB cannot separate disable USB port.	Change SU66 from GL852 to GL852G-MNY50.	0.3
4.	2016/04/26	Jasper	Lenovo request DP power need supply 2A.	Change F2/SF1/SF2 to 2A fuse and FB2/SFB29/SFB3 from 120 ohm/0.6A to 220 ohm/2A	0.3
5.	2016/04/27	Jasper	Check AMD schematic checklist v1.04	Reserve CLK_REQ1_M_2_SSD# pullup to +3V3_RUN	0.3
6.	2016/04/27	Jasper	Follow Lenovo DCLV2.7 special design item19 WOL: the wake up signal must choosed from SIO(RI) for non-intel LAN chip	Add LAN_WAKE# through R1604 to SIO RI2 for LAN WOL from G3 to S5.	0.3
7.	2016/04/28	Jasper	SMBus_MAIN have monotonic on KNOLL side	Add termination R2512/2513 on KNOLL side and SR1904/SR1905 on J1 side.	0.3
8.	2016/04/28	Jasper	Crystal Investigation report request	Change Y1 from 12M/30p to 12M/12p and SC1176 from 20pF to 12pF and SC1239 from 20pF to 15pF.	0.3
9.					
10.					

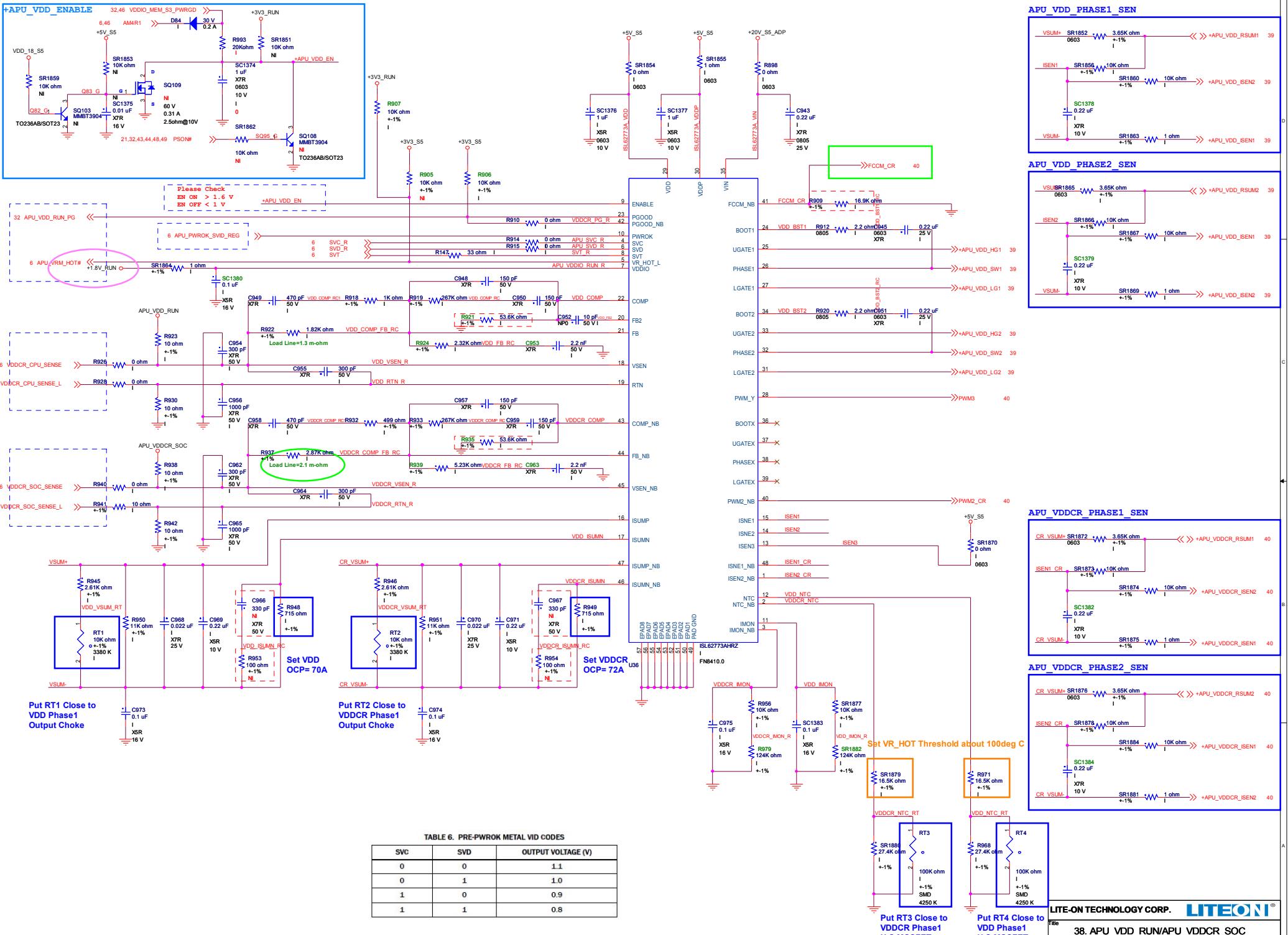


TABLE 6. PRE-PWROK METAL VID COD

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

at RT1 Close to
ID Phase1
Output Choke

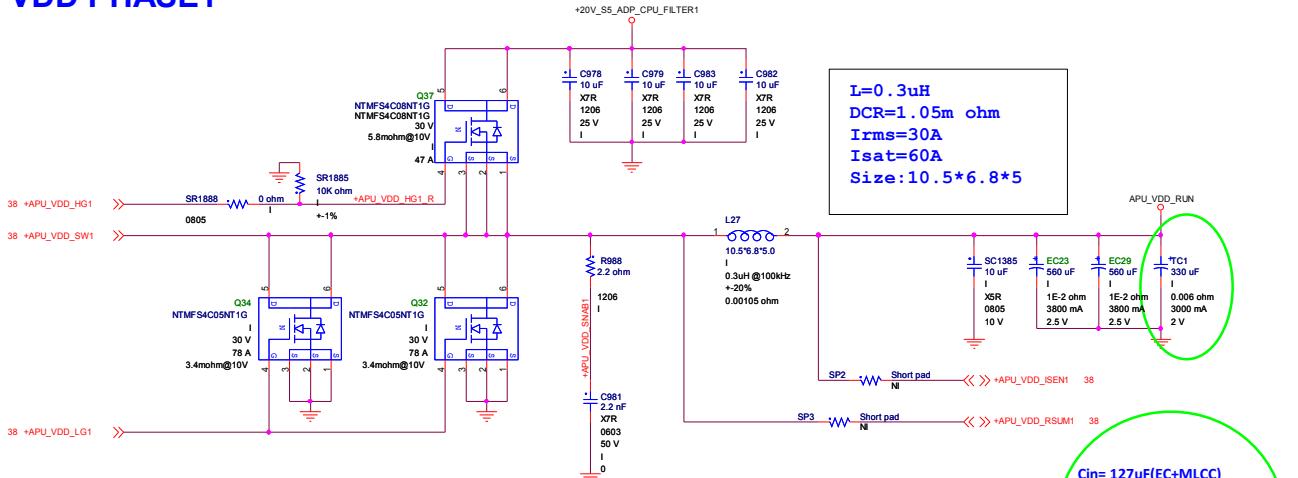
ut RT2 Close to
DDCR Phase1
utput Choke

VDD_IMON_R

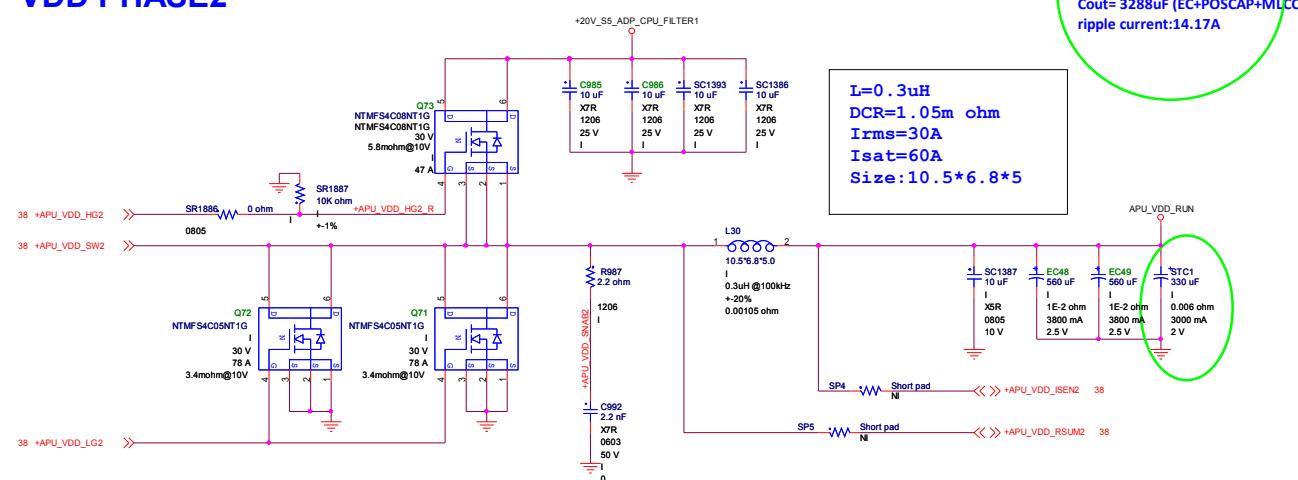
Put RT4 Close
VDD Phase1

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VDD PHASE1



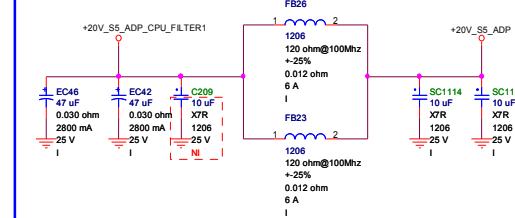
VDD PHASE2



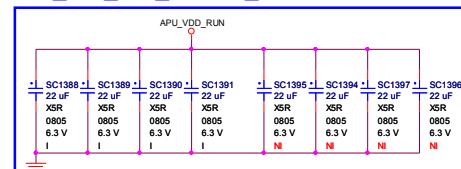
APU_VDD_RUN

TDC:39A
Imax:55A
OCP:70A
DC Load Line:1.3 mohm
Fsw:300KHz

APU_VDD_RUN_VIN_POWER

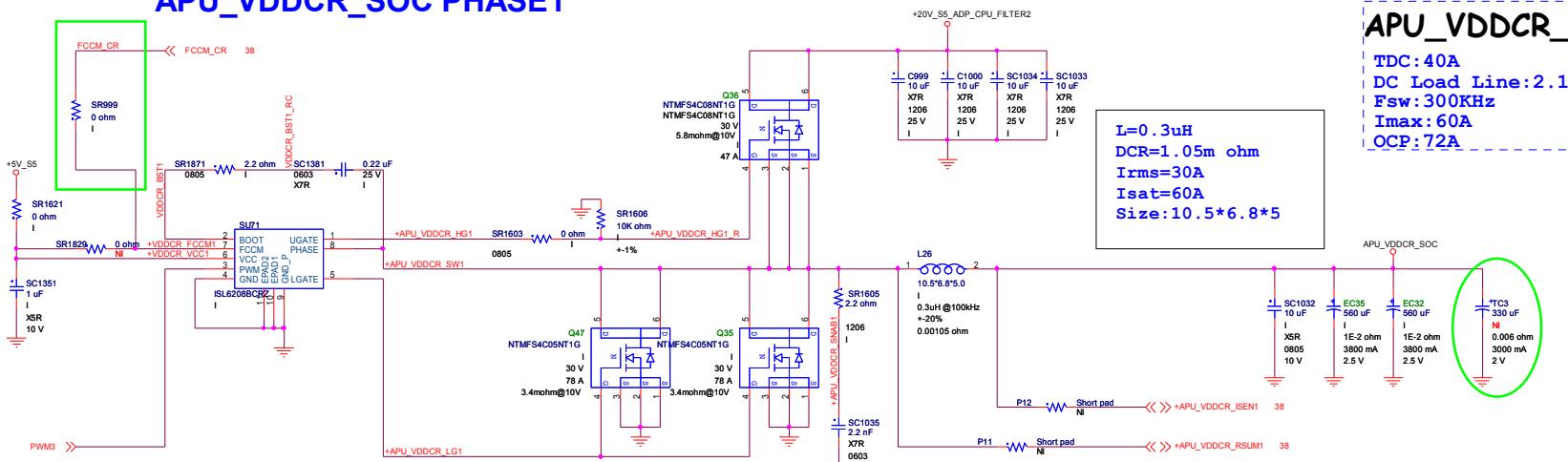


APU_VDD_RUN_Output_MLCC



MLCC ripple current(at 5 degree)= 2.49A, ESR= 4 mohm

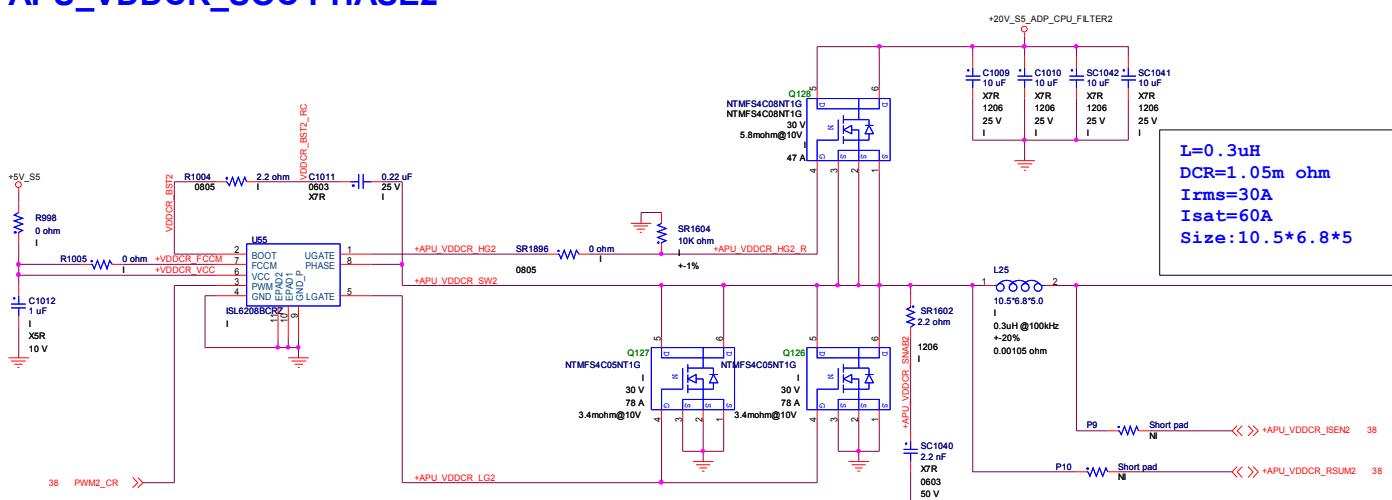
APU_VDDCR_SOC PHASE1



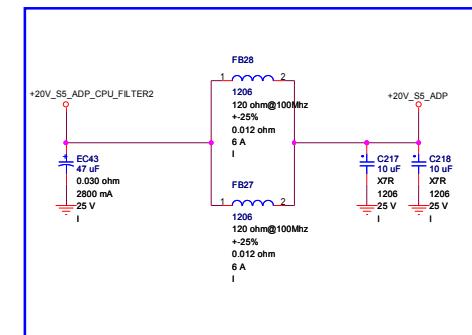
APU_VDDCR_SOC

TDC: 40A
DC Load Line: 2.1 mohm
Fsw: 300KHz
Imax: 60A
OCP: 72A

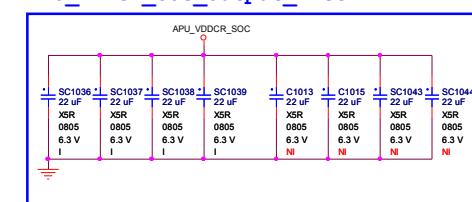
APU_VDDCR_SOC PHASE2



APU_VDDCR_SOC_VIN_POWER



APU_VDDCR_SOC_Output_MLCC



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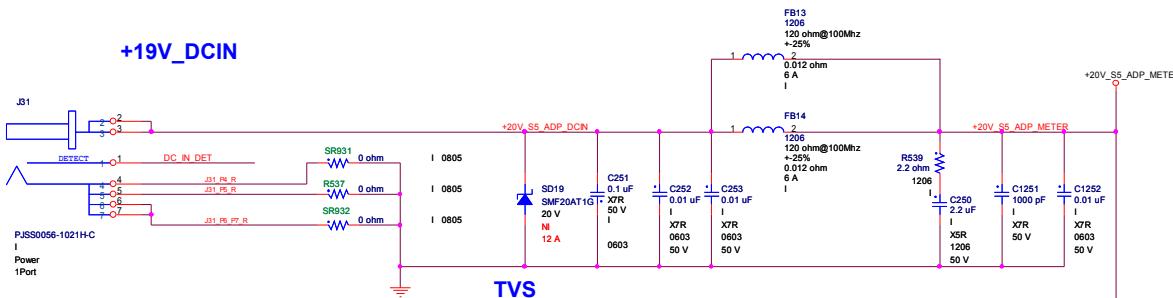
Title: 40. APU_VDDCR_SOC OUTPUT

Size: C Document Number: KC790

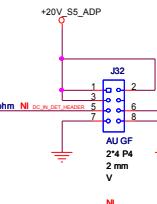
Date: Saturday, April 30, 2016 Sheet: 40 of 60

Rev X03

+19V_DCIN

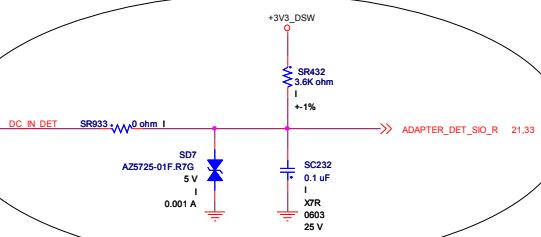


Power Header For 2L Box



TVS

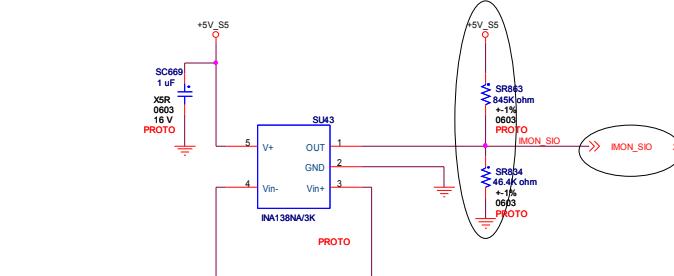
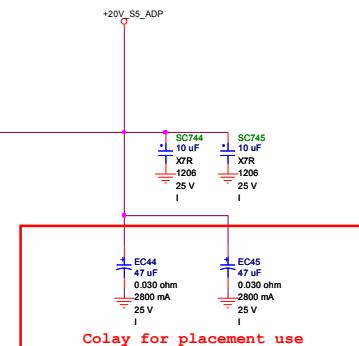
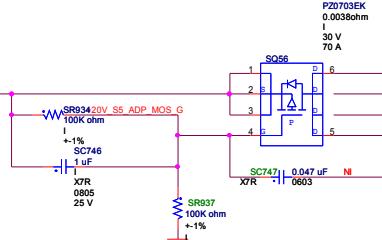
+3V_DSW



R540 0.033 ohm
I 2512



T-soft=3mS



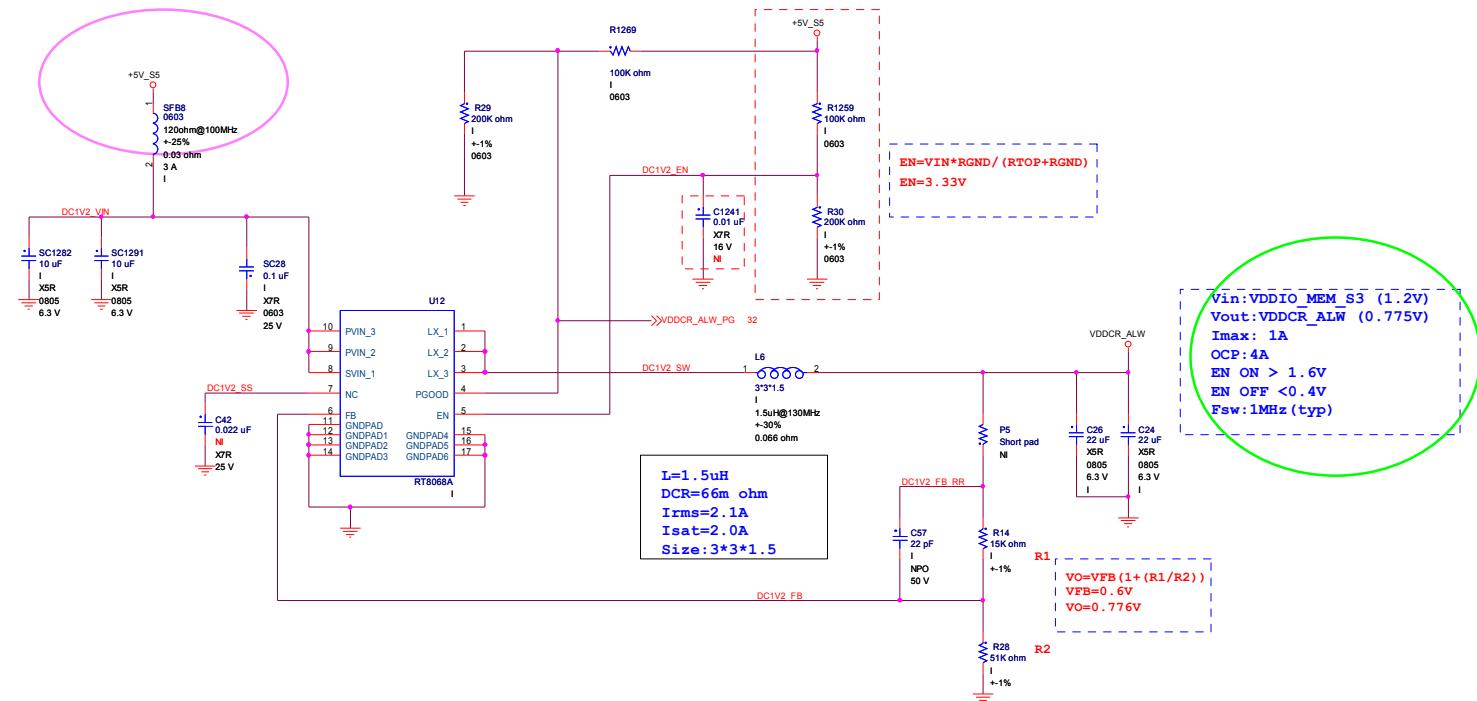
LITE-ON TECHNOLOGY CORP. **LITEONI**[®]

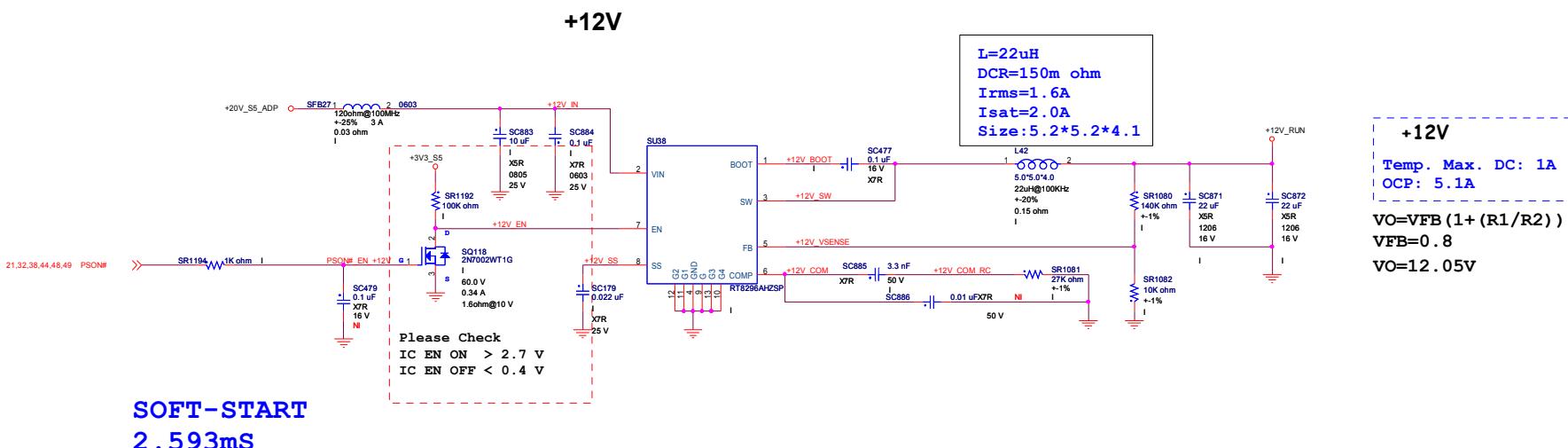
Title 41. +20V_S5_ADAP

Size C Document Number KC790

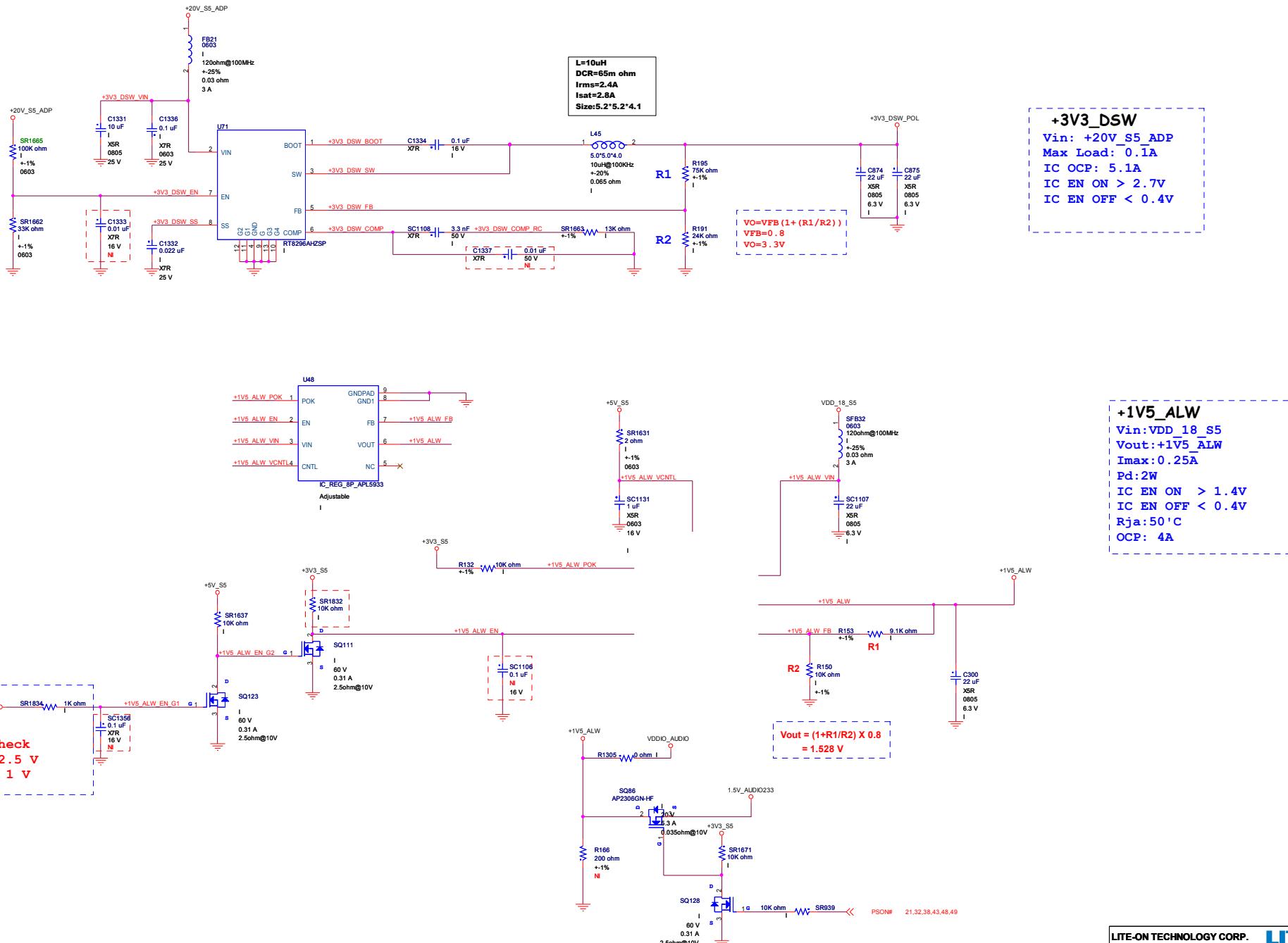
Date Saturday, April 30, 2016

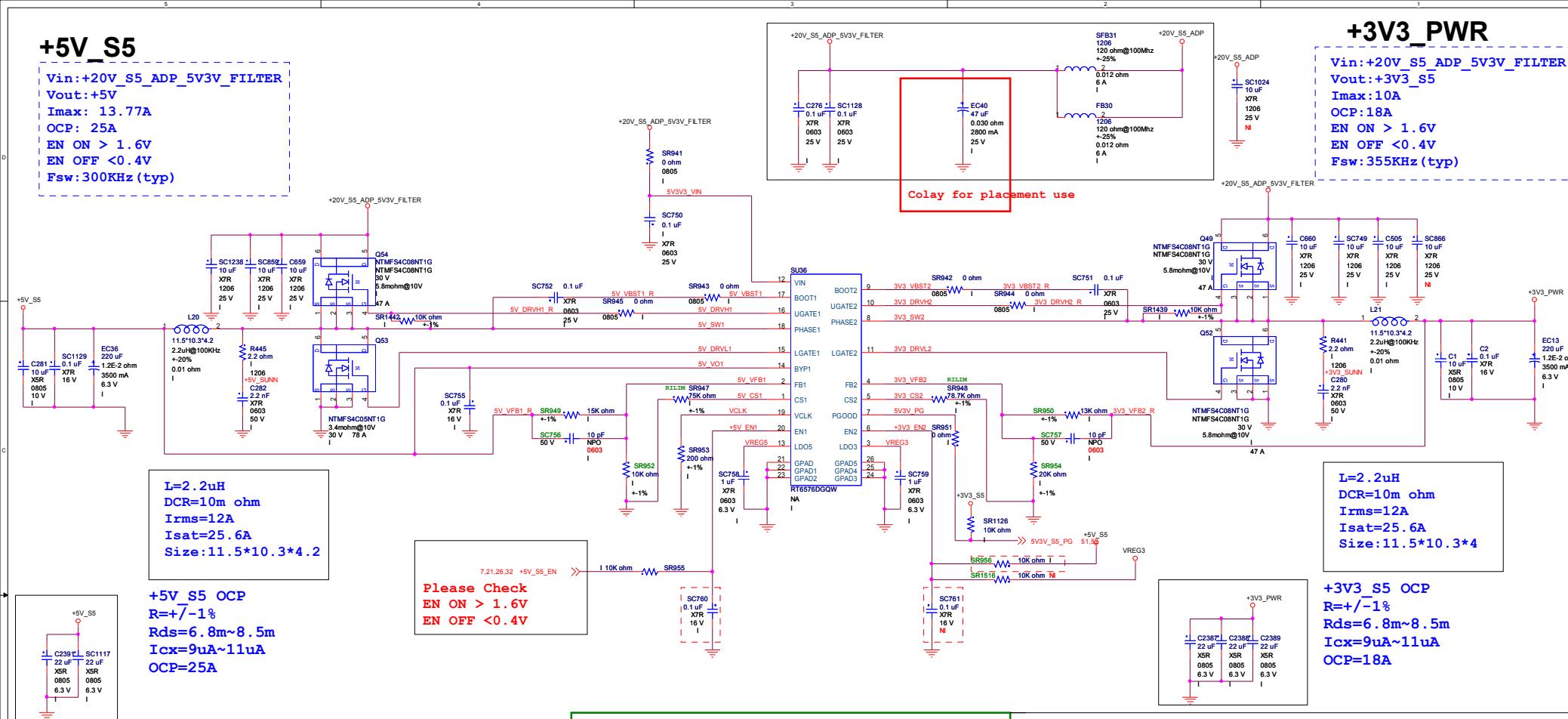
Sheet 41 of 60





SOFT-START
2.593mS





```

OCP
+3V3_S5
Rlimit=(Ilimit-ΔIL /2)*Ron*8/9uA=137K
+5V_S5
Rlimit=(Ilimit-ΔIL /2)*Ron*8/9uA=147K
    Ron=8.5m Icx=9uA R=-1%
```

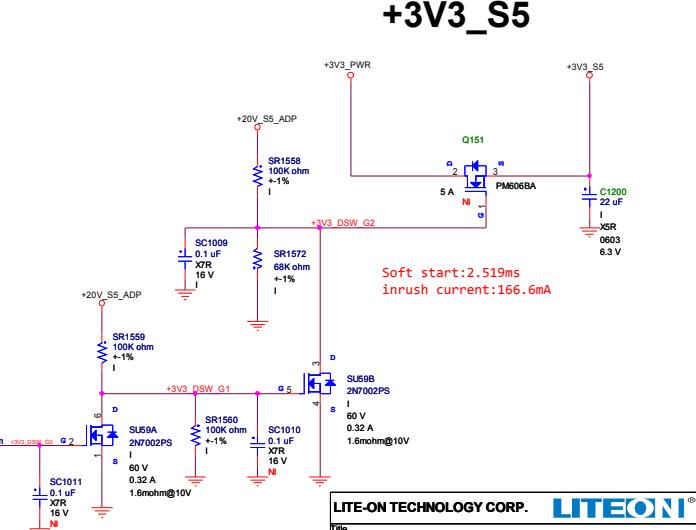
$$+3V3 \underline{S5}$$
$$\Delta IL /2 = 5.43/2 = 2.715$$

$$+5V_{S5}$$
$$\Delta IL / 2 = 5.82 / 2 = 2.91$$

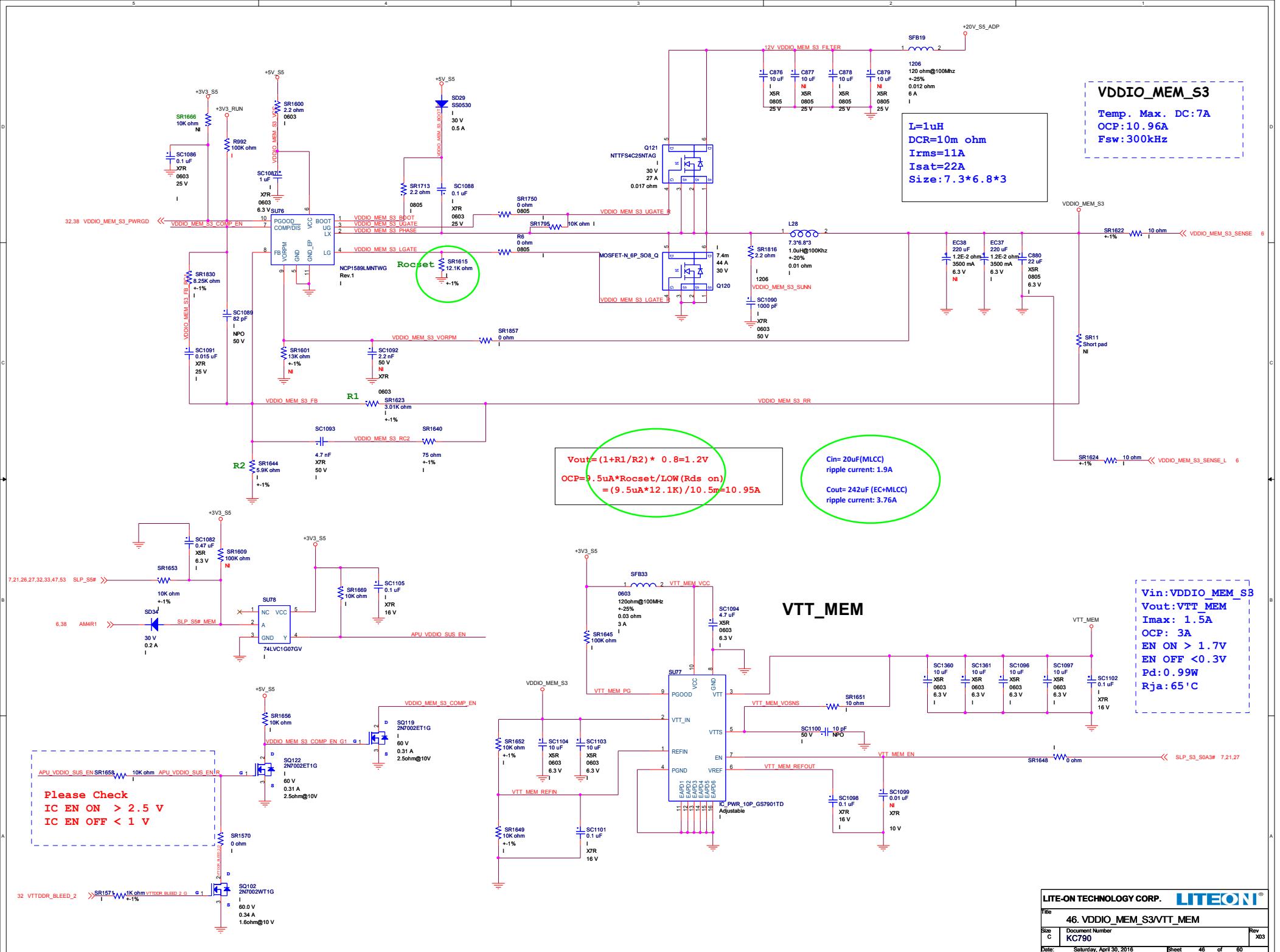
使用RT6576 (+3V3_DSW)
1.FB22-->NI
2.FB40-->NI
3.SR956-->NI
4.SP1516:SP1573.Q151:FB41-->Add

使用RT8296A (+3V3_DSW)
1. SR1516-->NI
2. FB41-->NI
3. SR1573-->NI
4. Q151-->NI
5. FB22; FB40; SR956 --> add

```
Cin=116uF  
ripple current:11.8A  
  
+5V_S5:  
Cout=220uF  
  
ripple current:3.5A  
  
+3V3_S5:  
Cout=220uF  
  
ripple current:3.5A
```



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 Be
45. +5V_S5/+3V3_S5
 Document Number KC790 Rev X03
 Date: Saturday, April 30, 2016 Sheet 45 of 60



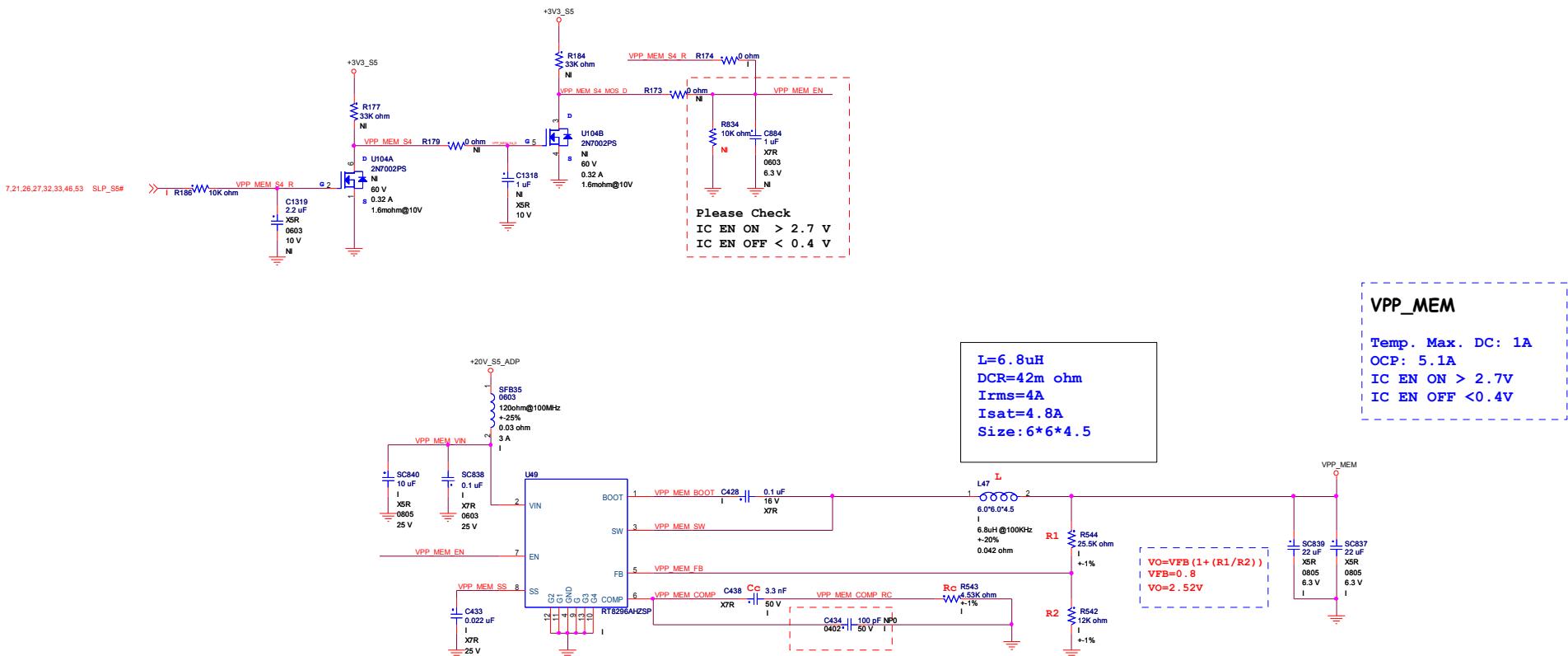
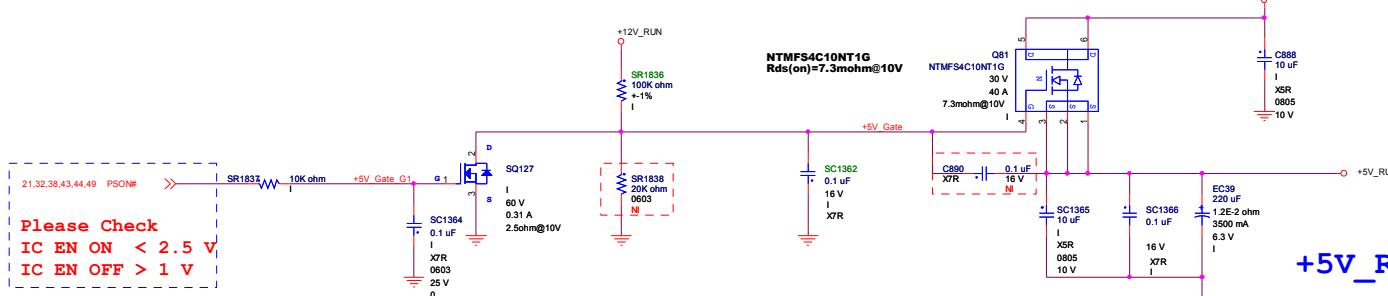


Table 1. Recommended Component Selection

V _{OUT} (V)	R ₁ (kΩ)	R ₂ (kΩ)	R _C (kΩ)	C _C (nF)	L(μH)	C _{OUT} (μF)
8	27	3	33	3.3	22	22 x 2
5	62	11.8	20	3.3	15	22 x 2
3.3	75	24	13	3.3	10	22 x 2
2.5	25.5	12	9.1	3.3	6.8	22 x 2
1.5	10.5	12	5.6	3.3	3.6	22 x 2
1.2	12	24	4.3	3.3	3.6	22 x 2
1	3	12	3.6	3.3	2	22 x 2

+5V_RUN

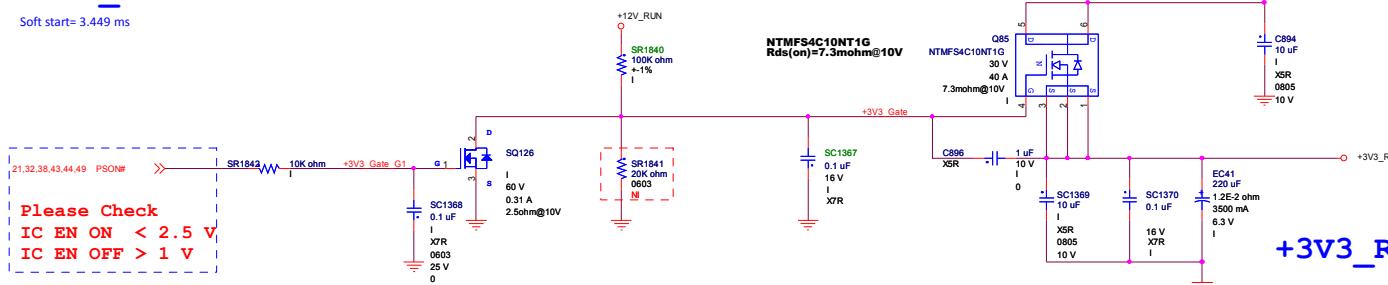
Soft start= 5.835 ms



+5V_RUN @Imax 2.6A

+3V3_RUN

Soft start= 3.449 ms



+3V3_RUN @Imax 5.76A

APU_VDDP_RUN

Soft start=3.449 ms



APU_VDDP_RUN @Imax 8.5A

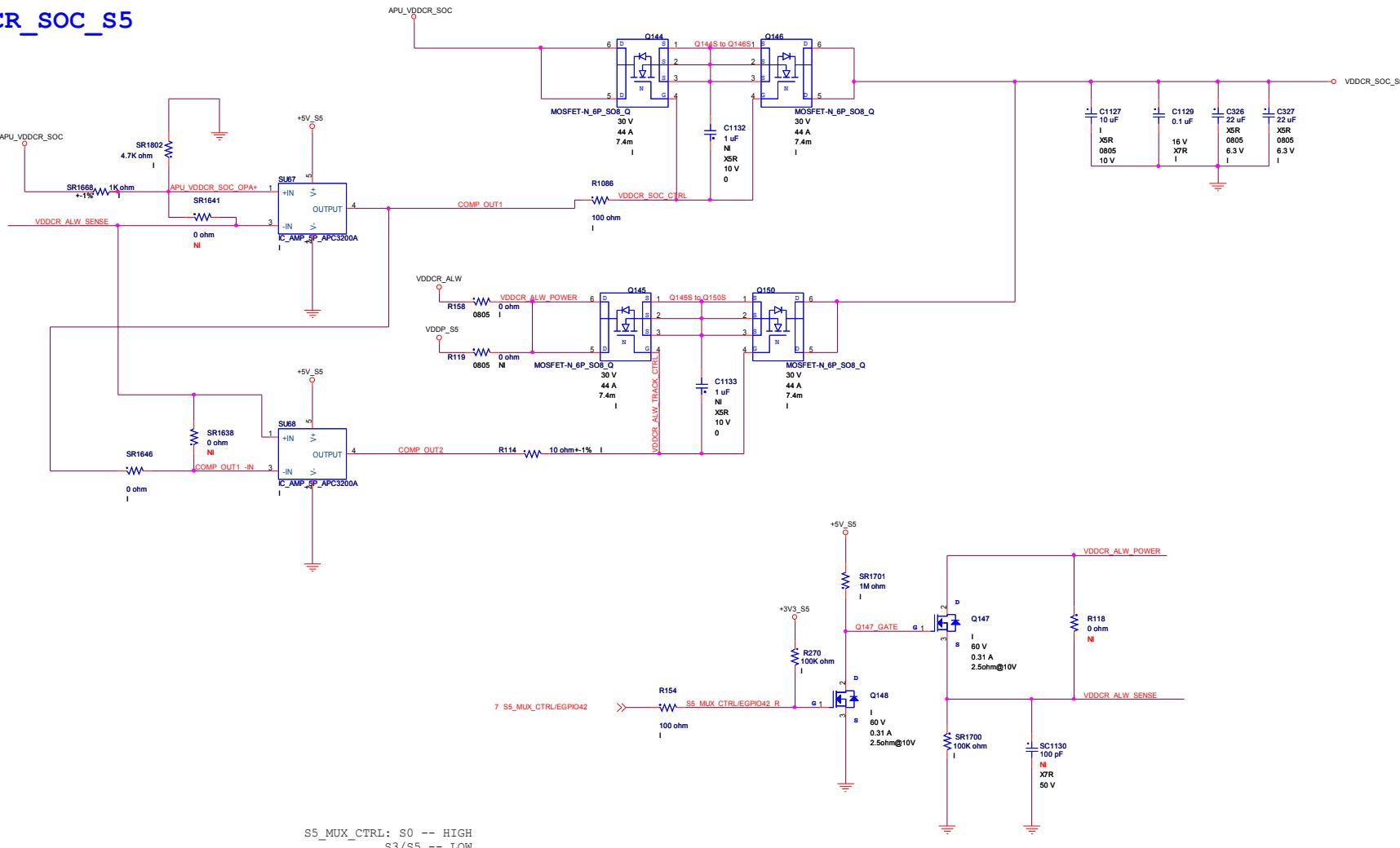
+1.8V_RUN

Soft start=3.449 ms



+1.8V_RUN @Imax 2A

VDDCR SOC S5

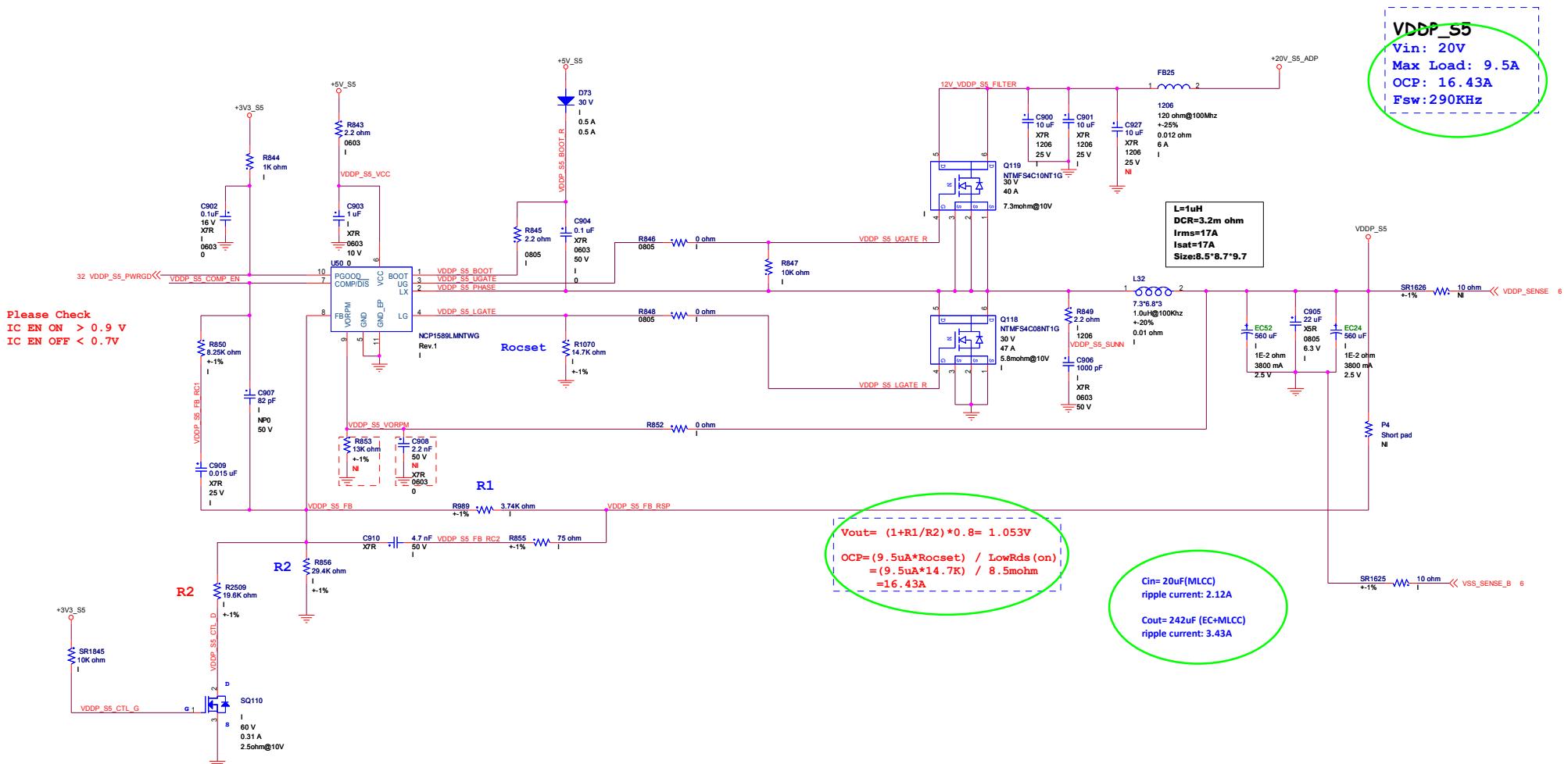


S5_MUX_CTRL: S0 -- HIGH
S3/S5 -- LOW

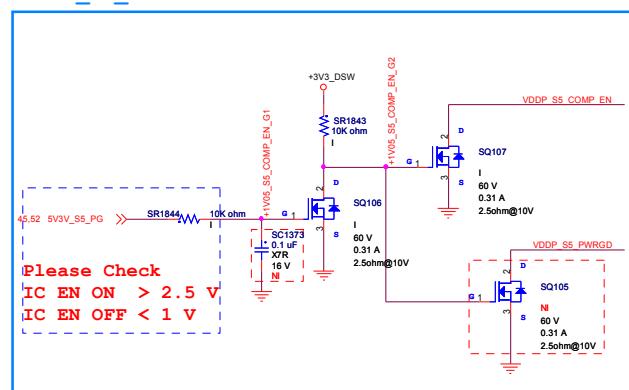
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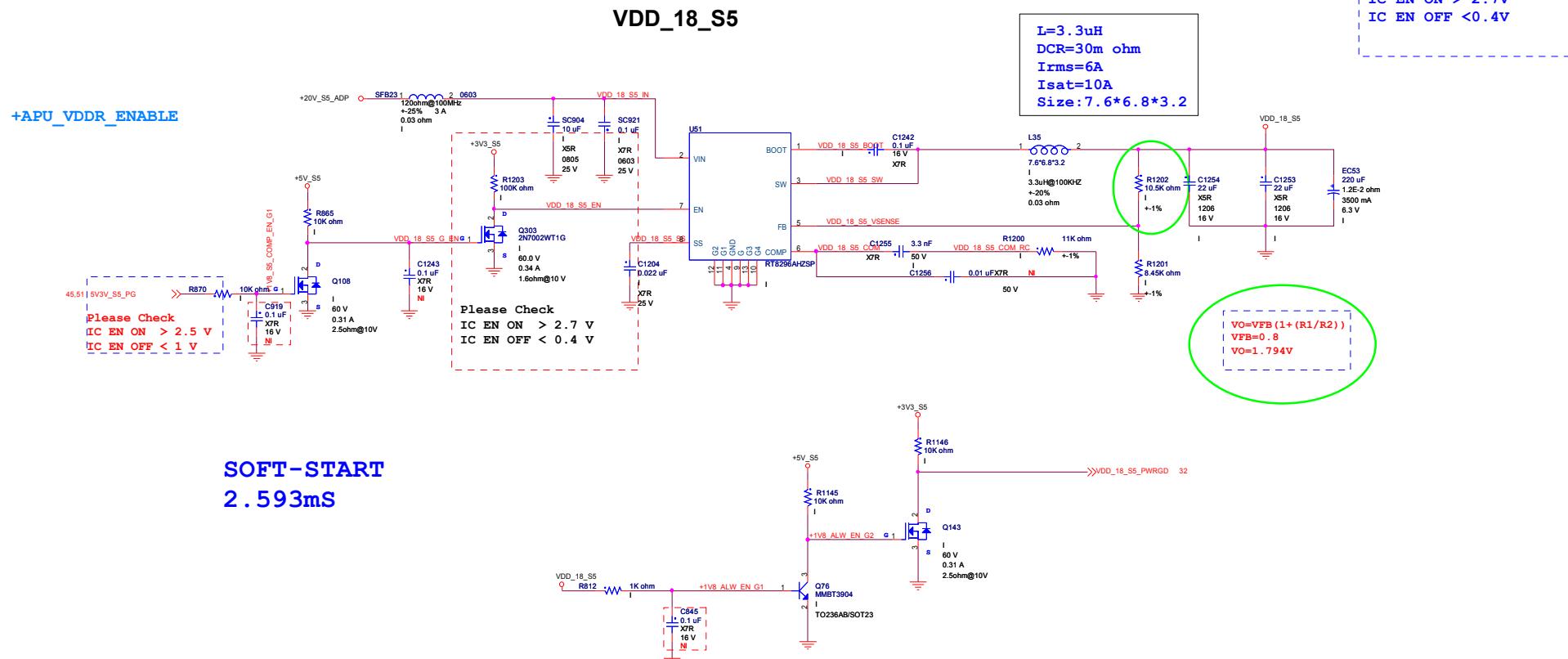
H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC < 0.775V (OR 0.85V), VDDCR_SOC_S5 = 0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

```



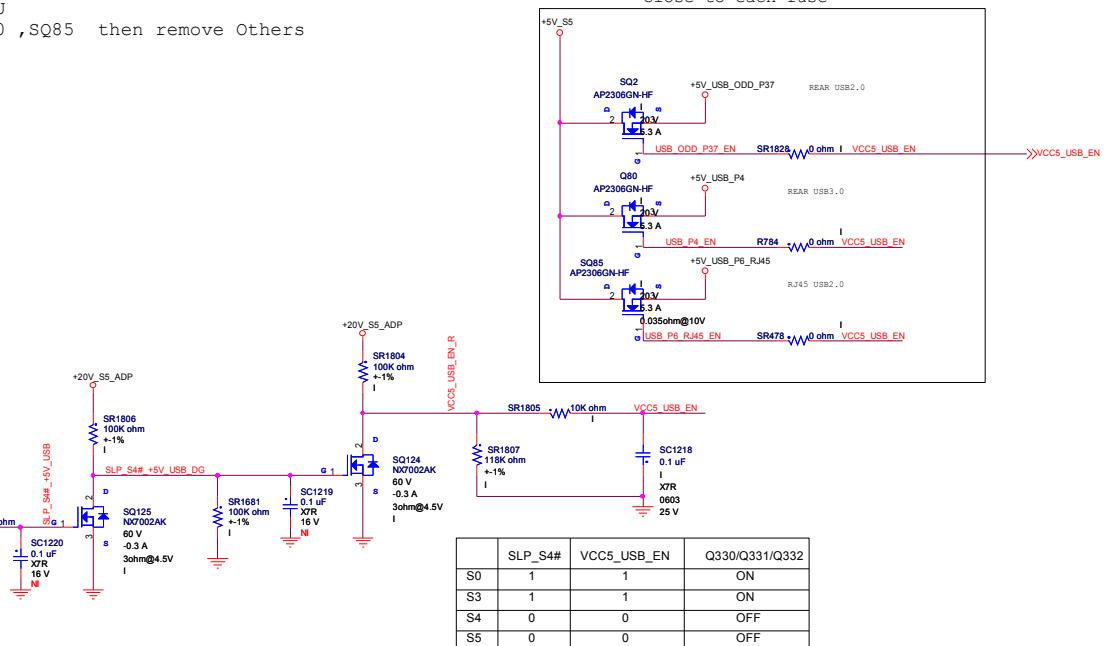
+1V05 S5 ENABLE





For Google SKU
Keep Q79, Q80, SQ85 then remove Others

+5V_USB



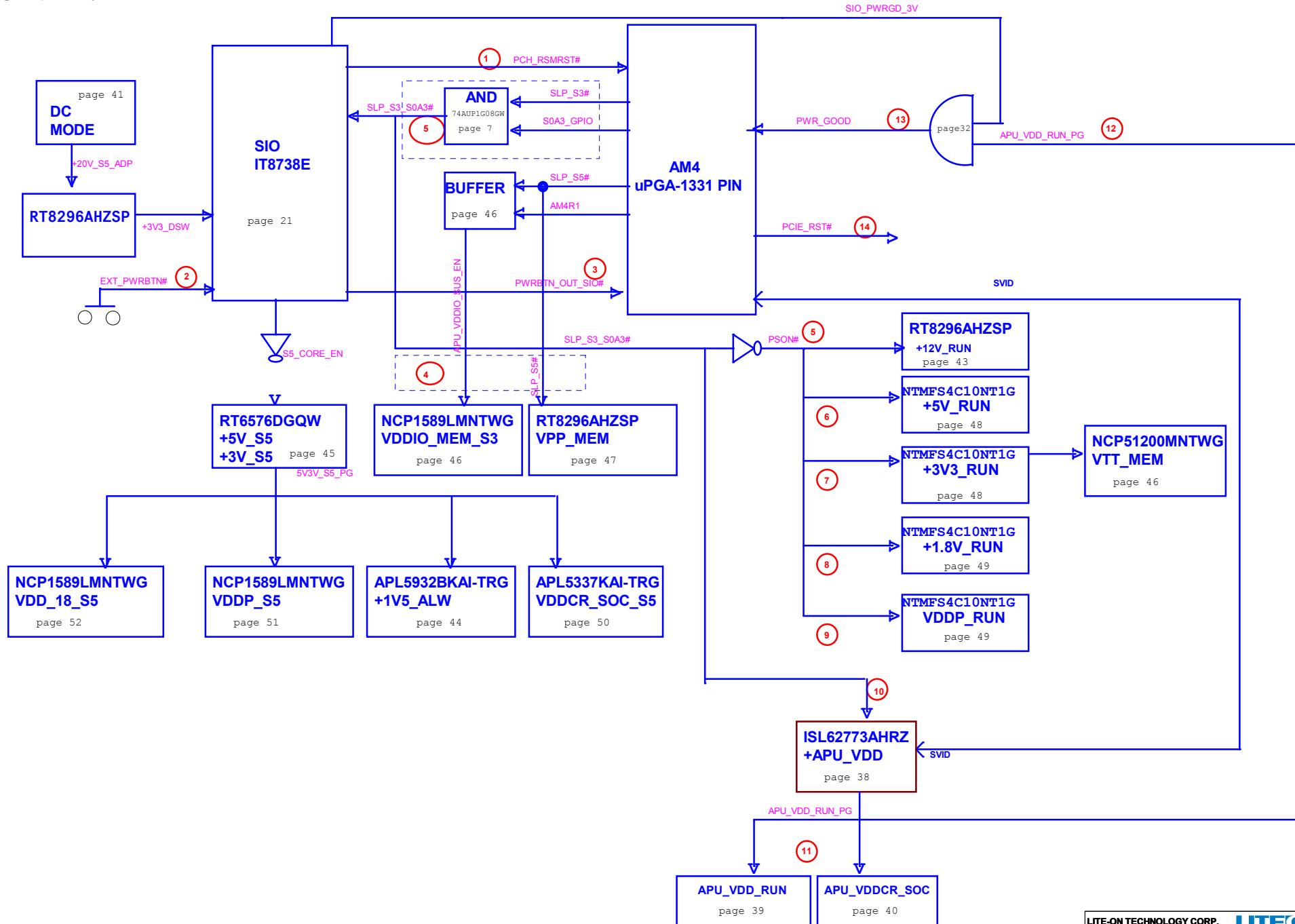
	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5\ resume) (DEFAULT)	SPI ROM (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLE (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic	LPC ROM	LPC ROM	short reset mode	Use 100Mhz PCIE clock as reference clock and generate internal clocks only
CZ/ST DIE ONLY							ZP DIE ONLY

AM4 GPIO TABLE

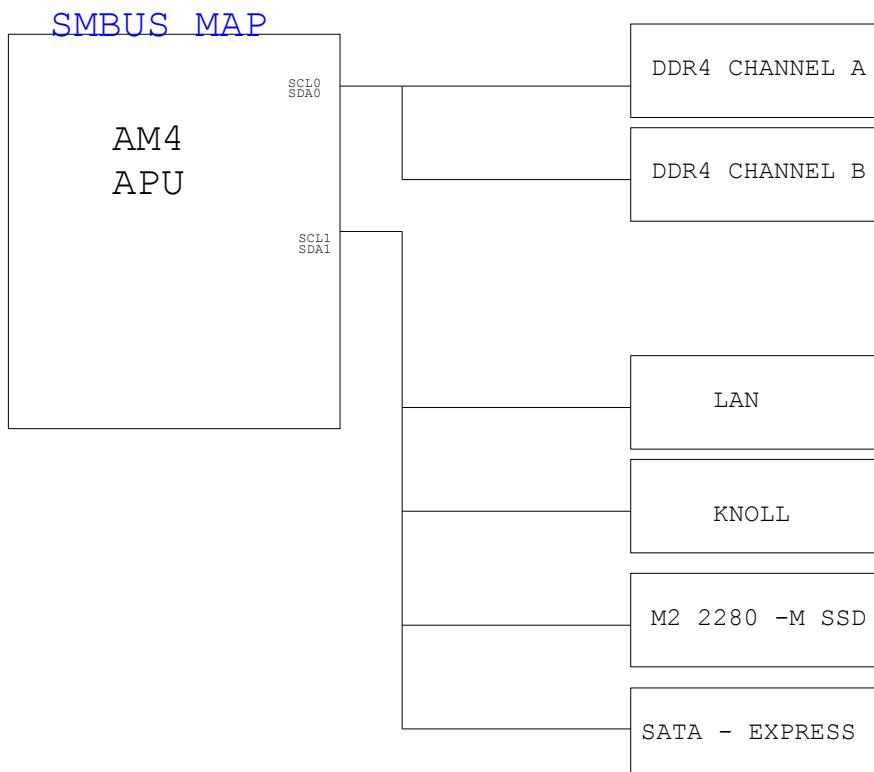
GPIO	Signal Name	Power Domain	Pin Type	Default State at Power-Up	ACTIVE H/L	Integrated Resistor	Default Function at Power-Up	KC700
AGPIO00	PWR_BTN_L/AGPIO00	S5	IN/OUT	Input	---	INT / HIGH	PWR_BTN_L	PWR_BTN#
AGPIO01	SYS_RESET_L/AGPIO01	S5	IN/OUT	Input	---	INT / HIGH	SYS_RESET_L	SYS_RESET#
AGPIO02	WAKE_L/AGPIO02	S5	IN/OUT	Input	---	INT / HIGH	WAKE_L	PCIE_WAKE#
AGPIO03	AGPIO03	S5	IN/OUT	Input	---	INT / HIGH	AGPIO03	APU_GPIO_03#
AGPIO05	AGPIO05	S5	IN/OUT	Input	---	INT / HIGH	AGPIO05	M2_WLAN_DISABLE#
AGPIO10	SOA3_GPIOAGPIO10/	S5	IN/OUT	Output	---	INT / HIGH	SOA3_GPIO	SOA3_GPIO
AGPIO11	SOPI00_CLK/BLINK/AGPIO11	S5	IN/OUT	Input	---	INT / HIGH	AGPIO11	PWR_LED#
AGPIO40	SOPI00_DATAIN/MIO0_SDA	S5	IN/OUT	Input	---	INT / HIGH	AGPIO40	SW_CLR_CMOS#
AGPIO09	AGPIO09/	S5	IN/OUT	Input	---	INT / HIGH	AGPIO09	AGPIO09/SGPIO0
AGPIO04	AGPIO04	S5	IN/OUT	Input	---	INT / HIGH	AGPIO04	GPIO4
AGPIO16	USB_CCO_L/AGPIO16	S5	IN/OUT	Input	---	INT / HIGH	USB_CCO_L	USB_OC_REAR_J21#
AGPIO17	USB_OCI_UTDII/	S5	IN/OUT	Input	---	INT / HIGH	USB_OCI_L	USB_OC_FRONT_J22#
AGPIO18	USB_OCI2_UTCK/	S5	IN/OUT	Input	---	INT / HIGH	USB_OC2_L	USB_OC_FRONT_J23#
AGPIO19	SC1I2C3_SCL/AGPIO19	S5	Open-Drain	Input	---	-	SC1I	SMB_CLK_SECOND
AGPIO21	LPC_I2C1_L/AGPIO21	S5	In/Out	Output	---	-	LPC_PDI_L	TPM_LPC_PDI#
AGPIO22	LPC_PME_L/AGPIO22	S5	In/Out	Input	---	INT / HIGH	LPC_PME	SIO_PME#
AGPIO23	AGPIO23/	S5	In/Out	Input	---	INT / HIGH	AGPIO23	DP_D_DET#_R
AGPIO24	AGPIO24/	S5	In/Out	Input	---	INT / HIGH	-	NA
AGPIO76	SPI_TPM_CS_L/AGPIO76	S0	In/Out	Input	-	SPI_TPM_CS_L	SPI_TPM_CS_L	
AGPIO84	FANIN0/AGPIO84	S0	In/Out	Input	INT / HIGH	FANIN0	HUB2_AMBER3_R	
AGPIO85	FANOUT0/AGPIO85	S0	In/Out	Input	INT / HIGH	AGPIO85	HUB2_AMBER4_R	
AGPIO86	AGPIO86	S0	In/Out	Input	INT / HIGH	AGPIO86	LPC_CABLE_DET2#	
AGPIO87	SERIRQ/AGPIO87	S0	In/Out	Input	INT / HIGH	SERIRQ	LPC_SERIRQ	
AGPIO88	LPC_CLKRUN_L/AGPIO88	S0	In/Out	Output	INT / HIGH	LPC_CLKRUN_L	LPC_CLKRUN#	
AGPIO90	GENINT2_L/AGPIO90	S0	In/Out	Input	INT / HIGH	GENINT2_L	TPM_SPI_I2C#	
AGPIO91	SPKR/AGPIO91	S0	In/Out	Input	INT / LOW	AGPIO91	APU_SPKR	
AGPIO92	CLK_REG0_L/SATA_ISQ_L/SATA_ZP0_L/AGPIO92	S0	In/Out	Input	-	CLK_REG0_L	CLK_REG1_M2_WLAN#	
AGPIO115	CLK_REG1_L/AGPIO115	S0	In/Out	Input	INT / HIGH	CLK_REG1_L	CLK_REG1_M2_SSD#	
AGPIO116	CLK_REG02_L/AGPIO116	S0	In/Out	Input	INT / HIGH	CLK_REG02_L	LOM_CLK_REG#	
AGPIO130	SATA_ACT_L/AGPIO130	S0	Open-Drain	Input	-	SATA_ACT_L	APU_HD_LED_OUT#	
EGPIO								
EGPIO26	PCIE_RST_L/EGPIO26	S5	In/Out	Output	-	PCIE_RST_L	PCIE_RST#_R	
EGPIO42	S5_MUX_CTRL/EGPIO42	S5	In/Out	Output	-	S5_MUX_CTRL	S5_MUX_CTRL/EGPIO42	
AGPIO05	AGPIO05/DEVSLP0	S5	In/Out	Input	-	AGPIO05	AGPIO05/DEVS LP0	
EGPIO74	LPCCLK0/EGPIO74	S5	In/Out	Output	-	LPCCLK0	CLK_SIO_33MHZ	
EGPIO75	LPCCLK1/EGPIO75	S0	In/Out	Output	-	LPCCLK1	CLK_SIO_33MHZ	
EGPIO70	EGPIO70	S0	In/Out	Input	INT / LOW	EGPIO70	EGPIO70	
EGPIO95	EGPIO95	S0	In/Out	Input	INT / LOW	EGPIO95	EGPIO95	
EGPIO96	EGPIO96	S0	In/Out	Input	INT / LOW	EGPIO96	NA	
EGPIO97	EGPIO97	S0	In/Out	Input	INT / LOW	EGPIO97	DP1_DP_HDMI#	
EGPIO98	EGPIO98	S0	In/Out	Input	INT / LOW	EGPIO98	DP2_DP_HDMI#	
EGPIO99	EGPIO99	S0	In/Out	Input	INT / LOW	EGPIO99	DP3_DP_HDMI#	
EGPIO100	EGPIO100	S0	In/Out	Input	INT / LOW	EGPIO100	COM_AB_DET#	
AGPIO108	AGPIO108	S0	In/Out	Input	INT / LOW	AGPIO108	LPC_CABLE_DET2#	
EGPIO113	SC1I2C2_SCL/EGPIO113	S0	Open-Drain	Input	INT / HIGH	SC1I	SMB_CLK_MAIN	
EGPIO114	SDI0I2C2_SDA/EGPIO114	S0	Open-Drain	Input	INT / HIGH	SDA0	SMB_DATA_MAIN	
EGPIO117	SPI_LKIESPI_CLK/EGPIO117	S0	In/Out	Input	INT / LOW	ESPI_CLK	SPI_CLK_APUs	
EGPIO118	SPI_CS1_L/EGPIO118	S0	In/Out	Input	-	SPI_CS1_L	SPI_CS0_OUT#_APU	
EGPIO119	SPI_CS2_L/EGPIO119	S0	In/Out	Input	-	SPI_CS2_L	SPI_CS2_OUT#	
EGPIO120	SPI_DIESPI_DAT1/EGPIO120	S0	In/Out	Input	INT / LOW	SPI_DI	SPI_MISO_APUs	
EGPIO121	SPI_DIESPI_DAT0/EGPIO121	S0	In/Out	Input	INT / LOW	SPI_DO	SPI_MOSI_APUs	
EGPIO122	SPI_WP_L/EGPIO122	S0	In/Out	Input	INT / HIGH	EGPIO122	SPI_WP#_APU	
EGPIO131	CLK_REG03_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131	S0	In/Out	Input	-	CLK_REG03_L	LPC_CABLE_DET1#	
EGPIO132	CLK_REG05_L/OSCIN/EGPIO132	S0	Input	Input	-	CLK_REG05_L	NA	
EGPIO133	SPI_DAT3/EGPIO133	S0	In/Out	Input	INT / HIGH	EGPIO133	SPI_HOLD#_APU	
EGPIO104	LA00/EGPIO104	S0	In/Out	Input	INT / LOW	LA00	LPC_A0	
EGPIO105	LA01/EGPIO105	S0	In/Out	Input	INT / LOW	LA01	LPC_A1	
EGPIO106	LA02/EGPIO106	S0	In/Out	Input	INT / LOW	LA02	LPC_A2	
EGPIO107	LA03/EGPIO107	S0	In/Out	Input	INT / LOW	LA03	LPC_A3	
EGPIO108	LDRO0_L/EGPIO108	S0	Input	Input	INT / LOW	LDRO0_L	LPC_DRO0#	
EGPIO109	LFRAME_L/EGPIO109	S0	In/Out	Output	-	LFRAME_L	LPC_FRAME#	

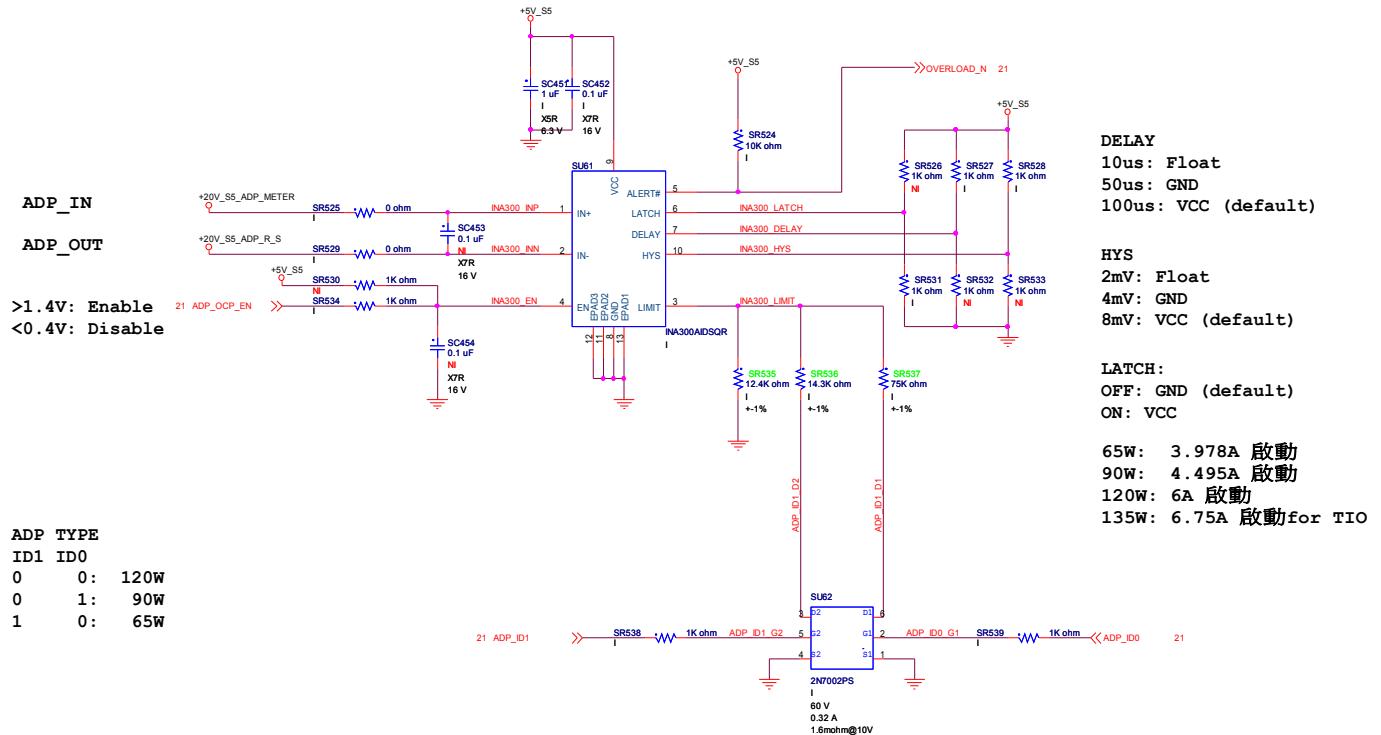
IT8730B/DX						
GPIO/Pin Num	Signal Name	KC790	Function_1	Function_2	Function_3	Function_4
GPIO10(78)	PCRS1T3#GP10	PCRS1T3	PCRS1T#(D0D08/VCC3)	GP1#(D0D08/3VSB)		
GPIO11(32)	PCRS1T2#GP11	+19V_VN_CTL_SIO	PCRS1T#(D0D08/VCC3)	GP1#(D0D08/3VSB)		
GPIO12(31)	PCRS1T#(PCH_D1)GP12	NA	PCRS1T#(D0D08/VCC3)	PCH_D1#(D0D08/VCC3)	GP1#(D0D08/3VSB)	
GPIO13(30)	PVROK1#GP13	SO_PVROK_3V	PVROK1#(D0D08/CC3)	GP1#(D0D08/3VSB)		
GPIO14(29)	VCORE_EN#(PCH_C1)GP14	NA	VCORE_EN#(D0D08/VCC3)	PCH_C1#(D0D08/VCC3)	GP1#(D0D08/3VSB)	
GPIO15(3)	PCRS1T#(CRT2#GP15)CRU_PG	PCRS1T	PCRS1T#(D0D08/VCC3)	CRT2#(D0D08/3VSB)	GP1#(D0D08/3VSB)	CPU_PG#(D0D08)
GPIO16(20)	SVSB_CTRL#(RRK2#GP16)	SVSB_CTRL	SVSB_CTRL#(D0D08/VSB)	DTR8#(D0D08/VCC3)	GP1#(D0D08/3VSB)	
GPIO17(26)	R2#GP17	R2#GP17	R2#GP17#(V3S)	GP1#(D0D08/3VSB)		
GPIO20(25)	CTSA#GP20	NA	GP2#(D0D08/VSB)	CTS2#(D0D08/VCC3)		
GPIO21(24)	DDCD#GP21	OVERLOAD_N_R	GP2#(D0D08/VSB)	DCD2#(D0D08/VCC3)		
GPIO22(23)	SCKG#GP22	SDI_SCK_R	SDI#(D0D08/VSB)	GP2#(D0D08/3VSB)		
GPIO23(22)	SWGP23	SDI_SD	SDI#(D0D08/VSB)	GP2#(D0D08/3VSB)		
GPIO24(21)	RTS2#GP24	NA	GP2#(D0D08/VSB)	RTS2#(D0D08/VCC3)		
GPIO25(20)	DSR2#GP25	NA	GP2#(D0D08/VSB)	DSR2#(D0D08/VCC3)		
GPIO26(19)	SOUT2#GP26	SOUTA	GP2#(D0D08/VSB)	SOUT2#(D0D08/VCC3)		
GPIO27(18)	SN#GP24	SNA	GP2#(D0D08/VSB)	SN#(D0D08/VCC3)		
GPIO30(17)	ATXP#GP30	PVRCG_P5	ATXP#(D0D08/VCC3)	GP3#(D0D08/3VSB)		
GPIO31(16)	PWMOUT#GP10#SPBVREN2#	SDI_CH2_USBPIREN	PWM_OUT#(D0D08/VSB)	GP3#(D0D08/3VSB)		
GPIO32(15)	DPW#GP32	SDI_SD2	DPW#(D0D08/VSB)	GP3#(D0D08/3VSB)		
GPIO35(14)	FAN_TAC4#GP35	INT1_O_SD1	FAN_TAC4#(D0D08/VSB)	GP3#(D0D08/3VSB)		
GPIO36(13)	FAN_CTL#GP36	NA	FAN_CTL#(D0D08/VSB)	GP3#(D0D08/3VSB)		
GPIO37(12)	FAN_TAC3#GP37	INT2_O_SD1	FAN_TAC3#(D0D08/VSB)	GP3#(D0D08/3VSB)		
GPIO40(73)	3VSB#(D0D08/VSB)F40#SC1	NA	3VSB#(D0D08/VSB)	GP4#(D0D08/3VSB)	SCL#(D0D08/A/VCC3)	
GPIO41(72)	PVRCO#GP41#SDA	NA	PVRCO#(D0D08/VSB)	GP4#(D0D08/VSB)	SDA#(D0D08/A/VCC3)	
GPIO42(70)	PSDN#GP42	SDI_PSON	PSDN#(D0D08/VSB)	GP4#(D0D08/3VSB)		
GPIO43(69)	PANSW#(H)GP43	SDI_PDI_IN	PANSW#(H)(D0D08/VSB)	GP4#(D0D08/3VSB)		
GPIO44(66)	PVRCM#GP44	SDI_PWRBTN_OUT#	PVRCM#(D0D08/VSB)	GP4#(D0D08/3VSB)		
GPIO45(65)	SUS#GP45	SDI_SUP_S3#	SUS#(D0D08/VSB)	GP4#(D0D08/3VSB)		
GPIO50(46)	SDGP50	SDI_SD73	SD#(D0D08/VSB)	GP5#(D0D08/3VSB)		
GPIO51(11)	FAN_CTL#GP51	SDI_PR11	FAN_CTL#(D0D08/VSB)	GP5#(D0D08/3VSB)		
GPIO52(10)	FAN_TAC#GP52	SP1_SEL	FAN_TAC#(D0D08/VSB)	GP5#(D0D08/3VSB)		
GPIO53(71)	SUS#GP53	SDI_SLP_S4#	SUS#(D0D08/VSB)	GP5#(D0D08/3VSB)		
GPIO54(87)	PME#(D0D08/VSB)VREN1#	SDI_PR67	PME#(D0D08/VSB)	GP5#(D0D08/3VSB)	USBPVREN1#(D0D08/3VSB)	
GPIO55(79)	RSWRST#(CRX1#GP55)	RSWRST_SD4	RSWRST#(D0D08/VSB)	CRX1#(D0D08/VSB)	GP5#(D0D08/3VSB)	
GPIO56(77)	MCLK#GP56	MCLK#(D0D08/VSB)	MCLK#(D0D024/VSB)	GP5#(D0D024/3VSB)		
GPIO57(76)	MDAT#GP57	MDAT#(D0D08/VSB)	MDAT#(D0D024/VSB)	GP5#(D0D024/3VSB)		
GPIO59(75)	KCLKG#GP60	KCLKG#(D0D08/VSB)	KCLKG#(D0D024/VSB)	GP6#(D0D024/3VSB)		
GPIO61(74)	KDAT#GP61	KDAT#(D0D08/VSB)	KDAT#(D0D024/VSB)	GP6#(D0D024/3VSB)		
GPIO62(43)	KRST#GP62	KRST#	KRST#(D0D08/VCC3)	GP6#(D0D08/3VSB)		
GPIO63(6)	VLDT_EN#GP63	NA	VLDT_EN#(D0D08/VSB)	GP6#(D0D08/3VSB)		
GPIO65(119)	SM8CLK4#GP65	NA	SM8CLK4#(D0D024/VSB)	GP6#(D0D024/3VSB)		
GPIO66(120)	SMBDAT4#GP66	NA	SMBDAT4#(D0D024/VSB)	GP6#(D0D024/3VSB)		
GPIO67(121)	FAN_CTL#GP67	SDI_PRN121	FAN_CTL#(D0D08/VSB)	GP6#(D0D08/3VSB)		
GPIO70(162)	K5#(D0D08/GP70)	2541_P2_EN	GPT#(D0D0024/VSB)	K5#(D0D08/VSB)	P0#(D0D24/VCC3)	
GPIO71(103)	K5#(D0D08/GP71)	2541_CLT2_R	GPT#(D0D0024/VSB)	K5#(D0D08/VSB)	P0#(D0D24/VCC3)	
GPIO72(104)	K5#(D0D08/GP72)	2542_EU1_R	GPT#(D0D0024/VSB)	K5#(D0D08/VSB)	P0#(D0D24/VCC3)	
GPIO73(105)	K5#(D0D08/GP73)	2542_CLT1_R	GPT#(D0D0024/VSB)	K5#(D0D08/VSB)	P0#(D0D24/VCC3)	
GPIO74(106)	K5#(D0D08/GP74)	NA	GPT#(D0D0024/VSB)	K5#(D0D08/VSB)	P0#(D0D24/VCC3)	
GPIO75(107)	K5#(D0D08/GP75)	NA	GPT#(D0D0024/VSB)	K5#(D0D08/VSB)	P0#(D0D24/VCC3)	
GPIO76(108)	K5#(D0D08/GP76)	NA	GPT#(D0D0024/VSB)	K5#(D0D08/VSB)	P0#(D0D24/VCC3)	
GPIO77(109)	K5#(D0D08/GP77)	NA	GPT#(D0D0024/VSB)	K5#(D0D08/VSB)	P0#(D0D24/VCC3)	
GPIO30(94)	PE/GP99	NA	PE#(VCC3)	GP8#(D0D24/3VSB)		
GPIO31(95)	BUSY#GP981	NA	BUSY#(D0D08/VCC3)	GP8#(D0D24/3VSB)		
GPIO32(96)	ACK#GP982	NA	ACK#(D0D08/VCC3)	GP8#(D0D24/3VSB)		
GPIO33(97)	SUH#GP983	ADP_01	SUH#(D0D024/VCC3)	GP8#(D0D024/3VSB)		
GPIO34(98)	INT#GP984	ADP_00	INT#(D0D024/VCC3)	GP8#(D0D024/3VSB)		
GPIO35(58)	ID_SC#(GP85#MEDAT0)	AP5_DC_DATA	ID_SC#(D0D024/VSB)	SMBDAT#(D0D024/3VSB)		
GPIO36(57)	GP86#SMBLCK0	AP5_DC_CLK	GP86#(D0D0024/VSB)	SMBLCK#(D0D0024/VSB)		
GPIO37(99)	ERR#GP987	ADP_OOP_EN	ERR#(D0D08/VCC3)	GP87#(D0D024/3VSB)		
GPIO39(93)	SLCT#GP97	NA	SLCT#(D0D08/VCC3)	GP87#(D0D024/3VSB)		
GPIO40(122)	RTS1#(D0D08)	RTS1-	RTS1#(D0D08/VCC3)	GP88#(D0D008/3VSB)		
GPIO41(123)	DSR1#(GP81)	DSR1-	DSR1#(D0D08/VCC3)	GP81#(D0D08/3VSB)		
GPIO42(124)	SOUT#(D0D08/GP82)	SOUT1-	SOUT#(D0D08/VCC3)	D_1TX1#(D0D08/3VSB)	GP82#(D0D06/3VSB)	
GPIO43(25)	SIN#(D0D08/GP83)	SIN1-	SIN#(D0D08/VCC3)	D_1RX1#(D0D08/3VSB)	GP83#(D0D06/3VSB)	
GPIO44(126)	DTR#(D0D08/GP84)	DTR1-	DTR1#(D0D08/VCC3)	GP84#(D0D06/3VSB)		
GPIO45(127)	DCD#GP85	DCD1-	DCD1#(D0D08/VCC3)	GP85#(D0D06/3VSB)		
GPIO46(128)	R1#(GP86)	R11-	R1#(D0D08/VSB)	GP86#(D0D06/3VSB)		
GPIO87(1)	CTS1#(GP87)	CTS1-	CTS1#(D0D08/VCC3)	GP87#(D0D06/3VSB)		

MODEL NAME: Power Sequence Block Diagram
 PCB NAME: XXXXX



SMBUS Block Diagram





LITE-ON TECHNOLOGY CORP.		LITEON	
Title		59. INA300	
Size	C	Document Number	Rev X03
		KC790	
Date:	Saturday, April 30, 2016		Sheet 59 of 60

P04
1. del SC1175, SC1151.
2. SC1060, SC1180 change to 22uF

For SIT (0421)
P39
1. add R907, R905 change to NI

P38
1. R905 change to I
2. +1.5V_ALW change to +1.8V_RUN

For SIT (0427)

P39
1. L27, L29 重抓

P45
1. R947 change to 75K

P40
1. L26, L25 重抓

P44
1. U48 change to APL5933C

P42
1. VDDIO_MEM_S3 change to +5V_S5
2. del U59 circuit

P42
1. add P5

P51
1. add EC24
2. EC52 change to 560uF

For SIT (0429)

P52
1. add EC53

P39
1. TC2 => STC1
2. add EC46

For SDV

P46
1. SU77 => GS7901TD
2. Q121 => NTTFS4C25NTAG
3. Q120 => NTTFS4C10NTAG

P38
1. R921 change to 53.6K
2. R935 change to 53.6K
3. C953 change to 2.2nF
4. C963 change to 2.2nF
5. R909 change to I
6. R937 change to 2.87K

For SIT

P45
1. SC760 change to I

P46
1. R992 change to I, SR1666 change to NI
2. SC1090 change to 1nF

P47
1. C884 change to I

P52
1. R1200 change to 11K
2. R1201 change to 8.45K

P44
1. C1332 change to 0.022uF
2. SR1832 change to I

P40
1. add SR999 = 0R & connect to P38 R909

P51
1. C906 change to 1nF

P38
1. del SR1861, del SR1868
2. R909 change to 16.9K