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Application Note

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Migration Guide—P1020 and P2020 Devices

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The P2020 and P1020 devices are members of the QorIQ™ family of dual processors built on Power Architecture™ technology with integrated system logic. Both devices contain system-level support for industry-standard interfaces required for networking, telecommunications, and wireless infrastructure.

Whereas the P1020 targets lower-cost, less performance-critical applications, the P2020 targets higher-performance applications. It is the next logical step when moving on from the P1020.

The purpose of this document is to discuss the small and unique differences that exist when migrating between the two devices, from both a hardware and a software perpsective. It demonstrates that it is possible to design a single platform that supports both the P2020 and the P1020. The Px020 RDB is an example of such a platform, and it is available for end customers to use, both for hardware reference and for software development.

Please check the Freescale website at www.freescale.com for the latest versions of the P2020 and P1020 reference manuals, hardware specifications, and device errata.

Contents

1 Device Comparisons

This section provides an overview of the similarities and differences between the P1020 and P2020. Figure 1 and Figure 2 show the block diagrams for the P2020 and P1020, and Table 1 summarizes the main differences between the two devices.

The remainder of document is broken into two logical sections:

- Section 2, “Hardware Design Considerations”
- Section 3, “Software Differences”

Each section provides further details on the unique differences between the devices.

Figure 1 shows the major functional units within the P2020.

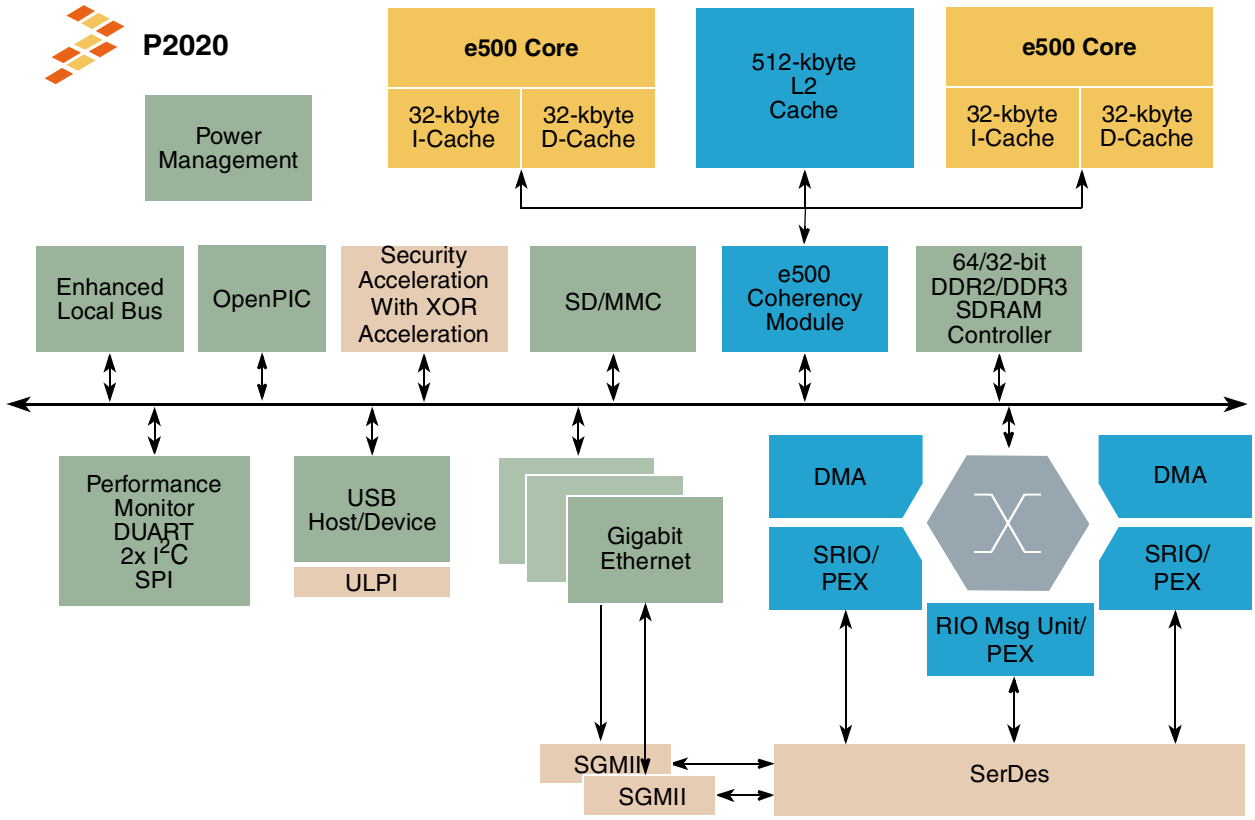

Figure 1. P2020 Block Diagram

Figure 2 shows the major functional units within the P1020.

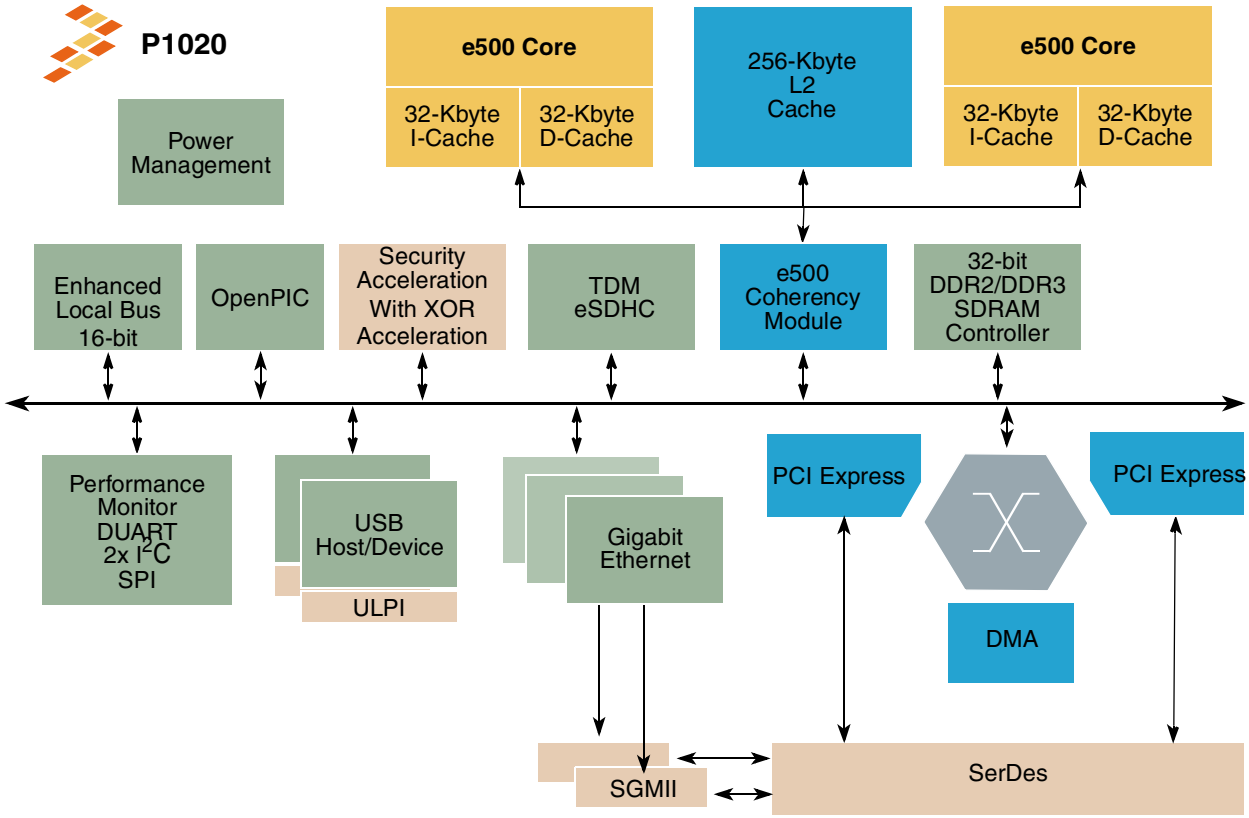

Figure 2. 1020 Block Diagram

Table 1 provides a quick summary of the main feature differences between the P2020 and the P1020 devices.

Table 1. Device Comparison Summary

Items	P2020	P1020
e500 core	same version	same version
e500 core frequency	800 MHz–1.2 GHz	333 MHz–800 MHz
L2 Cache Size	512 KB	256 KB
Platform Frequency	400–600 MHz	166 MHz–200 Mhz 266 MHz–400 MHz
No. of PCIe Express controllers	3 PCIe controllers	2 PCIe controllers
	Refer to Section 2.1, “Supported PCI Express Combinations	
DDR Interface	64-bit	32 and 16-bit
	Refer to Section 2.2, “DDR Interface.”	
Supported eTSEC configurations	Refer to Section 2.3, “Enhanced Three-Speed Ethernet Controllers.”	
Power Supply Differences	Refer to Section 2.4, “Voltage and Power Target Differences.”	

Table 1. Device Comparison Summary (continued)

Items	P2020	P1020
External SYSCLK and valid frequency combinations	33–133 MHz	33–100 Mhz
	Refer to Section 2.5, “Supported Frequencies.”	
Power Targets	< 8 W 800 MHz e500, 400 MHz platform	< 4.5 W 800 MHz e500, 400 MHz platform
Other Differences		
Individual clocking of eTSECs	No	Yes
	Refer to Section 2.7.1, “Optional Support for Second GTX_CLK125 Input.”	
TDM bus with dedicated DMA engine	No	Yes
	Refer to Section 2.7.2, “TDM Interface with Dedicated DMA.”	
Number of USBs available	1	2
	Refer to Section 2.7.3, “Second USB Port.”	
Number of Core Supply Rails	Single VDD rail for both cores	Option for two. One for each core
	Refer to Section 2.7.4, “Independent Core1 Power Rail.”	
Pin-Out	Slight differences, but a single PCB design can accommodate both devices. Refer to Section 2.8, “Signal Pin Differences.”	
POR configuration	Refer to Section 2.9, “POR Differences.”	
SRIO controller w/ message unit	Yes. Two SRIO controllers with message unit	No
FIFO Support	Yes	No

2 Hardware Design Considerations

The section elaborates on the hardware- and board-level differences that exist when migrating between the P2020 and P1020 devices, specifically items that are critical to the hardware design engineer. If proper attention is taken and a common feature set is utilized between the two devices, it is possible to design a platform that supports both devices. In such instances, simple BOM substitutions are needed when migrating between the devices.

2.1 Supported PCI Express Combinations

Table 2 shows all the viable PCI Express (PCIe) combinations available on both devices. A notable difference between the devices is that the P2020 supports three PCIe controllers whereas the P1020 supports two PCIe controllers.

Table 2. Supported PCIe Options—P2020 vs. P1020

	P2020				P1020			
Option	Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 2	Lane 3
Option #1	x1 (PCIe1)	off	off	off	x1 (PCIe1)	off	off	off
Option #2	x1 (PCIe1)	x1 (PCIe2)	x2 (PCIe3)		x1 (PCIe1)	x1 (PCIe2)	Not Supported	
Option #3	x2 (PCIe1)		x2 (PCIe3)		x2 (PCIe1)		Not Supported	
Option #4	x4 (PCIe1)				x4 (PCIe1)			

2.2 DDR Interface

When designing a common platform that supports both the P2020 and the P1020, the customer may choose either a 64/72 bit interface or a 32/36 bit interface. If the former is used, only 32 bits are valid when a P1020 is installed; the additional memory chips can be unpopulated. In addition, the P1020 only supports two memory banks.

Table 3 lists the major hardware differences between the P2020 and P1020 devices.

Table 3. DDR Controller Feature Differences

Items	P2020	P1020
Interface width supported	64/72-bit (with ECC)	32/36-bit (with ECC) 16-bit
ECC support	8-bit (when 64-bit)	4-bit (when 32-bit)
Data Rate	400–667 MHz (DDR2) 600–667 MHz (DDR3)	400–667 MHz (DDR2) 600–667 MHz (DDR3)
Number of chip selects supported	Four	Two
Number of memory banks supported	Four	Two
Page mode support	Up to 32 open pages	Up to 16 open pages

2.2.1 DDR Package Deltas

As the P2020 and P1020 are unique dies, there are slight variations in the substrate routing lengths and overall cumulative inductance. The worst case signal variation between the two packages, same signal to same signal, is expected to be less than 35 ps.

2.3 Enhanced Three-Speed Ethernet Controllers

Table 4 shows the eTSEC comparision between the devices. The most notable difference is that the P2020 supports three reduced ports or two full parallel ports whereas the P1020 supports two and one respectively.

Table 4. eTSEC configurations

Items	P2020	P1020
Number of eTSECs controllers	3 eTSEC1, eTSEC2, eTEC3	3 eTSEC1, eTSEC2, eTEC3
Number of reduced ports supported (RGMII)	3 eTSEC1, eTSEC2, eTSEC3	2 eTSEC1 and eTSEC3
Number of non-reduced ports supporteded (GMII)	2 eTSEC1 and eTSEC2	1 eTSEC1
Number of SGMII interfaces	2 eTSEC2 and eTSEC3	2 eTSEC2 and eTSEC3

Note: For P1020, eTSEC2 is only available in SGMII mode

When designing a common platform that supports both the P2020 and the P1020, the user can choose from either of the two common options shown in Table 5. Using one of these options provides an easy migration between the devices.

Table 5. Common eTSEC configurations between the P2020 and P1020

	P2020			P1020		
Option	eTSEC1	eTSEC2	eTSEC3	eTSEC1	eTSEC2	eTSEC3
Option #1	non-reduced mode	not used or SGMII	not used or SGMII	non-reduced mode	not used or SGMII	not used or SGMII
Option #2	reduced mode	not used or SGMII	reduced mode or SGMII	reduced mode	not used or SGMII	reduced mode or SGMII

2.4 Voltage and Power Target Differences

When designing a common platform that supports both the P2020 and the P1020, the power supply should be sized for the the worst case V_{DD} current requirements for the P2020. The power supply should also provide for an easy method of changing the output voltage feeding the V_{DD} pins of the device. On the Px020 RDB design, this was achieved by using TI's TPS54810 regulator. This particular device supports up to 9 A and allows the output voltage to be changed through external resistors.

Table 6 shows the voltage and power target differences between the P2020 and P1020 devices.

Table 6. Voltage and Power Target Differences

Item	Symbol	P2020	P1020
Core and Platform supply voltage	V_{DD}	1.05V ± 50 mV	0.95V ± 50 mV
PLL supply voltage	AV_{DD}	1.05V ± 50 mV	0.95V ± 50 mV
Core power supply for SerDes transceivers	SV_{DD}	1.05V ± 50 mV	0.95V ± 50 mV
Pad power supply for SerDes transceivers and PCI Express	XV_{DD}	1.05V ± 50 mV	0.95V ± 50 mV
Power target	Power	< 8 W @ 125C 800 MHz e500 400 MHz platform	< 4.5 W @ 125C, 800 MHz e500 400 MHz platform

2.5 Supported Frequencies

One of the key differences between the two devices is the supported frequency ranges that each can handle. When designing a common platform that supports both the P2020 and the P1020, the platform needs flexibility for configuring the PLL ratios that are sampled at POR configuration time. These PLL ratios control the cores, the platform, and DDR frequency. This flexibilty may be in the form of resistor stuff options and/or programmable logic. On the Px020 platform, a mixture of both is provided.

Table 7 compares the supported frequencies between the P2020 and P1020 devices.

Table 7. Comparison of Supported Frequencies

Items	P2020	P1020
SYSCLK Input Frequency Range	33–133 MHz	33–100 MHz
DDRCLK Input Frequency Range	66–166 MHz	66–166 MHz
Core Frequency	800–1200 MHz	333–800 MHz
CCB/Platform Frequency	400–600 MHz	166 MHz–200 Mhz 266 MHz–400 MHz
DDR2 Memory Bus Frequency (Note: Data rate is 2x this number)	200–333.33 MHz	200–333.33 MHz
DDR3 Memory Bus Frequency (Note: Data rate is 2x this number)	300–333.33 MHz	300–333.33 MHz
Local Bus Frequency	16.6–150 MHz	10–50 MHz

2.5.1 Comparision of Clocking Combination

Table 8 enumerates and compares several of the valid clocking options for the P2020 and the P1020 device.

NOTE

The table is not exhaustive as it does not include every valid input frequency and ratio combination. It merely highlights some of the more popular combinations for comparison. Moreover, additional frequency bins may be added at a later date. As such, consult the device datasheet for the latest information.

Table 8. Comparison of Supported Clocking Options

			P2020		P1020	
SYSCLK Frequency (MHz)	**Platform PLL Multiplier**	**Core PLL** Multiplier	**Platform Frequency (MHz)**	**Core Frequency (MHz)**	**Platform Frequency (MHz)** [1]	**Core Frequency (MHz)**
33.333	8	1.5	— [2]	—	266.66	400
33.333	10	1	—	—	333.33	333.33
33.333	10	1.5	—	—	333.33	500
33.333	10	2	—	—	333.33	666.66
33.333	12	1	—	—	400	400
33.333	12	1.5	—	—	400	600
33.333	12	2	400	800	400	800
33.333	12	2.5	400	1000	—	—
33.333	12	3	400	1200	—	—
66.666	4	1.5	—	—	266.66	400
66.666	4	2	—	—	266.66	533.33
66.666	4	2.5	—	—	266.66	666.66
66.666	4	3	—	—	266.66	800
66.666	5	1	—	—	333.33	333.33
66.666	5	1.5	—	—	333.33	500
66.666	5	2	—	—	333.33	666.66
66.666	6	1	—	—	400	400
66.666	6	1.5	—	—	400	600
66.666	6	2	400	800	400	800
66.666	6	2.5	400	1000	—	—
66.666	6	3	400	1200	—	—

Table 8. Comparison of Supported Clocking Options (continued)

			P2020		P1020	
SYSCLK Frequency (MHz)	**Platform PLL Multiplier**	**Core PLL** Multiplier	**Platform Frequency (MHz)**	**Core Frequency (MHz)**	**Platform Frequency (MHz)** [1]	**Core Frequency (MHz)**
66.666	8	1.5	533.33	800	—	—
66.666	8	2	533.33	1067	—	—
100	4	1	—	—	400	400
100	4	1.5	—	—	400	600
100	4	2	400	800	400	800
100	4	2.5	400	1000	—	—
100	4	3	400	1200	—	—
100	5	2	500	1000	—	—
100	6	1.5	600	900	—	—
100	6	2	600	1200	—	—
133.33	4	1.5	533.33	800	—	—
133.33	4	2	533	1067	—	—

1 Platform frequencies above 200 MHz and below 266 MHz are not supported by the P1020. Do not set a combination in this range.

2 A "—" indicates that this particular frequency is not currently available, but may be added at a later date.

2.6 DDR Clocking Comparison

Both the P2020 and P1020 are similar in their DDR clocking options, as shown in Table 9.

Table 9. Options for DDR Clocking

DDR: DDRCLK	**DDR Frequency (MHz)**			
	66.66	**100**	**133.33**	**166.66**
	DDR Data Rate (MHz)			
3	—	—	400	500
4	267	400	533	667
5	333	500	667	—
6	400	600	*800*[1]	
8	533	*800*[1]	—	—

Table 9. Options for DDR Clocking (continued)

DDR: DDRCLK	DDR Frequency (MHz)			
	66.66	100	133.33	166.66
	DDR Data Rate (MHz)			
10	667	—	—	—
12	*800* [1]	—	—	—
Note: DDR3 frequency must be ≥ 600 MHz per JEDEC.				

[1] Not officially supported at this time. May be added at a later date.

2.7 P1020—New Additions

This section describes the new features found in the P1020, as follows:

- Section 2.7.1, “Optional Support for Second GTX_CLK125 Input”
- Section 2.7.2, “TDM Interface with Dedicated DMA”
- Section 2.7.3, “Second USB Port”
- Section 2.7.4, “Independent Core1 Power Rail”

2.7.1 Optional Support for Second GTX_CLK125 Input

On the P2020, a single EC_GTX_CLK125 pin drives all eTSEC blocks. On the P1020, a second GTX_CLK125 is optionally supported, which allows eTSEC1 and eTSEC3 to be clocked separately. At reset the P1020 behaves like the P2020, and the EC_GTX_CLK125 pin provides clocking for both eTSEC blocks. If needed, the second GTX_CLK125 input can be enabled by means of the pin mux register. Once enabled, the EC_GTX_CLK125 pin provides clocking for eTSEC3, and the TSEC1_TX_CLK provides clocking for eTSEC1.

2.7.2 TDM Interface with Dedicated DMA

The P1020 adds a TDM interface along with a dedicated DMA engine. These features are not available in the P2020 product. The P1020’s TDM interface is a full-duplex serial port that allows communcation with external DSPs, codecs, and industry standard framers. It supports 128 channels running up to 50 Mbps with 8- and 16-bit word size. The TDM bus connects to most T1/E1 frames as well as to common buses such as H.110, SCAS, and MVIP.

The TDM pins are muxed on IRQ[6] and GPIO[0:4]. By default, the TDM interface is disabled, and the IRQ[6] and GPIO[0:4] pins retain their normal function as found in the P2020 product.

2.7.3 Second USB Port

A second USB interface is available on the P1020 device. The pins for this second port are muxed with eLBC LAD[0:14]. As such, if the second USB is needed and enabled, the local bus must be used exclusively for boot purposes only.

To mitigate the loading on the bus and any potential bus contention at boot, a bus switch is required on board. This bus switch isolates the external USB phy until the P1020 has finished booting. Once booted, the second USB can be enabled by means of the pin mux register. Additionally, the bus switch on the board must be enabled. A GPIO pin from the P1020 can be used to facilitate control of the bus switch. This particular scenario is demonstrated in the Px020 RDB schematics (see page 11).

NOTE

The prefix for the muxed USB is labeled USB2_xxxx. The primary USB port, the one that is common with the P2020, remains USB_xxxx to maintain pin naming conventions.

2.7.4 Independent Core1 Power Rail

The P1020 provides an independent power rail option for core1. On the P2020, both cores share a common V_{DD} rail device. The independent rail on the P1020 allows the second core to be completely powered off if necessary. When designing a common platform that supports both the P2020 and P1020, the platform has two options for how to use the core1 supply pins. The first is to create a separate power island. When a P2020 device is present, this separate power island connects to the V_{DD} supply in the system. The same applies to a P1020 device when both cores are utilized. If the second P1020 core is not needed, the core can be powered down using the independent plane. The second option is to use a single power island for both cores, which simplifies the PCB design. However, doing this causes unnecessary power leakage when the second P1020 core is not used. For the Px020 RDB platform, option one is implemented.

2.8 Signal Pin Differences

The vast majority of signal pins have the same name and functions in the P1020 as in the P2020. However, there are a few notable differences in either the primary pin function or in one of the alternate functions. Table 10 lists the all the known differences that exist between two devices. For a full signal description, please see the appropriate hardware specifications document and/or reference manual.

Table 10. Pinout Differences

Signal		Package Pin Number
P2020	**P1020**	
DDR Interface The P2020 supports a full 64/72-bit DDR bus whereas the P1020 supports a reduced 32-bit DDR bus. As such, the extra P2020 pins are no-connects in the P1020 package.		
MDQ[32:63]	NC	G4, G3, E2, E4, H5, H4, F2, E1, C1, C3, B4, A4, D1, D2, B3, A3, C5, E6, D9, E9, C4, E5, E8, D8, A6, B7, B10, A11, A5, B6, B9, A10
MECC[4:7]	NC	AB2, AD1, Y1, V6
$\overline{\text{MDM}}$[4:7]	NC	G1, C2, F8, A7
MDQS[4:7]	NC	F3, B2, D7, A9

Table 10. Pinout Differences (continued)

Signal		Package Pin Number
P2020	P1020	
MDQS_B[4:7]	NC	F4, B1, D6, A8
MCS_B[2]	NC	J1
MCS_B[3]	NC	G2
MCKE[2:3]	NC	U6, V2
MCK[4:5]	NC	AC6, F5
MCK_B[4:5]	NC	AC5, F6
MODT[2:3]	NC	J4, F1
eTSEC2 Interface eTSEC2 is only available in SGMII mode on the P1020 device. As such, the extra TSEC2 pins are no-connects in the P1020 package.		
TSEC2_TXD[6:7]	NC	AF26, AE26
TSEC2_TXD[2:3]	NC	AA25, AG29
TSEC2_TX_EN	NC	AA26
TSEC2_TX_CLK	NC	AA24
TSEC2_GTX_CLK	NC	AG28
TSEC2_RXD[7:0]	NC	AD27, AB26, AC26, AD26, AB27, AD28, AF29, AF28
TSEC2_RX_DV	NC	AD29
TSEC2_RX_ER	NC	AE28
TSEC2_RX_CLK	NC	AC29
eTSEC2 Interface continued On the P2020, eTSEC2 can be connected either serially (SGMII) or in a traditional parallel mode (RGMII, MII, etc). On the P1020, only the SGMII mode is supported for eTSEC2. Certain eTSEC2 pins have a secondary function for power-on config and eTSEC3 functionality. As a result, these secondary functions are the primary pin function for the P1020.		
TSEC2_TXD[5] (primary function)/ TSEC3_TX_EN (alternate function)	TSEC3_TX_EN	AB24
TSEC2_TXD[4] (primary function)/ TSEC3_GTX_CLK (alternate function)	TSEC3_GTX_CLK	AB25
TSEC2_CRS (primary function)/ TSEC3_RX_ER (alternate function)	TSEC3_RX_ER	AD25
TSEC2_COL (primary function)/ TSEC3_TX_CLK (alternate function)	TSEC3_TX_CLK	AE27
TSEC2_TXD[1] (primary function)/ cfg_dram_type (POR config)	cfg_dram_type	AF27

Table 10. Pinout Differences (continued)

Signal		Package Pin Number
P2020	**P1020**	
TSEC2_TX_ER (primary function)/ cfg_io_port[3] (POR config)	cfg_io_port[3]	AE29
eTSEC1 Interface The P1020 adds a new option for a second GTX_CLK125 input. This new option is supported as an alternate function on the TSEC1_TX_CLK pin.		
TSEC1_TX_CLK	TSEC1_TX_CLK (primary function)/ TSEC1_GTX_CLK125 (alternate function)	AJ24
DMA2 Interface The DMA2 interface is not supported on the P1020 device. However, the POR configs which are common between the P1020 and P2020 are preserved for pin compatibility.		
DMA2_DREQ_B[0]	NC	W28
DMA2_DACK_B[0] (primary function) / cfg_mem_debug (POR config)	cfg_mem_debug	T29
DMA2_DDONE_B[0] (primary function) / cfg_ddr_debug (POR config)	cfg_ddr_debug	Y29
Power The P2020 has a single VDD rail for both Core0 and Core1, whereas the P1020 allows Core1 to be independently powered, or optionally powered down. On P1020, the power to Core1 is labeld as VDD and the power to the platform and Core0 is labeled as VDDC (..for VDD continuous).		
VDD Powers both cores.	VDD The pin name has not changed, but internally these pins only power the Core1.	K10, K11, K12, L10, M10
	VDDC These pins power the platform along with Core0.	K13, K14, K15, K16, K17, K18, K19, K20, L20, N10, N20, M20, R10, R20, P10, P20, U10, U20, T10, T20, V10, V20, W10, W20, Y11, Y12, Y18, Y19, Y20
Local Bus A second USB port is available on the P1020 that is not available in the P2020 device. This second USB port is available as a alternate function off the Local bus. For further information see Section 2.7.3, “Second USB Port.”		
LSYNC_IN	NC	A13
LSYNC_OUT	NC	A14
LAD[0:7]	LAD[0:7] (primary function)/ USB2_D[7:0] (alternate function)	B18, E20, A19, B20, D19, A18, B17, C20
LAD[8]	LAD[8] (primary function)/ USB2_NXT (alternate function)	F19
LAD[9]	LAD[9] (primary function)/ USB2_DIR (alternate function)	E10

Table 10. Pinout Differences (continued)

Signal		Package Pin Number
P2020	**P1020**	
LAD[10]	LAD[10] (primary function)/ USB2_STP (alternate function)	B16
LAD[11]	LAD[11] (primary function)/ USB2_PWRFAULT (alternate function)	D14
LAD[12]	LAD[12] (primary function)/ USB2_CLK (alternate function)	D17
LAD[13]	LAD[13] (primary function)/ USB2_PCTL0 (alternate function)	E11
LAD[14]	LAD[14] (primary function)/ USB2_PCTL1 (alternate function)	A16
Other The P1020 supports a TDM interface that is not available on the P2020 device. This second USB port is available as a alternate function of certain GPIO/IRQ signals shown below. For further information see Section 2.7.2, "TDM Interface with Dedicated DMA."		
GPIO[0] (primary function)/ IRQ[7] (alternate function)	GPIO[0] (primary function)/ IRQ[7] (alternate function1)/ TDM_TX_DATA (alternate function2)	R28
GPIO[1] (primary function)/ IRQ[8] (alternate function)	GPIO[1] (primary function)/ IRQ[8] (alternate function1)/ TDM_TFS (alternate function2)	R26
GPIO[2] (primary function)/ IRQ[9] (alternate function)	GPIO[2] (primary function)/ IRQ[9] (alternate function1)/ TDM_TX_CLK (alternate function2)	P29
GPIO[3] (primary function)/ IRQ[10] (alternate function)	GPIO[3] (primary function)/ IRQ[10] (alternate function1)/ TDM_RFS (alternate function2)	N24
GPIO[4] (primary function)/ IRQ[11] (alternate function)	GPIO[4] (primary function)/ IRQ[11] (alternate function1)/ TDM_RX_DATA (alternate function2)	U29
IRQ[6] (primary function)	IRQ[6] (primary function) TDM_RX_CLK (alternate function1)	K27

2.9 POR Differences

Table 11–Table 25 identify key POR differences between the P1020 and the P2020.

Table 11. POR Comparison P2020 vs. P1020

P2020			P1020
POR Function	**Functional Signals**	**Reset Configuration Name**	**Comment**
System PLL Ratio	LA[29:31]	cfg_sys_pll[0:2]	Identical—No Change
DDR PLL Ratio	TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2	cfg_ddr_pll[0:2]	Identical—No Change
Core0 Ratio	LBCTL,LALE,LGPL2	cfg_core0_pll[0:2]	Identical—No Change
Core1 Ratio	$\overline{\text{LWE}}$[0],UART_SOUT[1], READY_P1	cfg_core1_pll[0:2]	Identical—No Change
Boot ROM Location	TSEC1_TXD[6:4], TSEC1_TX_ER	cfg_rom_loc[0:3]	See Table 12, “Boot ROM Location.”
Host/Agent Mode	LWE_B[1], LA[18:19]	cfg_host_agt[0:2	See Table 13, “Host/Agent Configuration.”
Serdes I/O Port Selection	TSEC1_TXD[3:1], TSEC2_TX_ER For P1020, the TSEC2_TX_ER pin name is changed to cfg_io_ports[3]. [1]	cfg_io_ports[0:3]	See Table 14, “I/O Port Selection.”
CPU Boot	LA[27], LA[16]	cfg_cpu0_boot, cfg_cpu1_boot	Identical—No Change
Boot Sequencer	LGPL3, LGPL5	cfg_boot_seq[0:1]	Identical—No Change
DDR SDRAM Type	TSEC2_TXD1 For P1020, TSEC2_TXD1 name is changed to cfg_dram_type.[1]	cfg_dram_type	Identical—No Change
Serdes Clock Selection	TSEC_1588_ALARM_OUT1	cfg_srds_refclk	Identical—No Change
eTSEC1 Protocol	TSEC1_TXD0, TSEC1_TXD7	cfg_tsec1_prtcl[0:1]	See Table 18, “eTSEC1 Protocol Configuration.”
eTSEC2 Protocol	TSEC2_TXD0, TSEC2_TXD7	cfg_tsec2_prtcl[0:1]	Not supported
eTSEC3 Protocol	$\overline{\text{UART\_RTS0}}$, $\overline{\text{UART\_RTS1}}$	cfg_tsec3_prtcl[0:1]	Identical—No Change
eTSEC2 SGMII Mode	LGPL1	cfg_sgmii2	Not supported
eTSEC3 SGMII Mode	TSEC_1588_ALARM_OUT2	cfg_sgmii3	Identical—No Change
eTSEC1 Width	EC_MDC	cfg_tsec_reduce	See Table 19, “eTSEC Width Configuration.”
Rapid IO Device ID	TSEC2_TXD[2:4]	cfg_device_ID[5:7]	Not supported
Rapid IO System Size	LGPL0	cfg_rio_sys_size	Not supported

Table 11. POR Comparison P2020 vs. P1020 (continued)

P2020			P1020
POR Function	**Functional Signals**	**Reset Configuration Name**	**Comment**
Memory Debug Mode	$\overline{\text{DMA2\_DACK}}$[0] For P1020, DMA2_DACK[0] name is changed to cfg_mem_debug.[1]	cfg_mem_debug	Identical—No Change
DDR Debug Mode	$\overline{\text{DMA2\_DDONE}}$[0] For P1020, DMA2_DDONE[0] name is changed to cfg_ddr_debug.[1]	cfg_ddr_debug	Identical—No Change
General-Purpose	LAD[0:15]	cfg_gpinput[0:15]	Identical—No Change
Engineering Use	LA[20:22], UART_SOUT[0], TRIG_OUT, MSRCID[1], MSRCID[4], DMA1_DDONE_B[0]	cfg_eng_use[0:7],	See Table 20, “Engineering Use.”
eLBC ECC Enable	MSRCID[0]	cfg_elbc_ecc	Identical—No Change
System Speed	LA28	cfg_sys_speed	Identical—No Change
Platform Speed	LA23,	cfg_plat_speed	See Table 21, “P2020 Platform Speed.”
Core 0 Speed	LA24	cfg_core0_speed	See Table 23, “Core 0 Speed.”
Core 1 Speed	LA25	cfg_core1_speed	See Table 24, “Core 1 Speed.”
DDR Speed	LA26	cfg_ddr_speed	See Table 25, “DDR Speed.”

[1] The P1020 does not support the P2020’s primary pin function but continues to support the POR config function.

Table 12. Boot ROM Location

Functional Signals	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
TSEC1_TXD[6:4], TSEC1_TX_ER Default: 1111	cfg_rom_loc[0:3]	0000	PCI Express 1	same as P2020
		0001	PCI Express 2	same as P2020
		0010	Serial RapidIO 1	not supported
		0011	Serial RapidIO 2	not supported
		0100	DDR controller	same as P2020
		0101	PCI Express 3	not supported
		0110	On-chip boot ROM—SPI configuration	same as P2020
		0111	On-chip boot ROM—eSDHC configuration	same as P2020
		1000	Local bus FCM—8-bit NAND flash small page	same as P2020
		1001	Reserved	same as P2020
		1010	Local bus FCM—8-bit NAND flash large page	same as P2020
		1011	Reserved	same as P2020
		1100	Reserved	same as P2020
		1101	Local bus GPCM—8-bit ROM	same as P2020
		1110	Local bus GPCM—16-bit ROM	same as P2020
		1111	Local bus GPCM—16-bit ROM	same as P2020

Table 13. Host/Agent Configuration

Functional Signals	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$ LA[18:19] Default (111)	cfg_host_agt[0:2]	000	P2020E acts as an agent on all its PCI Express and SRIO interfaces.	Same as P2020 for PCI Express. No SRIO option.
		001	P2020E acts as an agent on PCI Express 1 or host on serial RapidIO 2. P2020E acts as a host on PCI Express 2/serial RapidIO 1. P2020E acts as a host on PCI Express 3	Same as P2020 for PCI Express 1 and 2. No SRIO or PCI Express 3 option.
		010	P2020E acts as a host on PCI Express 1 or agent on serial RapidIO 2. P2020E acts as an agent on PCI Express 2/serial RapidIO 1. P2020E acts as a host on PCI Express 3	Same as P2020 for PCI Express 1 and 2. No SRIO or PCI Express 3 option.
		011	P2020E acts as a host on PCI Express 1/serial RapidIO 2. P2020E acts as a host on PCI Express 2/serial RapidIO 1. P2020E acts as an agent on PCI Express 3	not supported
		100	P2020E acts as an agent on PCI Express 1/serial RapidIO 2. P2020E acts as an agent on PCI Express 2/serial RapidIO 1. P2020E acts as a host on PCI Express 3	not supported
		101	P2020E acts as an agent on PCI Express 1 or host on serial RapidIO 2. P2020E acts as a host on PCI Express 2/serial RapidIO 1. P2020E acts as an agent on PCI Express	not supported
		110	P2020E acts as a host on PCI Express 1 or agent on serial RapidIO 2. P2020E acts as an agent on PCI Express 2/serial RapidIO 1. P2020E acts as an agent on PCI Express	not supported
		111	P2020E acts as the host processor/root complex for all PCI Express/serial RapidIO interfaces (default).	same as P2020

Table 14. I/O Port Selection

Functional Signal	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
TSEC1_TXD[3:1], TSEC2_TX_ER Default (1111)	cfg_IO_ports[0:3]	0000	PCI Express 1 (x1) (2.5 Gbps)→ SerDes lane 0 SerDes lanes 1–3 powered down	same
		0001	SerDes lanes 0–3 powered down	same
		0010	PCI Express 1 (x1) (2.5 Gbps) → SerDes lane 0 PCI Express 2 (x1) (2.5 Gbps) → SerDes lane 1 PCI Express 3 (x2) (2.5 Gbps) → SerDes lanes 2–3	not supported
		0011	Reserved	same
		0100	PCI Express 1 (x2) (2.5 Gbps) → SerDes lanes 0–1 PCI Express 3 (x2) (2.5 Gbps) → SerDes lanes 2–3	not supported
		0101	Reserved	same
		0110	PCI Express 1 (x4) (2.5 Gbps) → SerDes lanes 0–3	same
		0111	SRIO2 (1x) (3.125 Gbps) → SerDes lane 0 SRIO1 (1x) (3.125 Gbps) → SerDes lane 1 SerDes lanes 2–3powered down	not supported
		1000	SRIO2 (4x) (1.25 Gbps) → SerDes lanes 0–3	not supported
		1001	SRIO2 (4x) (2.5 Gbps) → SerDes lanes 0–3	not supported
		1010	SRIO2 (4x) (3.125 Gbps) → SerDes lanes 0–3	not supported
		1011	SRIO 2 (1x) (1.25 Gbps) → SerDes lane 0 SRIO 1 (1x) (1.25 Gbps) → SerDes lane 1 SGMII eTSEC2 (x1) (1.25 Gbps) → SerDes lane 2 SGMII eTSEC3 (x1) (1.25 Gbps) → SerDes lane 3	not supported
		1100	SRIO 2 (1x) (2.5 Gbps) → SerDes lane 0 SRIO 1 (1x) (2.5 Gbps) → SerDes lane 1 SGMII eTSEC2 (x1) (1.25 Gbps) → SerDes lane 2 SGMII eTSEC3 (x1) (1.25 Gbps) → SerDes lane 3	not supported
		1101	PCI Express 1 (x1) (2.5 Gbps) → SerDes lane 0 SRIO 1 (1x) (2.5 Gbps) → SerDes lane 1 SGMII eTSEC2 (x1) (1.25 Gbps) → SerDes lane 2 SGMII eTSEC3 (x1) (1.25 Gbps) → SerDes lane 3	not supported
		1110	PCI Express 1 (x1) (2.5 Gbps) → SerDes lane 0 PCI Express 2 (x1) (2.5 Gbps) → SerDes lane 1 SGMII eTSEC2 (x1) (1.25 Gbps) → SerDes lane 2 SGMII eTSEC3 (x1) (1.25 Gbps) → SerDes lane 3	same
		1111	PCI Express 1 (x2) (2.5 Gbps) → SerDes lanes 0–1 SGMII eTSEC2 (x1) (1.25 Gbps) → SerDes lane 2 SGMII eTSEC3 (x1) (1.25 Gbps) → SerDes lane 3	same

Table 15. eTSEC1 POR Configuration Summary

eTSEC1 Configuration	cfg_tsec_reduce	cfg_tsec1_prtcl	P2020	P1020
8-bit FIFO	0	00	supported	not supported
RMII	0	01	supported	supported
RGMII	0	10	supported	supported
RTBI	0	11	supported	supported
16-bit FIFO	1	00	supported	not supported
MII	1	01	supported	supported
GMII	1	10	supported	supported
TBI	1	11	supported	supported

Table 16. eTSEC2 POR Configuration Summary

eTSEC2 Configuration	cfg_sgmii2 [1]	cfg_tsec_reduce [2]	cfg_tsec1_prtcl	cfg_tsec2_prtcl	P2020	P1020
SGMII	0	—	—	—	supported	supported
8-bit FIFO	1	0	—	00	supported	not supported
RMII	1	0	—	01	supported	not supported
RGMII	1	0	—	10	supported	not supported
RTBI	1	0	—	11	supported	not supported
none [3]	1	1	00	—	supported	not supported
8-bit FIFO [4]	1	1	not 00	00	supported	not supported
MII	1	1	not 00	01	supported	not supported
GMII	1	1	not 00	10	supported	not supported
TBI	1	1	not 00	11	supported	not supported

1 cfg_sgmii2 polarity matches the MPC8572E definition.
2 cfg_tsec_reduce polarity matches MPC8572E definition.
3 eTSEC1 16-bit FIFO mode prohibits eTSEC2 parallel modes on P2020.
4 16-bit FIFO mode is not supported on eTSEC2 on P2020.

Table 17. eTSEC3 POR Configuration Summary

eTSEC3 Configuration	cfg_sgmii3 [1]	cfg_tsec_reduce [2]	cfg_tsec3_prtcl	P2020	P1020
SGMII	0	—	—	supported	supported
none	1	0	00	supported	supported
RMII	1	0	01	supported	supported
RGMII	1	0	10	supported	supported

Table 17. eTSEC3 POR Configuration Summary (continued)

eTSEC3 Configuration	cfg_sgmii3 [1]	cfg_tsec_reduce [2]	cfg_tsec3_prtcl	P2020	P1020
RTBI	1	0	11	supported	supported
none	1	1 [3]	—	supported	supported

1 cfg_sgmii3 polarity matches the MPC8572E definition.
2 cfg_tsec_reduce polarity matches MPC8572E definition.
3 A non-reduced configuration prohibits eTSEC3.

Table 18. eTSEC1 Protocol Configuration

Functional Signals	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
TSEC1_TXD0, TSEC1_TXD7 Default (11)	cfg_tsec1_prtcl[0:1]	00	The eTSEC1 controller operates using FIFO protocol.	not supported
		01	The eTSEC1 controller operates using the MII protocol (or RMII if configured in reduced mode.	same as P2020
		10	The eTSEC1 controller operates using the GMII protocol (or RGMII if configured in reduced mode.)	same as P2020
		11	The eTSEC1 controller operates using the TBI protocol (or RTBI if configured in reduced mode). (default)	same as P2020

Table 19. eTSEC1 Width Configuration

Functional Signals	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
EC_MDC Default (1)	cfg_tsec_reduce	0	eTSEC1 and eTSEC2 Ethernet interfaces operate in reduced pin mode (either RTBI,RGMII, RMII, or 8-bit FIFO mode).	eTSEC1 Ethernet interface operate in reduced pin mode (either RTBI, RGMII, RMII).
		1	eTSEC1 and eTSEC2 Ethernet interfaces operate in their standard width TBI, GMII, or MII mode. Only eTSEC1 can operate in 16-bit FIFO mode. The eTSEC2 FIFO width is always 8-bits regardless of the setting of this configuration bit (default).	eTSEC1 Ethernet interface operate in their standard width TBI, GMII, MII mode.

Table 20. Engineering Use

Functional Signals	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
LA[20:22], UART_SOUT[0], TRIG_OUT	cfg_eng_use[0:4]	11111	Spare POR pins. Reserved for future use.	Same as P1020

Table 20. Engineering Use (continued)

MSRCID[1]	cfg_eng_use[5]	1	cfg_eng_use[5]	Internal FSL use only
MSRCID[4]	cfg_eng_use[6]	1	Spare POR pins. Reserved for future use.	Same as P1020
DMA1_DDONE_B[0]	cfg_eng_use[7]	1	cfg_eng_use[7]	cfg_plat_speed1

Table 21. P2020 Platform Speed

Functional Signals	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
LA23 Default (1)	cfg_plat_speed	0	Platform clock frequency is below 333 MHz.	See P1020 Platform Speed table.
		1	Platform clock frequency is at or above 333 MHz.	See P1020 Platform Speed table.

Table 22. P1020 Platform Speed

Functional Signals	Reset Configuration Name	Value (Binary)	P1020 Meaning
LA[23] DMA1_DDONE_B[0]	cfg_plat_speed0 cfg_plat_speed1	00	Platform clock frequency is below 200 MHz.
		01	Reserved
		10	Reserved
		11	Platform clock frequency is at or above 267 MHz.

Table 23. Core 0 Speed

Functional Signals	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
LA24 Default (1)	cfg_core0_speed	0	Core 0 clock frequency is less than or equal to 1000 MHz.	Core 0 clock frequency is less than or equal to 450 MHz.
		1	Core 0 clock frequency is greater than 1000 MHz.	Core 0 clock frequency is greater than 450 MHz.

Table 24. Core 1 Speed

Functional Signals	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
LA25 Default (1)	cfg_core1_speed	0	Core 1 clock frequency is less than or equal to 1000 MHz.	Core 1 clock frequency is less than or equal to 450 MHz.
		1	Core 1 clock frequency is greater than 1000 MHz.	Core 1 clock frequency is greater than 450 MHz.

Table 25. DDR Speed

Functional Signals	Reset Configuration Name	Value (Binary)	P2020 Meaning	P1020 Meaning
LA26 Default (1)	cfg_ddr_speed	0	DDR clock frequency is less than 500 MHz.	DDR clock frequency is less than 450 MHz.
		1	DDR clock frequency is greater than or equal to 500 MHz.	DDR clock frequency is greater than or equal to 450 MHz.

3 Software Differences

This section describes the functional differences between the P2020 and the P1020, as follows:

- Section 3.1, “Core Frequency and L2 Cache”
- Section 3.2, “Device ID”
- Section 3.3, “DDR Controller”
- Section 3.4, “Local Access Windows”
- Section 3.5, “Serial RapidIO, DMA, and PCI Express”
- Section 3.6, “USB Controller”
- Section 3.7, “TDM Controller”

Table 26 provides a summary of the software differences.

Table 26. Software Differences

S No	Features	P2020	P1020
1	e500 core	Core running at 1200 Mhz (maximum core frequency)	Core can run at maximum speed of 800 Mhz
2	L2 Cache	512 KBytes	256 KBytes
3	Device ID	Different SVR & PVR values	
4	DDR Controller	Supports 64/32 bit	Supports only 32 bit
5	Local Access Windows (LAW)	Supports 12 LAWs	Supports 10 LAWs
6	Interrupts	Due to changes in some features, there are few changes in the interrupt table	
7	Serial RapidIO	Available	Not available
8	PCI Express	Three PCI Express Controllers	Two PCI Express Controllers
9	Direct Memory Access (DMA)	Dual DMA Controllers	Single DMA Controllers
10	USB 2.0 Controller	Single USB Controller	Two USB controllers
11	TDM	Not available	Available

3.1 Core Frequency and L2 Cache

The e500 core in P2020 can run at maximum frequency of 1200 Mhz while in P1020, the maximum frequency of e500 core is 800 Mhz. If any delay loop is present in the software, there might be an added time lag in P1020 due to slower speed.

The size of L2 cache is different in two devices. P2020 has 512 KBytes while P1020 has 256 KBytes. This should be taken care of while initializing the cache.

3.2 Device ID

Table 27 mentions PVR and SVR values for P1020 and P2020.

Table 27. PVR and SVR Values

Device	Processor Version Register (PVR)	System Version Register (SVR)
P2020 (without security)	0x8021_0040	0x80E2_0010
P2020E (with security)	0x8021_0040	0x80EA_0010
P1020 (without security)	0x8021_2030	0x80E4_ 0010
P1020E (with security)	0x8021_2030	0x80EC_ 0010

3.3 DDR Controller

The DDR controller of the P1020 supports only a 32-bit data bus width while the P2020 supports both 32-bit and 64-bit. The P1020 also supports only two banks of memory while the P2020 supports four banks.

Table 28 lists which bits of the DDR controller should be checked during migration from the P2020 to the P1020.

Table 28. DDR Controller Bits To Be Checked

Name	Description
DDR_SDRAM_CFG [DBW]	DRAM data bus width. 00 64-bit bus is used. 01 32-bit bus is used. 10 Reserved 11 Reserved
DDR_SDRAM_CFG [8_BE]	If a 64-bit bus is used, this should be set to 0. Otherwise, this should be set to 1.
DDR_SDRAM_CFG_2 [OBC_CFG]	This feature can only be used if a 64-bit data bus is used.
CAPTURE_ECC [ECE]	Error capture ECC is dependent on data bus width.

3.4 Local Access Windows

The P2020 has twelve local access windows that can be configured using LAWBAR0 to LAWBAR11 and LAWAR0 to LAWAR11. The P1020 provides ten local access windows that can be configured using LAWBAR0 to LAWBAR9 and LAWAR0 to LAWAR9.

3.5 Serial RapidIO, DMA, and PCI Express

The absence of Serial RapidIO in the P1020 means that there is no valid memory available from CCSRBAR + 0xC_0000 to CCSRBAR + 0xD_FFFF. Similarly, CCSRBAR + 0xC000 to CCSRBAR + 0xCFFF, meant for DMA2 in the P2020, and CCSRBAR + 0x8000 to CCSRBAR + 0x8FFF, meant for the PCI Express-3 controller in the P2020, are reserved space in the P1020.

Finally, all the interrupt bits, vectors, and priority registers meant for Serial RapidIO, DMA2, and PCI Express in P2020 are not valid in the P1020.

3.6 USB Controller

The P2020 has only one USB controller whereas the P1020 has two USB controllers. The second USB interface (named USB2) is multiplexed with eLBC pins, and its interrupts are mapped with Internal Interrupt Number 30 of the programmable interrupt controller. The USB2 controller registers are mapped at CCSRBAR + 0x2_3000 to CCSRBAR + 0x2_3FFF.

Table 29 describes the new bits defined for USB2 in Global Utilities Registers Block.

Table 29. New Bits Introduced for USB2

Register	Bit No	Name	Description
PMUXCR	7	eLBC_USB2	Exposes USB2 pins LAD[0:14] 0 LAD[0:14] are exposed to pins. 1 LAD[0:14] are exposed to pins as follows: LAD[0:7] functions as USB2_D[7:0] LAD[8] functions as USB2_NXT LAD[9] functions as USB2_DIR LAD[10] functions as USB2_STP LAD[11] functions as USB2_PWRFAULT LAD[12] functions as USB2_CLK LAD[13] functions as USB2_PCTL0 LAD[14] functions as USB2_PCTL1
DEVDISR	3	USB2	USB2 disable 0 USB2 enable 1 USB2 disable
ECMCR	8-11	USB2_UPRADR	The uppermost bits of the USB2 address bus for all transactions initiated by the USB2

3.7 TDM Controller

A TDM has been added to the P1020. It is multiplexed with GPIO pins, and its interrupts are mapped with Internal Interrupt Number 46 of programmable interrupt controller. The TDM controller registers are mapped at CCSRBAR + 0x1_6000 to CCSRBAR + 0x1_61FF.

Table 30 describes new bits defined for TDM in Global Utilities Registers Block.

Table 30. New Bits Introduced for the TDM

Register	Bit No	Name	Description
PMUXCR	8	TDM_EN	Exposes TDM pins 0 IRQ6, GPIO[0:4] are exposed to pins 1 IRQ6 functions as TDM_RX_CLK GPIO[0] functions as TDM_TX_DATA GPIO[1] functions as TDM_TFS GPIO[2] functions as TDM_TX_CLK GPIO[3] functions as TDM_RFS GPIO[4] functions as TDM_RX_DATA
DEVDISR	13	TDM	TDM disable 0 TDM enable 1 TDM disable
ECMCR	12–15	TDM_UPRADR	The uppermost bits of the DMAC address bus for all transactions initiated by the TDM-DMAC

4 Revision History

Table 31 provides a revision history for this application note.

Table 31. Document Revision History

Rev. Number	Date	Substantive Change(s)
A	12/2008	Initial release

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