中国科学院大学
University of Chinese Academy of Sciences

B0911006Y-01　2024-2025学年春季学期

计算机组成原理

Principles of Computer Organization

第 10 讲　计算机中数的运算IV

Booth乘法、快速乘法器、定点除法

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④ Booth 算法递推公式

$$[x \cdot y]_{补} = [x]_{补}[(y_1 - y_0) + (y_2 - y_1)2^{-1} + \cdots + (y_{n+1} - y_n)2^{-n}]$$

$$[z_0]_{补} = 0$$

$$[z_1]_{补} = 2^{-1}\{(y_{n+1} - y_n)[x]_{补} + [z_0]_{补}\} \qquad y_{n+1} = 0$$

$$\vdots$$

$$[z_n]_{补} = 2^{-1}\{(y_2 - y_1)[x]_{补} + [z_{n-1}]_{补}\}$$

$$[x \cdot y]_{补} = [z_n]_{补} + (y_1 - y_0)[x]_{补}$$

$-[x]_{补} = +[-x]_{补}$

最后一步不移位

如何实现

$y_{i+1} - y_i$ ？

y_i y_{i+1}	$y_{i+1} - y_i$	部分积的操作
0 0	0	→1
0 1	1	$+[x]_{补}$ →1
1 0	-1	$+[-x]_{补}$ →1
1 1	0	→1

Invented by Andrew Donald Booth in 1950 while doing research on crystallography at Birkbeck College in Bloomsbury, London

可能运算过程中部分积绝对值大于1，因此部分积和被乘数取双符号位

例6.23 已知 $x = +0.0011$ $y = -0.1011$ 求$[x \cdot y]_{补}$

6.3

乘数的符号位需参加运算

$[x]_{补} = 0.0011$

$[y]_{补} = 1.0101$

$[-x]_{补} = 1.1101$

解：

	y_i	y_{i+1}	
00.0000	1.0101	0	
+ 11.1101			$+[-x]_{补}$
11.1101			
11.1110	1 1010	1	→1 (这里附加位参与右移！这里不是C_j)
+ 00.0011			$+[x]_{补}$
00.0001	1		
00.0000	11 101	0	→1
+ 11.1101			$+[-x]_{补}$
11.1101	11		
11.1110	111 10	1	→1
+ 00.0011			$+[x]_{补}$
00.0001	111		
00.0000	1111 1	0	→1
+ 11.1101			$+[-x]_{补}$
11.1101	1111		最后一步不移位

补码右移

补码右移

补码右移

补码右移

y_i y_{i+1}	$y_{i+1}-y_i$	部分积的操作
0 0	0	→1
0 1	1	$+[x]_{补}$ →1
1 0	-1	$+[-x]_{补}$ →1
1 1	0	→1

∴ $[x \cdot y]_{补}$ =1.11011111

y_i y_{i+1}	$y_{i+1}-y_i$	部分积的操作
0 0	0	→1
0 1	1	$+[x]_{补}$ →1
1 0	-1	$+[-x]_{补}$ →1
1 1	0	→1

例 6.21　已知$[x]_{补}=0.1101$，$[y]_{补}=0.1011$，求$[x\cdot y]_{补}$。

解：表 6.16 列出了例 6.21 的求解过程。

表 6.16　例 6.21 求$[x\cdot y]_{补}$的过程

部分积	乘数 y_n	附加位 y_{n+1}	说
00.0000 + 11.0011	01011	0	初值$[z_0]_{补}=0$ $y_ny_{n+1}=10$，部分积加$[-x]_{补}$
11.0011 11.1001 11.1100 + 00.1101	10101 11010	1 1	→1 位，得$[z_1]_{补}$ $y_ny_{n+1}=11$，部分积→1 位，得$[z_2]_{补}$ $y_ny_{n+1}=01$，部分积加$[x]_{补}$
00.1001 00.0100 + 11.0011	11 11101	0	→1 位，得$[z_3]_{补}$ $y_ny_{n+1}=10$，部分积加$[-x]_{补}$
11.0111 11.1011 + 00.1101	111 11110	1	→1 位，得$[z_4]_{补}$ $y_ny_{n+1}=01$，部分积加$[x]_{补}$
00.1000	1111		最后一步不移位，得$[x\cdot y]_{补}$

故　$[x\cdot y]_{补}=0.10001111$

可能运算过程中部分积绝对值大于1，因此部分积和被乘数取双符号位

乘数的符号位需参加运算

y_i y_{i+1}	$y_{i+1}-y_i$	部分积的操作
0 0	0	→1
0 1	1	$+[x]_{补}$ →1
1 0	-1	$+[-x]_{补}$ →1
1 1	0	→1

例 6.22　已知$[x]_{补}=1.0101$，$[y]_{补}=1.0011$，求$[x$

部分积	乘数 y_n	附加位 y_{n+1}	说　明
00.0000	10011	0	
+00.1011			$y_ny_{n+1}=10$，部分积加$[-x]_{补}$
00.1011			
00.0101	11001	1	→1 位，得$[z_1]_{补}$
00.0010	11100	1	$y_ny_{n+1}=11$，部分积→1 位，得$[z_2]_{补}$
+11.0101			$y_ny_{n+1}=01$，部分积加$[x]_{补}$
11.0111	11		
11.1011	11110	0	→1 位，得$[z_3]_{补}$
11.1101	11111	0	$y_ny_{n+1}=00$，部分→1 位，得$[z_4]_{补}$
+00.1011			$y_ny_{n+1}=10$，部分积加$[-x]_{补}$
00.1000	1111		最后一步不移位，得$[x\cdot y]_{补}$

故 $[x\cdot y]_{补}=0.10001111$

Long Table → Short Table

算的省心（符号任意）、算的快（某些情况仅做右移操作）

Booth布斯算法举例

【这里的P即前述的部分积z，另外这里y的脚标序号是递减的，前述是递增的】

已知$[X]_{补}$ = 1_0110_1101，$[Y]_{补}$ = 0_1111_1110，计算$[X\times Y]_{补}$

$[-X]_{补}$ = 0_1001_0011 X=-147，Y=254，X×Y=-37338，

$[X\times Y]_{补}$应等于1_0110_1110_0010_0110

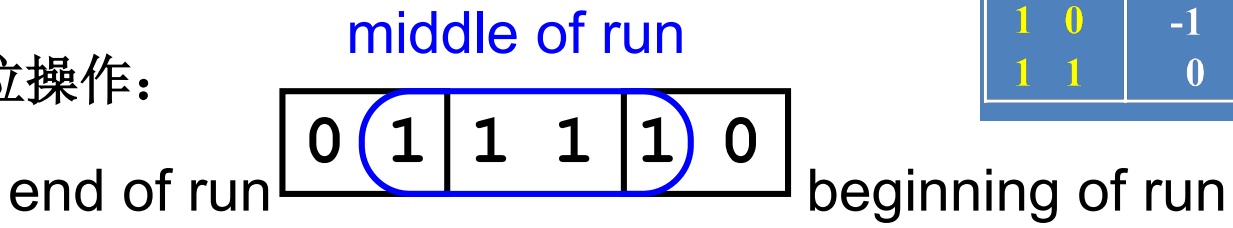
验证：$[Y]_{补}$中有连续1时，加速明显

P	Y	y_{-1}	说明
00_0000_0000	0_1111_1110	0	y_{-1}为0，$[P_0]_{补}$为0
00_0000_0000	0 0111_1111	0	$y_0y_{-1}=00$, P Y右移一位
+ 00_1001_0011 00_1001_0011 00_0100_1001	10 011_1111	1	$y_1y_0=10$, $+[-x]_{补}$， P Y右移一位
00_0010_0100	110 01_1111	1	$y_2y_1=11$, P Y直接右移一位
00_0001_0010	0110 0_1111	1	$y_3y_2=11$, P Y直接右移一位
00_0000_1001	0_0110 0111	1	$y_4y_3=11$, P Y直接右移一位
00_0000_0100	10_0110 011	1	$y_5y_4=11$, P Y直接右移一位
00_0000_0010	010_0110 01	1	$y_6y_5=11$, P Y直接右移一位
00_0000_0001	0010_0110 0	1	$y_7y_6=11$, P Y直接右移一位
+ 11_0110_1101 11_0110_1110	0010_0110		$y_8y_7=01$, $+[x]_{补}$， 最后一步不移位

Booth算法的实质和优点

y_i y_{i+1}	$y_{i+1}-y_i$	部分积的操作
0 0	0	→1
0 1	1	$+[x]_{补}$ →1
1 0	-1	$+[-x]_{补}$→1
1 1	0	→1

乘数的一轮移位操作：

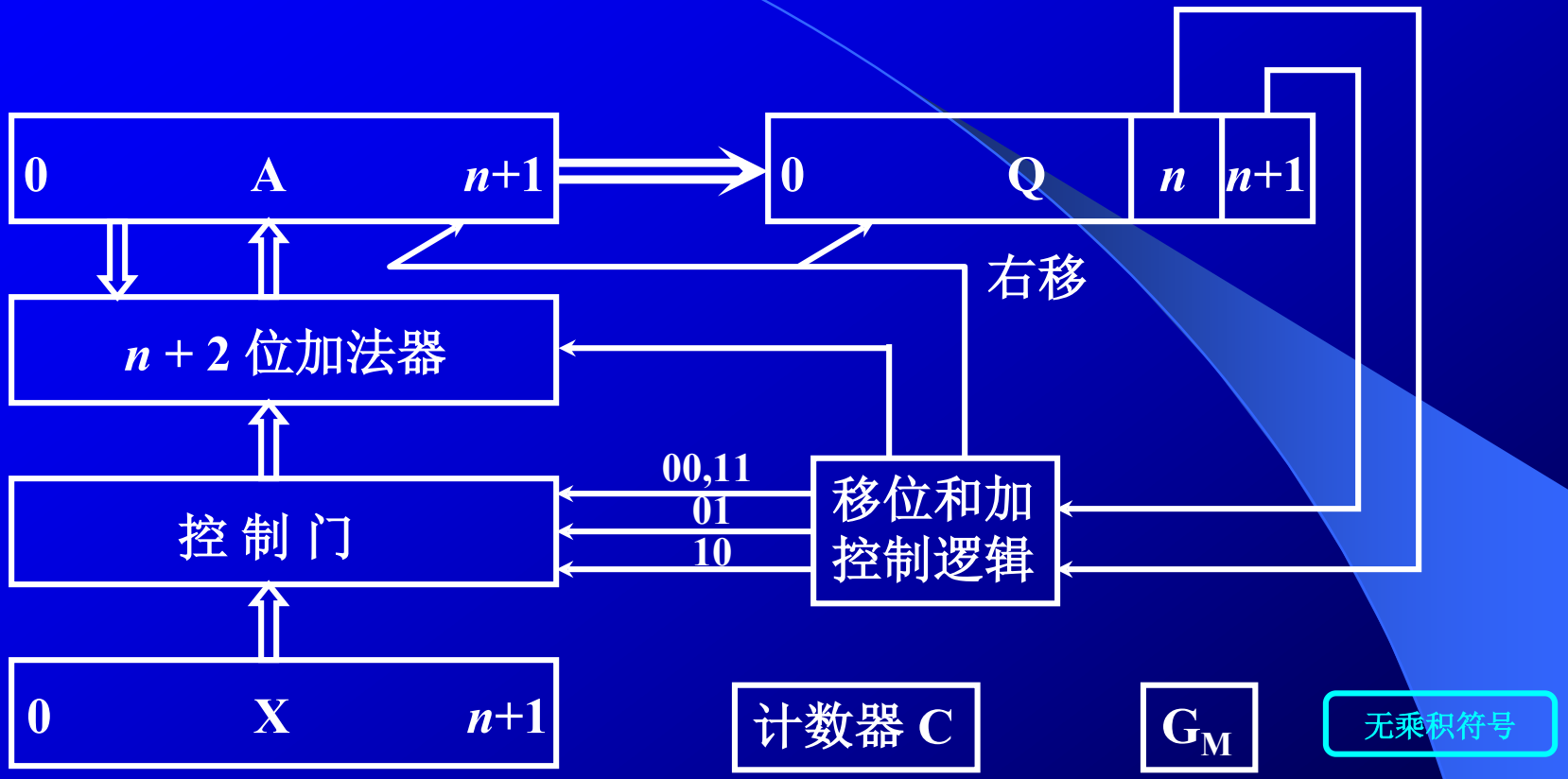


当前位 y_i	右边位 y_{i+1}	除移位外的操作	Example
1	0	减被乘数	0001111000
1	1	加0 (不操作)	0001111000
0	1	加被乘数	0001111000
0	0	加0 (不操作)	0001111000

- 在“1串”中，第一个1时做减法，最后一个1做加法，其余情况只要移位
- 同前面算法一样，将乘积寄存器右移一位。（这里是算术右移）
- 假设一个8位乘数：0111_1110，它将产生6行非零的部分积。如果把该数字记成另一种形式，(1)000_00(-1)0（-1是负1），则只需相加两个部分积，可以大大减少非零行的数目，意味着相加次数的减少，从而加快了运算速度
- Booth算法可以减少部分积的数目，用来计算有符号乘法，提高乘法速度

(2) Booth 算法的硬件配置

6.3



A、X、Q均为$n+2$位寄存器(A与X为双符号位，Q为单符号位+附加位)

移位和加操作受乘数的末两位控制

补充知识：补码两位乘法

- 补码两位乘可用布斯算法推导如下：【这里的P即前述的部分积z，另外这里y的脚标序号是递减的，前述是递增的】
  - $[P_{i+1}]_{补} = 2^{-1}([P_i]_{补} + (y_{i-1} - y_i)[X]_{补})$
  - $[P_{i+2}]_{补} = 2^{-1}([P_{i+1}]_{补} + (y_i - y_{i+1})[X]_{补})$

    $= 2^{-1}(2^{-1}([P_i]_{补} + (y_{i-1} - y_i)[X]_{补}) + (y_i - y_{i+1})[X]_{补})$

    $= 2^{-2}([P_i]_{补} + (y_{i-1} + y_i - 2y_{i+1})[X]_{补})$

- 开始置附加位y_{-1}为0，乘积寄存器最高位前面添加一位附加符号位0。
- 最终的乘积高位部分在乘积寄存器P中，低位部分在乘数寄存器Y中。
- 因为字长总是8的倍数，所以补码的位数n应该是偶数，因此，总循环次数为n/2。

y_{i+1}	y_i	y_{i-1}	操　作	迭代公式
0	0	0	0	$2^{-2}[P_i]_{补}$
0	0	1	$+[X]_{补}$	$2^{-2}\{[P_i]_{补}+[X]_{补}\}$
0	1	0	$+[X]_{补}$	$2^{-2}\{[P_i]_{补}+[X]_{补}\}$
0	1	1	$+2[X]_{补}$	$2^{-2}\{[P_i]_{补}+2[X]_{补}\}$
1	0	0	$+2[-X]_{补}$	$2^{-2}\{[P_i]_{补}+2[-X]_{补}\}$
1	0	1	$+[-X]_{补}$	$2^{-2}\{[P_i]_{补}+[-X]_{补}\}$
1	1	0	$+[-X]_{补}$	$2^{-2}\{[P_i]_{补}+[-X]_{补}\}$
1	1	1	0	$2^{-2}[P_i]_{补}$

小结：

1. 原码与补码的乘法，根本区别在于对符号位的处理
2. 补码（一位/两位）乘法：符号和数值一起运算，运算结果的符号是在数值部分的运算过程中自然形成
   ① 补码一位乘、乘数为负数时，校正法（加$[-x]_{补}$）
   ② 补码一位乘、乘数正负任意，比较法（Booth算法）
3. 注意区别$[-x^*]_{补}$和$[-x]_{补}$
   ① 原码两位乘法中使用$[-x^*]_{补}$
   ② 补码乘法中使用$[-x]_{补}$

y_i y_{i+1}	$y_{i+1}-y_i$	部分积的操作
0 0	0	→1
0 1	1	$+[x]_{补}$ →1
1 0	-1	$+[-x]_{补}$ →1
1 1	0	→1

4. 由于不同的机器数运算规则不同，运算器硬件组成各不相同（包括寄存器位数、全加器输入端控制电路等）

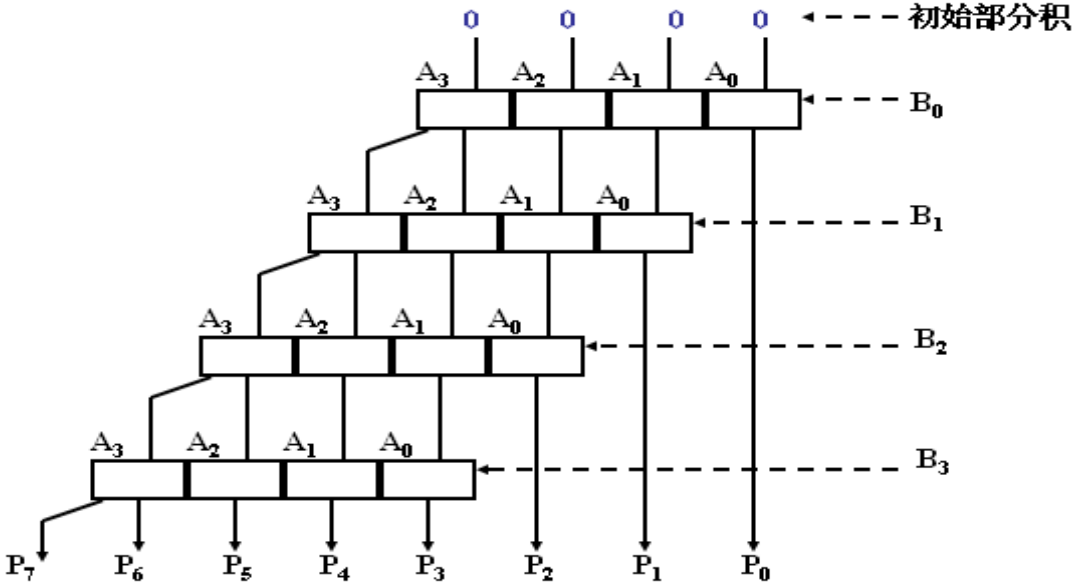
快速乘法器

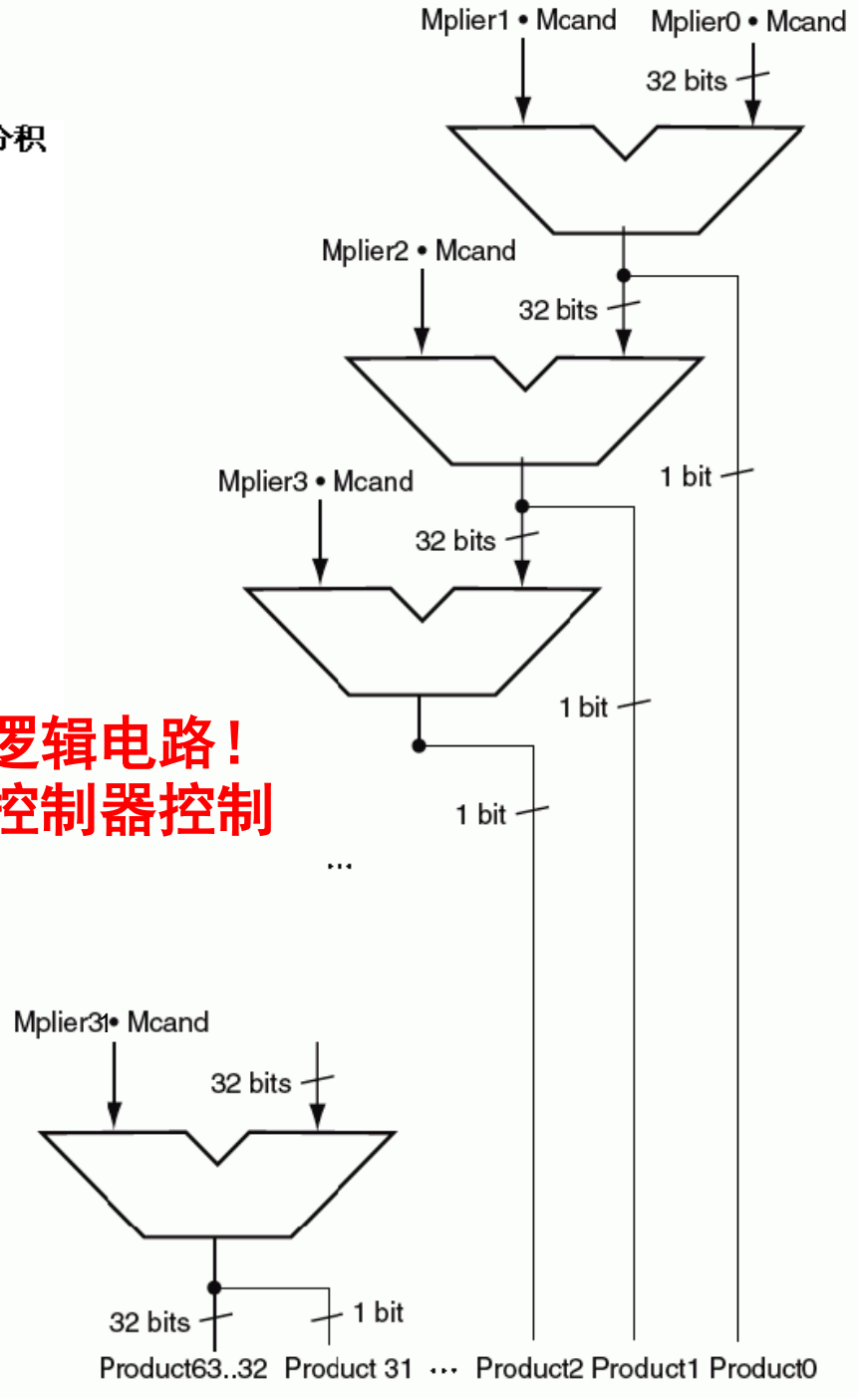
- 前面介绍的乘法部件的特点
  - 通过一个ALU多次做“加/减+右移”来实现
    - 一位乘法：约n次“加+右移”
    - 两位乘法：约n/2次“加+右移”

  所需时间随位数增多而加长，由时钟和控制电路控制
- 设计快速乘法部件的必要性
  - 大约1/3是乘法运算
- 快速乘法器的实现（由特定功能的组合逻辑单元构成）
  - 流水线方式/硬件叠加方式（如：阵列乘法器，附录6B）
    - 所有部分积并行相加，组织为二叉树结构，例如：16→8→4→2→结果
  - Booth算法(Andrew Donald Booth, 1950) + Wallace Tree(Chris Wallace, 1964)
    - 华莱士树（Wallace Tree）：硬件快速把n个数相加归约为2个数的相加，从而加速多个部分积相加速度【体系结构课程会继续介绍】

用“空间”换“时间”

流水线方式的快速乘法器



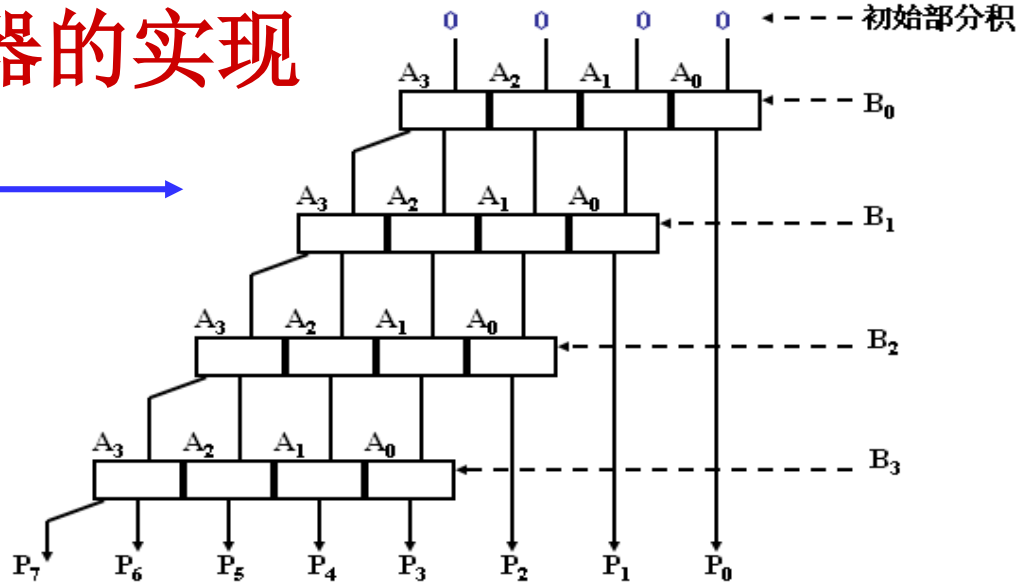


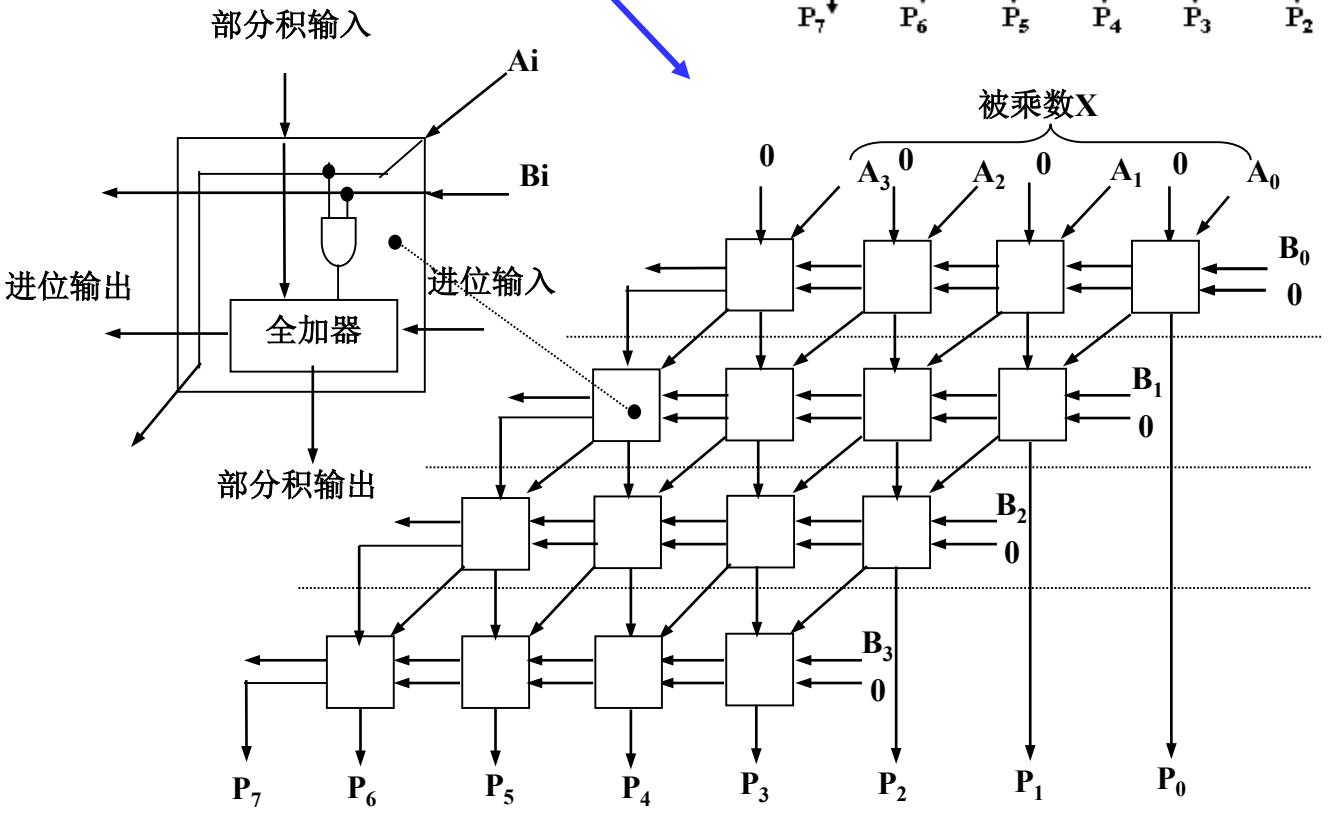
- 为乘数的每位提供一个n位加法器
- 每个加法器的两个输入端分别是：
  - 本次乘数对应的位与被乘数相与的结果（即：0或被乘数）
  - 上次部分积
- 每个加法器的输出分为两部分：
  - 和的最低有效位(LSB)作为本位乘积
  - 进位和高31位的和数组成一个32位数作为本次部分积

组合逻辑电路！
无需控制器控制

流水线式阵列乘法器的实现

- 手算乘法过程
- 阵列乘法器





速度仅取决于逻辑门和加法器的传输延迟

无符号阵列乘法器

增加符号处理电路、乘前及乘后求补电路，即可实现带符号数乘法器。

Google Tensor Processing Unit
(paper released on Apr 5, 2017)

In-Datacenter Performance Analysis of a Tensor Processing Unit

Norman P. Jouppi, Cliff Young, Nishant Patil, David Patterson, Gaurav Agrawal, Raminder Bajwa, Sarah Bates, Suresh Bhatia, Nan Boden, Al Borchers, Rick Boyle, Pierre-luc Cantin, Clifford Chao, Chris Clark, Jeremy Coriell, Mike Daley, Matt Dau, Jeffrey Dean, Ben Gelb, Tara Vazir Ghaemmaghami, Rajendra Gottipati, William Gulland, Robert Hagmann, C. Richard Ho, Doug Hogberg, John Hu, Robert Hundt, Dan Hurt, Julian Ibarz, Aaron Jaffey, Alek Jaworski, Alexander Kaplan, Harshit Khaitan, Daniel Killebrew, Andy Koch, Naveen Kumar, Steve Lacy, James Laudon, James Law, Diemthu Le, Chris Leary, Zhuyuan Liu, Kyle Lucke, Alan Lundin, Gordon MacKean, Adriana Maggiore, Maire Mahony, Kieran Miller, Rahul Nagarajan, Ravi Narayanaswami, Ray Ni, Kathy Nix, Thomas Norrie, Mark Omernick, Narayana Penukonda, Andy Phelps, Jonathan Ross, Matt Ross, Amir Salek, Emad Samadiani, Chris Severn, Gregory Sizikov, Matthew Snelham, Jed Souter, Dan Steinberg, Andy Swing, Mercedes Tan, Gregory Thorson, Bo Tian, Horia Toma, Erick Tuttle, Vijay Vasudevan, Richard Walter, Walter Wang, Eric Wilcox, and Doe Hyun Yoon
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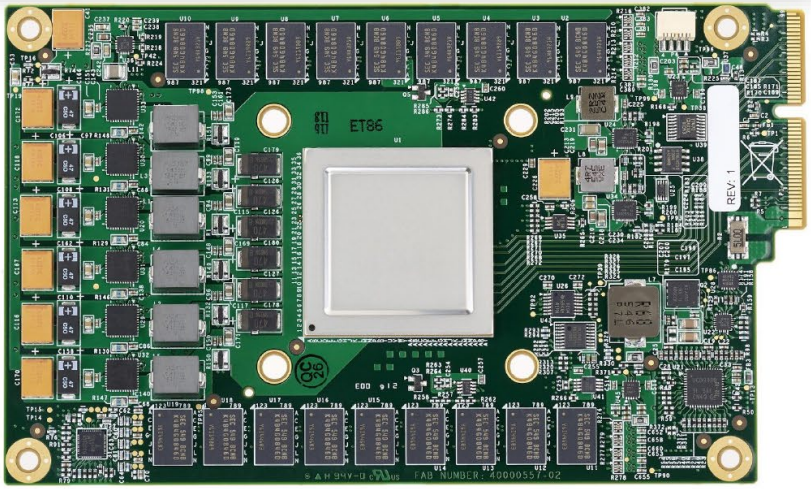


Figure 3. TPU Printed Circuit Board. It can be inserted in the slot for an SATA disk in a server, but the card uses PCIe Gen3 x16.

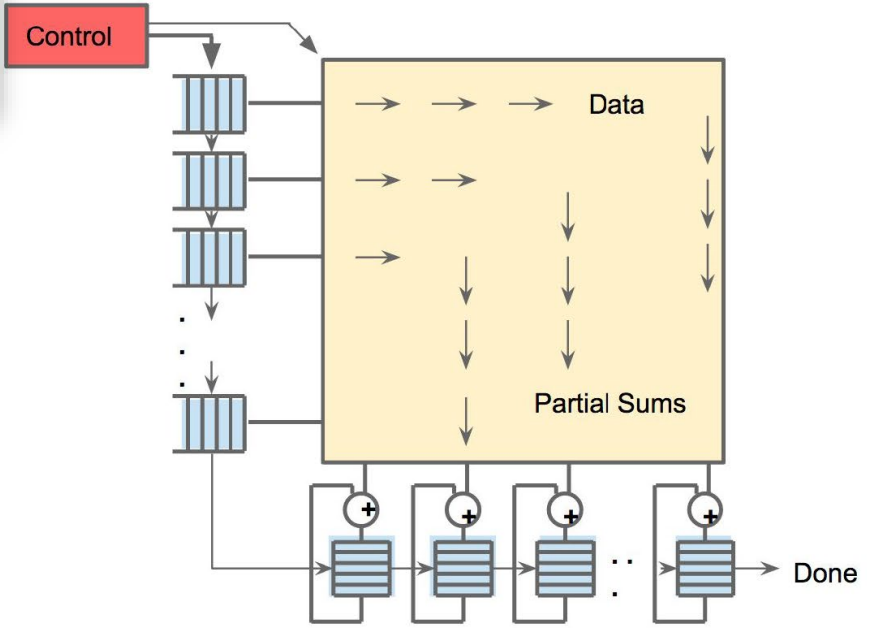


Figure 4. Systolic data flow of the Matrix Multiply Unit. Software has the illusion that each 256B input is read at once, and they instantly update one location of each of 256 accumulator RAMs.

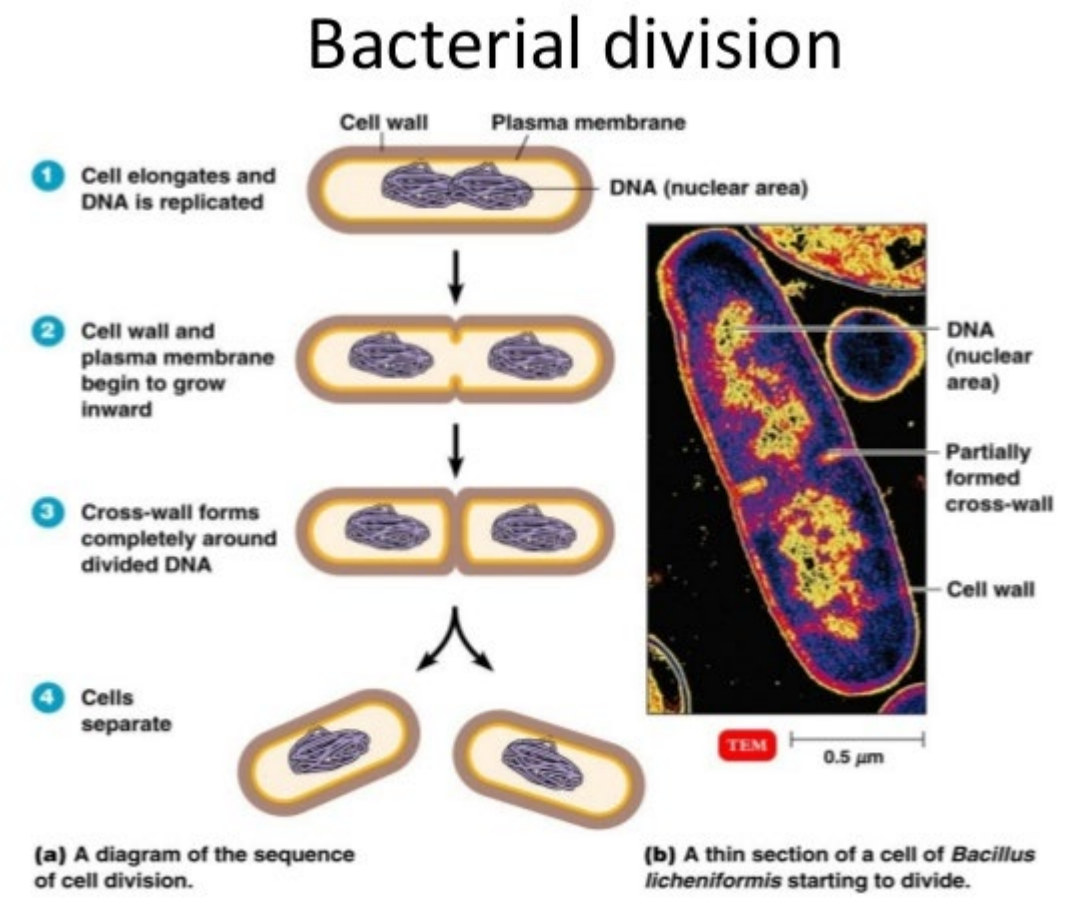
Norman P. Jouppi et al., In-Datacenter Performance Analysis of a Tensor Processing Unit, ISCA 2017

乘法小结

- 整数乘法与小数乘法完全相同
  可用 逗号 代替小数点
- 原码乘　符号位 单独处理
  补码乘　符号位 自然形成
- 原码乘去掉符号位运算　即为无符号数乘法
- 不同的乘法运算需有不同的硬件支持

Why are bacteria bad at math?

Because they multiply by dividing.



四、除法运算

6.3

1. 分析笔算除法

$x = -0.1011$　$y = 0.1101$　求 $x \div y$

```
                    0.1 1 0 1   (商)
              ┌──────────────
0.1101 ) 0.1011 0   (被除数)
         0.0 1 1 0 1  (右移的除数)
         ─────────
         0.0 1 0 0 1 0  (中间余数)
           0.0 0 1 1 0 1
           ─────────
           0.0 0 0 1 0 1 0 0
             0.0 0 0 0 1 1 0 1
             ─────────
             0.0 0 0 0 0 1 1 1  (余数)
```

(除数)

这里都是余数的绝对值。最后一步得到的是真正余数的绝对值R*，而R的实际符号位应与被除数一致，即从被除数直接获得，所以真正余数应为 -0.00000111

- ✓商符单独处理
- ？心算上商(是否够减，被除数或中间余数和除数比大小)
- ？余数不动低位补“0”减右移一位的除数
- ？上商位置不固定(商是从高位向低位逐位求得)

$x \div y = -0.1101$　商符心算求得

余数 0.0000 0111

这是余数的绝对值R*

真正余数R = - 0.00000111

2. 笔算除法和机器除法的比较 6.3

笔算除法	机器除法
商符单独处理	被除数与除数符号位异或
心算上商	$\|x\|-\|y\|>0$ (够减) 上商 1 $\|x\|-\|y\|<0$ (不够减) 上商 0
余数 不动 低位补“0” 减右移一位 的除数	余数 左移一位 低位补“0” 减 除数
2 倍字长加法器	1 倍字长加法器
上商位置 不固定	在寄存器 最末位上商，并且部分商左移一位

3. 原码除法

以小数为例

$$[x]_{原} = x_0.\, x_1x_2 \cdots x_n$$

$$[y]_{原} = y_0.\, y_1y_2 \cdots y_n$$

$$[\frac{x}{y}]_{原} = (x_0 \oplus y_0).\ \frac{x^*}{y^*}$$

式中 $x^* = 0.\, x_1x_2 \cdots x_n$ 为 x 的绝对值

$y^* = 0.\, y_1y_2 \cdots y_n$ 为 y 的绝对值

商的符号位单独处理 $x_0 \oplus y_0$　　数值部分为绝对值相除 $\frac{x^*}{y^*}$

约定

小数定点除法 $x^* < y^*$

被除数不等于 0

除数不能为 0

(在除法运算之前先做检查)

整数定点除法 $x^* > y^*$

商的位数与其他操作数位数相同

(位数达到一致则停止运算)

(1) 恢复余数法

例6.24 $x = -0.1011$ $y = -0.1101$ 求 $[\frac{x}{y}]_{原}$

解：$[x]_{原} = 1.1011$ $[y]_{原} = 1.1101$ $[y^*]_{补} = 0.1101$ $[-y^*]_{补} = 1.0011$

① $x_0 \oplus y_0 = 1 \oplus 1 = 0$

②

被除数（余数）	商	说　明
0.1011	0.0000	
+ 1.0011		$+[-y^*]_{补}$ (进行x^*-y^*作比较)
1.1110	0	余数为负，上商 0
+ 0.1101		恢复余数　$+[y^*]_{补}$
0.1011	0	恢复后的余数
1.0110	0	←1 (余数和商同时左移)
+ 1.0011		$+[-y^*]_{补}$
0.1001	01	余数为正，上商 1
1.0010	01	←1
+ 1.0011		$+[-y^*]_{补}$

逻辑左移

为什么是逻辑左移？

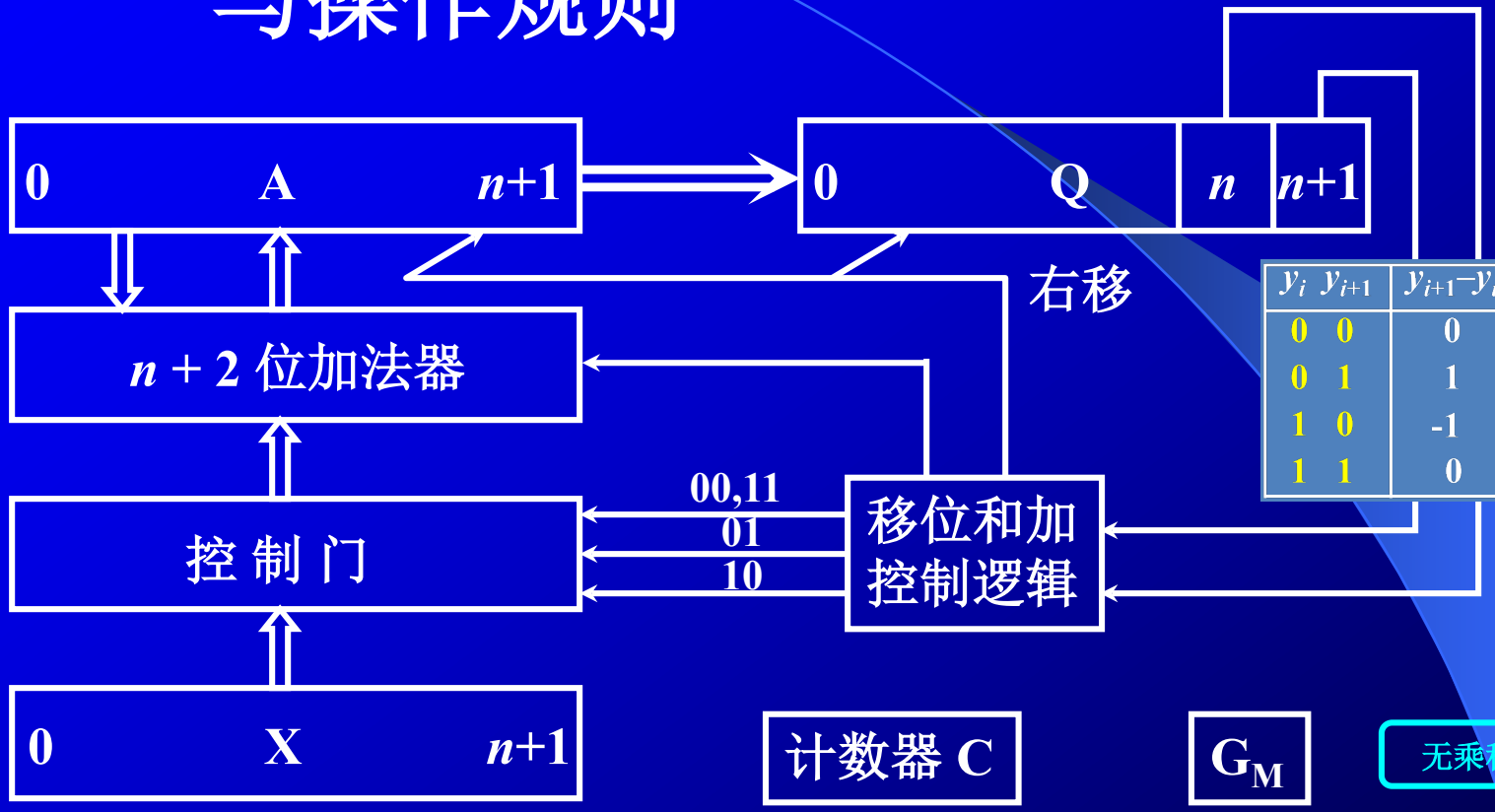
逻辑左移


主讲人 陈云霁
“全国五一劳动奖章”获得者
中国科学院计算技术研究所副所长、研究员
更是我愿意终其一生


Gordon Moore
Co-founder and Chairman Emeritus
Intel Corporation

复习：Booth 算法的硬件配置与操作规则

6.3



y_i y_{i+1}	$y_{i+1}-y_i$	部分积的操作
0 0	0	→1
0 1	1	$+[x]_{补}$ →1
1 0	-1	$+[-x]_{补}$ →1
1 1	0	→1

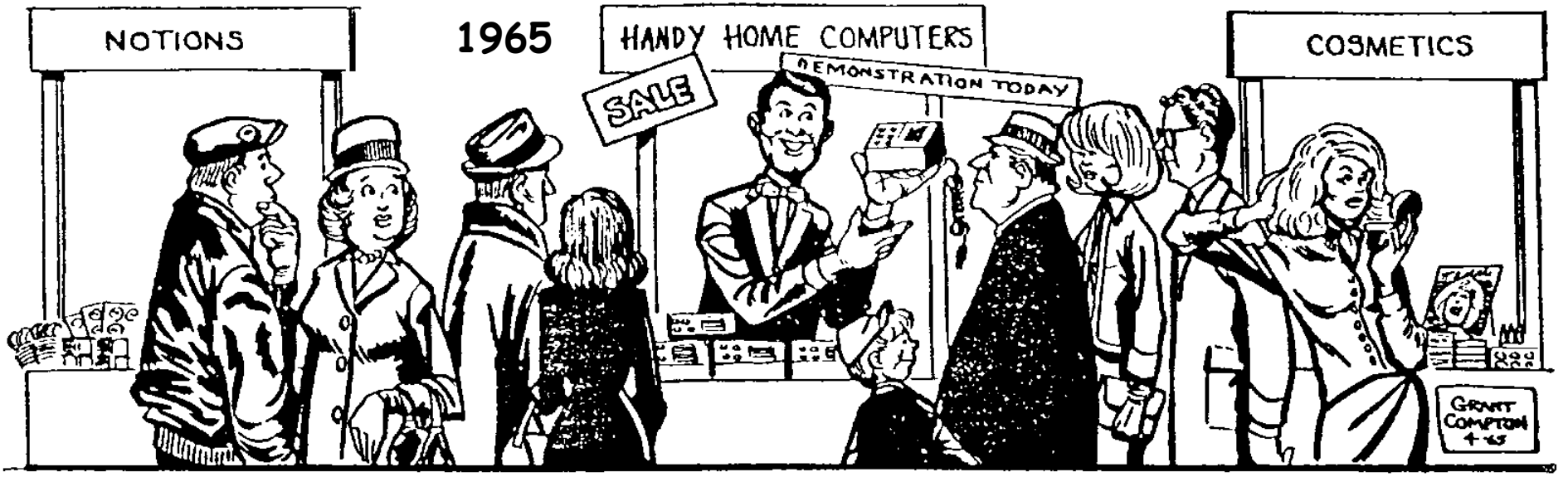
A、X、Q均为$n+2$位寄存器(A与X为双符号位，Q为单符号位+附加位)

移位和加操作受乘数的末两位控制

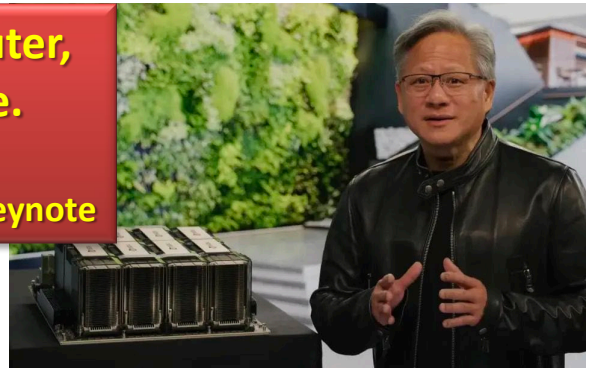
Best sellers in the BOOTH

2023

ChatGPT、GPT-4、Bard等大模型支撑下的
AIGC服务及其底层的软硬件系统与AI芯片

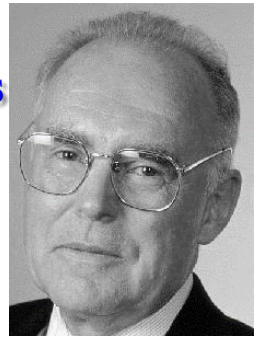


"Generative AI is a new kind of computer, one we program in human language. Now, everyone is a programmer"
---Jensen Huang, NVIDIA's Spring GTC 2023 Keynote



AIGC: Artificial Intelligence Generated Content
https://openai.com/research/gpt-4
https://bard.google.com
https://www.anandtech.com/show/18782/the-nvidia-gtc-spring-2023-keynote-live-blog-800am-pt1500-utc

Moore's Law Predicts: 2X Transistors / chip every 2 years



Gordon Moore
Intel Co-founder
1929/1/3-2023/3/24

The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the

The author

Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

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a two-mil square can also contain several kilohms of resistance or a few diodes. This allows at least 500 components per linear inch or a quarter million per square inch. Thus, 65,000 components need occupy only about one-fourth a square inch.

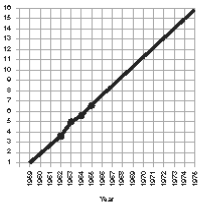
On the silicon wafer currently used, usually an inch or more in diameter, there is ample room for such a structure if the components can be closely packed with no space wasted for interconnection patterns. This is realistic, since efforts to achieve a level of complexity above the presently available integrated circuits are already underway using multilayer metalization patterns separated by dielectric films. Such a density of components can be achieved by present optical techniques and does not require the more exotic techniques, such as electron beam operations, which are being studied to make even smaller structures.

Increasing the yield

There is no fundamental obstacle to achieving device yields of 100%. At present, packaging costs so far exceed the cost of the semiconductor structure itself that there is no incentive to improve yields, but they can be raised as high as

is economically justified. No barrier exists comparable to the thermodynamic equilibrium considerations that often limit yields in chemical reactions; it is not even necessary to do any fundamental research or to replace present processes. Only the engineering effort is needed.

In the early days of integrated circuitry, when yields were



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The establishment

Integrated electronics is established today. Its techniques are almost mandatory for new military systems, since the reliability, size and weight required by some of them is achievable only with integration. Such programs as Apollo, for manned moon flight, have demonstrated the reliability of integrated electronics by showing that complete circuit functions are as free from failure as the best individual transistors.

Most companies in the commercial computer field have machines in design or in early production employing integrated electronics. These machines cost less and perform better than those which use "conventional" electronics.

Instruments of various sorts, especially the rapidly increasing numbers employing digital techniques, are starting to use integration because it cuts costs of both manufacture and design.

The use of linear integrated circuitry is still restricted primarily to the military. Such integrated functions are expensive and not available in the variety required to satisfy a major fraction of linear electronics. But the first applications are beginning to appear in commercial electronics, particularly in equipment which needs low-frequency amplifiers of small size.

Reliability counts

In almost every case, integrated electronics has demonstrated high reliability. Even at the present level of production—low compared to that of discrete components—it offers reduced systems cost, and in many systems improved performance has been realized.

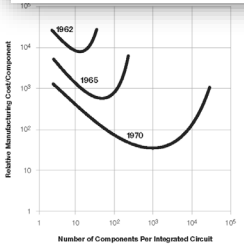
Integrated electronics will make electronic techniques more generally available throughout all of society, performing many functions that presently are done inadequately by other techniques or not done at all. The principal advantages will be lower costs and greatly simplified design—payoffs from a ready supply of low-cost functional packages.

For most applications, semiconductor integrated circuits will predominate. Semiconductor devices are the only reasonable candidates presently in existence for the active elements of integrated circuits. Passive semiconductor elements look attractive too, because of their potential for low cost and high reliability, but they can be used only if precision is not a prime requisite.

Silicon is likely to remain the basic material, although others will be of use in specific applications. For example, gallium arsenide will be important in integrated microwave functions. But silicon will predominate at lower frequencies because of the technology which has already evolved around it and its oxide, and because it is an abundant and relatively inexpensive starting material.

Costs and curves

Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate. For simple circuits, the cost per component is nearly inversely proportional to the number of components, the result of the



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grated stages of gain, giving high performance at cost, interspersed with relatively large tuning ele-

linear functions will be changed considerably. The nd tracking of similar components in integrated will allow the design of differential amplifiers of roved performance. The use of thermal feedback abilize integrated structures to a small fraction of ill allow the construction of oscillators with crys-

n the microwave area, structures included in the f integrated electronics will become increasingly The ability to make and assemble components pared with the wavelengths involved will allow umped parameter design, at least in the lower fre- to predict at the present time just how of the microwave area by integrated ssful realization of such items example, using a multiplicity r sources, could completely

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