EXPT NO.: 9

DESIGN OF 4-BIT SHIFT REGISTERS

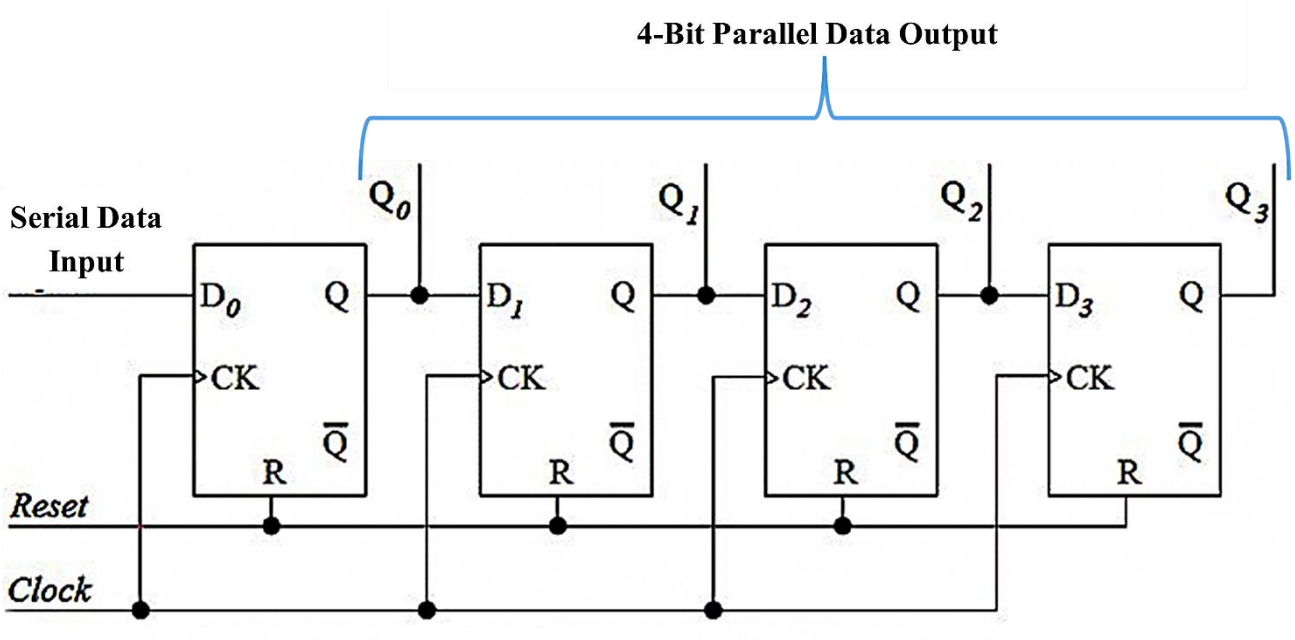
AIM:

To design and simulate 4-bit serial-in and parallel-out (SIPO) and 4-bit parallel-in and serial-out (PISO) shift registers.

4-BIT SERIAL-IN AND PARALLEL-OUT (SIPO) SHIFT REGISTER:

The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as the Serial-In Parallel-Out shift register. The logic circuit given below shows a serial-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal is connected in addition to the clock signal to all 4 flip flops in order to RESET them. The output of the first flip-flop is connected to the input of the next flip flop and so on. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip-flop.

Block diagram of SIPO:



In the diagram, the first flip flop output 'Q_0' is connected to the second flip flop input 'D_1'. The second flip flops output 'Q_1' is connected to the third flip flops input D_2, and the third flip flops output 'Q_2' is connected to the fourth flip flops input 'DD. Here, Q_0, Q_1, Q_2, and Q_3 are data outputs.

Initially, all the output will become zero so without CLK pulse; all the data will become zero. Let's take a 4-bit data input example like 1101. If we apply the first clock pulse '1' to the first flip-flop, the data to be entered into the FF and Q_0 becomes '1', and remaining all the outputs like Q_1, Q_2, and Q_3 will become zero. So, the first data output is '0001'

If we apply the second clock pulse as '1' to the first flip-flop then Q_0 becomes '1', Q_1 becomes '1', Q_2 becomes '0' and Q_3 becomes '0'. So, the second data output will become '0011' due to the shift right process.

If we apply the third clock pulse as '1' to the first flip flop then Q_0 becomes '1', Q_1 becomes '1', Q_2 becomes '1' and Q_3 becomes '0'. So, the third data output will become '0111' due to the shift right process.

If we apply the fourth clock pulse as '1' to the first flip flop then Q_0 becomes '1', Q_1 becomes '1', Q_2 becomes '1' and Q_3 becomes '1'. So, the third data output will become '1111' due to the shift right process.

Truth Table of SIPO:

CLOCK PULSE No.	SERIAL INPUT	PARALLEL OUTPUT			
		Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0
1	1	0	0	0	1
2	1	0	0	1	1
3	1	0	1	1	1
4	1	1	1	1	1

The i/o ports needed to be declared for the formation of SIPO is given below:

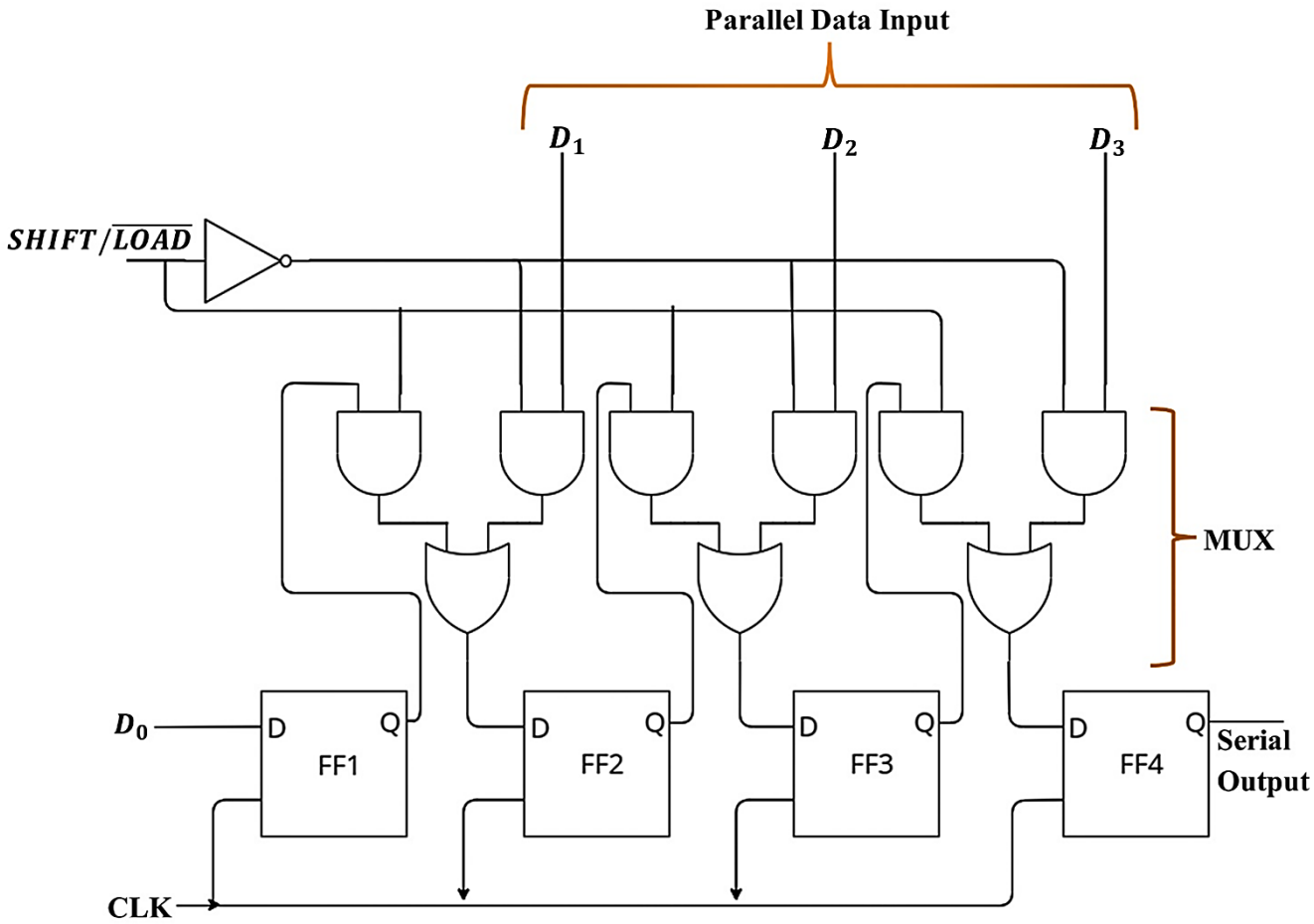
Port Name	INPUT/OUTPUT	Bus
Data	In	No
Rst	In	No
CLK	In	No
Q	Out	4-Bit Bus (3 downto 0)

- **NB: Use temporary variable where ever necessary.**

4-BIT PARALLEL-IN AND SERIAL-OUT (PISO) SHIFT REGISTER:

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and produces a serial output is known as a Parallel-In Serial-Out shift register. The logic circuit given below shows a parallel-in-serial-out shift register. The circuit consists of four D flip-flops which are connected. The clock input is directly connected to all the flip-flops but the input data is connected individually to each flip-flop through a multiplexer at the input of every flip-flop. The output of the previous flip-flop and parallel data input are connected to the input of the MUX and the output of MUX is connected to the next flip-flop. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip-flop.

Block diagram of PISO:



Truth Table of PISO:

CLOCK PULSE No.	PARALLEL INPUT				SERIAL OUTPUT	CHANGE IN 4-BIT No.			
	D_3	D_2	D_1	D_0		D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	0
2	1	1	1	1	1	1	1	0	0
3	1	1	1	1	1	1	0	0	0
4	1	1	1	1	1	0	0	0	0

The i/o ports needed to be declared for the formation of PISO is given below:

Port Name	INPUT/OUTPUT	Bus
Data	In	4-Bit Bus (3 downto 0)
Rst	In	No
CLK	In	No
Load	In	No
Dout_vector	Out	4-Bit Bus (3 downto 0)
Dout	Out	No

- **NB: Use temporary variable where ever necessary.**