ECE-GY 6913, Computing System Architecture

Project (Phase II)

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Schematic for a five stage processor:

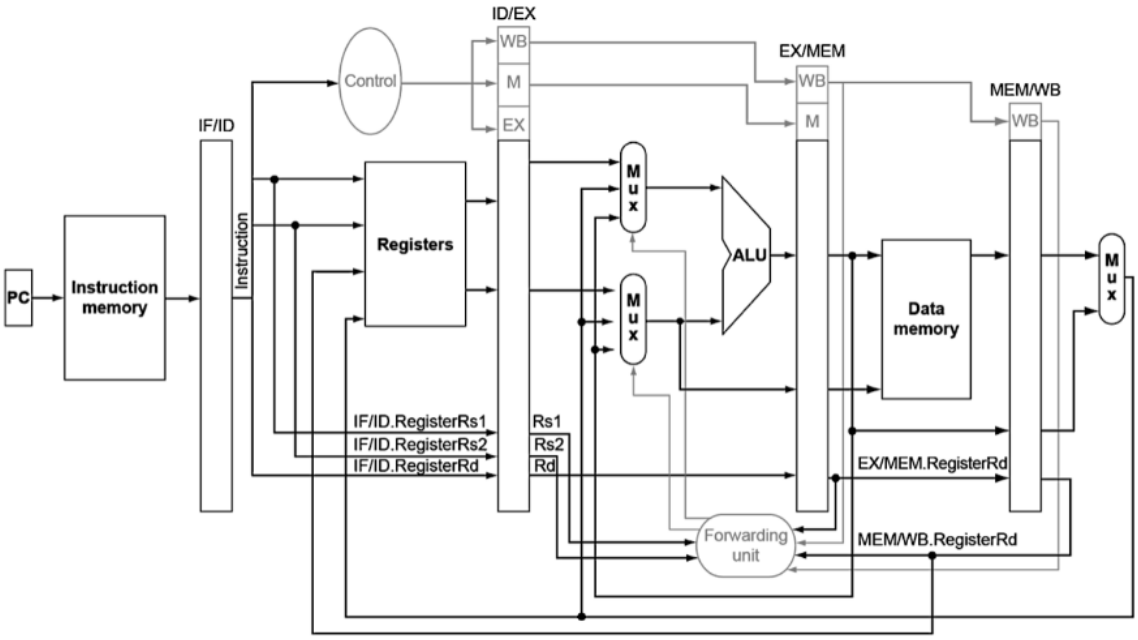

Fig: 1.1 Schematic for a five-stage processor

Key components in the five stage processor:

- Instruction Register (IR): Holds the fetched instruction from memory.
- Program Counter (PC): Keeps track of the address of the next instruction to be fetched.
- Register File: Stores intermediate results and operands.
- ALU (Arithmetic Logic Unit): Performs arithmetic and logical operations.
- Control Unit: Directs the flow of data based on the instruction opcode.
- Data Memory: Stores data values accessed by the CPU.
- Latches: Hold data between stages to ensure proper synchronization.

Five-stage processor stages:

- Instruction Fetch (IF):
    - PC is read to fetch the next instruction from memory.
    - Instruction is loaded into the Instruction Register (IR).
    - PC is incremented to point to the next instruction.
- Instruction Decode (ID):
    - The instruction in IR is decoded to identify the opcode and operands.
    - Source registers are read from the register file.
    - Operation to be performed is determined based on the opcode.
- Execute (EX):
    - Arithmetic or logical operations are performed by the ALU using the fetched operands.
    - Address calculations for memory access may be done in this stage if needed.
- Memory Access (MEM):
    - If the instruction is a load or store, data is accessed from or written to data memory based on the calculated address.
- Write Back (WB):
    - The result of the operation is written back to the destination register in the register file.

Important concepts to consider:

- Pipelining:

The key concept of a five-stage processor is that while one instruction is in the "Execute" stage, another instruction can be simultaneously in the "Fetch" stage, allowing for parallel processing and increased performance.

- Stalls and Hazards:

Potential issues like data dependencies between instructions might require pipeline stalls to ensure correct execution.

- Instruction Set Architecture (ISA):

The design of the processor's instruction set will influence the complexity of each stage and the overall pipeline structure.

CPI, Total execution cycles, and Instructions per cycle

The CPI, total execution cycles, and instructions per cycle are printed in PerformanceMetrics.txt file for each testcases.

Compare the results from both the single stage and five stage pipelined processor implementations and explain why one is better than the other.

Five-Stage Processor Advantages

- Higher Throughput: The rate of instruction execution increases significantly.
- Parallel Instruction Execution: More instructions can be processed simultaneously.
- Optimized ALU Design: Faster Arithmetic Logic Units (ALUs) are feasible due to pipelining.
- Higher Clock Frequency: The clock speed of a pipelined CPU surpasses that of a single-stage processor, leading to reduced execution time.
- Enhanced Performance: Overall CPU performance is greatly improved.

Single-Stage Processor Advantages

- Simpler Design: Easier to design and implement compared to a pipelined processor.
- Lower Instruction Latency: Instructions experience less latency.
- Predictable Throughput: Estimating performance is more straightforward.

- Reduced Hazard Issues: Minimal problems with branch hazards.
- Shorter Execution Time: Total time to execute instructions is generally less than in a pipelined setup.