

ASSIGNMENT-3

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IITH - Future Wireless Communications (FWC)

CONTENTS

1 QUESTION

1 Question

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- 1) The figure below shows the i^{th} full-adder block of a binary adder circuit. C_i is the input carry and C_{i+1} is the output carry of the circuit. Assume that each logic gate has a delay of 2 nanosecond, with no additional time delay due to the interconnecting wires. Of the inputs A_i , B_i are available and stable throughout the carry propagation, the maximum time taken for an input C_i to produce a steady-state output C_{i+1} is _____ nanosecond.

2 Components

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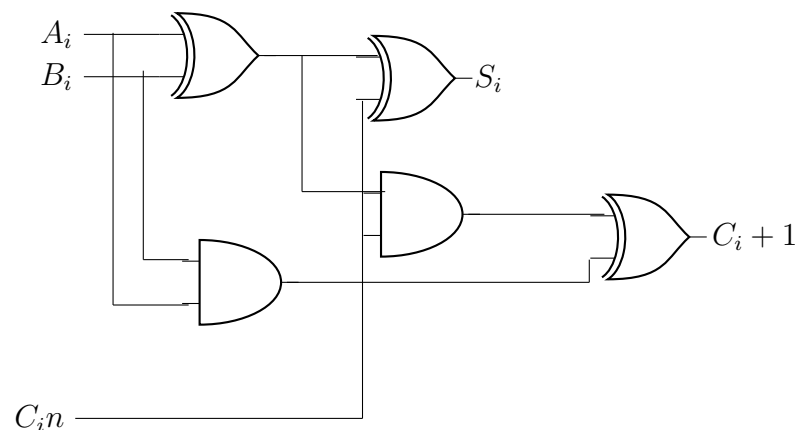


Fig. 1: full adder

2 COMPONENTS

Component	Values	Quantity
ArduinoUNO		1
JumperWires	M-M	5
Breadboard		1
LED		5
Resistor	220ohms	5

figure.a

3 TRUTHTABLE

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

TABLE I: Truth Table for "full adder"

4 K-MAPS

		BC_{in}			
		00	01	11	10
A	0		1		1
	1	1		1	

K-Map for sum equation.

$$S = A \oplus B \oplus C_{in} \quad (1)$$

		BC_{in}			
		00	01	11	10
A	0			1	
	1		1	1	1

K-Map for carry equation.

$$C_{out} = AB + C_{in}(A \oplus B) \quad (2)$$

5 IMPLIMENTATION

Arduino Pin	resistor	input	output
5	resistor	A	
4	resistor	B	
3	resistor	C_{in}	
8	resistor		S
9	resistor		C_{out}

TABLE II: implementation

6 PROCEDURE

- 1) Connect the circuit as per the above table.
- 2) The leds 1, 2 and 3 represent the values of inputs A , B and C_{in} respectively.
- 3) The leds 4 and 5 represent the output values i.e S and C_{out} respectively.
- 4) Execute the circuits using the below code.

<https://github.com/komatinenicharan/FWC/blob/main/platformia/code/ch.cpp>