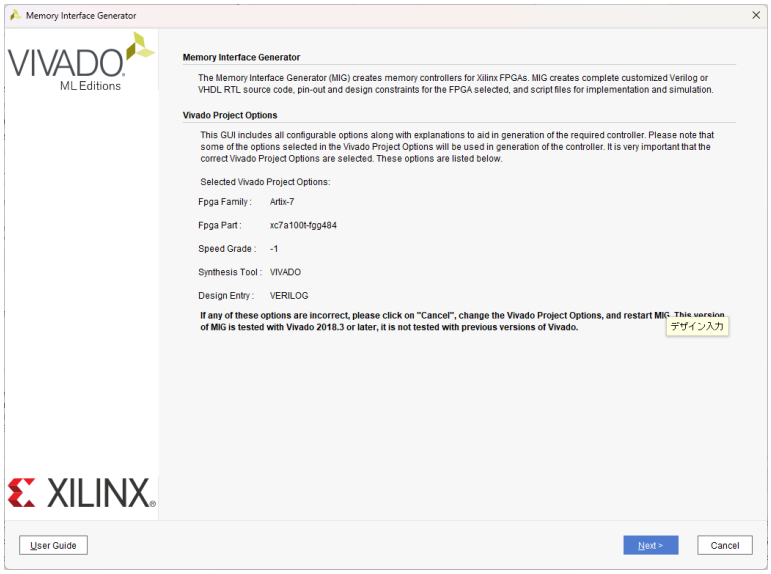
XCM-023-100T Memory Interface Generator

Next



・MIG Output Options

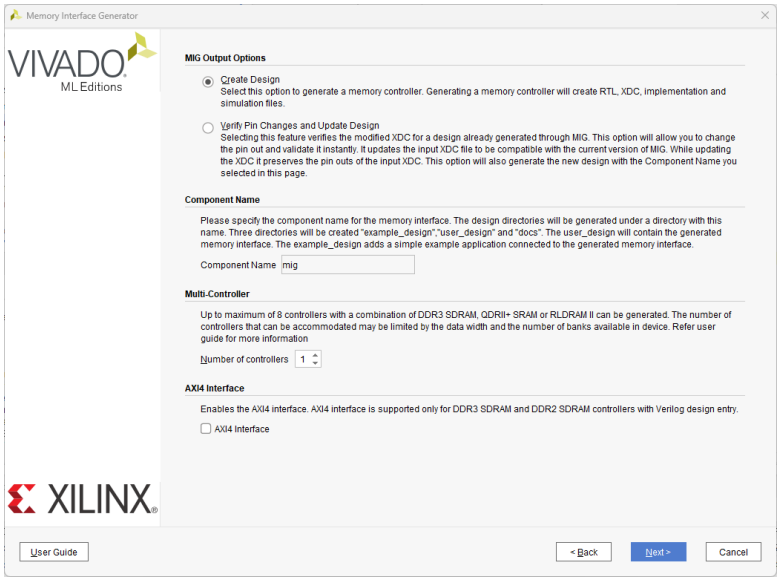
Create Design

・Component Name

Any Name

・Multi Controller

Number of controllers : 1

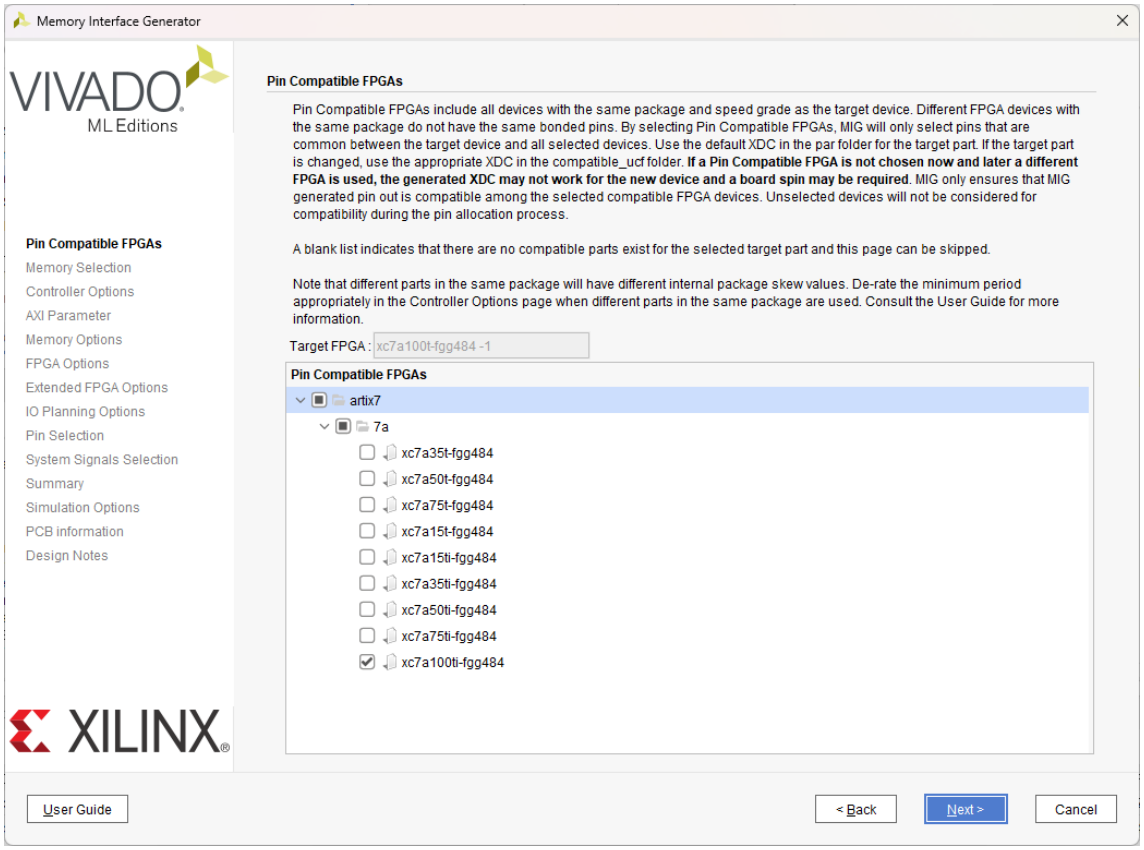


・Pin compatible FPGAs

Artix7

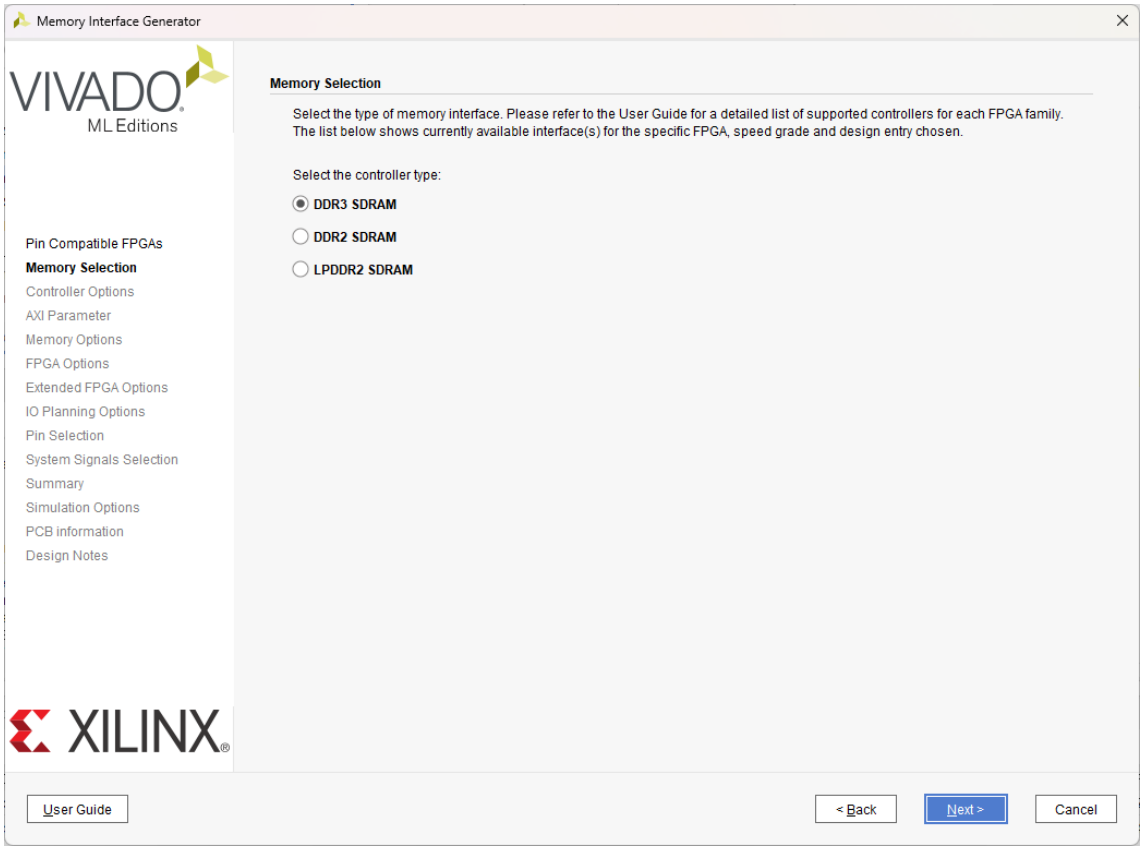
7a

xc7a100ti-fgg484



・Memory Selection

DDR3 SDRAM



- Clock period

  2500 ps
- Memory Type

  Components
- Memory Part

  MT41K64M16XX-107
- Memory Voltage

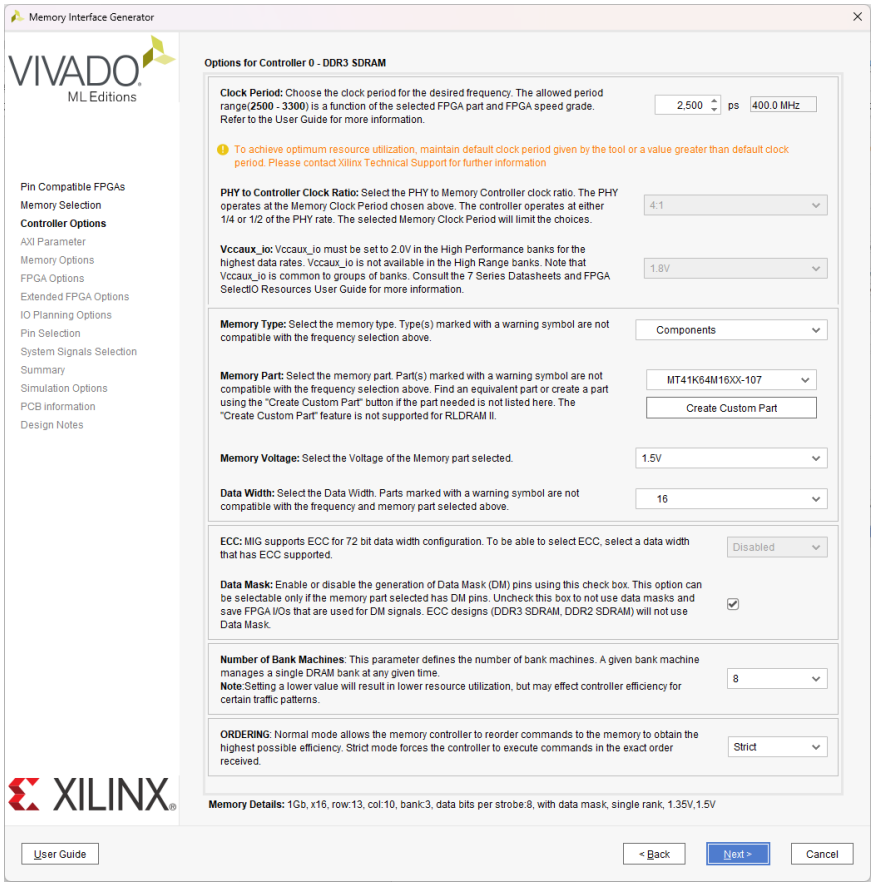
  1.5V
- Data Width

  16
- Data Mask

  True
- Number of Bank Machines

  8
- ORDERING

  Strict



・Input Clock Period

5000 ps

・Read Burst Type and Length

Sequential

・Output Driver Impedance Control

RZQ/7

・RTT

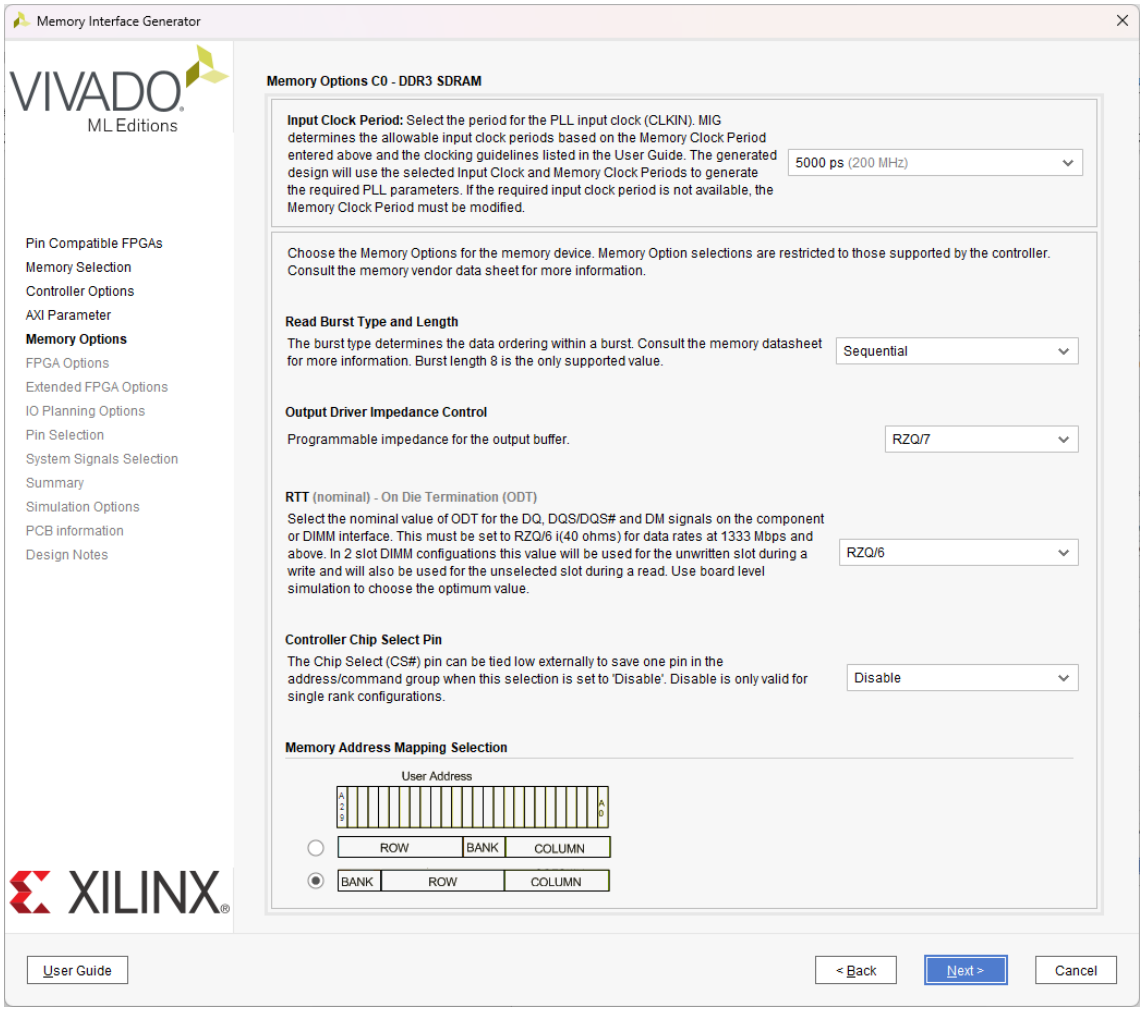
RZQ/6

・Controller Chip Select Pin

Disable

・Memory Address Mapping Selection

BANK ROW COLUMN



・System Clock

No Buffer

・Reference Clock

Use System Clock

・System Reset Polarity

ACTIVE LOW

・Debug Signals for Memory Controller

OFF

・Internal Vref

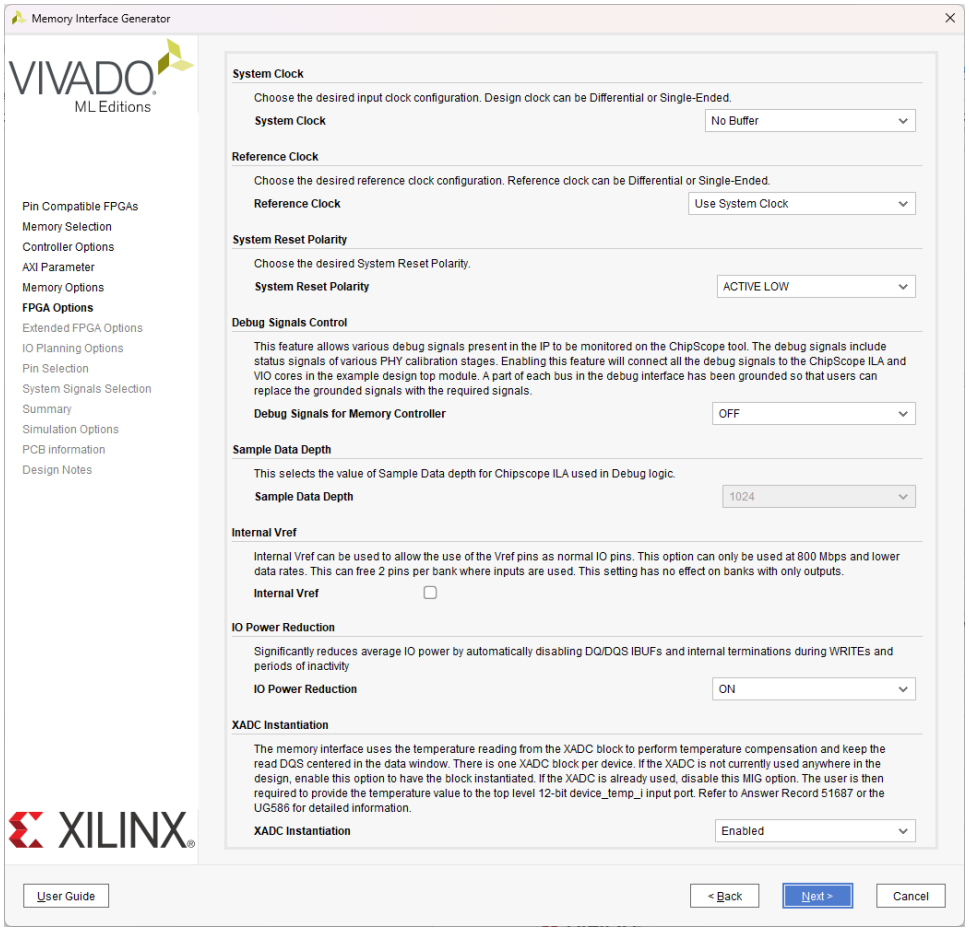
False

・IO Power Reduction

ON

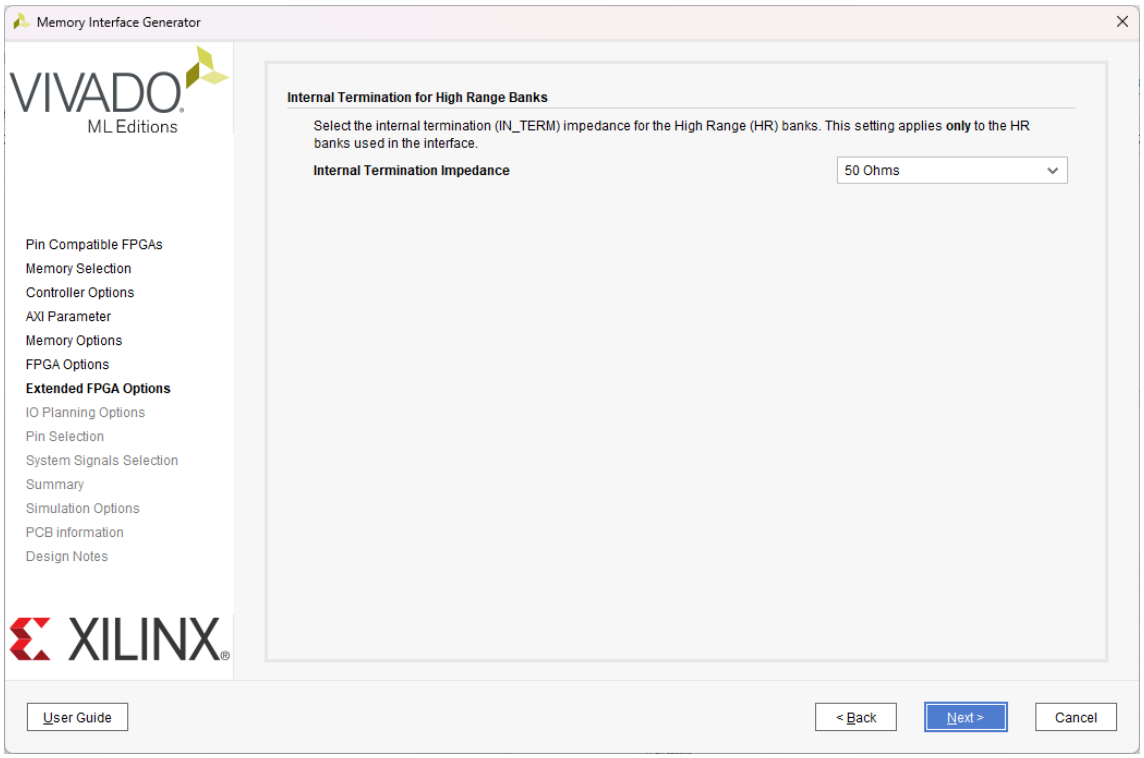
・XADC Instactiation

Enabled



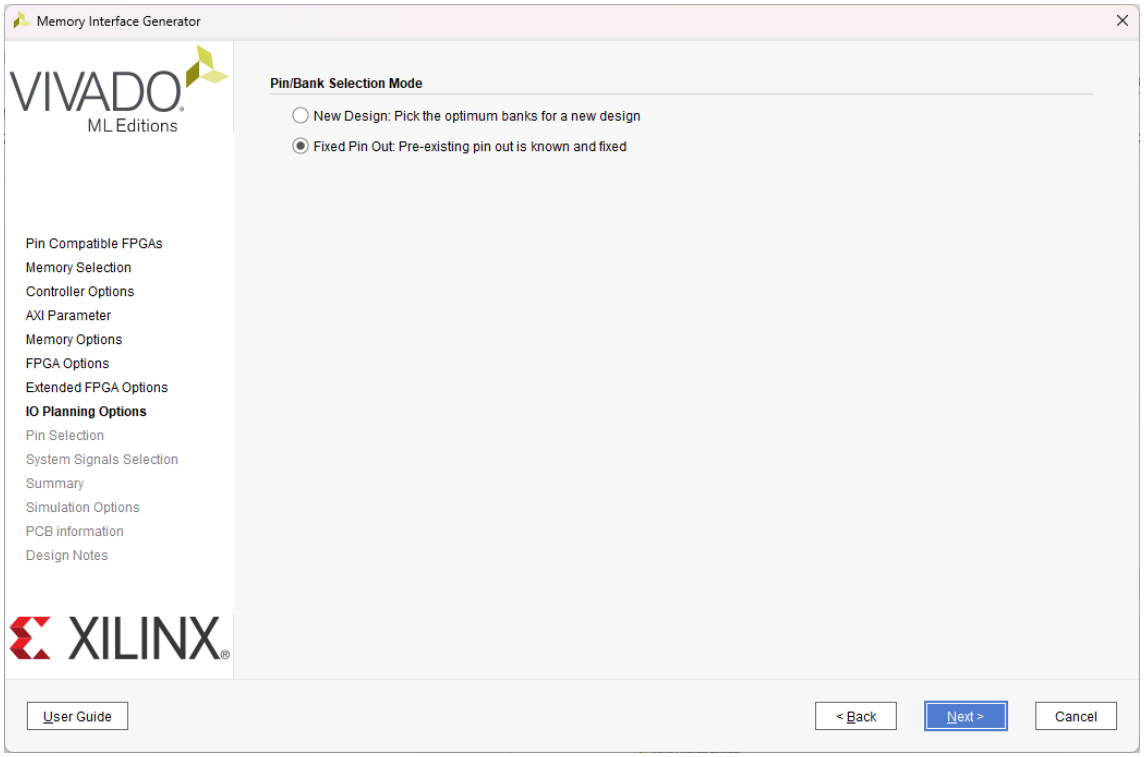
・Internal Termination Impedance

50 Ohms



・Pin/Bank Selection Mode

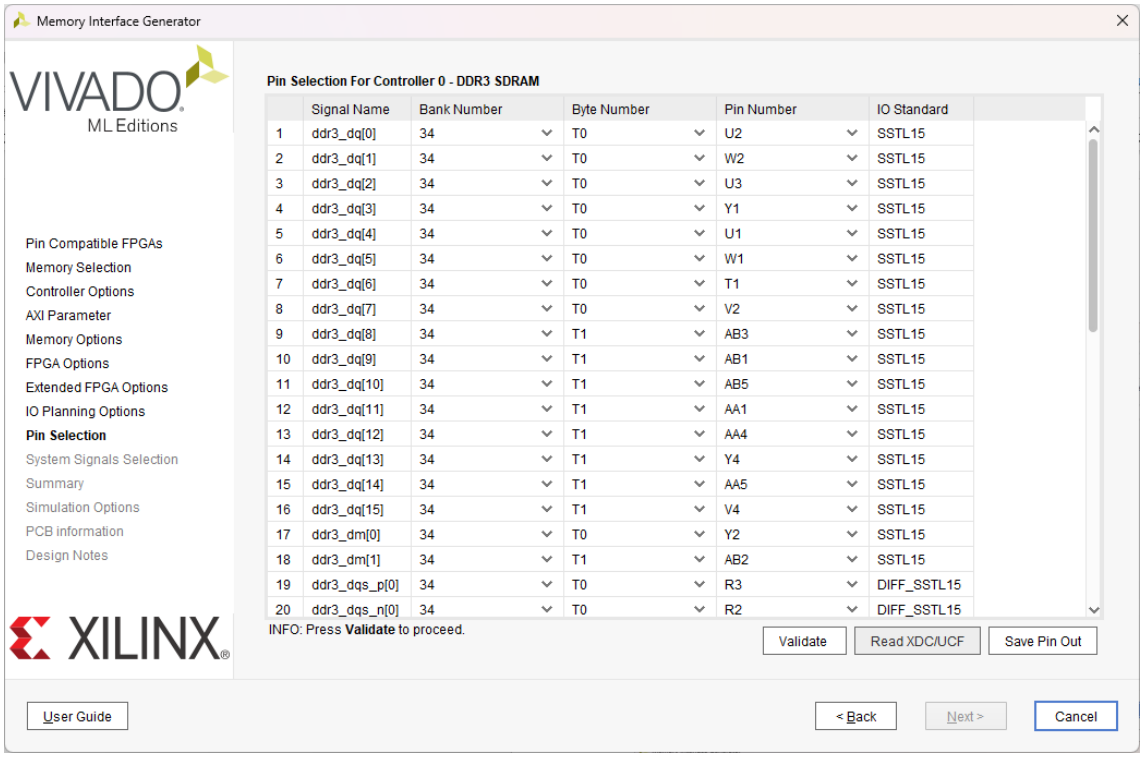
Fixed Pin Out: Pre-existing pin out is known and fixed



Read XDC/UCF

Download：https://github.com/komihori/XCM-023-100T/blob/main/XCM023Bmemorypinout.ucf

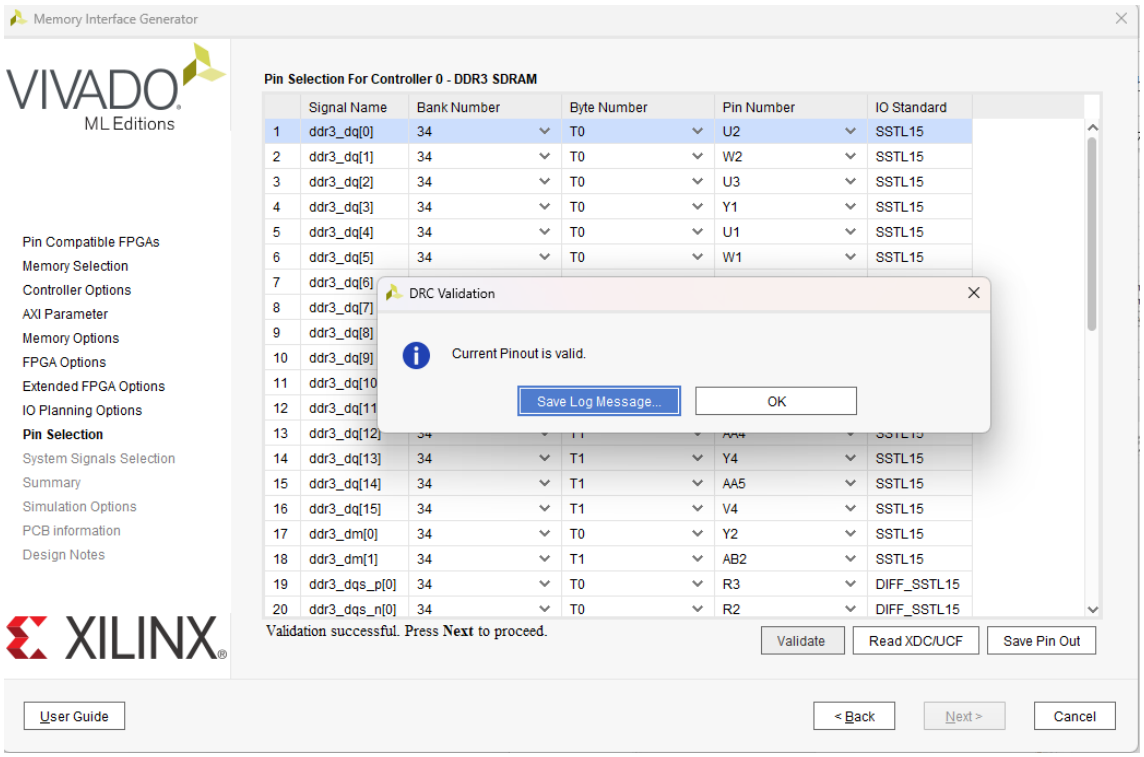
Open：XCM023Bmemorypinout.ucf



Click：Validate

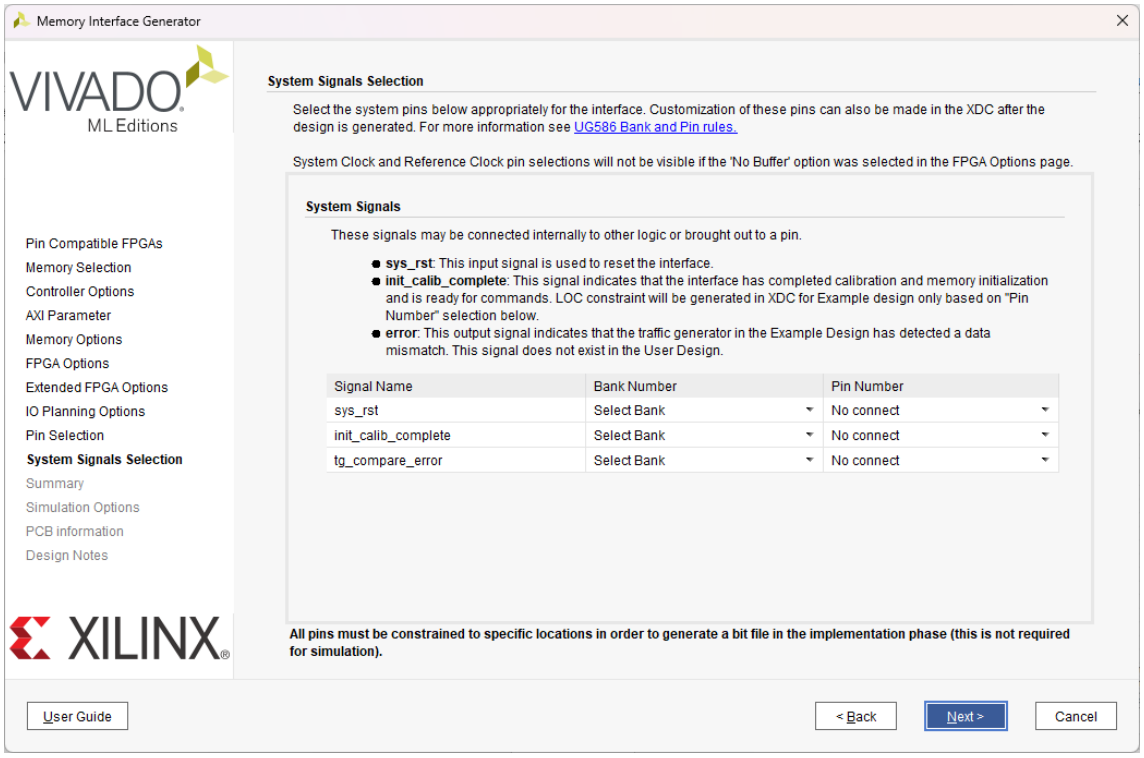
Click：OK

Click：Next

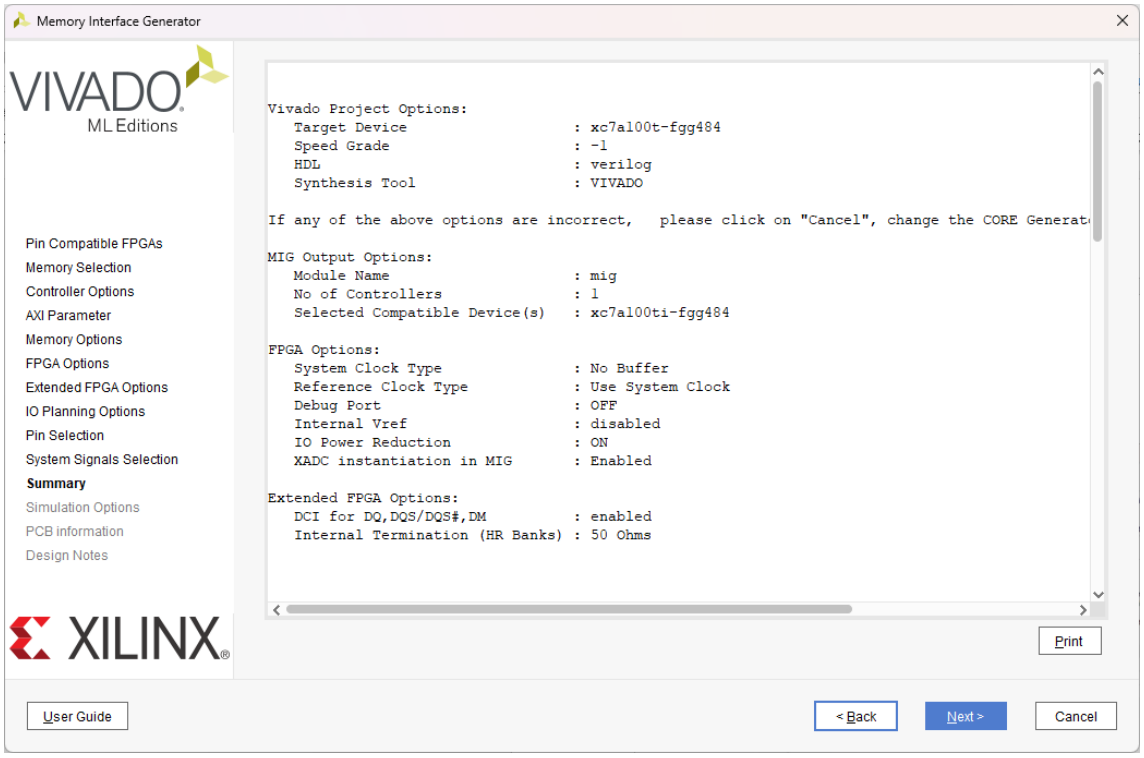


・System Signals

Signal Name	Bank Number	Pin Number
sys_rst	Select Bank	No Connect
init_calib_complete	Select Bank	No Connect
tg_compare_error	Select Bank	No Connect

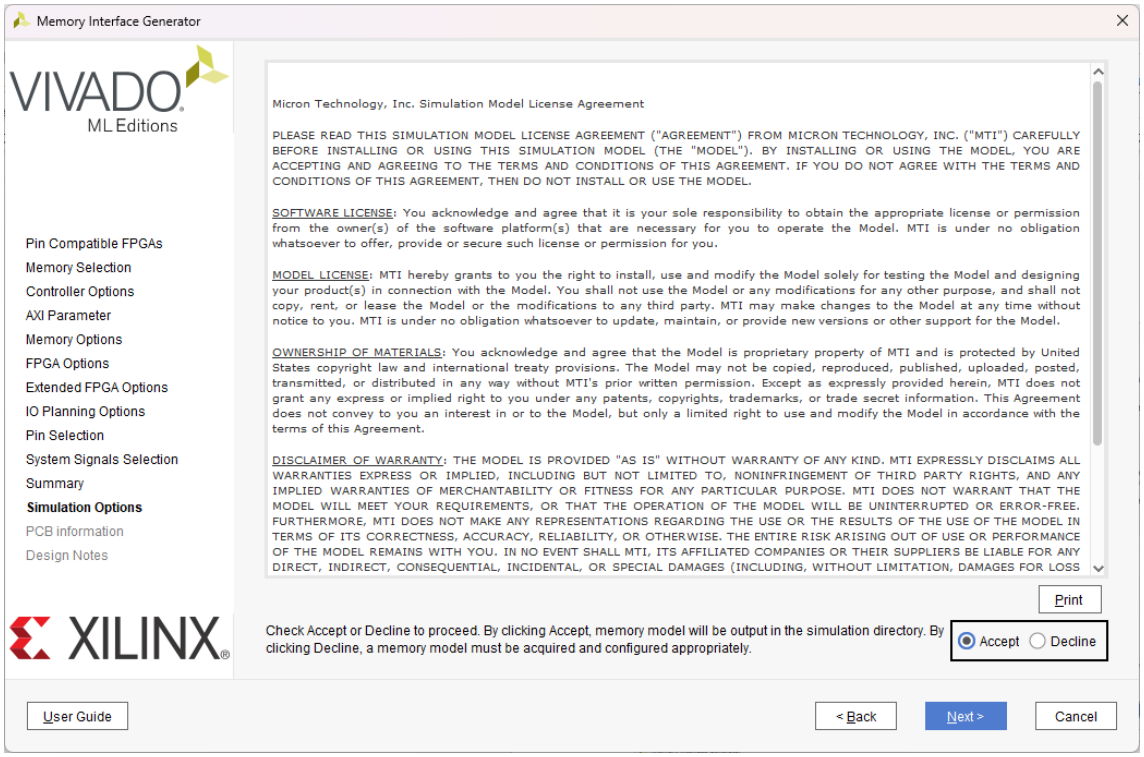


Click：Next

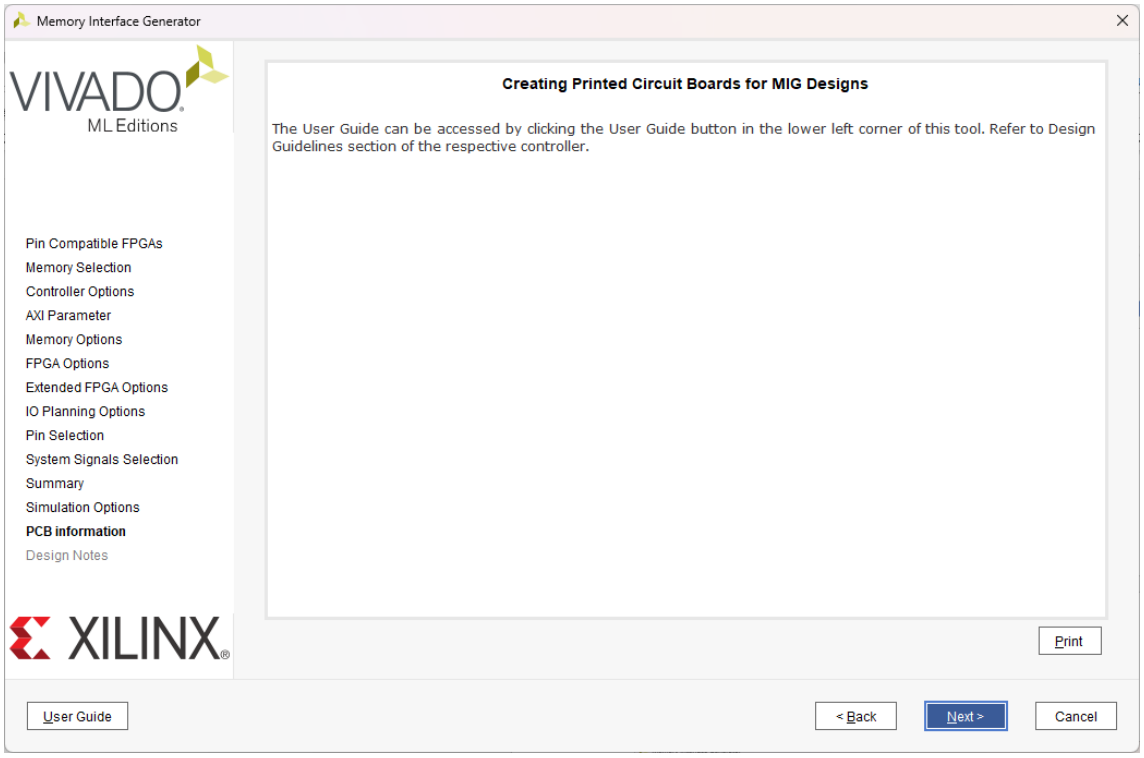

Memory Interface Generator
VIVADO
ML Editions
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Pin Selection
System Signals Selection
Summary
Simulation Options
PCB information
Design Notes
XILINX
Vivado Project Options:
Target Device : xc7a100t-fgg484
Speed Grade : -1
HDL : verilog
Synthesis Tool : VIVADO
If any of the above options are incorrect, please click on "Cancel", change the CORE Generat
MIG Output Options:
Module Name : mig
No of Controllers : 1
Selected Compatible Device(s) : xc7a100ti-fgg484
FPGA Options:
System Clock Type : No Buffer
Reference Clock Type : Use System Clock
Debug Port : OFF
Internal Vref : disabled
IO Power Reduction : ON
XADC instantiation in MIG : Enabled
Extended FPGA Options:
DCI for DQ,DQS/DQS#,DM : enabled
Internal Termination (HR Banks) : 50 Ohms
Print
User Guide
< Back
Next >
Cancel

Select：Accept

Click：Next



Click：Next


Memory Interface Generator
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XILINX
Creating Printed Circuit Boards for MIG Designs
The User Guide can be accessed by clicking the User Guide button in the lower left corner of this tool. Refer to Design Guidelines section of the respective controller.
Print
User Guide
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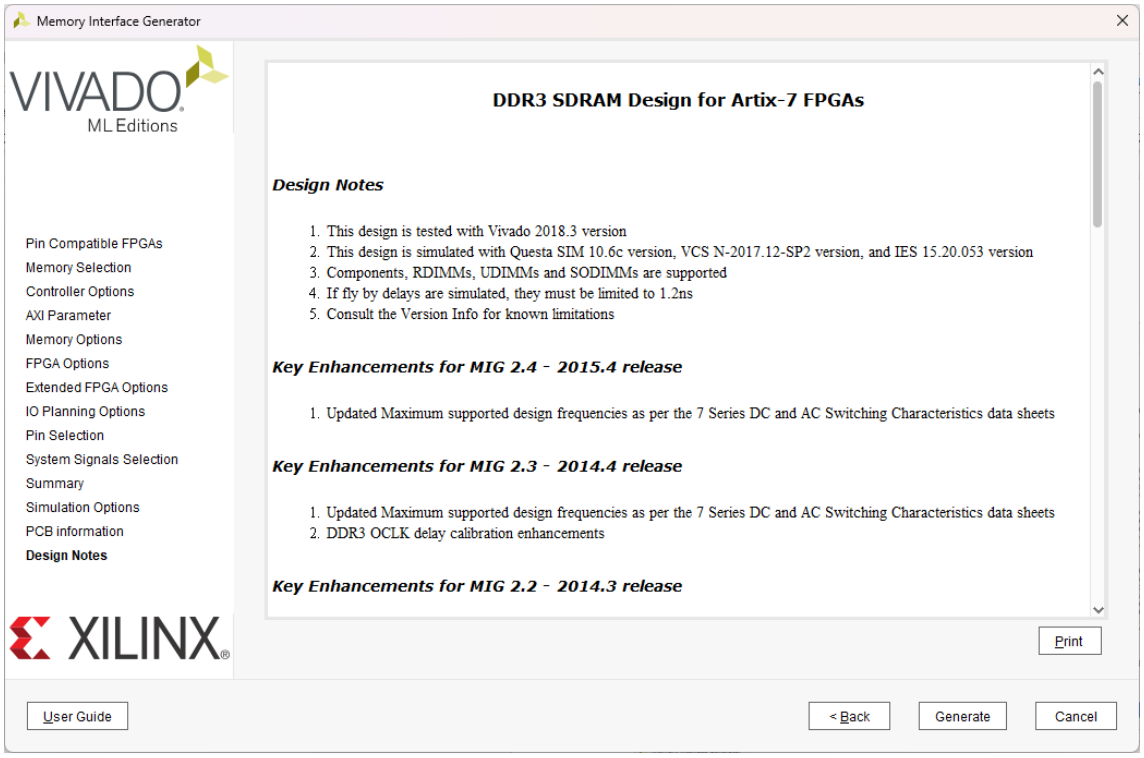
Next >
Cancel

Click：Generate



・Synthesis Options

Out of context per IP

・Run Settings

On local host：Any

Click：Generate