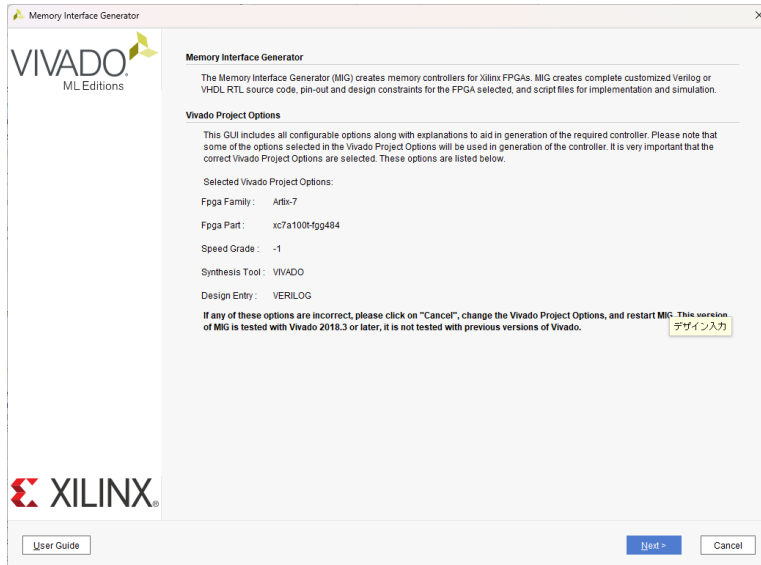


XCM-023-100T Memory Interface Generator

Next



- MIG Output Options

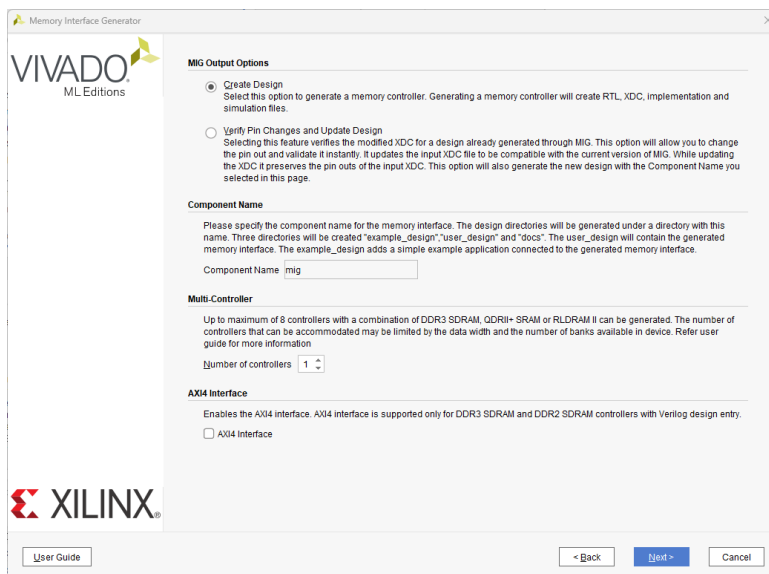
Create Design

- Component Name

Any Name

- Multi Controller

Number of controllers : 1

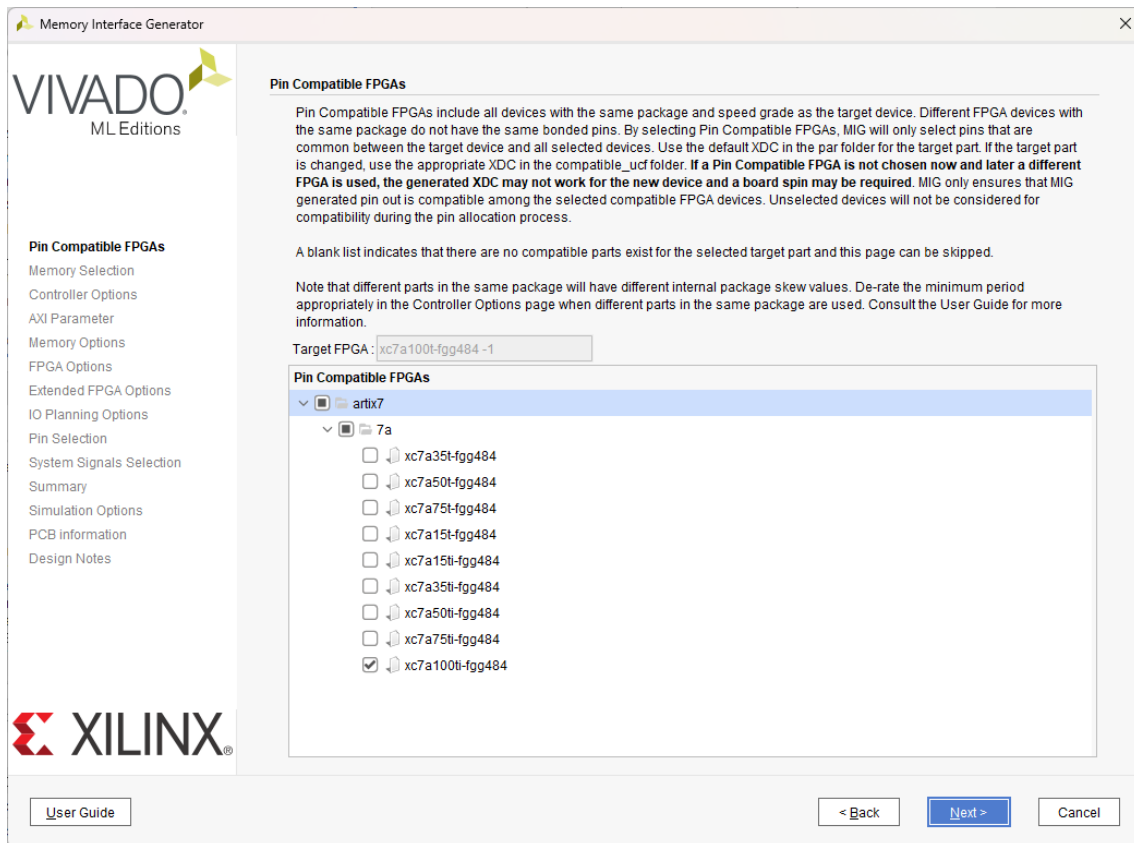


- Pin compatible FPGAs

Artix7

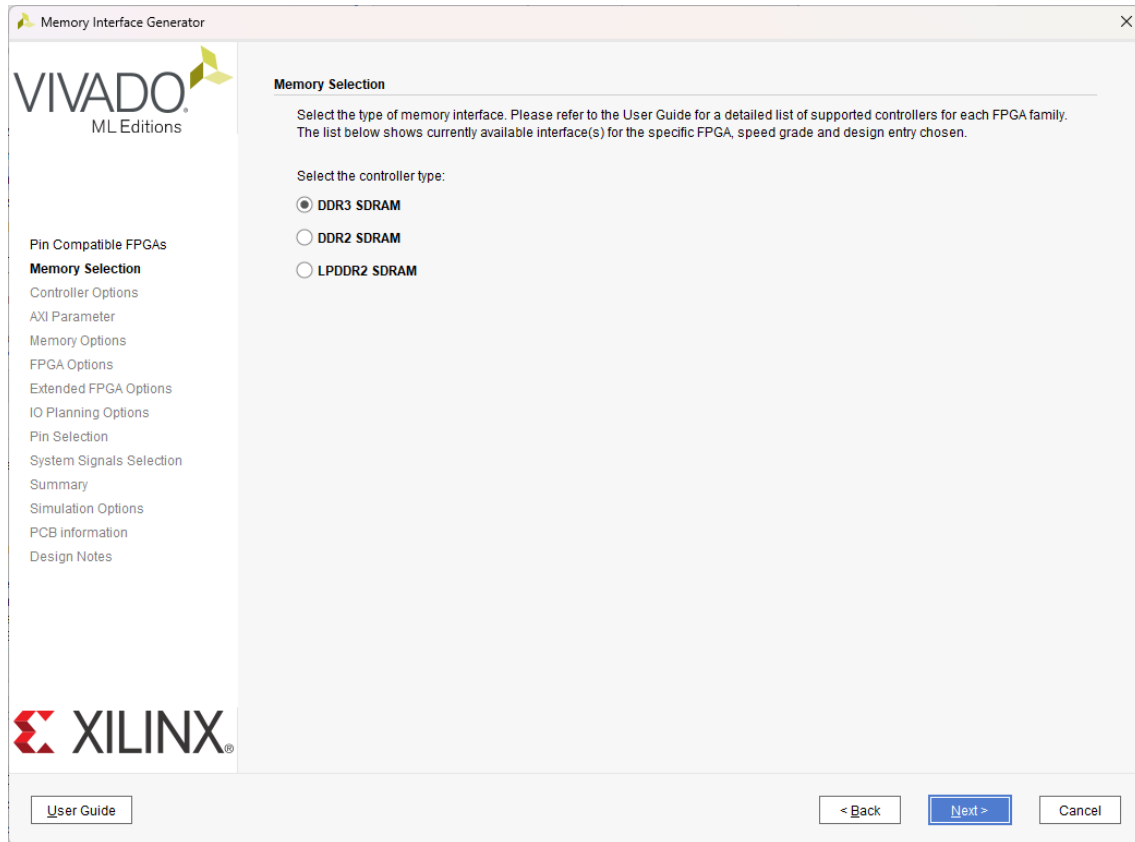
7a

xc7a100ti-fgg484



• Memory Selection

DDR3 SDRAM



The screenshot shows the 'Memory Interface Generator' window in Vivado ML Editions. The left sidebar contains a list of steps: Pin Compatible FPGAs, Memory Selection (highlighted), Controller Options, AXI Parameter, Memory Options, FPGA Options, Extended FPGA Options, IO Planning Options, Pin Selection, System Signals Selection, Summary, Simulation Options, PCB information, and Design Notes. The main area is titled 'Memory Selection' and contains the following text: 'Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA, speed grade and design entry chosen.' Below this text, it says 'Select the controller type:' followed by three radio button options: 'DDR3 SDRAM' (which is selected), 'DDR2 SDRAM', and 'LPDDR2 SDRAM'. At the bottom of the window, there is a 'User Guide' button on the left, and '< Back', 'Next >', and 'Cancel' buttons on the right.

Memory Interface Generator

VIVADO[®]
ML Editions

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Memory Selection

Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA, speed grade and design entry chosen.

Select the controller type:

☒ DDR3 SDRAM
☐ DDR2 SDRAM
☐ LPDDR2 SDRAM

XILINX[®]

User Guide < Back Next > Cancel

- Clock period
 - 2500 ps
- Memory Type
 - Components
- Memory Part
 - MT41K64M16XX-107
- Memory Voltage
 - 1.5V
- Data Width
 - 16
- Data Mask
 - True
- Number of Bank Machines
 - 8
- ORDERING
 - Strict

Memory Interface Generator

VIVADO
ML Editions

Pin Compatible FPGAs

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Options for Controller 0 - DDR3 SDRAM

Clock Period: Choose the clock period for the desired frequency. The allowed period range(2500 - 3300) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information.

2500 ps 400.0 MHz

PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices.

4:1

Vccaux_lo: Vccaux_lo must be set to 2.0V in the High Performance banks for the highest data rates. Vccaux_lo is not available in the High Range banks. Note that Vccaux_lo is common to groups of banks. Consult the 7 Series Datasheets and FPGA SelectIO Resources User Guide for more information.

1.8V

Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above.

Components

Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLD RAM II.

MT41K64M16XX-107

Create Custom Part

Memory Voltage: Select the Voltage of the Memory part selected.

1.5V

Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.

16

ECC: MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported.

Disabled

Data Mask: Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs (DDR3 SDRAM, DDR2 SDRAM) will not use Data Mask.

☒

Number of Bank Machines: This parameter defines the number of bank machines. A given bank machine manages a single DRAM bank at any given time.
Note: Setting a lower value will result in lower resource utilization, but may effect controller efficiency for certain traffic patterns.

8

ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.

Strict

Memory Details: 1Gb, x16, row:13, col:10, bank:3, data bits per strobe:8, with data mask, single rank, 1.35V, 1.5V

User Guide < Back Next > Cancel

- Input Clock Period
5000 ps
- Read Burst Type and Length
Sequential
- Output Driver Impedance Control
RZQ/7
- RTT
RZQ/6
- Controller Chip Select Pin
Disable
- Memory Address Mapping Selection
BANK ROW COLUMN

Memory Interface Generator

VIVADO ML Editions

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Memory Options C0 - DDR3 SDRAM

Input Clock Period: Select the period for the PLL input clock (CLKIN). MIG determines the allowable input clock periods based on the Memory Clock Period entered above and the clocking guidelines listed in the User Guide. The generated design will use the selected Input Clock and Memory Clock Periods to generate the required PLL parameters. If the required input clock period is not available, the Memory Clock Period must be modified.

5000 ps (200 MHz)

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

Read Burst Type and Length
The burst type determines the data ordering within a burst. Consult the memory datasheet for more information. Burst length 8 is the only supported value.

Sequential

Output Driver Impedance Control
Programmable impedance for the output buffer.

RZQ/7

RTT (nominal) - On Die Termination (ODT)
Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the component or DIMM interface. This must be set to RZQ/6 (40 ohms) for data rates at 1333 Mbps and above. In 2 slot DIMM configurations this value will be used for the unwritten slot during a write and will also be used for the unselected slot during a read. Use board level simulation to choose the optimum value.

RZQ/6

Controller Chip Select Pin
The Chip Select (CS#) pin can be tied low externally to save one pin in the address/command group when this selection is set to 'Disable'. Disable is only valid for single rank configurations.

Disable

Memory Address Mapping Selection

User Address

☐ ROW BANK COLUMN

☒ BANK ROW COLUMN

User Guide

< Back

Next >

Cancel

- System Clock
 - No Buffer
- Reference Clock
 - Use System Clock
- System Reset Polarity
 - ACTIVE LOW
- Debug Signals for Memory Controller
 - OFF
- Internal Vref
 - False
- IO Power Reduction
 - ON
- XADC Instactiation
 - Enabled

Memory Interface Generator

VIVADO
ML Editions

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System Clock
Choose the desired input clock configuration. Design clock can be Differential or Single-Ended.
System Clock: No Buffer

Reference Clock
Choose the desired reference clock configuration. Reference clock can be Differential or Single-Ended.
Reference Clock: Use System Clock

System Reset Polarity
Choose the desired System Reset Polarity.
System Reset Polarity: ACTIVE LOW

Debug Signals Control
This feature allows various debug signals present in the IP to be monitored on the ChipScope tool. The debug signals include status signals of various PHY calibration stages. Enabling this feature will connect all the debug signals to the ChipScope ILA and VIO cores in the example design top module. A part of each bus in the debug interface has been grounded so that users can replace the grounded signals with the required signals.
Debug Signals for Memory Controller: OFF

Sample Data Depth
This selects the value of Sample Data depth for Chipscope ILA used in Debug logic.
Sample Data Depth: 1024

Internal Vref
Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This option can only be used at 800 Mbps and lower data rates. This can free 2 pins per bank where inputs are used. This setting has no effect on banks with only outputs.
Internal Vref: ☐

IO Power Reduction
Significantly reduces average IO power by automatically disabling DQ/DQS IBUFs and internal terminations during WRITES and periods of inactivity.
IO Power Reduction: ON

XADC Instantiation
The memory interface uses the temperature reading from the XADC block to perform temperature compensation and keep the read DQS centered in the data window. There is one XADC block per device. If the XADC is not currently used anywhere in the design, enable this option to have the block instantiated. If the XADC is already used, disable this MIG option. The user is then required to provide the temperature value to the top level 12-bit device_temp_i input port. Refer to Answer Record 51687 or the UG586 for detailed information.
XADC Instantiation: Enabled

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XILINX

- Internal Termination Impedance

50 Ohms

The screenshot shows the 'Memory Interface Generator' window in Vivado ML Editions. The left sidebar contains a list of configuration steps: Pin Compatible FPGAs, Memory Selection, Controller Options, AXI Parameter, Memory Options, FPGA Options, Extended FPGA Options (highlighted), IO Planning Options, Pin Selection, System Signals Selection, Summary, Simulation Options, PCB information, and Design Notes. The main panel is titled 'Internal Termination for High Range Banks' and contains the instruction: 'Select the internal termination (IN_TERM) impedance for the High Range (HR) banks. This setting applies **only** to the HR banks used in the interface.' Below this, the 'Internal Termination Impedance' is set to '50 Ohms' in a dropdown menu. The bottom of the window features a 'User Guide' link, '< Back' and 'Next >' navigation buttons, and a 'Cancel' button.

Memory Interface Generator

VIVADO[®]
ML Editions

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XILINX[®]

[User Guide](#)

< Back Next > Cancel

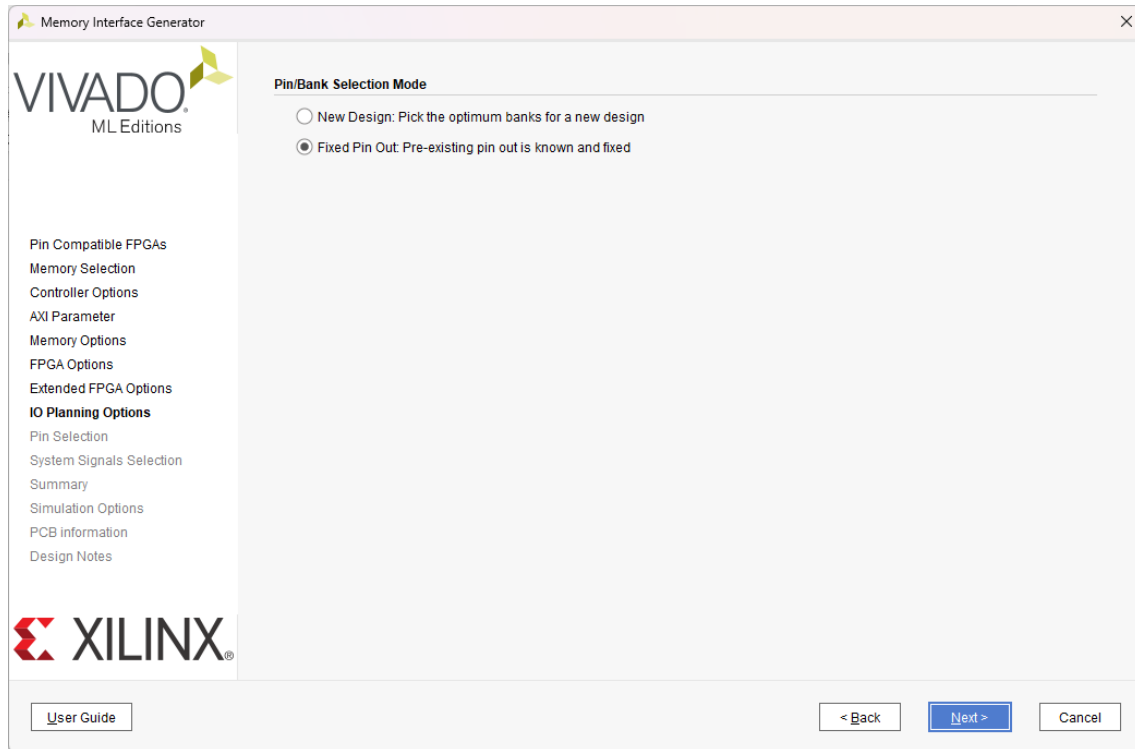
Internal Termination for High Range Banks

Select the internal termination (IN_TERM) impedance for the High Range (HR) banks. This setting applies **only** to the HR banks used in the interface.

Internal Termination Impedance 50 Ohms

- Pin/Bank Selection Mode

Fixed Pin Out: Pre-existing pin out is known and fixed



Read XDC/UCF

Download : <https://github.com/komihori/XCM-023-100T/blob/main/XCM023Bmemorypinout.ucf>

Open : XCM023Bmemorypinout.ucf

The screenshot shows the 'Memory Interface Generator' window in Vivado ML Editions. The 'Pin Selection' tab is active, displaying a table of pin assignments for Controller 0 - DDR3 SDRAM. The table lists 20 signals, their bank numbers, byte numbers, pin numbers, and IO standards. The signals are: ddr3_dq[0] through ddr3_dq[15], ddr3_dm[0] through ddr3_dm[1], and ddr3_dqs_p[0] through ddr3_dqs_n[0]. The pin numbers range from U2 to R2. The IO standards are SSTL15 and DIFF_SSTL15. The window includes a sidebar with navigation options, a 'User Guide' button, and a 'Validate' button at the bottom right.

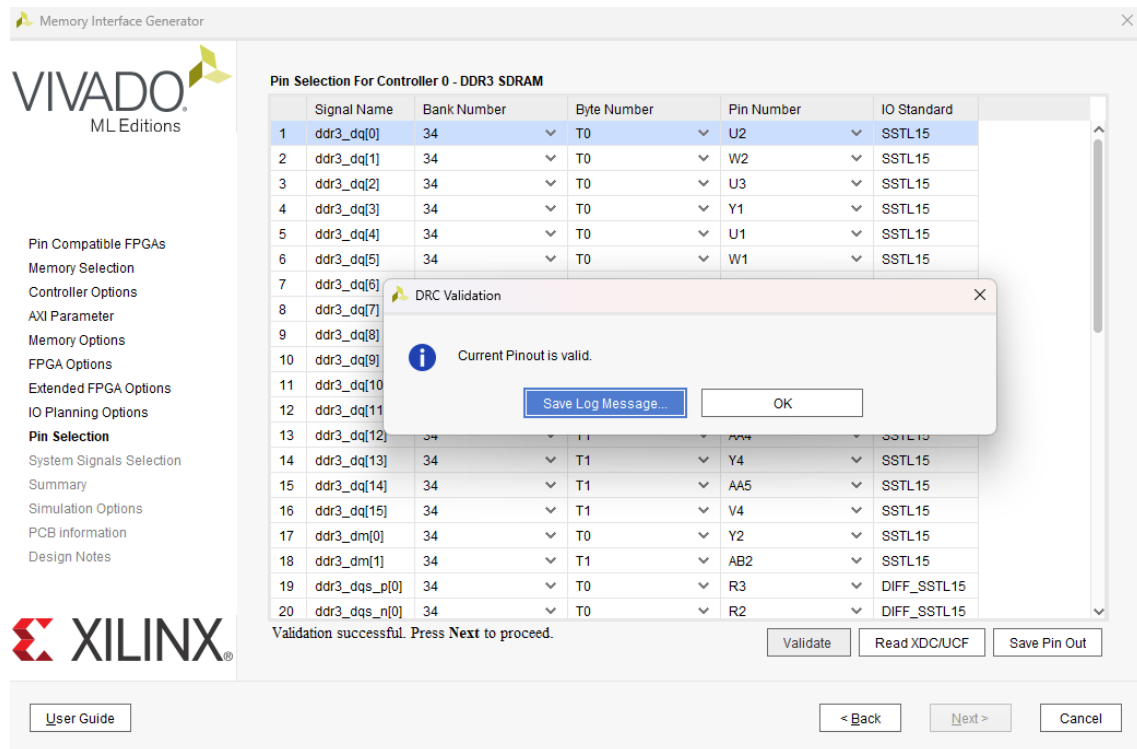
	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	34	T0	U2	SSTL15
2	ddr3_dq[1]	34	T0	W2	SSTL15
3	ddr3_dq[2]	34	T0	U3	SSTL15
4	ddr3_dq[3]	34	T0	Y1	SSTL15
5	ddr3_dq[4]	34	T0	U1	SSTL15
6	ddr3_dq[5]	34	T0	W1	SSTL15
7	ddr3_dq[6]	34	T0	T1	SSTL15
8	ddr3_dq[7]	34	T0	V2	SSTL15
9	ddr3_dq[8]	34	T1	AB3	SSTL15
10	ddr3_dq[9]	34	T1	AB1	SSTL15
11	ddr3_dq[10]	34	T1	AB5	SSTL15
12	ddr3_dq[11]	34	T1	AA1	SSTL15
13	ddr3_dq[12]	34	T1	AA4	SSTL15
14	ddr3_dq[13]	34	T1	Y4	SSTL15
15	ddr3_dq[14]	34	T1	AA5	SSTL15
16	ddr3_dq[15]	34	T1	V4	SSTL15
17	ddr3_dm[0]	34	T0	Y2	SSTL15
18	ddr3_dm[1]	34	T1	AB2	SSTL15
19	ddr3_dqs_p[0]	34	T0	R3	DIFF_SSTL15
20	ddr3_dqs_n[0]	34	T0	R2	DIFF_SSTL15

INFO: Press **Validate** to proceed.

Click : Validate

Click : OK

Click : Next



• System Signals

Signal Name	Bank Number	Pin Number
sys_rst	Select Bank	No Connect
init_calib_complete	Select Bank	No Connect
tg_compare_error	Select Bank	No Connect

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System Signals Selection

Select the system pins below appropriately for the interface. Customization of these pins can also be made in the XDC after the design is generated. For more information see [UG586 Bank and Pin rules](#).

System Clock and Reference Clock pin selections will not be visible if the 'No Buffer' option was selected in the FPGA Options page.

System Signals

These signals may be connected internally to other logic or brought out to a pin.

- **sys_rst**: This input signal is used to reset the interface.
- **init_calib_complete**: This signal indicates that the interface has completed calibration and memory initialization and is ready for commands. LOC constraint will be generated in XDC for Example design only based on "Pin Number" selection below.
- **error**: This output signal indicates that the traffic generator in the Example Design has detected a data mismatch. This signal does not exist in the User Design.

Signal Name	Bank Number	Pin Number
sys_rst	Select Bank	No connect
init_calib_complete	Select Bank	No connect
tg_compare_error	Select Bank	No connect

All pins must be constrained to specific locations in order to generate a bit file in the implementation phase (this is not required for simulation).

User Guide

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Cancel

Click : Next

Memory Interface Generator

VIVADO
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XILINX

Vivado Project Options:
Target Device : xc7a100t-fgg484
Speed Grade : -1
HDL : verilog
Synthesis Tool : VIVADO

If any of the above options are incorrect, please click on "Cancel", change the CORE Generator

MIG Output Options:
Module Name : mig
No of Controllers : 1
Selected Compatible Device(s) : xc7a100ti-fgg484

FPGA Options:
System Clock Type : No Buffer
Reference Clock Type : Use System Clock
Debug Port : OFF
Internal Vref : disabled
IO Power Reduction : ON
XADC instantiation in MIG : Enabled

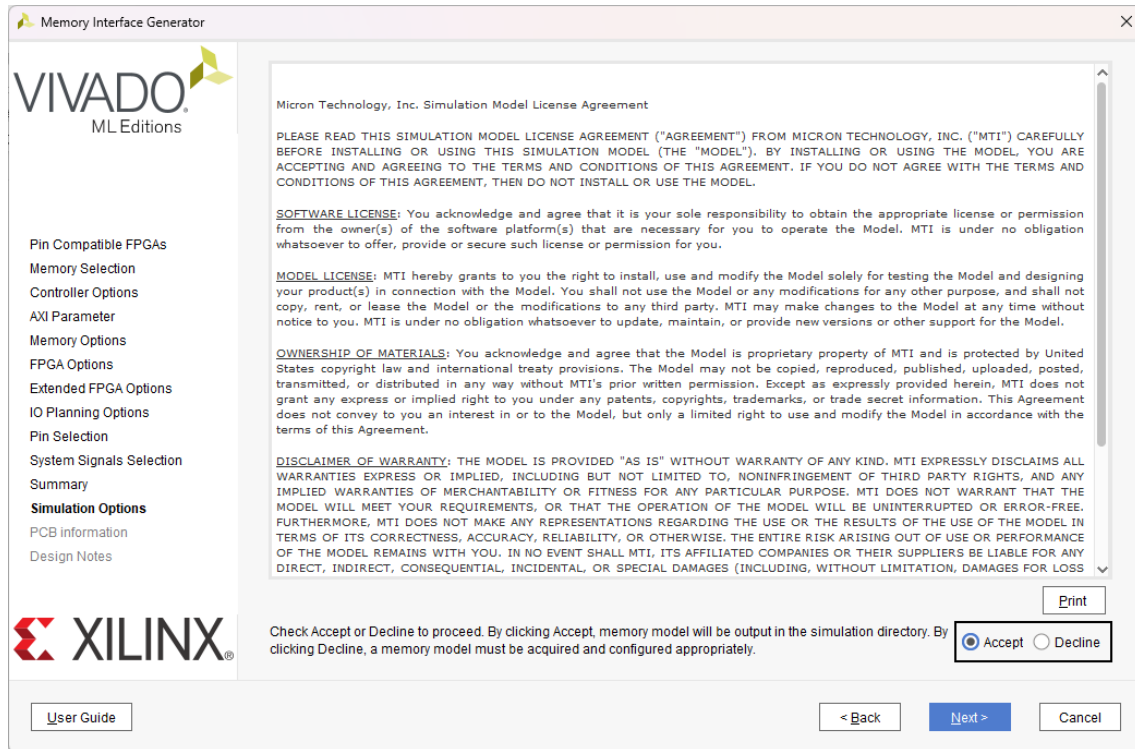
Extended FPGA Options:
DCI for DQ,DQS/DQS#,DM : enabled
Internal Termination (HR Banks) : 50 Ohms

Print

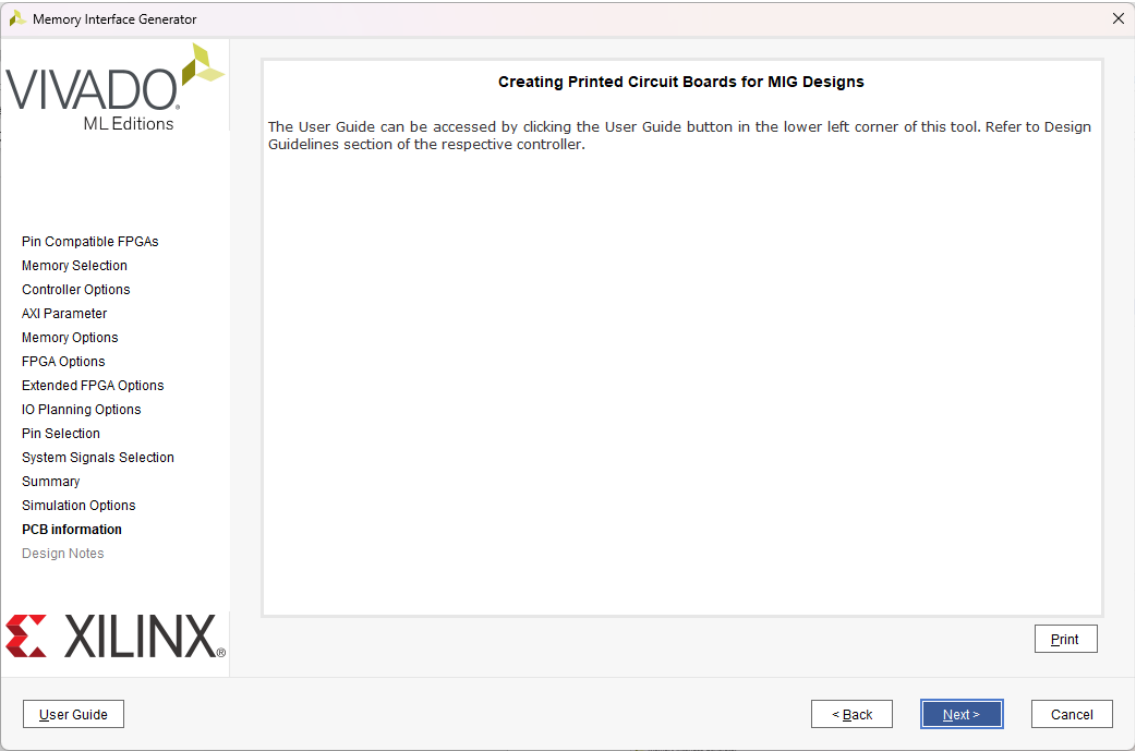
User Guide < Back Next > Cancel

Select : Accept

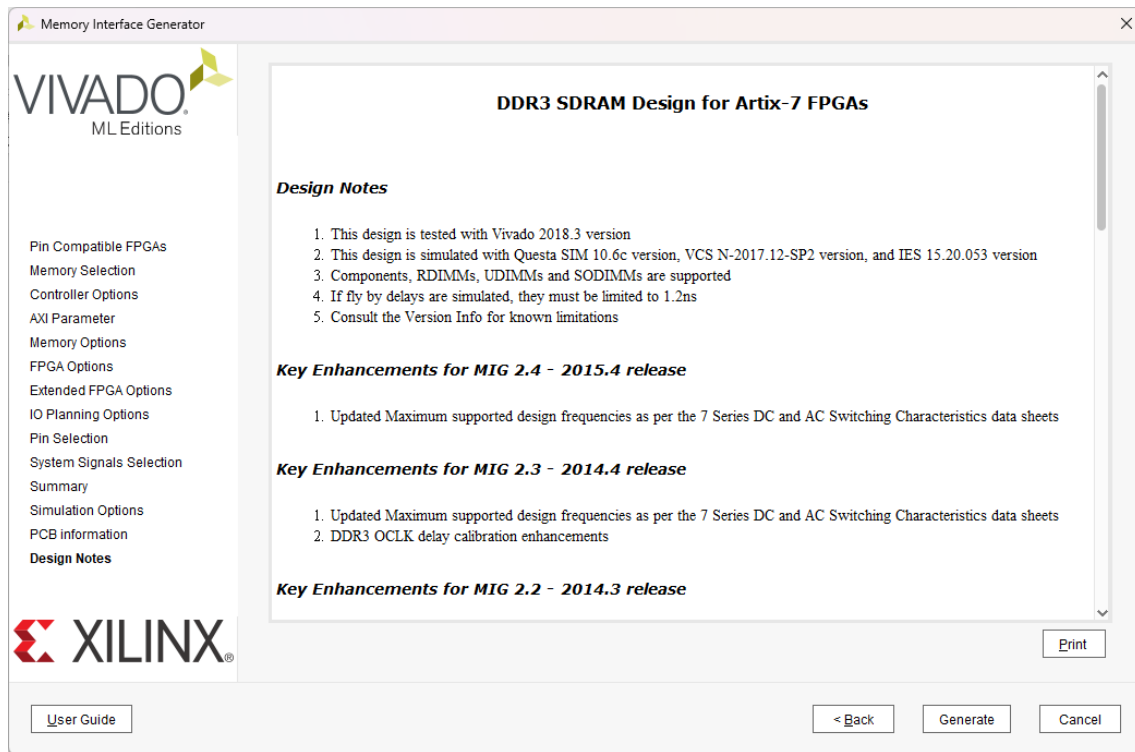
Click : Next



Click : Next

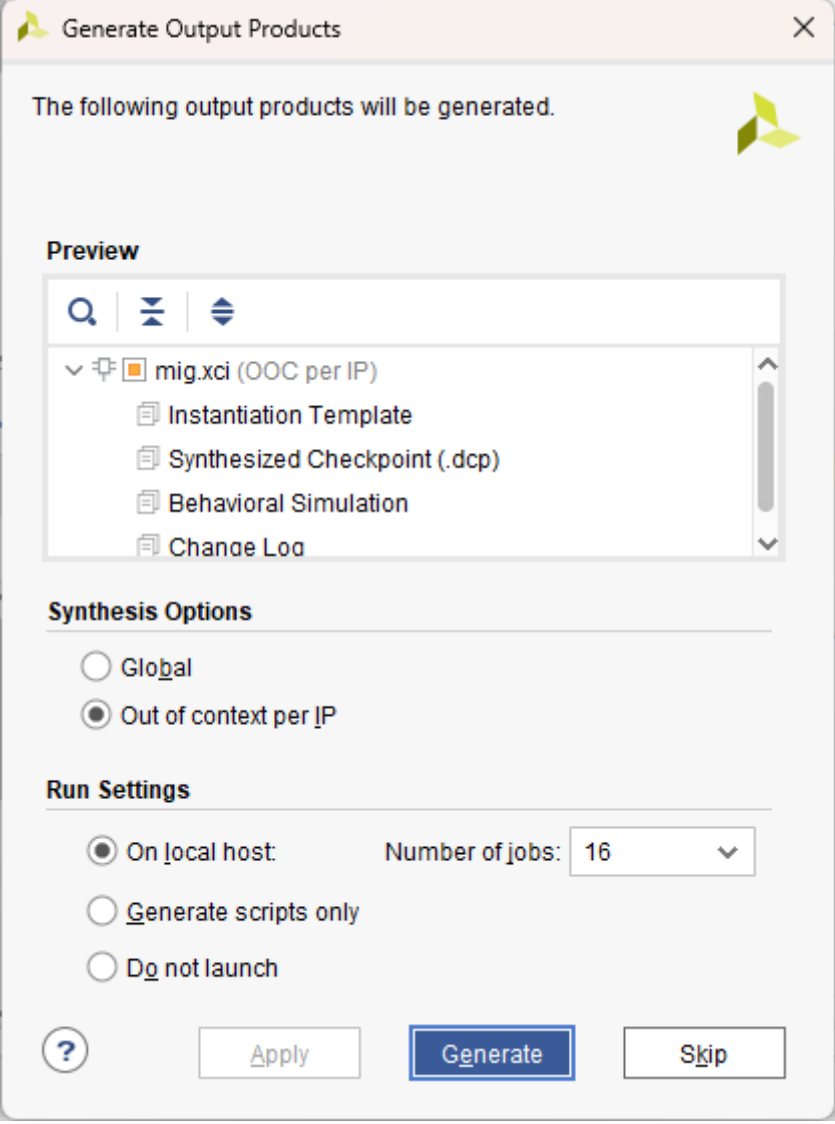


Click : Generate



- Synthesis Options
 - Out of context per IP
- Run Settings
 - On local host : Any

Click : Generate



The following output products will be generated.

Preview

Search, Sort, Filter icons

- ▼ mig.xci (OOC per IP)
 - Instantiation Template
 - Synthesized Checkpoint (.dcp)
 - Behavioral Simulation
 - Change Log

Synthesis Options

☐ Global

☒ Out of context per IP

Run Settings

☒ On local host: Number of jobs: 16 ▼

☐ Generate scripts only

☐ Do not launch

Buttons: ? Apply Generate Skip