

## UNIT-V

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# MEMORIES AND ASYNCHRONOUS SEQUENTIAL LOGIC

### Introduction:

A Memory unit is a collection of Storage cells together with associated circuits needed to transfer information in and out of storage. The memory stores binary information in groups of bits called words.

→ A word in memory is an entity of bits that move in & out of storage as a unit. A word is a group of 0's and 1's may represent a number, an instruction code, one or more alphanumeric character, or any other binary coded information.

→ The capacity of memories in commercial computer is usually stated as the total no. of bytes that can be stored.

→ Units of computer memory measurement

$$1 \text{ Bit} = 1 \text{ Binary digit}$$

$$8 \text{ Bits} = 1 \text{ byte}$$

$$1024 \text{ bytes} = 1 \text{ kilobyte}$$

$$1024 \text{ KB} = 1 \text{ Megabyte}$$

$$1024 \text{ MB} = 1 \text{ Gigabyte}$$

$$1024 \text{ GB} = 1 \text{ terabyte}$$

$$1024 \text{ TB} = 1 \text{ petabyte}$$

$$1024 \text{ PB} = 1 \text{ exabyte}$$

$$1024 \text{ EB} = 1 \text{ zetta byte}$$

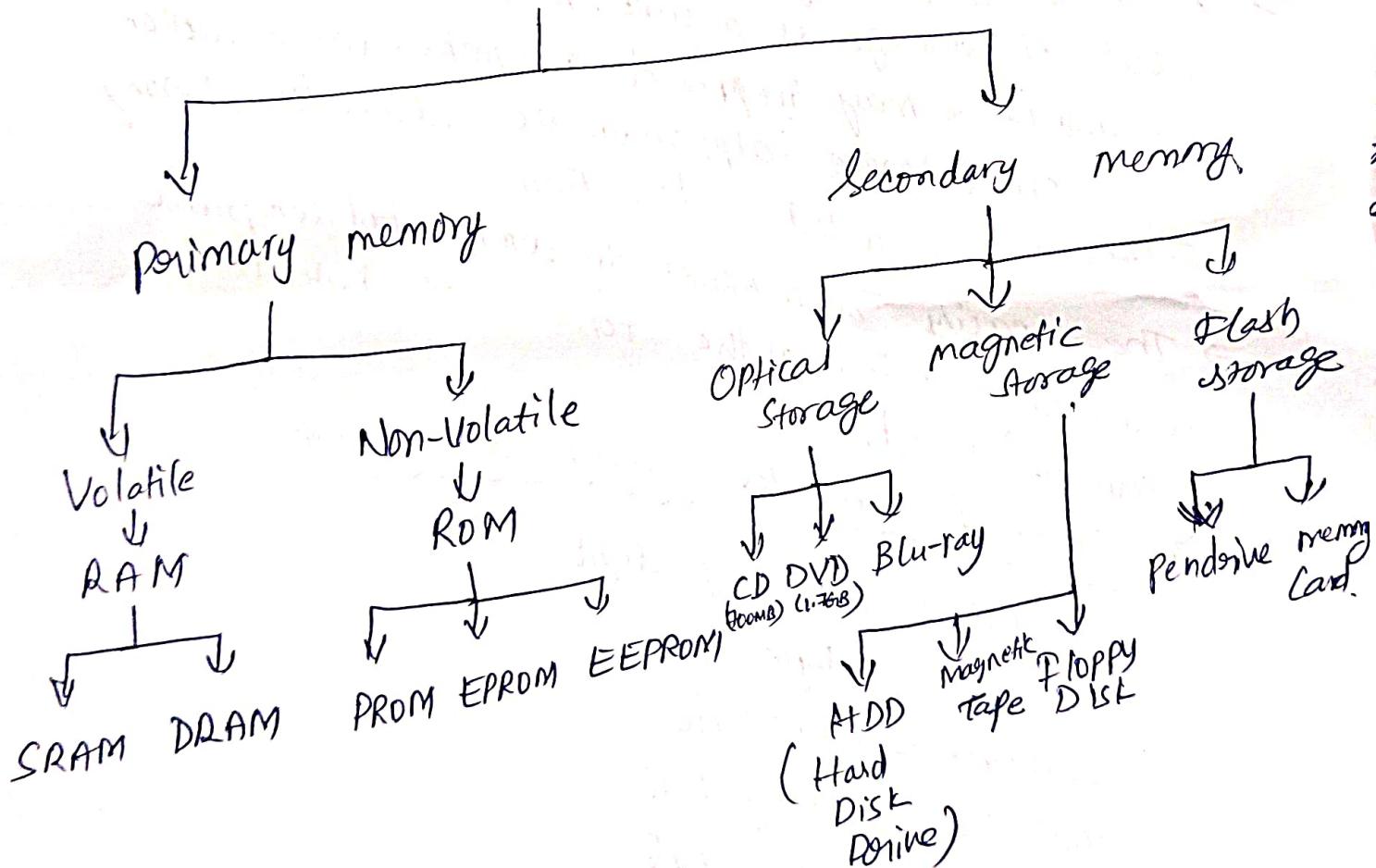
$$1024 \text{ ZB} = 1 \text{ yotta byte}$$

$$1024 \text{ YB} = 1 \text{ Bronto byte}$$

$$1024 \text{ BB} = 1 \text{ Geabyte}$$

→ the internal structure of a memory unit is specified by the no. of words it contains & the no. of bits in each word. Special input lines called address lines select one particular word. Each word in memory is assigned an identify number, called an address.

→ starting from '0' and continuing with 1, 2, 3 up to  $2^k - 1$  where 'k' is the number of address lines  
 V.Typ. \* → Memory is any physical device capable of storing information temporarily (or) permanently.  
 Computer memory



Computer memory is classified into two types

- ① Primary memory
- ② Secondary memory

→ Again Primary memory is divided into two types

(i) RAM (ii) ROM.

→ RAM is Random Access memory.

→ ROM is Read only memory.

(i) RAM (Random Access memory):-

→ RAM is a form of computer memory that can be read and changed in any order, typically used to store working data & machine code.

→ (i) SRAM (Static Random Access memory):-  
The memory which retains its contents as long as power remains applied. However, data is lost when the power gets down due to volatile nature.

(ii) DRAM (Dynamic Random Access memory):-  
DRAM is used mostly because it is cheap & small. All DRAM's are made up of memory cells. These are composed of one capacitor & one transistor. DRAM consumes less power by it is cheaper than SRAM. It does both read & write operations.

→ Primary memory stores the information temporarily until type of memories loss the memory (Content) when the power is last (off).

Eg RAM, ROM.

→ In this temporary stored data is used by quick access the computer processor to automatically increase the processing speed of the computer.

→ Secondary memory stores the information permanently. In this type of memories doesn't loss the memory (Content) until we delete.

→ Eg Hard disk, CD

- RAM is Volatile memory, in this type of memory data loss occurs when sudden changes in power.
- ROM is Non-Volatile memory, in this type of memory data doesn't loss when sudden changes in power.

### → Secondary memory :-

Optical:- In this type of memory data stored by recording in the form of optical we can read the data with the help of laser beam.

Magnetic:- In this type of memory data stored by recording in the form of magnetic. We can read the data with the help of read and write heads.

### \* \* Differences between SRAM and DRAM :-

① SRAM : Static Random Access memory

② Transistors are used to store information in SRAM

③ It has less storage capacity

④ SRAM are low density devices

⑤ SRAM are used in cache memories

⑥ SRAM is expensive than DRAM

① DRAM

② DRAM : Dynamic Random Access memory.

③ Capacitors are used to store data in DRAM.

④ It has large storage capacity.

⑤ DRAM's are high density devices

⑥ DRAM are used in main memories.

⑦ DRAM is cheaper than SRAM.

## SRAM

- ⑦ The power consumption of SRAM is more.
- ⑧ SRAM's structure is complex than DRAM.
- ⑨ SRAM does not need periodic refreshment to maintain data.
- ⑩ SRAM is faster than DRAM.

## DRAM

- ⑦ The power consumption of DRAM is less.
- ⑧ DRAM's structure is simpler than SRAM.
- ⑨ DRAM needs periodic refreshment to maintain the charge in the capacitors for data.
- ⑩ DRAM is slower than SRAM.

## \* ROM (Read only memory) : \*

- The memory from which we can only read but cannot write on it. This type of memory is non-volatile. The information is stored permanently in such memories during manufacture.
- A ROM stores such instruction as are required to start computer when electricity is first turned on, this operation is referred to as bootstrap. ROM chips are not only used in the computer but also in other electronic items like washing machine, microwave oven.

## Types of ROM

- ① MROM
- ② PROM
- ③ EEPROM
- ④ EEPROM.

1st Erasable

## ① MROM (Masked ROM):-

→ The very first ROM's were hard-wired devices that contained a pre-programmed set of data (or) instructions. These kind of ROM's are known as masked ROM's. It is expensive ROM.

## ② PROM (Programmable Read only memory):-

→ PROM is read-only memory that can be modified only once by a user. The user buys a blank PROM & enters the desired contents using a PROM programmer. Inside the PROM chip there are small fuses which are burnt open during programming. It can be programmed only once & is not erasable.

## → EPROM (Erasable & Programmable Read only memory)

→ The EPROM can be erased by exposing it to ultra-violet light for a duration of up to 60 minutes. Usually, an EPROM eraser achieves this function. During programming an electrical charge is trapped in an insulated gate region. The charge is retained for more than ten years because the charge has no leakage path. For erasing this charge, ultra-violet light is passed through a quartz crystal window (lid). This exposure to ultra-violet light dissipates the charge. During normal use the quartz lid is sealed with a sticker.

~~EEPROM~~ (Electrically Erasable & Programmable Read-only memory)

→ The EEPROM is programmed & erased electrically. It can be erased & reprogrammed about ten thousand times. Both erasing and programming take about 4 to 10ms (millisecond). In EEPROM, any location can be selectively erased & programmed. EEPROM's can be erased one byte at a time, rather than erasing the entire chip. Hence, the process of reprogramming is flexible but slow.

→ ~~Programmable Logic Device~~:-

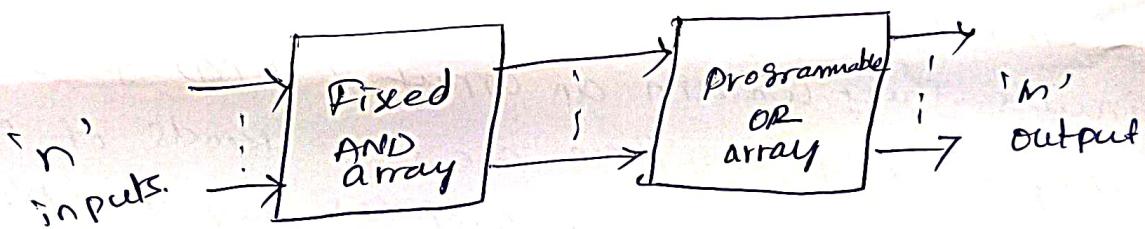
→ programmable logic devices PLD's are the integrated circuits. They contain an array of AND gates & another array of OR gates. There are three kinds of PLD based on the type of array's, which has programmable feature.

- Programmable Read only memory
- programmable Array logic
- programmable logic array.

→ The process of entering the information into these devices is known as programming. Basically, users can program these devices (or) IC's electrically in order to implement the Boolean functions based on the requirement. Here, the term programming refers to H/w (hardware) programming but not software programming.

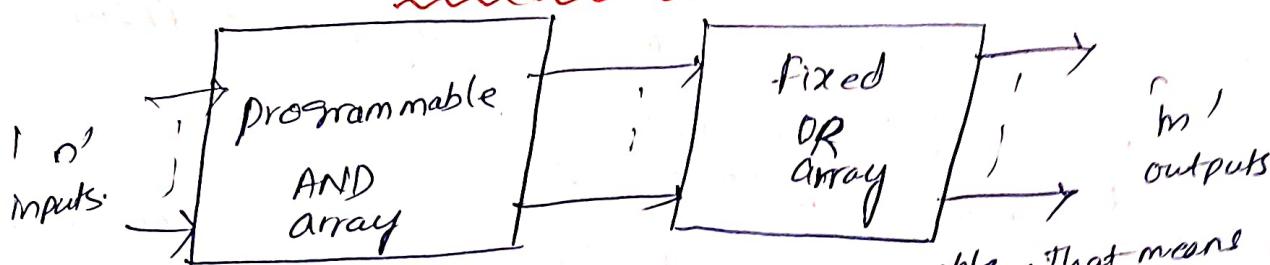
## PROM (Programmable Read only memory) :

- Read only memory ROM is a memory device, which stores the binary information permanently. That means, we can't change that stored information by any means later. If the ROM has programmable feature, then it is called as programmable ROM, PROM. The user has the flexibility to program the binary information electrically once by using PROM programmer.
- PROM is a programmable logic device that has fixed AND array and programmable OR array
- The block diagram of PROM is shown in the following figure.



Block diagram of PROM

- Here, the inputs of AND gates are not of programmable type. So, we have to generate  $2^n$  product terms by using  $2^n$  AND gates having  $n$  inputs each. We can implement these product terms by using  $n \times n$  decoder. So, this decoder generates ' $n$ ' minterms.
- Here, the inputs of OR gates are programmable. That means, we can program any no. of required product terms, since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PROM will be in the form of sum of minterms.

Block diagram of PAL

→ Here, the inputs of AND gates are programmable. That means each AND gate has both normal & complemented inputs of variables. So, based on the requirement, we can program any of those inputs. So, we can generate only the required product terms by using these AND gates.

→ Here, the inputs of OR gates are not programmable type. So the no. of inputs to each OR gate will be of fixed type. Hence, apply those required product terms to each OR gate as input. Therefore, the outputs of PAL will be in the form of sum of products form.

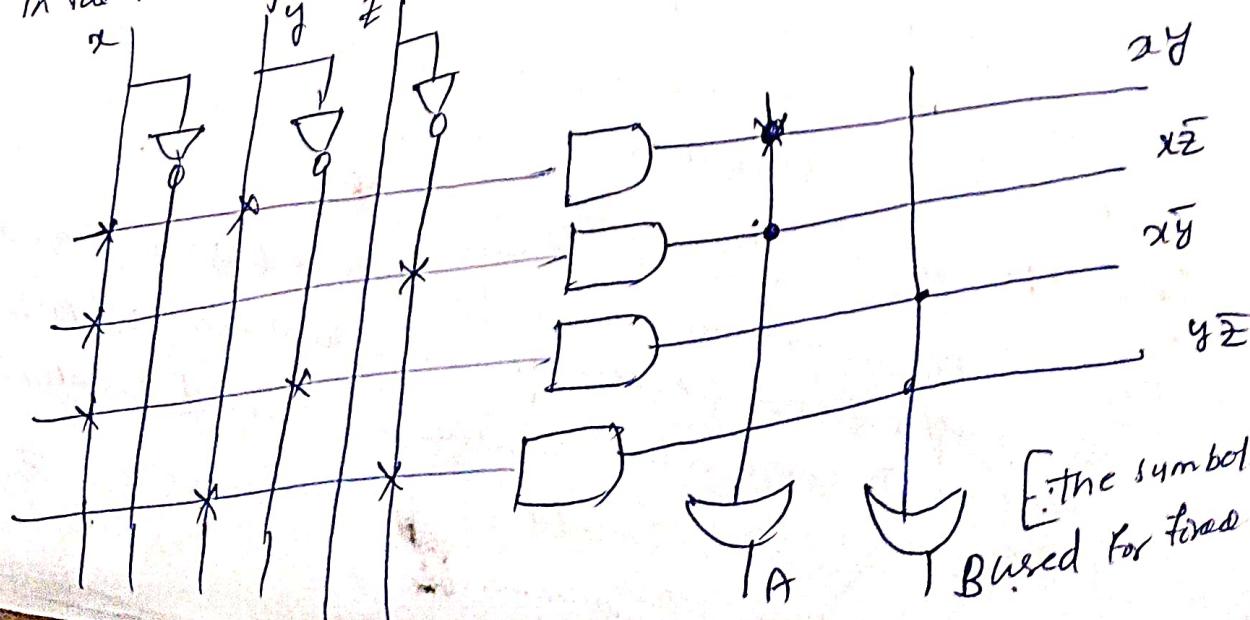
Example

(Q) Implement the following Boolean function using PAL

$$A = xy + \bar{x}\bar{z}$$

$$B = x\bar{y} + y\bar{z}$$

(Q) The given two functions are in sum of product form. Therefore two product terms present in each boolean function. So we require four programmable AND gates & two fixed OR gates for producing those two functions. The corresponding PAL is shown in the following figure.





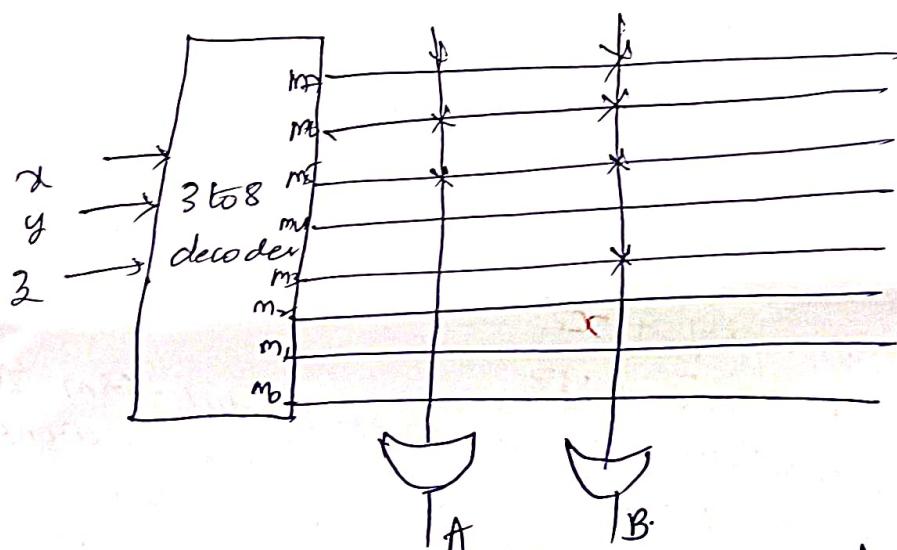
### Example

⑥ Implement the following Boolean function using PROM

$$A(x_1, y_1, z_1) = \sum m(5, 6, 7)$$

$$B(x_1, y_1, z_1) = \sum m(13, 5, 6, 7)$$

⑦ The given two functions are in sum of min terms form and each function is having three variables,  $x_1, y_1, z_1$ . So, we require 3 to 8 decoder & two programmable OR gates for producing these two functions. The corresponding PROM is shown in the following figure.



→ Here, 3 to 8 decoder generates eight min terms. The two programmable OR gates have the access of all these min terms. But only the required min terms are programmed in order to produce the respective boolean function by each OR gate. The symbol 'x' is used for programmable connections.

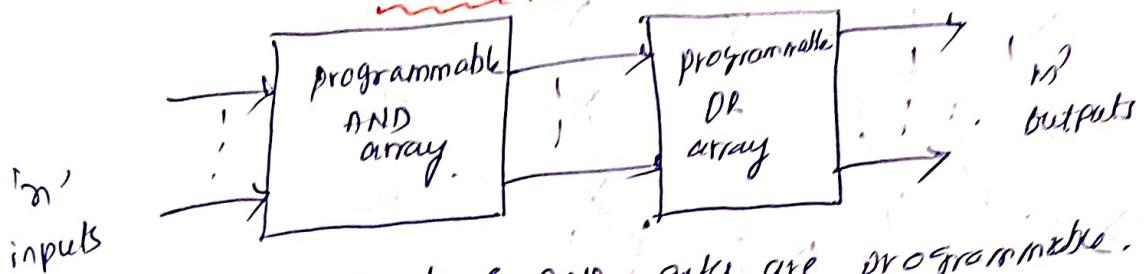
### \* PAL (Programmable Array logic) \*

→ PAL is programmable logic device that has programmable AND array & fixed OR array. The advantage of PAL is that we can generate only the required product terms of Boolean function instead of generating all the min terms by using programmable AND gates.

\* Programmable logic array (PLA)

→ PLA is PLD that has both programmable AND array & programmable OR array. Hence, it is the most flexible PLD.

Block diagram of PLA



→ Here, the inputs of AND gates are programmable. That means each AND gate has both normal & complemented inputs of variables. So, based on the requirement, we can program any of those inputs. So, we can generate only the required product terms by using <sup>these</sup> AND gates.

→ Here, the inputs of OR gates are also programmable, so we can program any no. of required product terms, since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PLA will be in terms of sum of product form.

\* Example \*

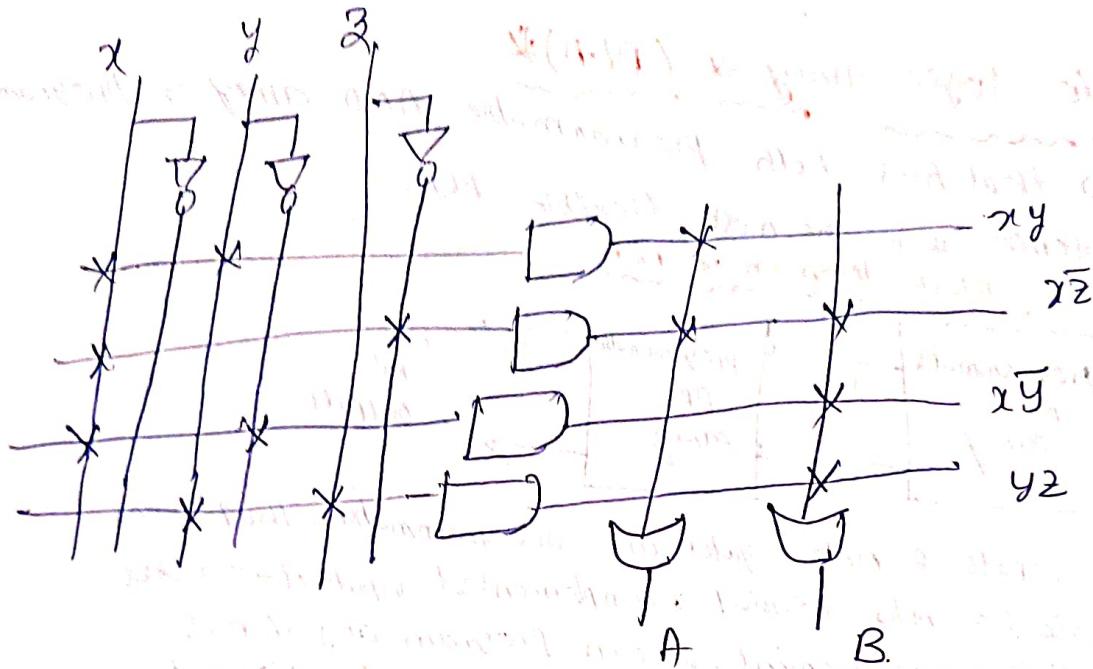
Implement the following Boolean functions using PLA

$$A = xy + x\bar{z}$$

$$B = \bar{x}y + yz + x\bar{z}$$

→ The given two functions are in sum of product form. The no. of product terms present in the given Boolean function A & B are two & three respectively. One product term,  $\bar{x}z$  is common in each function.

→ So, we require four programmable AND gates & two programmable OR gates for producing those two functions. The corresponding PLA is shown in the following figure.



→ The programmable AND gates have the access of both normal & complemented inputs of ~~the~~ variables. In the above figure, the inputs  $x, y, z, \bar{x}, \bar{y}, \bar{z}$  are available at the inputs of each AND gate. So, programs only the required literals in order to generate one product term by each AND gate.

→ All these product terms are available at the inputs of each programmable OR gate, but only programs the required product terms in order to produce the respective boolean functions by each OR gate. The symbol 'x' is used for programmable connections.

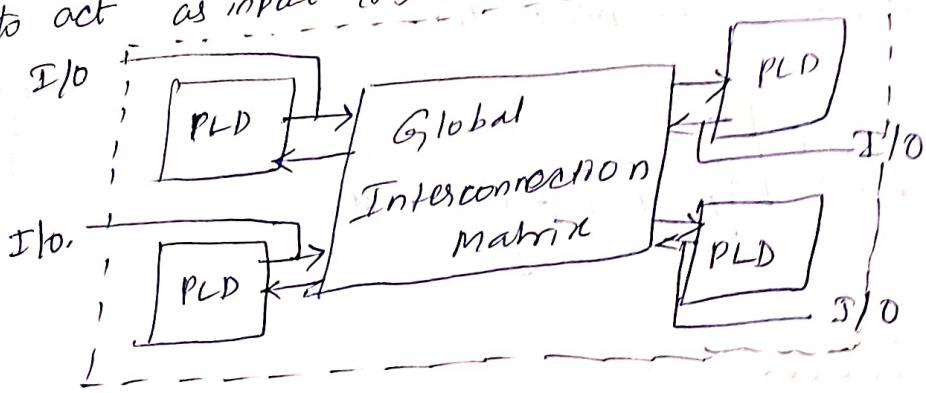
#### 4. Sequential programmable devices \*

- The combinational PLD consists only of gates.
- Sequential programmable devices includes both gates and flip flop.
- Type of sequential programmable devices.

- (1) Sequential (simple) Programmable logic device (SPLD).
- (2) Complex programmable logic device (CPLD).
- (3) Field programmable gate array (FPGA).

## → The Internal Structure

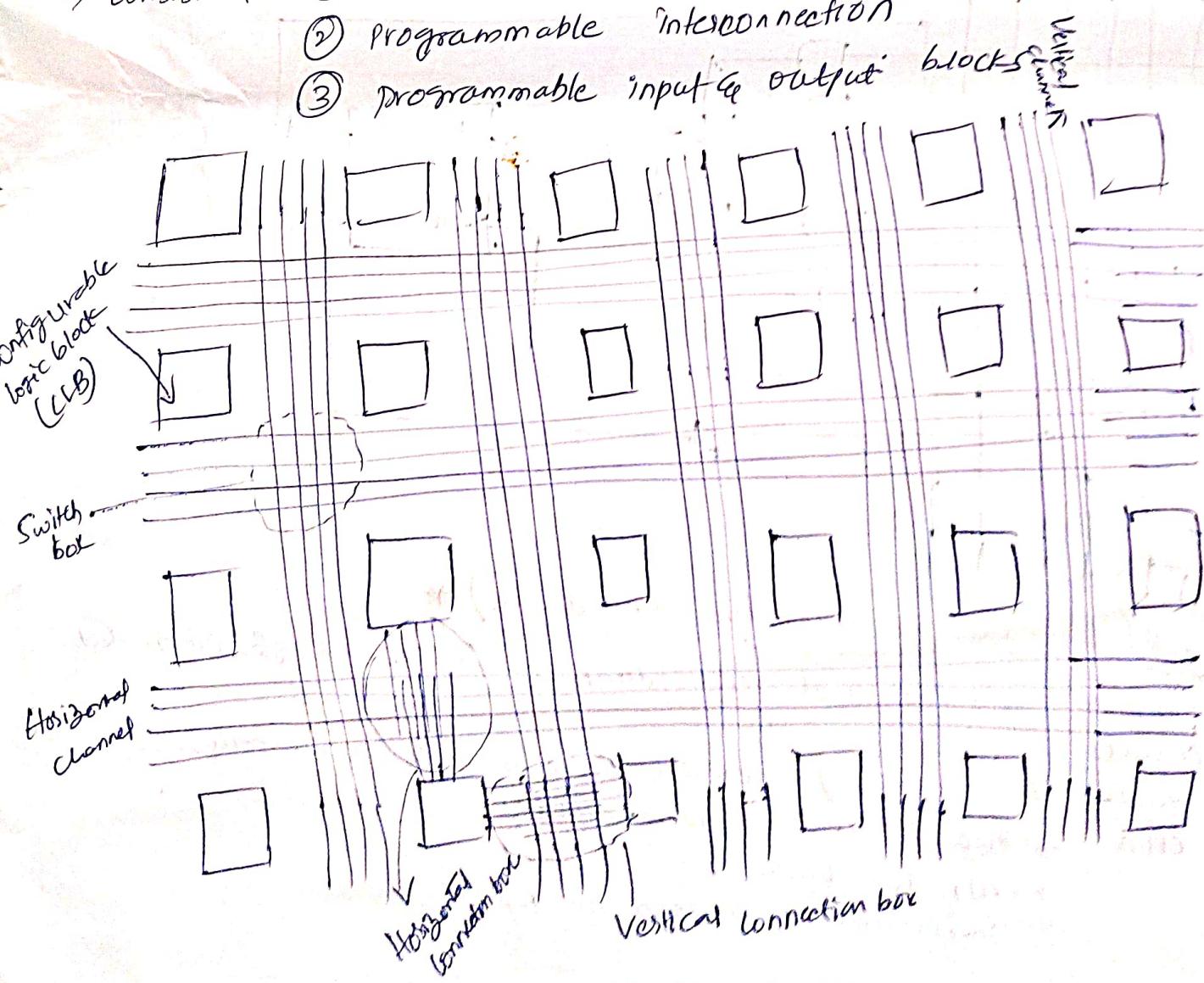
→ Each I/O pin is driven by a three state buffer and can be programmed to act as input (or) output.



## \* FPGA (Field programmable Gate array)

→ FPGA is a VLSI circuit that can be programmed at the user's location.

- consist of
  - ① hundreds (or) thousands of logic blocks
  - ② programmable interconnection
  - ③ programmable input & output blocks

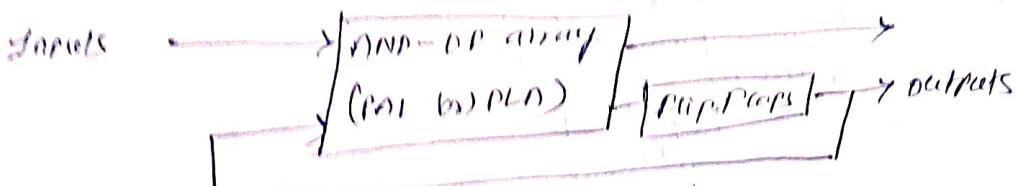


→ The internal structure of a memory unit is specified by the no. of words it contains & the no. of bits in each word.

### \* CPLD (Complex Programmable Logic Device) \*

→ CPLD consist PAL & D-Flip flop.

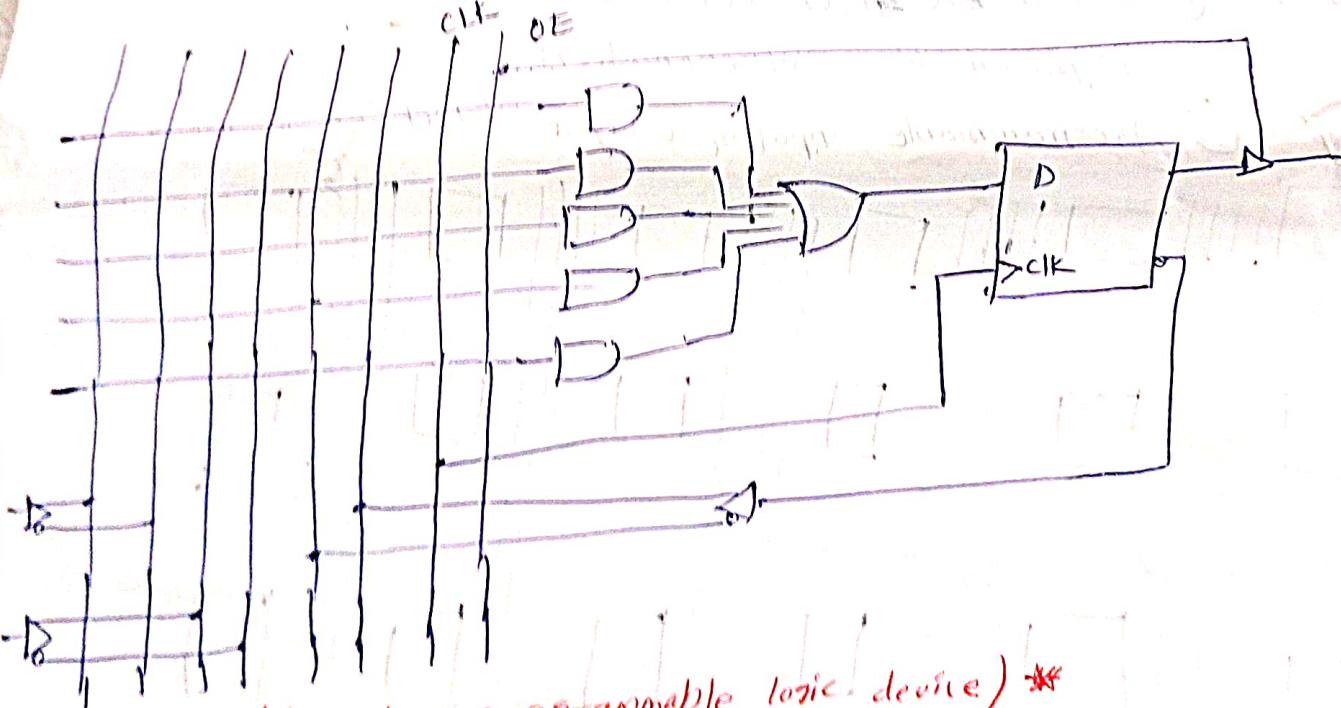
→ Each section in CPLD is called macrocell.



Block diagram

→ The basic macrocell logic → ① NAND-OR array  
② Edge-triggered D-Flip Flop  
③ Three-state buffer (inverter)

→ A typical CPLD has from 8 to 16 macrocells within one IC package.



### \* CPLD (Complex Programmable Logic Device) \*

→ CPLD is a collection of individual PLD's on a single integrated circuit.

→ Each PLD typically contains from 8 to 16 macrocells.

→ CPLD has two levels of programmability.

→ Each PLD block

→ Interconnections between the PLD's