

## UNIT-1 (EDC)

→ From these presentation we will start the introduction of EDC.

→ Introduction of EDC is semi conductor material.

→ Backbone of EDC is semi conductor material.

→ In this course first topic is current.

→ In this flow of charge across the cross

conductor the area called current.

sectional area of materials are

the cross sectional area

into 3 types

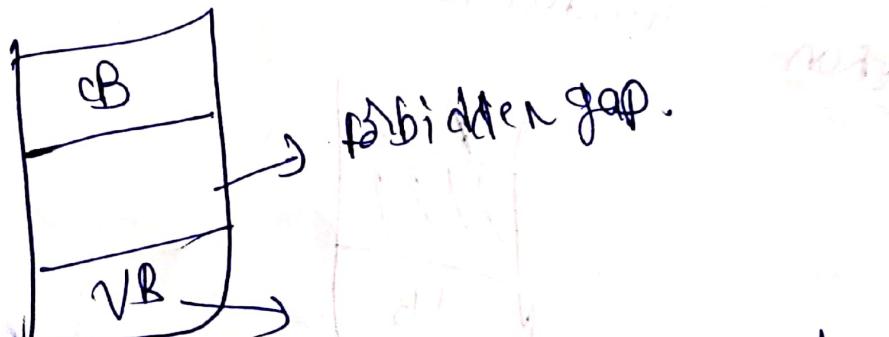
classified conductor

conductors insulators

semiconductors

diagram of conductor is

energy band



forbidden gap.

→ The maximum conduction is done

→ In this no free e<sup>-</sup> exist at room temp.

because there is no forbidden gap. hence VB &

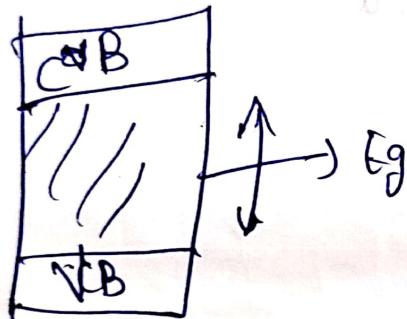
so both are overlapped each other.

CB

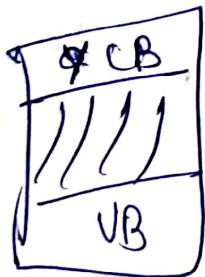
→ These materials have large no. of free electrons in their atomic structure which allows flow of current. Materials which allows electric current to flow.

e.g.: Gold, silver, copper, Al.

Insulator:- The material does not have free electrons. Hence current does not flow through them.



Semi-conductor: In this material the conduction takes place more than insulator less than conduction



→ The e<sup>-</sup> moves from VB to CB for conduction.

→ Its ability to conduct electric current increase with increase in temp or by applying voltage e.g. Si, Ge.

→ The  $e^-$  having energy for go to conduction band.

$$\rho = \frac{R \cdot A}{l}$$

conductivity  
resistivity  
Area of cross section  
length of the wire

→ if  $R \uparrow \downarrow I$

$$R \propto T$$

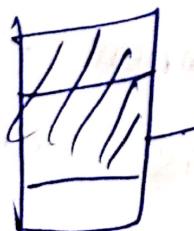
→ In insulator  $\rightarrow 10^{12} \text{ A/cm}$  (flow of charge)

resistivity of the Si is  $50 \times 10^3 \Omega \text{ cm}$   
Ge is  $50 \Omega \text{ cm}$ .

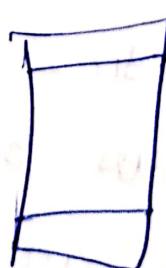
$$\rho_c < \rho_s < \rho_i$$

$$I_c < I_s < I_i$$

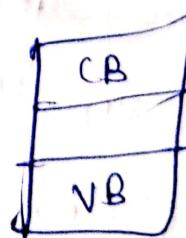
energy band diagram:



forbidden gap  
conductor



insulator



semiconductor

→ The  $e^-$  Jumped from VB & CB & The  $e^-$  present in the CB will participate in the conduction.

→ The amount of energy it takes for moves from VB to CB is equal to this gap. is called **forbidden gap.**

→ In Insulator  $E_g$  is very high so because it is not a good conductor.

→  $E_0 \approx 6\text{eV}$  &  $1\text{eV} = 1.6 \times 10^{-19}\text{J}$

→ In semiconductor  $E_F = 0.75\text{eV}$   $\Rightarrow$   $E_F \approx 1.16\text{eV}$  **forbidden gap.**

→ In case of conductor VB & CB is overlapping.

Intrinsic Semiconductor

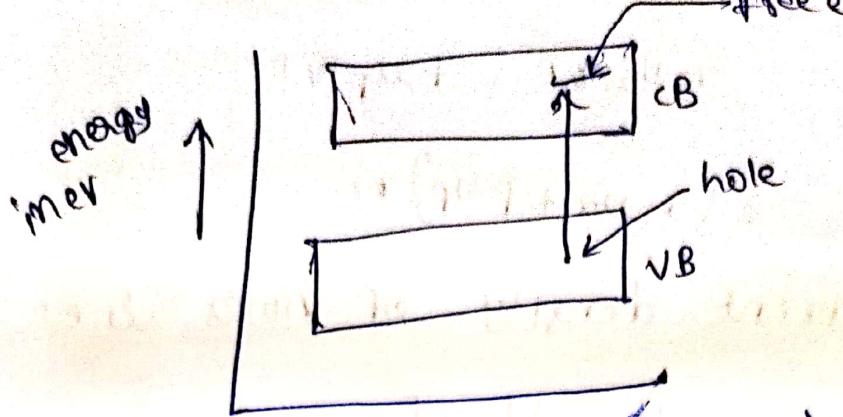
→ Intrinsic semiconductors are pure semiconductors

→ If we increase temperature the resistance decreases

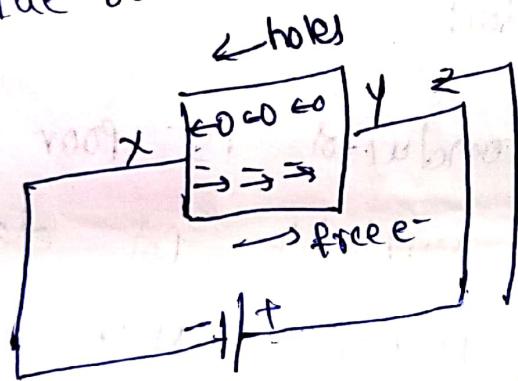
→ In an intrinsic semiconductor, even at room

temp, e-hole pairs are created. when electric field is applied across an intrinsic semiconductor current conduction takes place by two processes

namely free  $e^-$  & holes.



under the influence of electric field total current of the semiconductor is sum of currents due to free e- & holes.  $I = I_n + I_p$



- The current in the external wire is fully by e<sup>-</sup>
- Intrinsic semiconductor behaves as a perfect insulator at absolute '0' temp.
- Intrinsic semiconductor is not useful in electronic devices.
- In intrinsic semiconductor the concentration of holes and e<sup>-</sup> are equal.
- $J = J_p + J_n$

$$= n\mu_n E + p\mu_p E$$

$$= (n\mu_n + p\mu_p) E$$

$J$  - current density of holes &  $e^-$

$\mu_n$  - mobility of  $e^-$

" hole

$\mu_p$  - "

$n$  - concentration of  $e^-$

" hole.

$p$  - "

Extrinsic semi conductor

$\Rightarrow$

Intrinsic semi conductor is poor at room temp

$\rightarrow$  Intrinsic semi conductor is not suitable for electronic device

so it is not suitable for electronic device

so current conduction capability of intrinsic

$\rightarrow$  The current conduction should be increased. This

semi conductor can be achieved by adding small amount of

impurity of intrinsic semi conductor, so that

it becomes extrinsic (N) impure semi conductor.

$\rightarrow$  This process of adding impurity is known as

doping.

$\rightarrow$  The amount of impurity added is extremely small i.e 1 to 2 atoms of impurity for  $10^6$  intrinsic atoms.

extrinsic Semiconductors are classified into 2 types

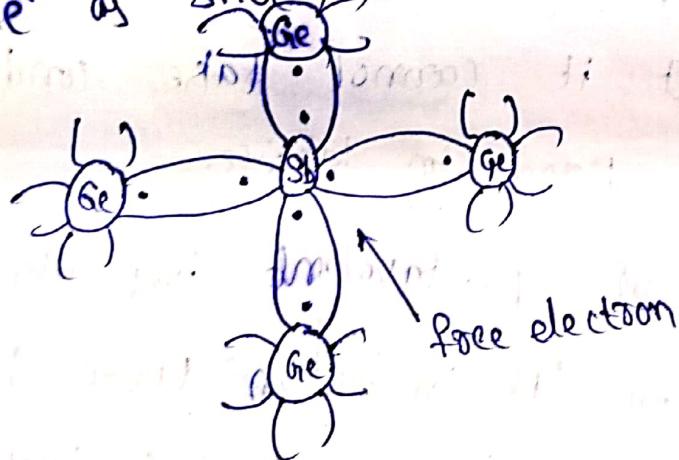
1. p-type semi conductor
2. n-type semi conductor.

### N-type semi conductor

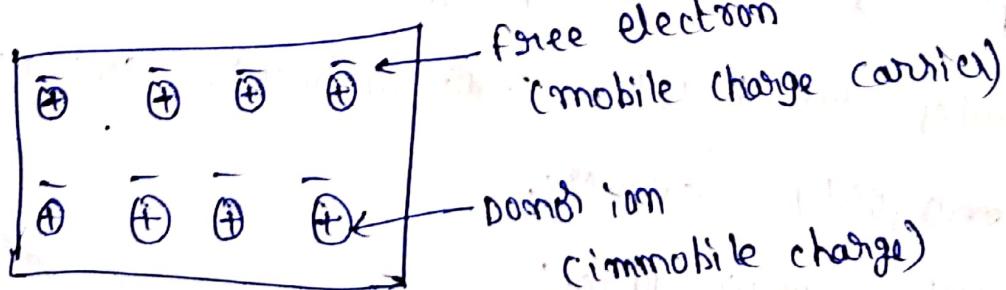
→ A small amount of pentavalent impurities such as arsenic, antimony or phosphorous is added to the pure semiconductor (Ge or Si) crystal to get N-type semiconductor.

→ Ge atom has 4 valence e<sup>-</sup> & antimony has 5

valence e<sup>-</sup> as shown in fig ①



### n-type semiconductor (a) formation of covalent bonds



### (b) charged carriers

→ Antimony atom forms a covalent bond with surrounding four Ge atoms. & fifth valence e<sup>-</sup> is

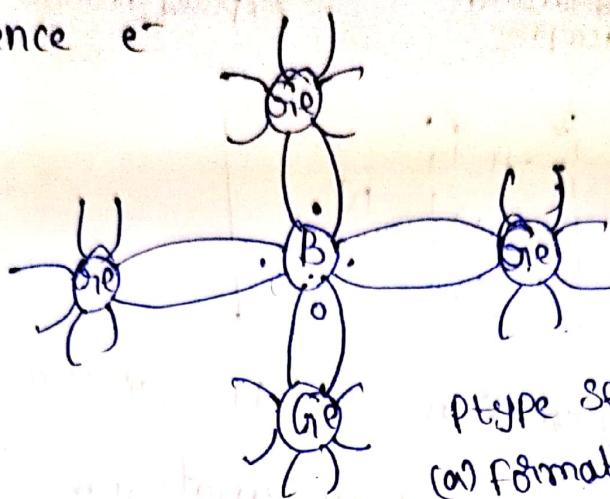
left free which is loosely bound to the antimony(Sb) atom.

- The loosely bound  $e^-$  can be easily excited from the VB to CB by increasing the thermal energy.
- every Antimony(Sb) atom contributes one conduction  $e^-$  without creating a hole. such pentavalent impurities are called donor impurities.
- It donates one  $e^-$  for conduction, the donor atom becomes positively charged ion because it lost one  $e^-$  but it ~~cannot~~ take conduction.
- it is firmly fixed in lattice.
- The addition of pentavalent impurity increases the no. of  $e^-$  in the conduction thereby increasing the conductivity of N-type semi conductor.
- As a result of doping, the no. of  $e^-$  exceeds the no. of holes in N-type semi conduct. so  $e^-$  are called majority carriers.

### P-type semiconductor

- A small amount of trivalent impurities such as boron, aluminium is added to the pure semiconductor.

→ Boron atom has 3 valence e<sup>-</sup> & Boron has 3 valence e<sup>-</sup> →



p-type semi conductor

(a) formation of covalent bonds

→ 3 valence e<sup>-</sup> in boron atom forms a covalent bond

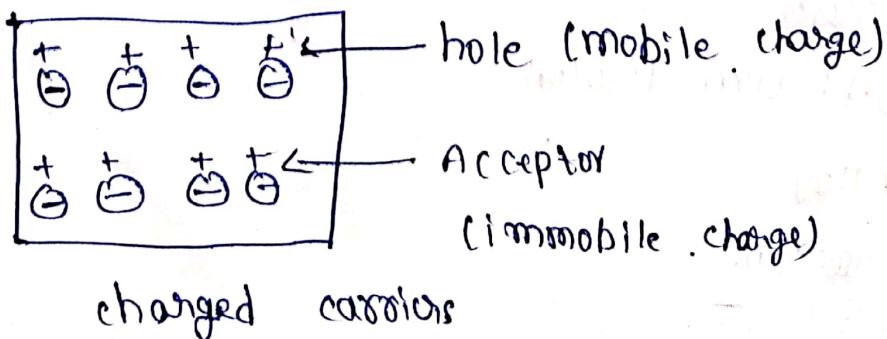
→ Ge atom leaving one bond incomplete which gives rise to a hole.

→ Trivalent impurities added to the pure semiconductor and introduce a large number of holes in the intrinsic semiconductor.

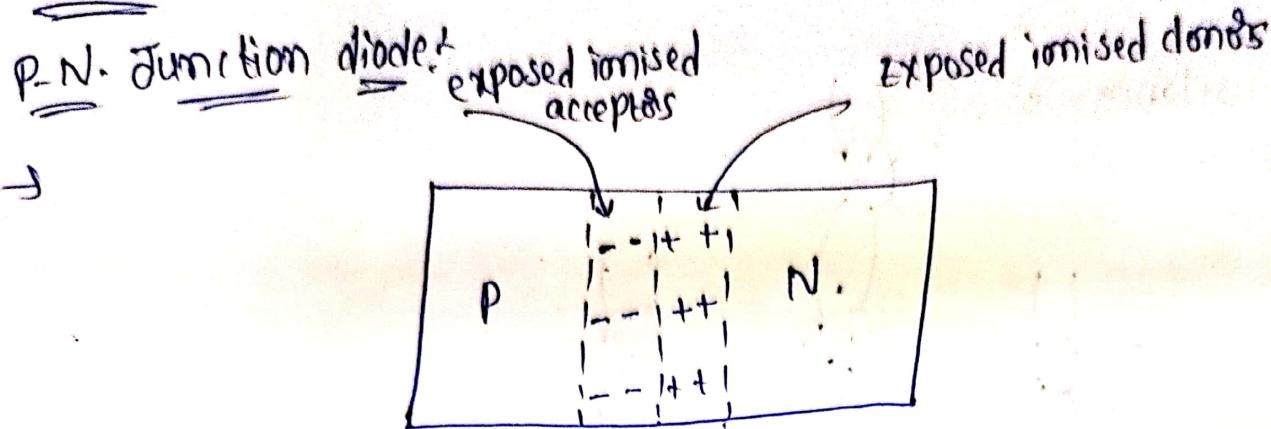
→ Trivalent impurity such as boron is called acceptor impurity.

→ each boron atom donates a hole for conduction. it becomes a -ve charged ion.

→ no. of holes is very much greater than the no. of electrons the majority charge carriers are holes.



## Diode



formation of PN junction

- In a piece of semi conductor material, if the one half is dopped by P-type impurity and the other half is dopped by N-type impurity, a PN junction is formed.
- In fig N-type material has high concentration of free e- & a P-type material has high concentration of holes.
- A PN junction is formed when P&N type materials are formed in such a way that a continuous crystal lattice is established across the junction.
- This continuity is obtained by 3 types of processes.

1. Diffusion process

2. Alloy

3. Growth.

## Diffusion Process:

- The process of movement of charge carriers from higher concentration to lower concentration, is called as diffusion. & the current is called diffusion current.
  - As free e<sup>-</sup> move from N-type to P-type across the junction. The donor ions become positively charged, hence a positive charge is built in N-side.
  - The e<sup>-</sup> that cross the junction undergo the -ve accepted ions by filling in the holes.
  - therefore a net -ve charge is established on P-side.
  - therefore a net -ve charge prevents the diffusion process.
  - these -ve charged ions prevent the charged ions on the N-side of e<sup>-</sup> into P-side. The charged ions on the N-side repels the hole, crossing from P-side to N-side.
  - because of the barrier set up near the junction.
  - As a consequence of the induced electric field across the depletion layer an electrostatic potential difference is established between P & N regions, which is called potential barrier, junction barrier, diffusion potential or contact potential  $V_0$ .
  - The magnitude of the contact potential varies depends upon the temp, doping levels.
- $V_0$  is 0.3V for Ge  
0.12V for Si

## Formation of Depletion region!

- Depletion region is formed at the junction.
- Depletion region is the region which is depleted of charge carriers i.e. no mobile charge carriers are present in this region.
- If the P-type and N-type materials are equally doped then the depletion layer is equally divided on both sides of junction.

## P-N Junction diode

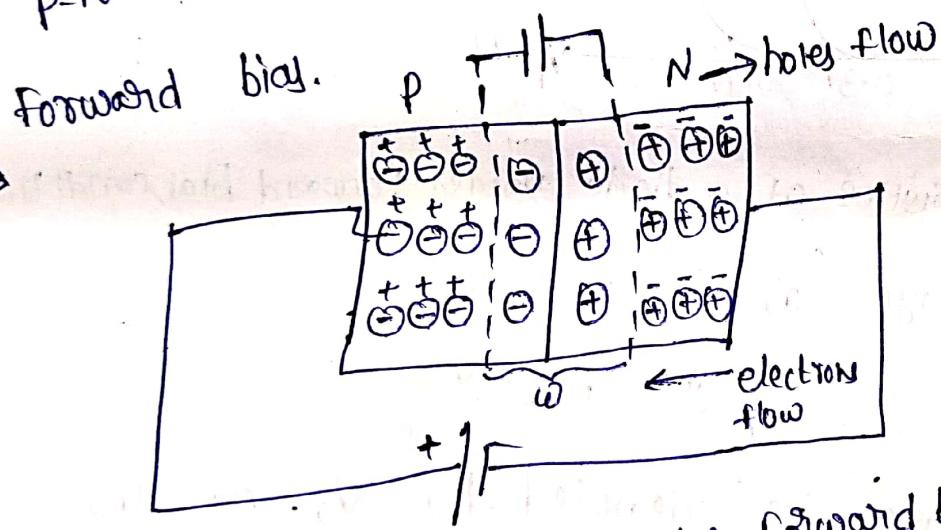


- PN junction diode having two terminals anode & cathode upon the polarities P-N junction diode
- Depending having two biasing condition
- Bias - It is defined as the application of external voltage across the positive terminal.
- There are two types of Biasing condition
  1. forward Bias condition
  2. Reverse Bias condition.

X Diffusion process:  
The movement of charge particles from high concentration to low concentration is called diffusion process.)

Under forward Bias condition:

→ here the positive terminal of the battery is connected to the p-type and negative terminal to the N-type of the p-N junction diode. the bias applied is known as



under forward bias with external battery acting as internal potential barrier.

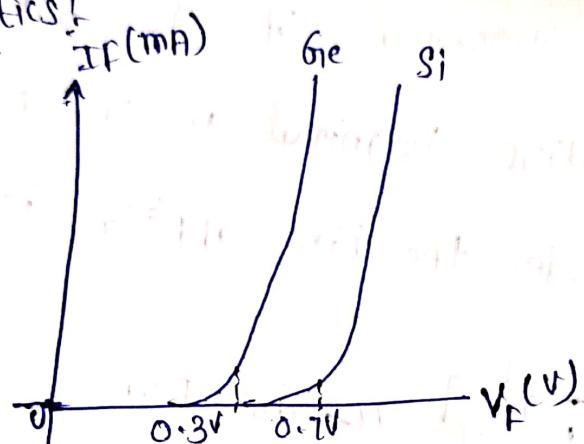
→ The applied potential is in opposition to the internal potential barrier.

→ Under the forward bias condition the applied positive potential repels the holes in p-type region so that holes move towards the junction and applied negative potential repels the e<sup>-</sup> in the N-type region.

the  $e^-$  moves towards the junction.

→ Eventually when the applied potential is more than the barrier potential the depletion region and internal potential barrier disappear.

V-I characteristics:



V-I characteristics of a diode under forward bias condition.

→ The threshold voltage of Ge is 0.3V

Si is 0.7V

→ here threshold voltage is denoted by  $V_0$ . As the forward voltage is increased if  $V_F \geq V_0$ , the forward current  $I_F$  is almost zero. hence  $V_0$  to prevent holes from p-region &  $e^-$  from N-region to flow across the depletion region in the opposite direction.

→ for  $V_F > V_0$  the potential barrier at the junction completely disappears. Hence the

⑧

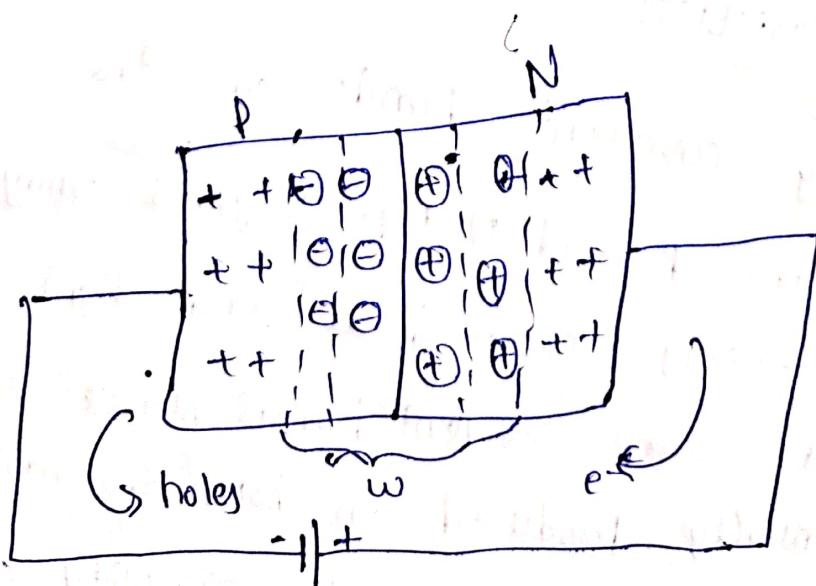
the holes cross the junction from P-type to N-type  
& e<sup>-</sup> cross the junction in the opposite direction.  
→ resulting relatively large current flow in external circuit.

→ At the cut in voltage (8) threshold voltage, the potential barrier is overcome and the current through the junction starts to increase rapidly.

Under Reverse Bias condition:

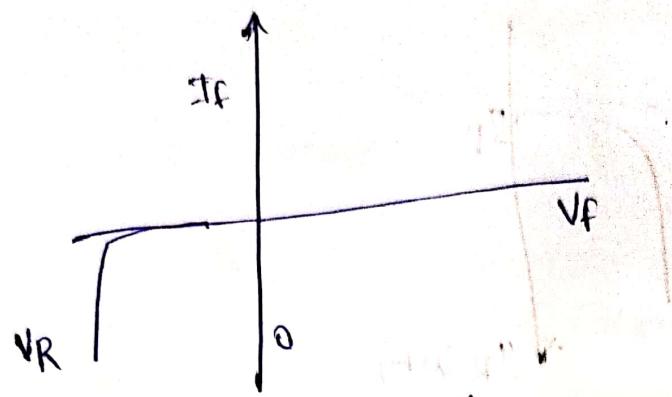
The -ve terminal of the battery is connected to P-type and +ve terminal of the battery is connected to the N-type of the PN-junction. The bias applied is known as reverse bias.

Operation:



PN Junction diode reverse Bias.

- The majority charge carriers on P-side ie holes move towards the -ve terminal of the battery &
  - The minority charge carrier on N-side ie e<sup>-</sup> move towards the +ve terminal of the battery.
  - hence the width of the depletion region which is depleted of mobile charge carriers increases.
  - hence, the resultant potential barrier is increased which prevents the flow of majority carriers in both directions. therefore theoretically no current flow in the external circuit.
  - But a very small current of the order of a few micro amperes flows. under RB condition.
- V-I characteristics:
- e<sup>-</sup> forming covalent bonds of the semi conductor atoms in the P and N-type regions may absorb sufficient energy from heat and light to cause breaking of some covalent bonds. hence e<sup>-</sup>-hole pairs are continually produced in both the regions.
  - The conduction is due to minority charge carriers



Break down voltage

V-I characteristics under Reverse bias.

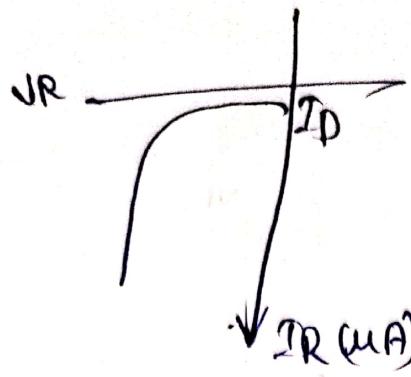
→ The reverse current flows due to minority charge carriers. which are in small in number hence reverse current is very small (in the order of microamperes) always minority charge carriers depends upon the temperature and produces Reverse saturation current (or) leakage current  $I_o$ . through the reverse current is independent of applied voltage.

→ If we inverse the voltage beyond certain limit large current reverse current flows through it and it may damaged to the diode. There is called reverse breakdown. These occurs due to 2 effects.

1. Avalanche Breakdown
2. Zener Breakdown.

### V-I characteristics in the III quadrant

→ The reverse is due to minority charge carriers and it is spotted in the III Quadrant



- when we increase the reverse voltage initially reverse current ( $I_D$ ) is constant.
  - when we increase the voltage further the breakdown occurs at point 'A' as shown in fig and then the current increases rapidly.
  - The voltage when breakdown occurs is called as Breakdown voltage or Avalanche Breakdown voltage.
- Diode Resistance
- An ideal diode have zero resistance in FB condition & infinite resistance in RB condition.
  - But in practical no diode can acts as an ideal diode, ie an actual diode does not behave as a perfect conductor when forward biased & as a perfect insulator when Reverse biased.

10

→ Depending upon the applied voltage, the resistance level changed.

→ Resistance of crystal diode:

- 1. static resistance →
  - forward resistance
  - reverse resistance
- 2. dynamic resistance →
  - forward
  - reverse
- AC resistance

→ static resistance in f.B

$$R_F = \frac{V_F}{I_F}$$

→ static resistance in R.B

$$R_R = \frac{V_R}{I_R}$$

→ dynamic resistance in f.B

$$r_f = \mu \frac{\Delta V_F}{\Delta I_F} \rightarrow 0 \frac{\Delta V_F}{\Delta I_F} = \frac{dV_F}{dI_F}$$

→ Dynamic resistance in Reverse bias

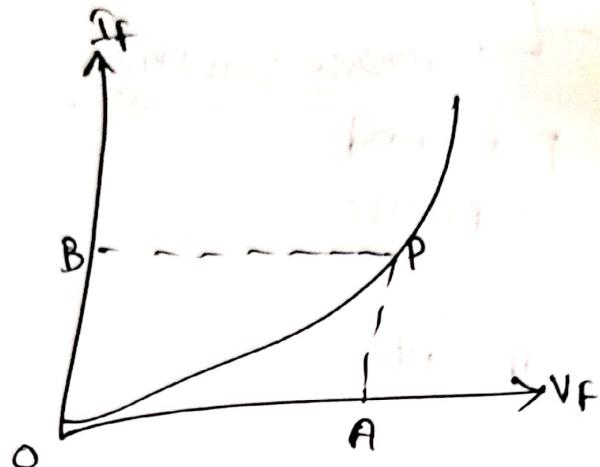
$$r_R = \mu \frac{\Delta V_R}{\Delta I_R} \rightarrow 0 \frac{\Delta V_R}{\Delta I_R} = \frac{dV_R}{dI_R}$$

→ The static resistance exhibits large variation with voltage and current. It is not useful

Parameter. dynamic resistance useful for small signal operation.

## DC forward Resistance:

$$r_f = \frac{\text{DC voltage across the diode}}{\text{DC current}}$$



$$R_f = \frac{OA}{OB}$$

i) ac forward resistance:

$$r_f = \frac{\text{change in voltage across diode}}{\text{corresponding change in current through the diode}}$$

→ The forward resistance of the diode is small changing from 1 to 2Ω

2. Reverse resistance:

→ The resistance offered by the diode to the reverse bias is known as reverse resistance.

→ It can be DC or AC reverse resistance depending on whether the reverse bias is direct or changing voltage.

→ Reverse resistance of diode is infinite.

→ It is very large compared to forward resistance.

→ Great range from MSL

→ Dynamic resistance varies inversely with current

$$\text{ie } \delta_F = \frac{nV_T}{I}$$

when  $V_T = \frac{I}{11600} \rightarrow$  The volt equivalent of Temperature

$n$  - constant

$n$  is 1 for Ge

$n = 2$  for Si At room temp  $V_T = 26mV$ .

→ AC resistance of the diode is sum

$$\delta_F = \delta_b + \delta_j$$

↙ Function resistance

bulk resistance

→ Bulk resistance is the sum of the ~~other~~ ohmic resistance of the p and N-type semiconductor.

Transition

Equivalent circuit:

Equivalent circuit is a combination of elements (like R, L, C) properly chosen to best represent the actual characteristics of device in a operating region.

→ To simplify the circuit and reduce time we use the equivalent circuit

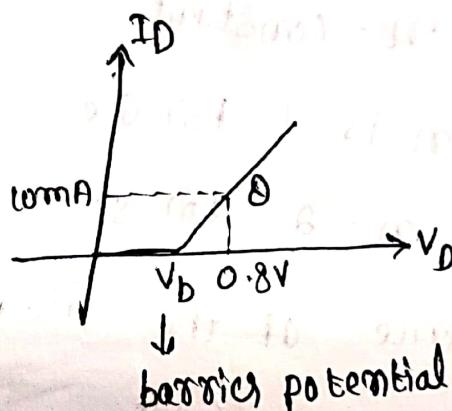
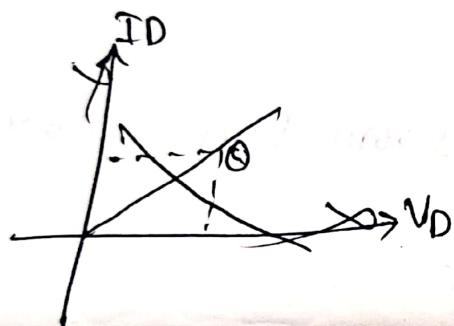
→ 3 types of equivalent circuits

1. Piecewise linear equivalent circuit

2. constant voltage drop / simplified equivalent circuit

3. Ideal equivalent circuit

1. piecewise linear equivalent ckt:



$$\text{Si} \rightarrow 0.7V$$
$$\text{Ge} \rightarrow 0.3V$$

$$\text{diode resistance } r_d = \frac{1}{\text{slope}}$$

slope = tan $\theta$  from mathematics

$$\tan\theta = \frac{p}{B} \rightarrow \frac{\text{Perpendicular}}{\text{Base}}$$

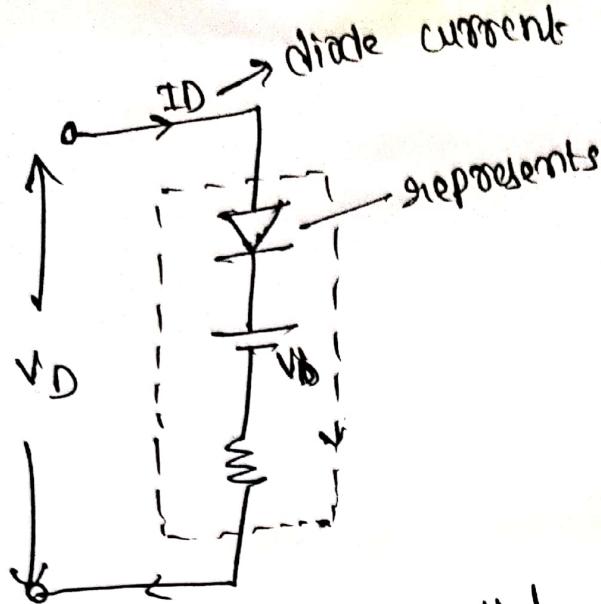
$$\text{slope} = \frac{I_D}{V_D}$$

$$\text{Ohm's law } V_D = I_D r_d$$

$$\frac{1}{\text{slope}} = \frac{V_D}{I_D}$$

$$r_d = \frac{V_p}{I_D}$$

$$\frac{1}{\text{slope}} = r_d$$



→  $V_b$  is barrier potential of diode current which opposes the flow

$$r_d = \frac{0.8 - 0.7}{(10 - 0) \cdot 10^{-3}} = \frac{0.1}{10^1 \times 10^{-3}} = \frac{0.1}{10^{-2}} = \frac{0.1 \times 10^2}{10} = 0.1 \times 100 = 10$$

$$\therefore r_d = 10 \Omega$$

↓  
for piecewise linear equ. ckt model

ii) simplified equivalent circuit:

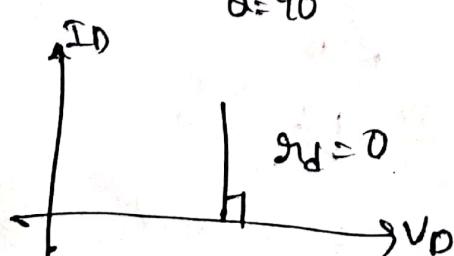
$$r_d = 0$$

$$\frac{1}{\text{slope}} = 0 \Rightarrow \text{slope} = \infty$$

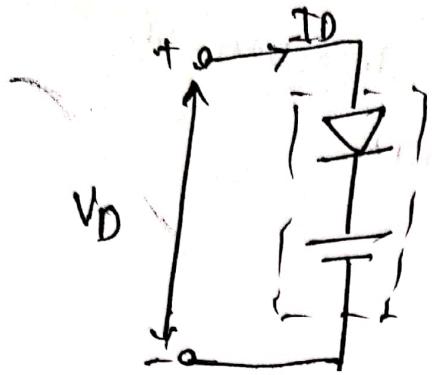
$$\tan \theta = \infty$$

$$\theta = \tan^{-1}(\infty)$$

$$\theta = 90^\circ$$



→ here there is no diode resistance,

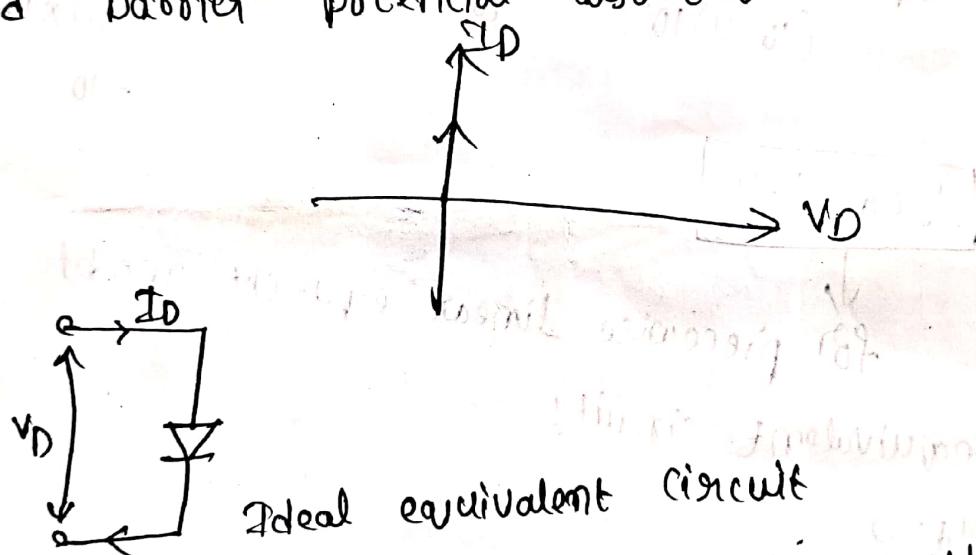


iii) Ideal equiv. Ckt:-

$$R_d = 0$$

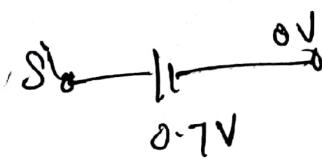
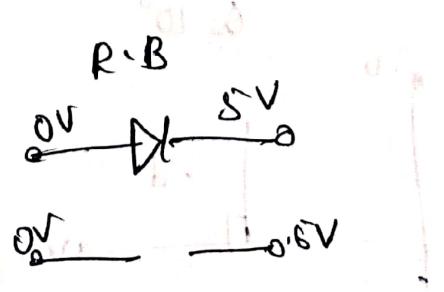
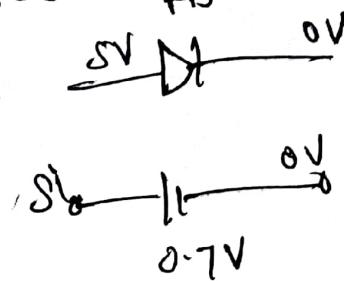
$$V_D = 0$$

→ In case of ideal equivalent circuit diode resistance and barrier potential also zero.



→ compared to 3 models we mostly used as a simplified equivalent circuit.

→ when you solve numerical problem we use and model. fB



## Transition (Ø) space charge (Ø) Depletion Region capacitance (C<sub>T</sub>)!

- Under reverse bias condition, The majority carriers move away from the junction, thereby uncovering more immobile charges.
- Hence the width of the depletion layer at the junction increases with reverse voltage.
- This voltage may be considered as a capacitive effect with applied electric field.
- capacitor stores electric charge in the form of electric field between two electrically conducting plates.
- These plates separated by an insulating material called dielectric.
- ΔQ - increase in charge caused by change in voltage dV.
- A change in voltage dV in a time dt will result in a current I =  $\frac{dQ}{dt}$
- I = C<sub>T</sub>  $\frac{dV}{dt}$

## CT - transition capacitance.

- A PN Junction is formed from a single crystal intrinsic semiconductor by doping part of it with acceptor impurities.
- The change in impurity concentration from p to n-type semiconductor occurs in very short length, typically much less than 1μm.
- The P-type material is formed by addition of acceptor type impurity atoms (Ra, In) to pure silicon crystals.
- The number of holes added is equal to the no. of boron atoms (acceptor impurity) because each atom contributes one hole.
- When hole moves from P-type to N-type the remaining atom becomes -ve ion.
- In reverse biased condition, the width of the space charge region at the junction increases with reverse voltage.

due to this reason the capacitive effect (4)  
exhibited.

$$\rightarrow I = C_T \frac{dV}{dt} \cdot m$$

→  $C_T$  is not a constant but it changes  
with reversed voltage.

Abrupt alloy (or) step graded junction's

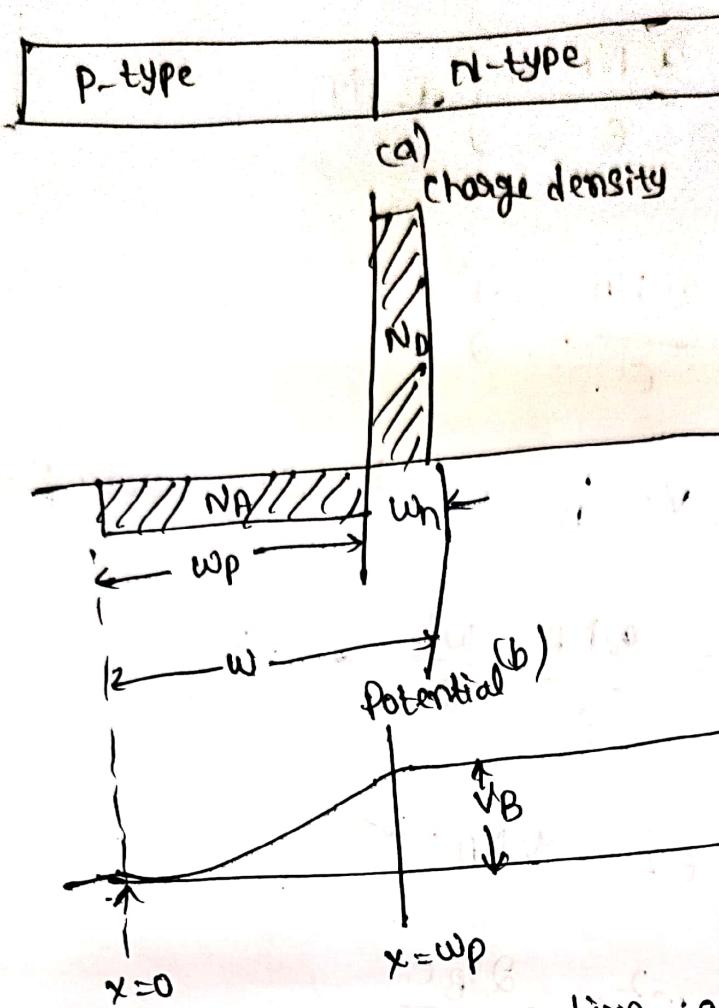
→ In this, there is a sudden step change from  
acceptor ions on one side to donor ions on the  
other side.

→ such a junction is fabricated by placing  
trivalent indium against N-type Ge and heating  
the combination to a high temperature, for a short  
time.

→ Since some of the indium dissolve into Ge,  
the N-type Ge is changed into P-type at the  
junction. Such a step graded junction is called  
alloy (or) fusion junction.

→ Step graded Junction is also formed between  
emitter and base of integrated transistor.

- In grown junction the doping concentration is equal for both p-type and n-type which case the donor and acceptor concentrations are functions of distance across the junction.
- NA - density of acceptor concentration  
 ND - density of donor concentration
- the acceptor density  $N_A$  gradually decreases and the donor density  $N_D$  increases till  $N_A = N_D$ .  
 ∵  $N_D$  increase,  $N_D \downarrow$  decreases to zero
- figure shows PN diode which is asymmetrically doped at the junction if  $N_A < N_D$  then  $w_p > w_n$   
 $w_p$  - width of depletion region at P-type  
 $w_n$  - width of depletion region at N-type



charge density and potential variation at an Alloy  
PN junction

According to poisson equation:

$$\frac{d^2V}{dx^2} = \frac{\alpha r N_A}{\epsilon} \quad \text{①}$$

Integrated eqn ① w.r.t  $x'$

$$\int \frac{d^2V}{dx'^2} \cdot dx' = \int \frac{\alpha r N_A}{\epsilon} \cdot dx'$$

$$\therefore \int dx = 1$$

$$\frac{dV}{dx} = \frac{\alpha r N_A}{\epsilon} \cdot x$$

again integration on both sides w.r.t  $x'$

$$\int \frac{dV}{dx} dx = \frac{qVNA}{\epsilon} \int qx dx$$

$$\int qx dx = \frac{x^2}{2}$$

$$V = \frac{qVNA}{\epsilon} \cdot \frac{x^2}{2}$$

At  $x = w$ ,  $V = V_B$  ie barrier potential

$$V_B = \frac{qVNA}{\epsilon} \cdot \frac{w^2}{2} \quad \text{--- (3)}$$

$$V_B \cdot \epsilon \cdot 2 = qVNA \cdot w^2$$

$$w^2 = \frac{2V_B \epsilon}{qVNA}$$

$$w = \left( \frac{2V_B \epsilon}{qVNA} \right)^{1/2}$$

$$w \propto (V_B)^{1/2} \quad \text{(3)} \quad w \propto \sqrt{V_B}$$

Differentiate eqn (3) w.r.t  $V$

$$\frac{dV_B}{dV} = \frac{qVNA}{2\epsilon} \cdot \frac{d}{dV} w^2$$

$$\therefore \frac{d}{dV} w^2 = 2w \cdot \frac{dw}{dV}$$

$$\Rightarrow \frac{dV_B}{dV} \rightarrow \text{constant}$$

$$I = \frac{qVNA}{2\epsilon} \cdot \frac{dw}{dV} \cdot 2w$$

(6)

$$\frac{dw}{dv} = \frac{\epsilon}{\pi N A w} \quad \text{--- (1)}$$

→ If  $A$  is the area of cross section of junction, the net charge  $Q$  in the distance  $w$  is

$Q = \text{no. of charge particle} \times \text{charge on each particle}$

$$Q = (N A \times \text{volume}) \sigma$$

$$Q = N A w \sigma$$

Apply differentiation with  $w$

$$\frac{dQ}{dv} = N A \sigma w \cdot \frac{dw}{dv}$$

$$\text{from eqn (1)} \quad \frac{dw}{dv} = \frac{\epsilon}{\pi N A w}$$

$$\frac{dQ}{dv} = N A \sigma w \cdot \frac{\epsilon}{\pi N A w}$$

$$\boxed{\therefore \frac{dQ}{dv} = \frac{\epsilon A}{w}}$$

$A$  - Area of cross section

$w$  - width of depletion region

## Diffusion capacitance! (i) storage capacitance!

- Diffusion capacitance can be considered in forward biased condition.
- The holes move from P-type to N-type and e<sup>-</sup> move from n-side. that means the holes will be injected into n-region, e<sup>-</sup> will be injected into p-region.
- so due to that there will be change in the charge in the P-N junction diode.
- The change in the charge w.r.t voltage in PN junction diode is considered as a capacitive effect. This capacitance is diffusion capacitance.
- $C_D = \frac{dQ}{dV} = \frac{\text{Rate of change of charge at Junction}}{\text{Rate of change of applied forward voltage.}}$

→ The diode current

$$I = \frac{Q}{T}$$

$$Q = I \cdot T \quad \text{---(1)}$$

∴ The average mean life time of holes & e<sup>-</sup>

Diode current equation

$$I = I_0 (e^{\frac{V}{nV_T}} - 1) \quad \text{--- (2)}$$

$$I = I_0 e^{\frac{V}{nV_T}} - I_0$$

$$I + I_0 = I_0 e^{\frac{V}{nV_T}} \quad \text{--- (3)}$$

Substitute eqn (2) in eqn (1)

$$Q = IT$$

$$Q = I_0 (e^{\frac{V}{nV_T}} - 1) T$$

$$Q = I_0 T e^{\frac{V}{nV_T}} - I_0 T$$

Differentiation both sides w.r.t 'V'

$$\frac{dQ}{dV} = I_0 T \underbrace{\frac{d}{dV} e^{\frac{V}{nV_T}}}_{J_1} - \underbrace{\frac{d}{dV} I_0 T}_{\text{This term is also constant i.e (zero)}}$$

$$\frac{dQ}{dV} = T I_0 \cdot e^{\frac{V}{nV_T}} \cdot \frac{1}{nV_T}$$

$$\therefore \frac{d}{dx} e^{ax} = e^{ax} \cdot a$$

From eqn (3) substitute

$$I + I_0 = I_0 e^{\frac{V}{nV_T}}$$

$$\therefore \frac{dQ}{dV} = \frac{T}{nV_T} \cdot (I + I_0)$$

$$I \gg I_0 \text{ so}$$

↓  
Total current

$$\frac{dQ}{dV} = \frac{nI}{qA}$$

$$\therefore Q = \frac{dQ}{dV} = \frac{nI}{qV_T}$$

I - reverse saturation current

The current equation of the diode?

$$I_D = I_0 (e^{\frac{V}{nV_T}} - 1)$$

$I_0$  - Diode current

$I_0$  - Reverse saturation current

V - Applied voltage  $\rightarrow$  forward Bias  $V = +ve$

V - Applied voltage  $\rightarrow$  reverse Bias  $V = -ve$

n - constant  $n=1$  for Ge

$n=2$  for Si

$V_T$  - Thermal voltage in K

$$27^\circ C + 273 = 300^\circ K$$

$$V_T = \frac{kT}{qV}$$

K - Boltzmann constant  $\rightarrow 1.38 \times 10^{-23} J/K$

T - Temperature

$$\text{or} - \text{charge of an } e^{-} = e^{-\frac{(T_2-T_1)}{k}}$$

$\rightarrow$  Saturation current  $I_{D2} = I_{D1} \alpha^{\frac{(T_2-T_1)}{k}} / 10$

Solving Problem!

1. A Si diode has saturation current of 7.5 mA at 300K temperature. Calculate the saturation current at 400K.

$$\text{Given} \Rightarrow I_{D1} = 7.5 \text{ mA}$$

$$300 - 273 = 27^\circ C$$

$$T_1 = 300^\circ K$$

$$400 - 273 = 127^\circ C$$

$$T_2 = 400^\circ K$$

$$I_{D2} = \frac{I_{D1} \alpha^{\frac{(T_2-T_1)}{k}}}{10}$$

$$= \frac{7.5 \times 10^{-6} \times \alpha^{(127-27)}}{10}$$

$$= 7.68 \times 10^{-4}$$