$R_f$ are the two

## 2.2.6 Clamping Circuit Theorem

Under steady-state conditions, for any input waveform, the shape of the output waveform of a clamping circuit is fixed and also the area in the forward direction (when the diode conducts) and the area in the reverse direction (when the diode does not conduct) are related.

***The clamping circuit theorem states that, for any input waveform under steady-state conditions, the ratio of the area $A_f$ under the output voltage curve in the forward direction to that in the reverse direction $A_r$ is equal to the ratio $R_f/R$.***

This theorem applies quite generally independent of the input waveform and the magnitude of the source resistance. The proof is as follows:

Consider the clamping circuit of Figure 2.79, the equivalent circuits in Figures 2.80(a) and 2.80(b), and the input and output waveforms of Figures 2.82(a) and 2.82(b) respectively.

In the interval $0 < t < T_1$, the input is at its upper level, the diode is ON, and the equivalent circuit of Figure 2.80(a) results. If $v_f(t)$ is the output waveform in the forward direction, then the capacitor charging current is

$$i_f(t) = \frac{v_f(t)}{R_f}$$

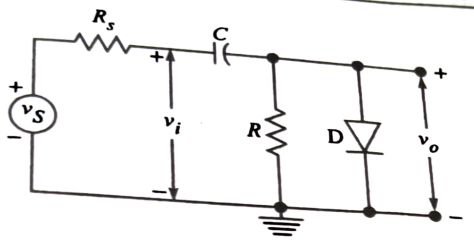



**Figure 2.79** Clamping circuit considering the source resistance and the diode forward resistance.

The precision of operation of the circuit depends on the condition that $R >> R_f$, and $R_r >> R$. When the input is positive, the diode is ON and the equivalent circuit shown in Figure 2.80(a) results. When the input is negative, the diode is OFF and the equivalent circuit shown in Figure 2.80(b) results.

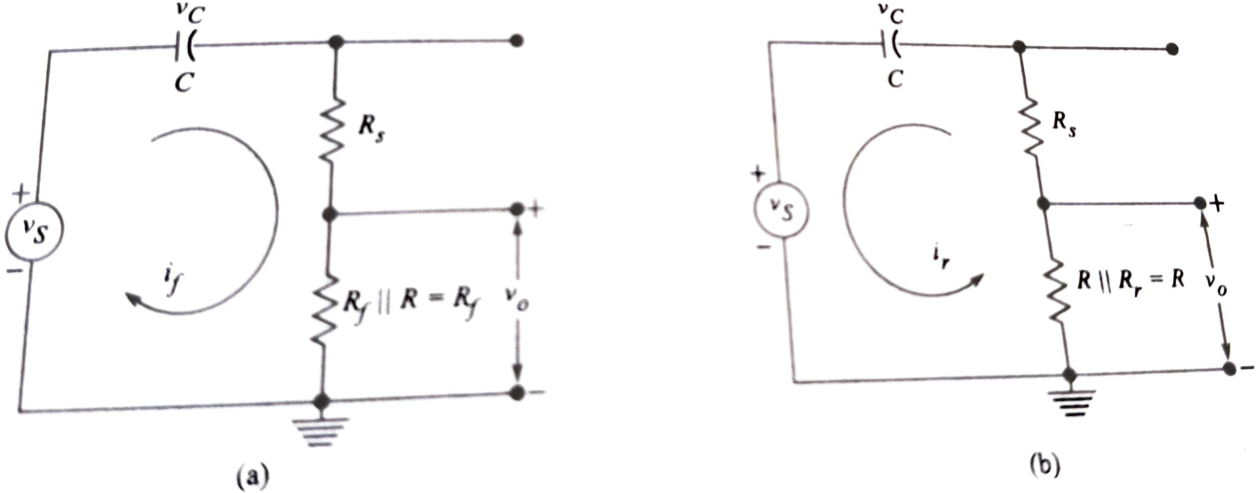



**Figure 2.80** (a) Equivalent circuit when the diode is conducting and (b) the equivalent circuit when the diode is not conducting.

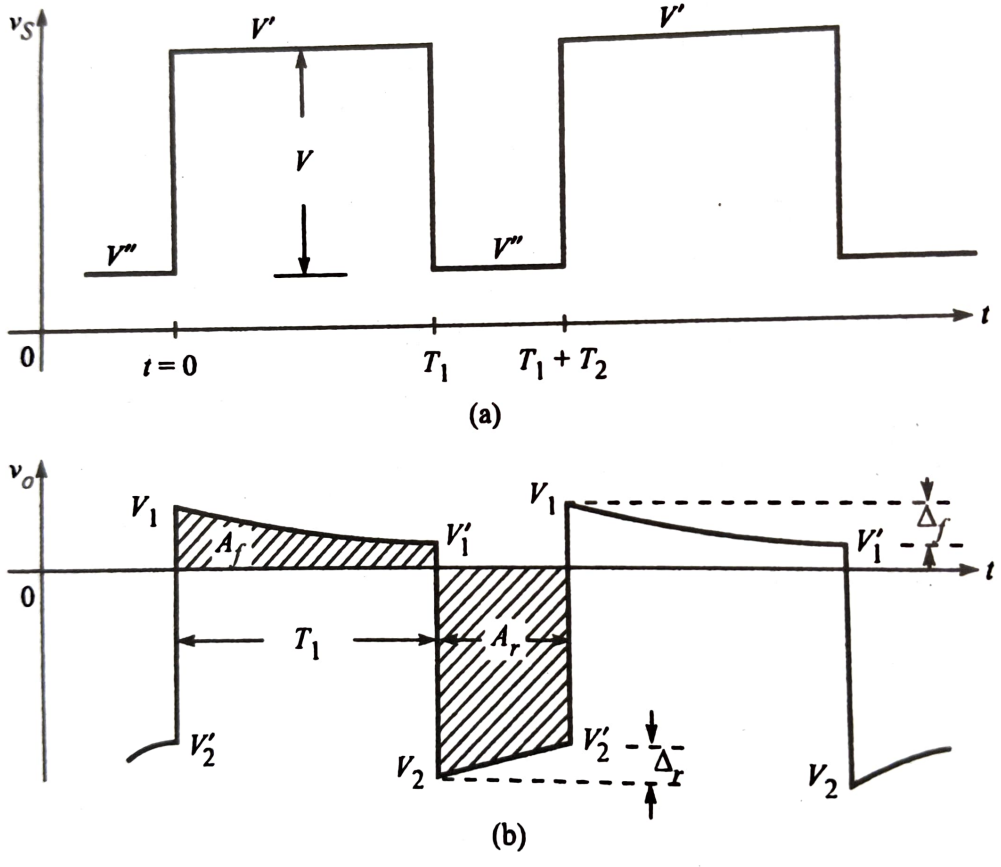



**Figure 2.82** (a) A square wave input signal of peak-to-peak amplitude $V$, (b) the general form of the steady-state output of a clamping circuit with the input as in (a).

Therefore, the charge gained by the capacitor during the forward interval is

$$Q_g = \int_0^{T_1} i_f(t)dt = \frac{1}{R_f}\int_0^{T_1} v_f(t)dt = \frac{A_f}{R_f}$$

In the interval $T_1 < t < T_1 + T_2$, the input is at its lower level, the diode is OFF, and the equivalent circuit of Figure 2.80(b) results. If $v_r(t)$ is the output voltage in the reverse direction, then the current which discharges the capacitor is

$$i_r(t) = \frac{v_r(t)}{R}$$

Therefore, the charge lost by the capacitor during the reverse interval is

$$Q_l = \int_{T_1}^{T_1+T_2} i_r(t)\,dt = \frac{1}{R}\int_{T_1}^{T_1+T_2} v_r(t)dt = \frac{A_r}{R}$$

Under steady-state conditions, the net charge acquired by the capacitor over one cycle must be equal to zero. Therefore, the charge gained in the interval $0 < t < T_1$, will be equal to the charge lost in the interval $T_1 < t < T_1 + T_2$, i.e. $Q_g = Q_l$.

$$\therefore \qquad \frac{A_f}{R_f} = \frac{A_r}{R} \qquad \text{i.e.} \qquad \frac{A_f}{A_r} = \frac{R_f}{R}$$

**EXAMPLE 2.25** An unsymmetrical square wave with $T_1 = 1$ ms and $T_2 = 1$ μs has an amplitude of 20 V. This

3. As timing markers generated
4. In phase meters
5. In amplitude distribution analyzers
6. To obtain square wave from a sine wave
7. In analog-to-digital converters.

## 2.2 CLAMPING CIRCUITS

Clamping circuits are circuits, which are used to clamp or fix the extremity of a periodic waveform to some constant reference level $V_R$. Under steady-state conditions, these circuits restrain the extremity of the waveform from going beyond $V_R$. Clamping circuits may be one-way clamps or two-way clamps. When only one diode is used and a voltage change in only one direction is restrained, the circuits are called one-way clamps. When two diodes are used and the voltage change in both the directions is restrained, the circuits are called two-way clamps.

### 2.2.1 The Clamping Operation

When a signal is transmitted through a capacitive coupling network (*RC* high-pass circuit), it looses its dc component, and a clamping circuit may be used to introduce a dc component by fixing the positive or negative extremity of that waveform to some reference level. For this reason, the clamping circuit is often referred to as *dc restorer* or *dc reinserter*. In fact, it should be called a *dc inserter*, because the dc component introduced may be different from the dc component lost during transmission. The clamping circuit only changes the dc level of the input signal. It does not affect its shape

### Classification of clamping circuits

Basically clamping circuits are of two types: (1) positive-voltage clamping circuits and (2) negative-voltage clamping circuits.

In positive clamping, the negative extremity of the waveform is fixed at the reference level and the entire waveform appears above the reference level, i.e. the output waveform is positively clamped with reference to the reference level. In negative clamping, the positive

extremity of the waveform is fixed at the reference level and the entire waveform appears below the reference, i.e. the output waveform is negatively clamped with respect to the reference level. The capacitors are essential in clamping circuits. The difference between the clipping and clamping circuits is that while the clipper clipps off an unwanted portion of the input waveform, the clamper simply clamps the maximum positive or negative peak of the waveform to a desired level. There will be no distortion of waveform.

### 2.2.2 Negative Clamper

Figure 3.1(a) shows the circuit diagram of a basic negative clamper. It is also termed a positive peak clamper since the circuit clamps the positive peak of a signal to zero level. Assume that the signal source has negligible output impedance and that the diode is ideal. $R_f = 0\ \Omega$ and $V_\gamma = 0$ V in that, it exhibits an arbitrarily sharp break at 0 V, and that its input signal shown in Figure 2.71(b) is a sinusoid which begins at $t = 0$. Let the capacitor $C$ be uncharged at $t = 0$.

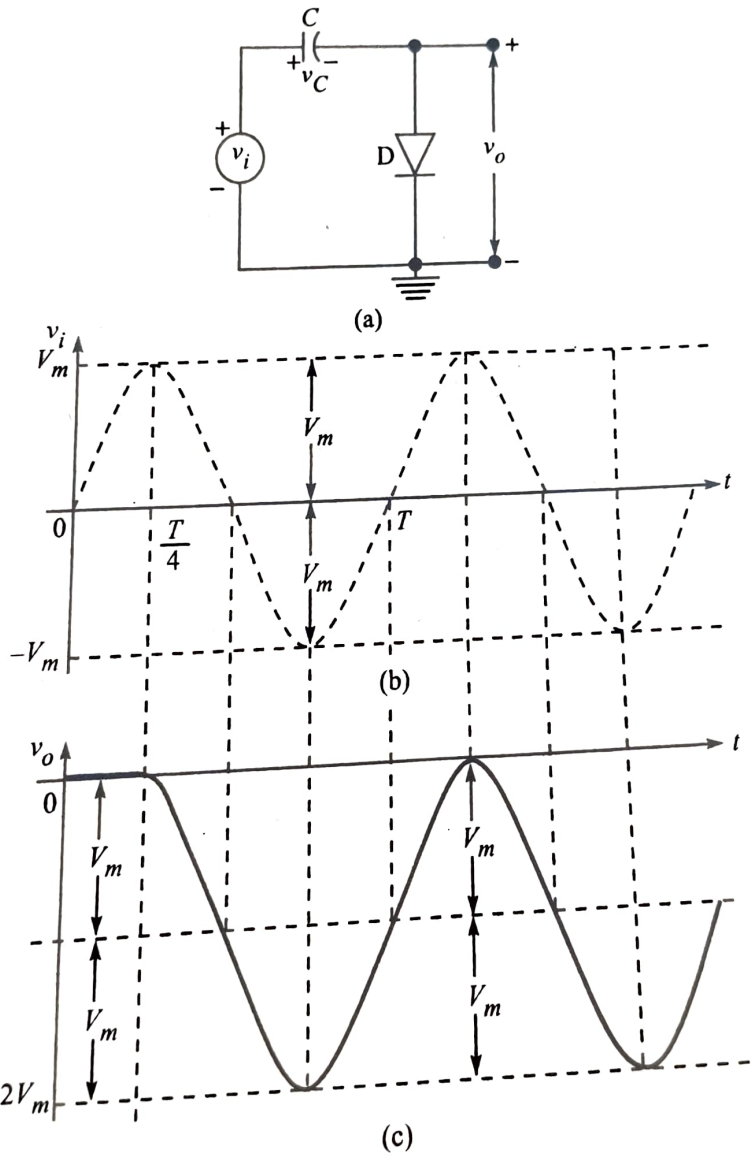



**Figure 2.71** (a) A negative clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

During the first quarter cycle, the input signal rises from zero to the maximum value. The diode conducts during this time and since we have assumed an ideal diode, the voltage across it is zero. The capacitor $C$ is charged through the series combination of the signal source and the diode and the voltage across $C$ rises sinusoidally. At the end of the first quarter cycle, the voltage across the capacitor, $v_C = V_m$.

When, after the first quarter cycle, the peak has been passed and the input signal begins to fall, the voltage $v_C$ across the capacitor is no longer able to follow the input, because there is no path for the capacitor to discharge. Hence, the voltage across the capacitor remains constant at $v_C = V_m$, and the charged capacitor acts as a voltage source of $V$ volts and after the first quarter cycle, the output is given by $v_o = v_i - V_m$. During the succeeding cycles, the positive extremity of the signal will be *clamped* or *restored* to zero and the output waveform shown in Figure 2.71(c) results.

Therefore,

for $v_i = 0$, $v_o = -V_m$.

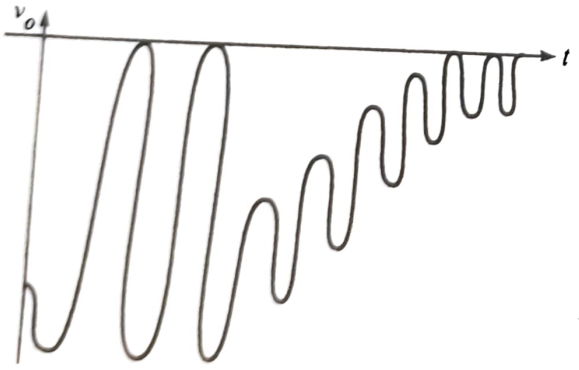
for $v_i = V_m$, $v_o = 0$,

and

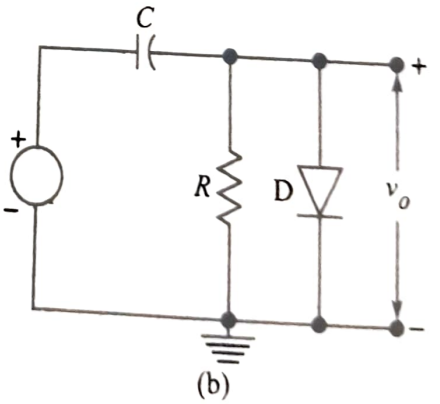
for $v_i = -V_m$, $v_o = -2V_m$.

Suppose that after the steady-state condition has been reached, the amplitude of the input signal is increased, then the diode will again conduct for at most one quarter cycle and the dc voltage across the capacitor would rise to the new peak value, and the positive excursions of the signal would be again restored to zero.

Suppose the amplitude of the input signal is decreased after the steady-state condition has been reached. There is no path for the capacitor to discharge. To permit the voltage across the capacitor to decrease, it is necessary to shunt a resistor across $C$, or equivalently to shunt a resistor across D. In the latter case, the capacitor will discharge through the series combination of the resistor $R$ across the diode and the resistance of the source, and in a few cycles the positive extremity would be again clamped at zero as shown in Figure 2.72(b). A circuit with such a resistor $R$ is shown in Figure 2.72(a).




(a)




(b)

**gure 2.72** (a) Clamping circuit with a resistor $R$ across the diode D and (b) output during transient period.

### 2.2.3 Positive Clamper

Figure 2.73(a) shows a positive clamper. This is also termed as negative peak clamper since this circuit clamps the negative peaks of a signal to zero level. The negative peak clamper, i.e. the positive clamper introduces a positive dc.

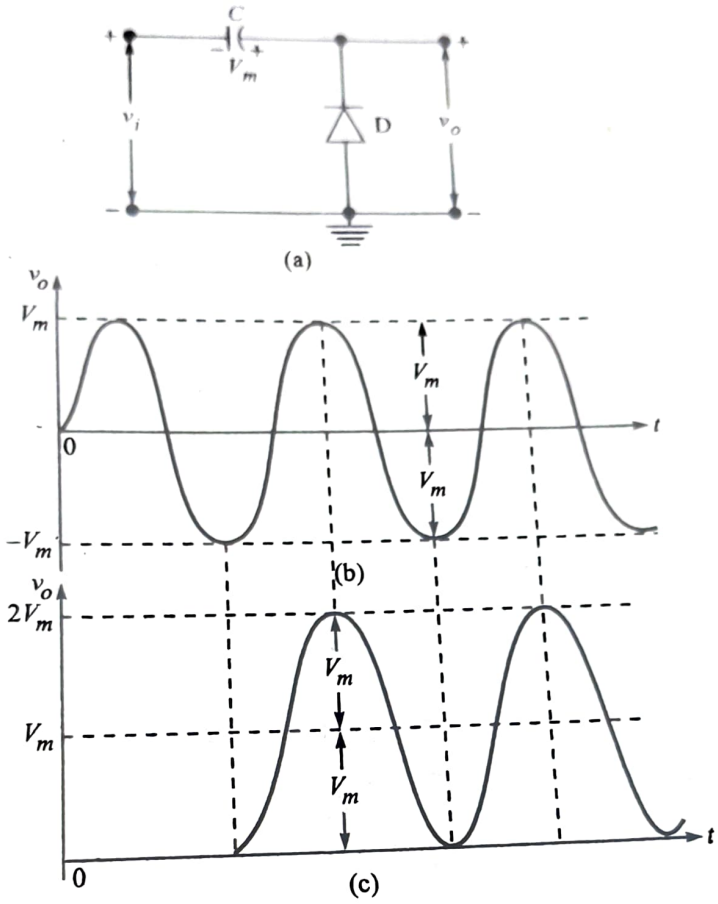



**Figure 2.73** (a) A positive clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

Let the input voltage be $v_i = V_m \sin \omega t$ as shown in Figure 2.73(b). When $v_i$ goes negative, the diode gets forward biased and conducts and in a few cycles the capacitor gets charged to $V_m$ with the polarity shown in Figure 2.73(a). Under steady-state conditions, the capacitor acts as a constant voltage source and the output is

$$v_o = v_i - (-V_m) = v_i + V_m$$

Based on the above relation between $v_o$ and $v_i$, the output voltage waveform is plotted. As seen in Figure 2.73(c) the negative peaks of the input signal are clamped to zero level. Peak-to-peak value of output voltage = peak-to-peak value of input voltage = $2V_m$. There is no distortion of waveform. To accommodate for variations in amplitude of input, the diode D is shunted with a resistor as shown in Figure 2.74(a). When the amplitude of the input waveform is reduced, the output will adjust to its new value as shown in Figure 2.74(b).

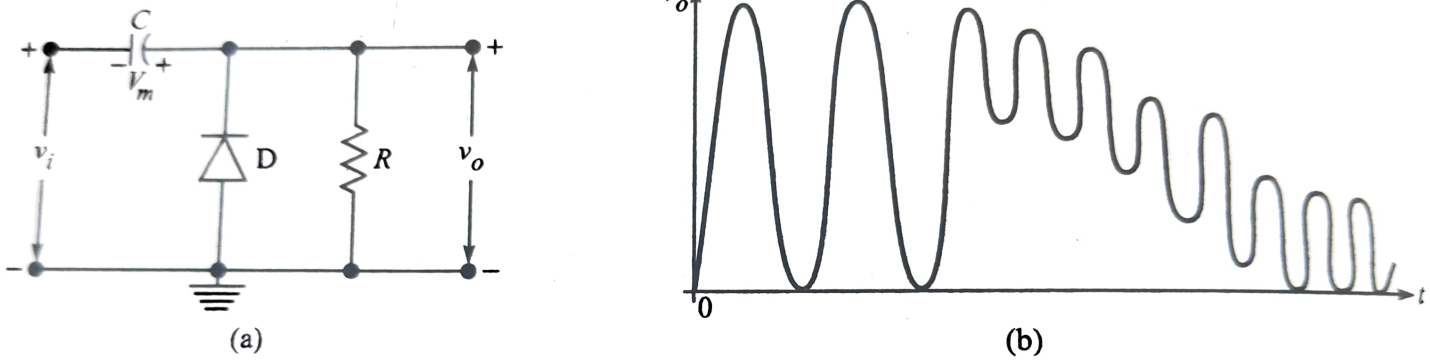



**Figure 2.74** (a) Clamping circuit with a resistor $R$ across D and (b) output during transient period.

### 2.2.4 Biased Clamping

If a voltage source of $V_R$ volts is connected in series with the diode of a clamping circuit, the input waveform will be clamped with reference to $V_R$. Depending on the position of the diode, the input waveform may be positively clamped with reference to $V_R$, or negatively clamped with reference to $V_R$.

**EXAMPLE 2.20** A 100 V peak square wave with a period of 20 ms shown in Figure 2.75(a) is to be positively clamped at 25 V. Draw the circuit di... for this