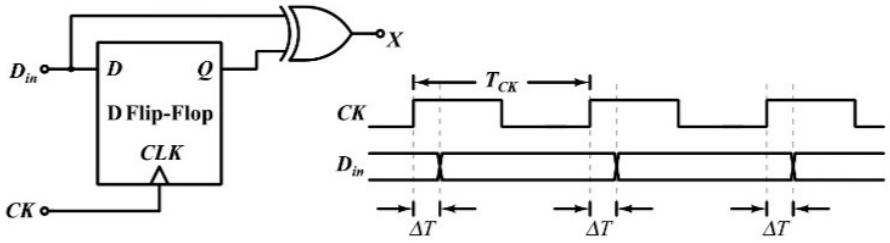
solution assginment 10

lahari

January 2021

1 question

If probability of input data bit(D input) transition in each clock period is 0.3, the average value (in volts,accurate to two decimal places) of voltage at node X,is o.8145V.



2 answer

In the circuit shown above, a positive edge-triggered D Flip-Flop is used for sampling input
data Din using clock CK. The XOR gate outputs 3.3 volts for logic HIGH and 0 volts for logic LOW levels.
The data bit and clock periods are equal and the value of $\Delta T/TCK = 0.15$, where the parameters ΔT and TCK are shown in the figure. Assume that the Flip-Flop and the XOR gate are ideal.
If probability of input data bit(D input) transition in each clock period is 0.3, the average value (in volts,accurate to two decimal places) of voltage at node X,is o.8145V. volatage at $X=\frac{T-\Delta T}{T}.(probability).(voltagevalue)$

$X=1-\frac{\Delta T}{T}.(0.3).(3.3)$

$X=(1-0.15).(0.3).(3.3)=0.8415V$