Ziyan Li

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EDUCATION

Shanghai Jiao Tong University (SJTU) Shanghai, China

Bachelor of Engineering in Computer Science Sept. 2022 – Present

- **ACM Honor Class**: An elite CS program for the top 5% talented students at SJTU.
- **Selected Courses:** Programming Practices: 94, Large Language Model: 98.8, Machine Learning: 91, Computer Vision 100, Visual Content Generation: 95, Reinforcement Learning: 91

RESEARCH GOAL

- My primary research goal is to push robot learning toward an ultimate **generalization** and **dexterity** capability that performs the full spectrum of human skills.

RESEARCH EXPERIENCE

Gupta AI Lab, University of Illinois Urbana-Champaign IL, United States

Research Intern, advised by **Prof. Saurabh Gupta** May 2025 – Present

Project: TALOS: Learning Closed-Loop Tracking forAutonomous Loco-Manipulation in Open-world Scenarios with Humanoid Robots

- Proposed a scalable alternative to demonstration-heavy humanoid learning by formulating loco-manipulation as a structured modular pipeline rather than end-to-end policy learning.
- Built a four-module system—RGB-D perception for 6-DoF grasp pose estimation, motion planning for collision-free trajectories, a unified RL tracking controller trained on human motion data, and a Dex3-hand grasping policy validated with the AnyGrasp dataset.
- Implemented and deployed the complete pipeline on the Unitree G1, enabling reliable mobile pick-and-place behaviors across diverse open-world scenes without imitation learning or real-world data collection.
- Demonstrated strong zero-shot generalization, showing that principled modularization of perception, planning, and control can simplify humanoid behavior synthesis and outperform fragile monolithic policies in novel environments.
- **Co-lead** the project; aiming for submission to **RSS 2026**.

APEX Lab, Shanghai Jiao Tong University Shanghai, China

Research Intern, advised by **Prof. Weinan Zhang** July 2024 – May 2025

Project: Unified Latent Steering and Residual Refinement for Online Improvement of Diffusion Policy Models

- Identified complementary limitations of online adaptation methods in manipulation: sample steering is constrained by the base policy, and residual refinement requires fragile step-size tuning.
- Proposed USR, a unified online adaptation algorithm for diffusion policies that employs a single lightweight actor to jointly generate noise and refine trajectories, enabling multimodal steering and controlled policy deviation without parameter updates of the pretrained policy.
- Released MultiModalBench, a benchmark of six robot manipulation tasks with multiple demonstration modes, providing the first systematic testbed for multimodal policy adaptation.
- Demonstrated the real-world applicability of USR by effectively improving a VLA model on a physical robot, validating its potential for scalable fine-tuning of behavioral foundation models.
- **Co-lead** the project; paper currently under review at **ICLR 2026**. Pdf

PROJECT EXPERIENCE

RAY_TRACER *Rust*

- Achieved highly realistic image rendering by implementing path tracing algorithms to simulate light intensity changes of single rays.
- Modeled objects with varying shapes and materials (dielectrics, metals) based on the *Ray Tracing in One Weekend* series.
- Implemented 7k lines of code in **Rust**. [Code]

Parkour but Safe: Agile Navigation with Parkour Skills *Python, RL*

- Developed a hybrid navigation framework that dynamically switches between parkour skills and obstacle avoidance to balance agility and safety.
- Designed a depth-based policy selector to analyze environmental complexity and execute the optimal strategy, validating improved reliability in simulation.
- Implemented 5k lines of code in **Python**. [Webpage]

Mx* COMPILER *Java, RISC-V*

- Designed a compiler transforming a C/Java-like language (Mx*) to RV32I Assembly.
- Realized a complete pipeline including semantic checking, IR generation, and code optimization.
- Optimized the translation from IR to assembly using the Graph Coloring Register Allocation algorithm.
- Implemented 8k lines of code in **Java**. [Code]

RISC-V CPU *Verilog*

- Designed a RISC-V CPU featuring Write Buffer, ICache, and Branch Prediction.
- Implemented Out-of-Order execution using the Tomasulo algorithm.
- Utilized Vivado to generate bitstream and program the FPGA board.
- Implemented 3k lines of code in **Verilog**. [Code]

❤ Selected Honors and Awards

- **2022 Zhiyuan Honors Scholarship**, top 2% Dec 2022
- **2023 Zhiyuan Honors Scholarship**, top 2% Dec 2023
- **2024 Zhiyuan Honors Scholarship**, top 2% Dec 2024
- **2025 Zhiyuan Honors Scholarship**, top 2% Dec 2025

TECHNICAL SKILLS

- **Robot Platforms**: Unitree G1, XArm
- **Programming**: Python, C++, Java, Rust, Verilog
- **Tools & Frameworks**: PyTorch, Isaac Gym, Isaac Sim, MuJoCo, ROS
- **Languages**: English (TOEFL iBT: 101), Chinese (Native)

Teaching Experience

- **Programming Practice** Jun. - Jul. 2024
- **Computer Architecture** Sep. - Dec. 2024

Role: teaching assistant. Work includes giving lectures, writing guidebooks or guiding documents, creating exam questions, etc