PM8001

Tachyon SPC 8x6G

Firmware Forensic Data Format

Application Note

Released

Issue No. 3: December 2009

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Revision History

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3	December 2009	3.3.4 Corrections: Added missing registers [3300] – [3323]: 3.3.5 Corrections: [4020] - [402F]: => [4020] - [4027]:, [402C]: [41EC] - [4227]: => [41EC]:, [41F8] - [4227]: [43D0] - [43EF]: => [43D0] - [43E7]:, [43EC]: [45B0] - [45E7]: => [45B0] - [45BF]:, [45D0] - [45E7]: [46D0] - [46EF]: => [46D0] - [46E7]:, [46EC]: [47D0] - [4827]: => [47D0] - [47E7]:, [47EC]:,[47F8] - [4827]: [48D0] - [48EF]: => [48D0] - [48E7]:, [48EC]: 3.3.7 Corrections: [0000] - [0023]: => [0000] - [001B]: [0028] - [0037]: => [0028] - [002F]: [003C] - [004B]: => [003C] - [0043]: [0050] - [005F]: => [0050] - [0057]: [0064] - [0073]: => [0064] - [006B]: [0078] - [0087]: => [0078] - [007F]: [008C] - [009B]: => [008C] - [0093]: [00A8] - [00FF]: => [00B0] - [00DF]:,[00F0] - [00FF]: [0930] - [0937]: [0938] - [093F]: => [0930] - [093F]: 3.3.9 Corrections: [6074] - [60CF]: => [6074] - [60AB]:, [60B8] - [60CF]: [A074] - [A0CF]: => [A074] - [A0AB]:, [A0B8] - [A0CF]: [E074] - [E0CF]: => [E074] - [E0AB]:, [E0B8] - [E0CF]: 3.3.11 Formatting changes: [0000] - [005F]: [0060] - [006B]: => [0000] - [006B]: 3.3.14 Formatting changes: [0000] - [005F]: [0060] - [006B]: => [0000] - [006B]: 3.3.19 Formatting changes: [005C]: [0060] - [006F]: => [005C] - [006F]: [007C]: [0080] - [008F]: => [007C] - [008F]: [009C]: [00A0] - [00AF]: => [009C] - [00AF]: [0290] - [02BF]: [0260] - [028F]: [02C0] - [02EB]: => [0260] - [02EB]: 3.4 Corrections: [0040] - [007B]: => [0040] - [0077]:
2	November 2009	Added complete SPC register map accessible over PCIe
1	June 2009	Application note created.

Table of Contents

List of Tables

1 Introduction

This application note describes what data is required to troubleshoot and firmware issues for the PM8001 Tachyon SPC 8x6G and the data format that PMC-Sierra Applications prefers to receive. The intent of this document is to define a format for all of the information available to the host over PCIe in the SPC memory space.

Numeric Notation

This document uses the following numeric notation:

Table 1 Numeric Notation

Type	Notation	Example
Binary	'b' suffix	00100110b
Decimal	(default)	13
Hexadecimal	'0x' prefix 'x'hxx' prefix	0x5F 13'h0000

Related Standards and Publications

PM8001 SPC 8x6G Documents

1. PMC-2080222, *PM8001 Tachyon SPC 8x6G Programmers Manual*

2 File Formats

Please provide the GSM memory region dumps in Section 3.1 in either a binary or an ASCII file format. If providing a memory dump in ASCII-coded hexadecimal format, please structure the file output so that 8 DWORDs appear per row with 64K per block.

Example

```
3C1B9FE0 277B0A68 03600008 00000000 26F70008 0217B823 3C080040 35080002
40886000 40809000 24080007 40889800 40806800 40804800 2408FFFF 40885800
40086000 00000000 3C010040 01014025 40886000 3C09E000 25291FF8 01304821
3C013FFF 3421F000 01214824 40897801 3C010000 242104F8 00300821 0020F809
:
00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
```

3 Forensic Data

3.1 Host GSM Memory Regions Dump

Provide five dump files of the GSM memory regions as listed in the table below: IO Status Table (IOST), Ring Buffer Storage (RB_storage), Ring Buffer Pointers (RB_pointers), Ring Buffer Access (RB_access), and GSM 1M Shared Memory (GSM_SM).

The shift address in column 4 is the address that is loaded into the MEMBASE-III inbound window shift register to allow host process access of the specified memory region. The use of this register is explained in detail see [1], Section 2.6.1 of the PM8001 Tachyon SPC 8x6G Programmers Manual (PMC-2080222).

Table 2 GSM Memory Regions

Memory Region	Size	Offset	Shift Address
IO Status Table	64KB	0x0000 to 0xFFFF	0x64_0000
IO Status Table	64KB	0x0000 to 0xFFFF	0x65_0000
IO Status Table	64KB	0x0000 to 0xFFFF	0x66_0000
IO Status Table	64KB	0x0000 to 0xFFFF	0x67_0000
RB Storage 0~64K	64KB	0x0000 to 0xFFFF	0x68_0000
RB Storage 64K~128K	64KB	0x0000 to 0xFFFF	0x69_0000
RB Pointers		0x1000 to 0x1FFF	0x6A_0000
RB Access		0x8000 to 0x8FFF	0x6A_0000
GSM SM0	64KB	0x0000 to 0xFFFF	0x40_0000
GSM SM1	64KB	0x0000 to 0xFFFF	0x41_0000
GSM SM2	64KB	0x0000 to 0xFFFF	0x42_0000
:::::			
GSM SM16	64KB	0x0000 to 0xFFFF	0x4F_0000

3.2 Inbound and Outbound Queue Dumps

Please provide dumps of all the inbound and outbound queues that are in use on your SPC 8x6G controller in an ASCII hexadecimal format shown below. The SPC 8x6G controller uses Inbound Queues (IQs) to receive messages from the host. Outbound Queues (OQs) are used to transfer messages to a host. IQs and OQs are circular queues located in host memory. Depending on the host use model, the host can program up to 32 IQs and 32 OQs. See [1] Section 2.3, “Inbound Queues” and Section 2.4, “Outbound Queues” for complete queue descriptions.

Please dump all elements of each queue to the depth defined in the queue’s configuration table. Please do not truncate the queue dump to an arbitrary size that is less than the queue size specified in the queue configuration table.

The example shows a queue created to service Port 0 only. There should be a queue dump file for each queue in use where [X] = the queue number.

IQ[0] Details

```
        depth = 0x100
        latest ci = 0xf6
        latest pi = 0x61
IOMB[0]:
0x81002006 0xd21c28b0 0x00000001 0x00000208 0x00000102 0x00000000 0x00000000 0x00020000
0x9dd20908 0x00000001 0x00000000 0x00000000 0xad89a000 0x00000000 0x00000208 0x00000000
IOMB[1]:
0x81002006 0xa26d2870 0x00000002 0x00000208 0x00000102 0x00000000 0x00000000 0x00000000
0x57d30908 0x00000001 0x00000000 0x00000000 0xad89a000 0x00000000 0x00000208 0x00000000
:
:
:
IOMB[254]:
0x81002006 0x327826b0 0x00000009 0x00000208 0x00000102 0x00000000 0x00000000 0x00000000
0x19d80908 0x00000001 0x00000000 0x00000000 0xad89a000 0x00000000 0x00000208 0x00000000
IOMB[255]:
0x81002006 0xe26c26b0 0x00000009 0x00000208 0x00000102 0x00000000 0x00000000 0x00000000
0x1ad80908 0x00000001 0x00000000 0x00000000 0xad89a000 0x00000000 0x00000208 0x00000000
```

IQ[X] Details

```
        depth = 0x100
        latest ci = 0xf6
        latest pi = 0x61
IOMB[0]:
0xc100202d 0xcafecafe 0x3e000000 0x00000002 0x00100010 0x00000002 0x00000000 0x00000000
0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000
IOMB[1]:
0xc1002004 0xf0f0f0f0 0x00001700 0x000e0010 0x60010650 0x01000000 0x60010650 0x01000000
0x00000100 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000
:
:
:
IOMB[254]:
0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000
0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000
IOMB[255]:
0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000
0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000 0x00000000
```

3.3 GSM Register Dumps

Please provide register dumps of the GSM registers in the format shown below.

Notes:

1. The registers are sparse. Make sure that host does not blindly read a range of addresses. **If the address is not defined, the SPC MIPS CPU will hit a fatal bus exception error.**
2. Register Dump: 4-byte reading each time.
3. Strictly following the order below.
4. All values listed are in hexadecimal.
5. Values enclosed in brackets [0000] refer to a memory address.
6. Individual addresses that aren't part of an address range are shown as [0000]:
7. Consecutive memory address ranges are shown as [0000] - [00B8].

3.3.1 SPC - 0xBF800000 [MEMBASE-III SHIFT = 0x00_0000]

```
Offset:
[0000] - [00FF]:
```

3.3.2 SPC - 0xBF850000 [MEMBASE-III SHIFT = 0x05_0000]

```
Offset:
[0000] - [002F]:
```

3.3.3 BDMA - BF810000 [MEMBASE-III SHIFT = 0x01_0000]

```
Offset:
[0000] - [000B]:
[0010]:
[0020] - [006F]:
[0070]:
[0084] - [008B]:
[0090] - [0097]:
[009C] - [00A3]:
[00A8] - [00AF]:
[00D0] - [00D7]:
[00F0] - [00FB]:
[0100] - [010B]:
[0110] - [011B]:
[0120] - [012B]:
[0130] - [013B]:
[0140] - [014B]:
[0150] - [015B]:
[0160] - [016B]:
[0200] - [027F]:
[0300]:
[0340]:
```

3.3.4 PCIe APP - BF813000 [MEMBASE-III SHIFT = 0x01_0000]

```
Offset:
[3000] - [300B]:
[3010] - [304F]:
[3060] - [306B]:
[3070] - [308B]:
[3100] - [317B]:
[3200] - [327B]:
[3280] - [32A3]:
[3300] - [3323]:
[3328] - [339F]:
[33C0] - [33C7]:
```

```
[3400] - [34FF]:
[3800]:
```

3.3.5 PCIe PHY - BF814000 [MEMBASE-III SHIFT = 0x01_0000]

```
Offset:
[4000] - [401B]:
[4020] - [4027]:
[402C]:
[4040] - [4057]:
[405C]:
[4064] - [406F]:
[40A0] - [40B3]:
[40C0] - [40DF]:
[4100] - [4127]:
[4130] - [413F]:

[4180]:
[41B0] - [41BF]:
[41D0] - [41E7]:
[41EC]:
[41F8] - [4227]:
[4230] - [423F]:
[4280]:
[42B0] - [42BF]:
[42D0] - [42E7]:
[42EC]:
[42F8] - [4327]:

[4330] - [433F]:
[4380]:
[43B0] - [43BF]:
[43D0] - [43E7]:
[43EC]:
[43F8] - [4427]:
[4430] - [443F]:
[4480]:
[44B0] - [44BF]:
[44D0] - [44E7]:

[44EC]:
[44F8] - [4527]:
[4530] - [453F]:
[4580]:
[45B0] - [45BF]:
[45D0] - [45E7]:
[45EC]:
[45F8] - [4627]:
[4630] - [463F]:
[4680]:
[46B0] - [46BF]:
[46D0] - [46E7]:

[46EC]:
[46F8] - [4727]:
[4730] - [473F]:
[4780]:
[47B0] - [47BF]:
[47D0] - [47E7]:
[47EC]:
[47F8] - [4827]:
[4830] - [483F]:
[4880]:
[48B0] - [48BF]:
[48D0] - [48E7]:
[48EC]:
[48F8] - [494B]:
```

3.3.6 PCIe CORE - BF818000 [MEMBASE-III SHIFT = 0x01_0000]

```
Offset:
[8000] - [8047]:
[8050] - [805F]:
[8070] - [808B]:
```

[8094] - [80B7]:
[8100] - [812B]:
[9010] - [9027]:
[9030]:

3.3.7 OSSP - BF820000 [MEMBASE-III SHIFT = 0x02_0000]

Offset:
[0000] - [001B]:
[0028] - [002F]:
[003C] - [0043]:
[0050] - [0057]:
[0064] - [006B]:
[0078] - [007F]:
[008C] - [0093]:
[00B0] - [00DF]:
[00F0] - [00FF]:
[0120] - [0127]:
[0220] - [0227]:
[0320] - [0327]:
[0420] - [0427]:
[0520] - [0527]:
[0620] - [0627]:
[0720] - [0727]:
[0820] - [0827]:
[0908]:
[0910] - [0917]:
[0920] - [0927]:
[0930] - [093F]:

3.3.8 SSPA - 0xBF832000 [MEMBASE-III SHIFT = 0x03_0000]

Offset:
[2000] - [2033]:
[2074] - [20AB]:
[20B8] - [20CF]:
[20E0]:

[6000] - [6033]:
[6074] - [60AB]:
[60B8] - [60CF]:
[60E0]:

[A000] - [A033]:
[A074] - [A0AB]:
[A0B8] - [A0CF]:
[A0E0]:

[E000] - [E033]:
[E074] - [E0AB]:
[E0B8] – [E0CF]:
[E0E0]:

3.3.9 SSPA - 0xBF8420000 [MEMBASE-III SHIFT = 0x04_0000]

Offset:
[2000] - [2033]:
[2074] - [20AB]:
[20B8] - [20CF]:
[20E0]:
[6000] - [6033]:
[6074] - [60AB]:
[60B8] - [60CF]:
[60E0]:
[A000] - [A033]:
[A074] - [A0AB]:
[A0B8] - [A0CF]:
[A0E0]:
[E000] - [E033]:
[E074] - [E0AB]:
[E0B8] - [E0CF]:
[E0E0]:

3.3.10 HSST - 0xBF821000 [MEMBASE-III SHIFT = 0x02_0000]

```
Offset:
[1000] - [104B]:
```

3.3.11 LMS_DSS(A) - 0xBF830000 [MEMBASE-III SHIFT = 0x03_0000]

```
Offset:
[0000] - [006B]:
[4000] - [406B]:
[8000] - [806B]:
[C000] - [C06B]:
```

3.3.12 SSPL_6G - 0xBF831000 [MEMBASE-III SHIFT = 0x03_0000]

```
Offset:
[1000] - [105B]:
[1060] - [107F]:
[10A0] - [10AB]:

[5000] - [505B]:
[5060] - [507F]:
[50A0] - [50AB]:

[9000] - [905B]:
[9060] - [907F]:
[90A0] - [90AB]:

[D000] - [D05B]:
[D060] - [D06B]:
[D06C] - [D07F]:
[D0A0] - [D0AB]:
```

3.3.13 HSST(A) - 0xBF833000 [MEMBASE-III SHIFT = 0x03_0000]

```
Offset:
[3000] - [301B]:
[3020] - [3067]:
[3084] - [30E7]:

[7000] - [701B]:
[7020] - [7067]:
[7084] - [70E7]:

[B000] - [B01B]:
[B020] - [B067]:
[B084] - [B0E7]:

[F000] - [F01B]:
[F020] - [F067]:
[F084] - [F0E7]:
```

3.3.14 LMS_DSS(A) - 0xBF840000 [MEMBASE-III SHIFT = 0x04_0000]

```
Offset:
[0000] - [006B]:
[4000] - [406B]:
[8000] - [806B]:
[C000] - [C06B]:
```

3.3.15 SSPL_6G - 0xBF841000 [MEMBASE-III SHIFT = 0x04_0000]

```
Offset:
[1000] - [105B]:
[1060] - [107F]:
[10A0] - [10AB]:

[5000] - [505B]:
[5060] - [507F]:
[50A0] - [50AB]:

[9000] - [905B]:
```

```
[9060] - [907F]:
[90A0] - [90AB]:

[D000] - [D05B]:
[D060] - [D06B]:
[D06C] - [D07F]:
[D0A0] - [D0AB]:
```

3.3.16 HSST(A) - 0xBF843000 [MEMBASE-III SHIFT = 0x04_0000]

```
Offset:
[3000] - [301B]:
[3020] - [3067]:
[3084] - [30E7]:

[7000] - [701B]:
[7020] - [7067]:
[7084] - [70E7]:

[B000] - [B01B]:
[B020] - [B067]:
[B084] - [B0E7]:

[F000] - [F01B]:
[F020] - [F067]:
[F084] - [F0E7]:
```

3.3.17 MBIC IOP - BF860000 [MEMBASE-III SHIFT = 0x06_0000]

```
Offset:
[0000] - [00BB]:
[00C0]:
[00C8]:
[00D0]:
[00D8]:
[00E0]:
[00E8]:
[00F0]:
[00F8]:
[0100] - [012B]:
[0130] - [013B]:
[0140] - [0167]:
[0180] - [019F]:
[0400] - [040B]:
[0410] - [0507]:
```

3.3.18 MBIC AAP1 - BF870000 [MEMBASE-III SHIFT = 0x07_0000]

```
Offset:
[0000] - [00BB]:
[00C0]:
[00C8]:
[00D0]:
[00D8]:
[00E0]:
[00E8]:
[00F0]:
[00F8]:
[0100] - [012B]:
[0130] - [013B]:
[0140] - [0167]:
[0180] - [019F]:
[0400] - [040B]:
[0410] - [0507]:
```

3.3.19 SPBC - 0xBF890000 [MEMBASE-III SHIFT = 0x09_0000]

```
Offset:
[0000] - [002F]:
[003C] - [004B]:
[005C] - [006F]:
[007C] - [008F]:
[009C] - [00AF]:
```

```
[0100] - [01A3]:
[01C0] - [024B]:
[0260] - [02EB]:
[0360] - [036B]:
[1014] - [1033]:
[1054] - [1073]:
[1094] - [10A7]:
[1400] - [141F]:
[1800] - [181F]:
```

3.3.20 GSM - BFF00000 [MEMBASE-III SHIFT = 0x70_0000]

NOTE: none of the GSM register space is contigious.

```
Offset:
[0000]:
[0008]:
[0020]:
[0028]:
[0070]:
[0078]:
[0080]:
[0090]:
[0098]:
[00A8]:
[0100]:
[0108]:
[0110]:
[0118]:
[0120]:
[0128]:
[0130]:
[0138]:
[0140]:
[0148]:
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[0200]:
[0208]:
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[0218]:
[0220]:
[0228]:
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[0AA8]:
[0AB0]:
[0AB8]:
[0AC0]:
[0AC8]:
[0AD0]:
[0AD8]:
[0AE0]:
[0AE8]:
[0AF0]:
[0AF8]:
[0B00]:
[0B08]:
[0B10]:
[0B18]:
[0B20]:
[0B28]:
[0B30]:
[0B38]:
[0B40]:
[0B48]:
[0B50]:
[0B58]:
[0B60]:
[0B68]:
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[0B78]:
[0B80]:
[0B88]:
[0B90]:
[0B98]:
[0BA0]:
[0BA8]:
[0BB0]:
[0BB8]:
[0BC0]:
[0BC8]:
[0BD0]:
[0BD8]:
[0BE0]:
[0BE8]:
[0BF0]:
[0BF8]:
[0C00]:
[0C08]:
[0C10]:
[0C18]:
[0C20]:
[0C28]:
[0C30]:
[0C38]:
[1000]:
[1008]:
[1010]:
[1018]:
[1020]:
[1028]:
[1030]:
[1038]:
[1040]:
[1048]:
[1050]:
[1058]:
[1060]:
[1068]:
[1070]:
```

```
[1078]:
[1080]:
[1088]:
[1090]:
[1098]:
[10A0]:
[10A8]:
[10B0]:
[10B8]:
[10C0]:
[10C8]:
[10D0]:
[10D8]:
[10E0]:
[10E8]:
[10F0]:
[10F8]:
[1100]:
[1108]:
[1110]:
[1118]:
[1120]:
[1128]:
[1130]:
[1138]:
[1140]:
[1148]:
[1150]:
[1158]:
[1160]:
[1168]:
[1170]:
[1178]:
[1180]:
[1188]:
[1190]:
[1198]:
[11A0]:
[11A8]:
[11B0]:
[11B8]:
[11C0]:
[11C8]:
[11D0]:
[11D8]:
[11E0]:
[11E8]:
[11F0]:
[11F8]:
[1200]:
[1208]:
[1210]:
[1218]:
[1220]:
[1228]:
[1230]:
[1238]:
[1240]:
[1248]:
[1250]:
[1258]:
[1260]:
[1268]:
[1270]:
[1278]:
[1280]:
[1288]:
[1290]:
[1298]:
[12A0]:
[12A8]:
[12B0]:
[12B8]:
[12C0]:
[12C8]:
[12D0]:
```

```
[12D8]:
[12E0]:
[12E8]:
[12F0]:
[12F8]:
[1300]:
[1308]:
[1310]:
[1318]:
[1320]:
[1328]:
[1330]:
[1338]:
[1340]:
[1348]:
[1350]:
[1358]:
[1360]:
[1368]:
[1370]:
[1378]:
[1380]:
[1388]:
[1390]:
[1398]:
[13A0]:
[13A8]:
[13B0]:
[13B8]:
[13C0]:
[13C8]:
[13D0]:
[13D8]:
[13E0]:
[13E8]:
[13F0]:
[13F8]:
[1800]:
[1808]:
[1810]:
[1818]:
[1820]:
[1828]:
[1830]:
[1838]:
[1840]:
[1848]:
[1850]:
[1858]:
[1860]:
[1868]:
[1870]:
[1878]:
[1880]:
[1888]:
[1890]:
[1898]:
[18A0]:
[18A8]:
[18B0]:
[18B8]:
[18C0]:
[18C8]:
[18D0]:
[18D8]:
[18E0]:
[18E8]:
[18F0]:
[18F8]:
[1900]:
[1908]:
[1910]:
[1918]:
[1920]:
[1928]:
[1930]:
```

```
[1938]:
[1940]:
[1948]:
[1950]:
[1958]:
[1960]:
[1968]:
[1970]:
[1978]:
[1980]:
[1988]:
[1990]:
[1998]:
[19A0]:
[19A8]:
[19B0]:
[19B8]:
[19C0]:
[19C8]:
[19D0]:
[19D8]:
[19E0]:
[19E8]:
[19F0]:
[19F8]:
[1A00]:
[1A08]:
[1A10]:
[1A18]:
[1A20]:
[1A28]:
[1A30]:
[1A38]:
[1A40]:
[1A48]:
[1A50]:
[1A58]:
[1A60]:
[1A68]:
[1A70]:
[1A78]:
[1A80]:
[1A88]:
[1A90]:
[1A98]:
[1AA0]:
[1AA8]:
[1AB0]:
[1AB8]:
[1AC0]:
[1AC8]:
[1AD0]:
[1AD8]:
[1AE0]:
[1AE8]:
[1AF0]:
[1AF8]:
[1B00]:
[1B08]:
[1B10]:
[1B18]:
[1B20]:
[1B28]:
[1B30]:
[1B38]:
[1B40]:
[1B48]:
[1B50]:
[1B58]:
[1B60]:
[1B68]:
[1B70]:
[1B78]:
[1B80]:
[1B88]:
[1B90]:
```

```
[1B98]:
[1BA0]:
[1BA8]:
[1BB0]:
[1BB8]:
[1BC0]:
[1BC8]:
[1BD0]:
[1BD8]:
[1BE0]:
[1BE8]:
[1BF0]:
[1BF8]:
[2000]:
[2008]:
[2010]:
[2018]:
[2020]:
[2028]:
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[2038]:
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[2090]:
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[20A8]:
[20B0]:
[20B8]:
[20C0]:
[20C8]:
[20D0]:
[20D8]:
[20E0]:
[20E8]:
[20F0]:
[20F8]:
[2100]:
[2108]:
[2110]:
[2118]:
[2120]:
[2128]:
[2130]:
[2138]:
[2140]:
[2148]:
[2150]:
[2158]:
[2160]:
[2168]:
[2170]:
[2178]:
[2180]:
[2188]:
[2190]:
[2198]:
[21A0]:
[21A8]:
[21B0]:
[21B8]:
[21C0]:
[21C8]:
[21D0]:
[21D8]:
[21E0]:
[21E8]:
[21F0]:
```

```
[21F8]:
[2200]:
[2208]:
[2210]:
[2218]:
[2220]:
[2228]:
[2230]:
[2238]:
[2240]:
[2248]:
[2250]:
[2258]:
[2260]:
[2268]:
[2270]:
[2278]:
[2280]:
[2288]:
[2290]:
[2298]:
[22A0]:
[22A8]:
[22B0]:
[22B8]:
[22C0]:
[22C8]:
[22D0]:
[22D8]:
[22E0]:
[22E8]:
[22F0]:
[22F8]:
[2300]:
[2308]:
[2310]:
[2318]:
[2320]:
[2328]:
[2330]:
[2338]:
[2340]:
[2348]:
[2350]:
[2358]:
[2360]:
[2368]:
[2370]:
[2378]:
[2380]:
[2388]:
[2390]:
[2398]:
[23A0]:
[23A8]:
[23B0]:
[23B8]:
[23C0]:
[23C8]:
[23D0]:
[23D8]:
[23E0]:
[23E8]:
[23F0]:
[23F8]:
```

3.4 Messaging Unit Register Capture

MSGU Registers [MEMBASE-III SHIFT = Not applicable. These registers are located in MEMBASE I]

The 64-bit BAR specified at PCI configuration address 0x10 (MEMBASE-I) contains the following doorbell and scratchpad registers.

```
Offset:
[0004]:
[0020]:
[0040] - [0077]:
```

3.5 Event Logs

The SPC 8x6G firmware event logs should be retrieved for all firmware debug purposes. The event log entries are encoded in a firmware-defined format. After the event log is retrieved, it is fed to an event log parser, which translates the event log entries to useful descriptions that can be displayed in a user-friendly way.

For details about the event logs, see [1], Section 3.17, “Event Log Operation”. For SPC firmware debug requests the minimum firmware event log requirement is to provide the firmware event logs that are DMA transferred to the host memory. Firmware event logging is based on the MPI configuration table settings for logging level, host address, and host buffer size.

In the case of a SPC 8x6G critical error the last event log transfer from the SPC is written to the flash non-volatile memory (NVM). Please provide the event log written to the flash for complete critical error debug information. For detailed information on critical error reporting, see [1], Section 11.2, “Device Specific Fatal Errors”.

3.5.1 MSGU (AAP1) Event Logs

The MSGU (AAP1) event log that is in the SPC 8x6G is written to the host memory and in the case of a critical error to the flash memory. Please provide this log for complete firmware debug and critical error analysis. PMC recommends a minimum AAP1 event log size of 1M.

3.5.2 IOP Event Logs

The IOP event log that is in the SPC 8x6G is written to the host memory and in the case of a critical error to the flash memory. Please provide the firmware event log for complete firmware debug and critical error analysis. PMC recommends a minimum IOP event log size of 1M.

3.6 MPI Configuration Table

Please provide the MPI configuration table in an ASCII hexadecimal format (firmware revision information highlighted). The MPI configuration information is stored in a configuration table, a memory region mapped to the PCIe memory space and accessible by the host. See [1], Section 5, “Message Passing Interface (MPI) Configuration”.

```
[0000] 53434d50 00000001 01071003 00001000 04000000 0c454040 0000008c 000000f0
[0020] 000008f0 00000020 00000000 09060300 00000000 0a070401 00000000 0a070401
[0040] 00000000 0a070401 00000000 00000000 00000003 799f0060 00380000 00000004
[0060] 00000003 79d70060 00380000 00000004 00000000 0000001c 00003fc0 0000401c
[0080] 00003fc0 0000000e 000011f0
```

3.7 MPI General Status Table (GST)

Please provide the MPI status table in an ASCII hexadecimal format. See [1], Section 5.2.2, “MPI General Status Table Fields”. All fields in the GST are host read-only access.

```
[0000] 91010000 00000000 00000000 85000000 7B000000 00000000 01000000 03000000
[0020] 01000000 01000000 01000000 01000000 01000000 01000000 F9FF0600 00000000
[0040] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[0060] 00000000
```

3.8 MPI Queue Configuration Tables

Provide a file or files with the lists of the configuration parameters for both the IQs and OQs. Show all the inbound and outbound queue configuration tables in an ASCII hexadecimal format. This example shows one IQ and one OQ configuration tables. See [1], Section 5.2.3, “MPI Inbound Queue Configuration Table Fields” and Section 5.2.4, “MPI Outbound Queue Configuration Table Fields”.

MPI IBQ 0 Configuration Table

```
[0000] 01044000 00000000 0090BE04 00000000 8043E104 24000000 00D80000 00000000
```

MPI OBQ 0 Configuration Table

```
[0000] 01044040 00000000 4097BF04 00000000 8C43E104 24000000 00E00000 00000000
[0020] 00000000
```

3.9 PCI Configuration Table

Please provide the PCIe configuration space table from the host.

The following example was created using pci32.exe on a Windows 2003 system. For a Linux system the output of lspci –xxx is suggested.

```
Bus 1 (PCI Express), Device Number 0, Device Function 0
 Vendor 11F8h PMC-Sierra Inc
 Device 8001h Unknown
 Command 0147h (I/O Access, Memory Access, BusMaster, Parity Error Response, System
Errors)
 Status 0010h (Has Capabilities List, Fast Timing)
 Revision 05h, Header Type 00h, Bus Latency Timer 00h
 Self test 00h (Self test not supported)
 Cache line size 32 Bytes (8 DWords)
```

```
PCI Class Storage, type Serial Attached SCSI
Address 0 is a Memory Address (anywhere in 64-bit space) : DD130000h
Address 2 is a Memory Address (anywhere in 64-bit space) : DD120000h
Address 4 is a Memory Address (anywhere in 0-4Gb) : DD110000h
Address 5 is a Memory Address (anywhere in 0-4Gb) : DD100000h
System IRQ 16, INT# A
Expansion ROM of 1Mb decoded by this card (Currently disabled)
New Capabilities List Present:
  Power Management Capability, Version 1.2
    Supports low power State D1
    Supports PME# signalling from mode(s) D0
    PME# signalling is currently disabled
    Current Power State : D0 (Device operational, no power saving)
  Message Signalled Interrupt Capability
    MSI is disabled
    MSI function can generate 64-bit addresses
  PCI Express Capability, Version 2
    Device/Port Type :
      PCI Express Endpoint Device
    Device Capabilities :
    Device Control :
      Unsupported Request Severity is Fatal
    Device Status :
      Correctable Error Detected
      Unsupported Request Detected
    Link Capabilities :
      Maximum Link Speed : Unknown (02h)!!
      Maximum Link Width : x8
      Link Port Number   : 0
    Link Control :
      Asynchronous Clocking in Use
    Link Status :
      Current Link Speed : 2.5Gb/s
      Current Link Width : x4
  MSI-X Capability
```

Hex-Dump of device configuration space follows:

```
0000 F8 11 01 80 47 01 10 00 05 00 07 01 08 00 00 00    ø..€G...........
0010 04 00 13 DD 00 00 00 00 04 00 12 DD 00 00 00 00    ...Ý........Ý....
0020 00 00 11 DD 00 00 10 DD 00 00 00 00 00 00 00 00    ...Ý...Ý........
0030 00 00 00 00 40 00 00 00 00 00 00 00 10 01 00 00    ....@...........
0040 01 50 C3 0B 08 00 00 00 00 00 00 00 00 00 00 00    .PÃ.............
0050 05 70 8A 00 00 00 00 00 00 00 00 00 00 00 00 00    .pŠ.............
0060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00    ................
0070 10 AC 02 00 01 87 D0 01 10 28 09 00 82 3C 03 00    .¬...‡Ð..(..‚<..
0080 00 00 41 10 00 00 00 00 00 00 00 00 00 00 00 00    ..A.............
0090 00 00 00 00 10 00 00 00 00 00 00 00 00 00 00 00    ................
00A0 02 00 01 00 00 00 00 00 00 00 00 00 11 00 0F 00    ................
00B0 00 20 00 00 00 00 40 00 00 00 00 00 00 00 00 00    . ....@.........
00C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00    ................
00D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00    ................
00E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00    ................
00F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00    ................
```

3.10 Version Information (Optional)

Please provide the version information for your firmware and controller in this format:

```
Firmware Release Type = 0x3
       Sub-Minor Number = 0x9
       Minor Number   = 0x7
       Major Number   = 0x1
SPC DeviceId = 0x00008001
SPC Device Revision = 0x00000002
SPC BootStrap Reg = 0x02c0a6a2
SPC Reset Reg = 0x87fe01ff
```

3.11 Host Driver Trace (Optional)

If possible please provide a host driver trace of the IOMB commands sent to the SPC 8x6G in the format shown below. Due to performance considerations this can be a driver configuration option that can be enabled only for problem recreation and advanced debug:

```
Format:

Host driver IQ/OQ IOMB trace (ASCII) - in the order the driver sends commands to and
processes events from the SPC - the format is 32byte Header followed by 64byte IOMB
32byte header format:
DWORD0: 0xCCCC - marker1
DWORD1: 0xDDDD - marker2
DWORD2: seq_number - incremented for every IQ command sent and OQ message processed
DWORD3: 0
DWORD4: Type  - 1 indicates SPC event(OQ), 2 is for IQ command IOMB
DWORD5: Length - number of DWORDs of payload always 0x40 - IOMB size
DWORD6: Host Port ID (phy0..1 port0, phy2..3 port1, phy4..5 port2, phy6..7 port3)
DWORD7: SPC Port ID
--------------------
Current trace sequence number = 0xc2a352
----------------------traces-----------------------
0000CCCC 0000DDDD 00C29078 00000000 00000002 00000040 00000000 00000000 << Host
Information Marker, RQ#, IB/OB flag,
81002006 21E926F0 00000008 00000208 00000102 00000000 00000000 00000000 << IOMB DW1 ~
DW8
89C60908 00000001 00000000 00000000 AD89A000 00000000 00000208 00000000 << IOMB DW9 ~
DW16

0000CCCC 0000DDDD 00C29079 00000000 00000002 00000040 00000000 00000000
81002006 E22B26B0 00000009 00000208 00000102 00000000 00000000 00000000
18D70908 00000001 00000000 00000000 AD89A000 00000000 00000208 00000000

:
:

0000CCCC 0000DDDD 00C29077 00000000 00000002 00000040 00000000 00000000
81002006 92372730 00000007 00000208 00000102 00000000 00000000 00000000
DACA0908 00000001 00000000 00000000 AD89A000 00000000 00000208 00000000
```

3.12 HSST State Capture (Optional)

The steps involved in collecting this information:
1) The related registers are
a) HSST(A) - SM_DEBUG_CNTRL

Phy	Shifted Destination Address : Offset	MEMBASE
0	0x3_0000 : 0x30C8	MEMBASE- III
1	0x3_0000 : 0x70C8	MEMBASE-III
2	0x3_0000 : 0xB0C8	MEMBASE-III
3	0x3_0000 : 0xF0C8	MEMBASE-III
4	0x4_0000 : 0x30C8	MEMBASE-III
5	0x4_0000 : 0x70C8	MEMBASE-III

Phy	Shifted Destination Address : Offset	MEMBASE
6	0x4_0000 : 0xB0C8	MEMBASE-III
7	0x4_0000 : 0xF0C8	MEMBASE-III

b) HSST(A) - SM_STATEMACHE_0

Phy	Shifted Destination Address : Offset	MEMBASE
0	0x3_0000 : 0x30CC	MEMBASE-III
1	0x3_0000 : 0x70CC	MEMBASE-III
2	0x3_0000 : 0xB0CC	MEMBASE-III
3	0x3_0000 : 0xF0CC	MEMBASE-III
4	0x4_0000 : 0x30CC	MEMBASE-III
5	0x4_0000 : 0x70CC	MEMBASE-III
6	0x4_0000 : 0xB0CC	MEMBASE-III
7	0x4_0000 : 0xF0CC	MEMBASE-III

c) HSST(A) - SM_STATEMACHE_1

Phy	Shifted Destination Address : Offset	MEMBASE
0	0x3_0000 : 0x30D0	MEMBASE-III
1	0x3_0000 : 0x70D0	MEMBASE-III
2	0x3_0000 : 0xB0D0	MEMBASE-III
3	0x3_0000 : 0xF0D0	MEMBASE-III
4	0x4_0000 : 0x30D0	MEMBASE-III
5	0x4_0000 : 0x70D0	MEMBASE-III
6	0x4_0000 : 0xB0D0	MEMBASE-III
7	0x4_0000 : 0xF0D0	MEMBASE-III

2) The steps to capture the states for one of the phy is as follows

1. First write 0x0000_0000 in register (a)
2. Than write 0x0000_0100 in register (a)

3. Read register (b)
4. Read register (c)
5. Repeat(loop) the above 4 steps by incrementing by 1 for step 1 & 2 until you have written 0x0000_0105 in register (a). I.e. for 0x0000_0001 & 0x0000_0101, 0x0000_0002 & 0x0000_0102, 0x0000_0003 & 0x0000_0103, 0x0000_0004 & 0x0000_0104 and 0x0000_0005 & 0x0000_0105,

3) Finally capture the above information for all 8 phys

3.13 SSPA State Capture (Optional)

Just before you capture the Register Dumps, you need to perform a write to trigger a bit that will push the SSPA state values into the status registers. Such that when you perform the register dump, the latest states can be captured.

CONTROL REGISTER

Phy	Shifted Destination Address : Offset	MEMBASE
0	0x3_0000 : 0x2000	MEMBASE-III
1	0x3_0000 : 0x6000	MEMBASE-III
2	0x3_0000 : 0xA000	MEMBASE-III
3	0x3_0000 : 0xE000	MEMBASE-III
4	0x4_0000 : 0x2000	MEMBASE-III
5	0x4_0000 : 0x6000	MEMBASE-III
6	0x4_0000 : 0xA000	MEMBASE-III
7	0x4_0000 : 0xE000	MEMBASE-III

Instruction to set the bit
1) First read the register
2) Set bit 27 to 1
3) Write back the modified value to the Control Register
4) Proceed with register dump

End of Document