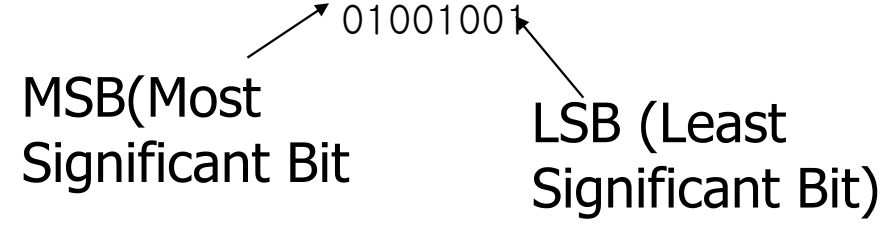
Chap. 5 Logic gates

- **Decimal number** : 0,1 9
- **Binary number** : using 0, and 1
  - Eg. binary 1101=> decimal
    $(1101)_2 = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 1 = 13$

- Hexadecimal: 0-9,A,B,C,D,E,F 16 number
- Eg. $2AC_H = 2 \times 16^2 + 10 \times 16 + 12 = 684$
- BCD code: binary=> decimal for every digit
  - Eg. 345
  - 3->0011, 4->0100, 5 ->0101

- Data structure :1 Byte= 8 bits



00000000=0

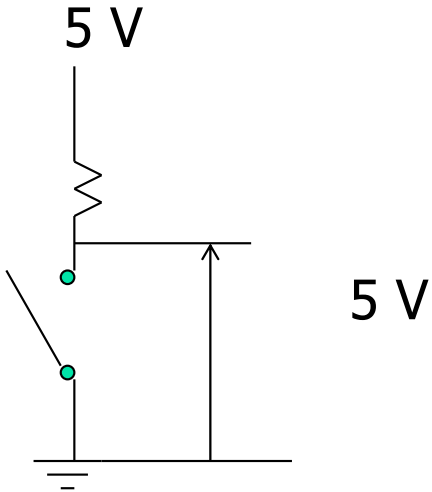
00000001=1

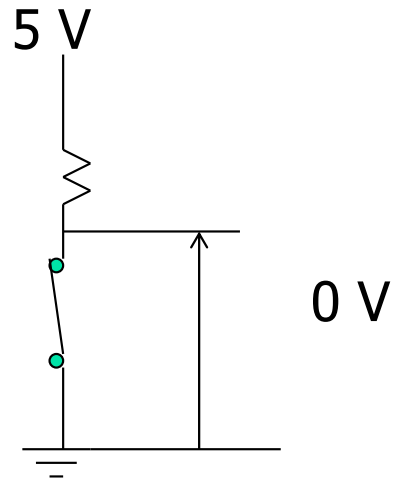
.

.

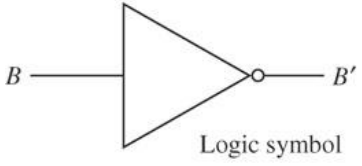
11111111=255

- **Logical level and voltage**
  - Voltage 5 V= “1” digitally
  - Voltage 0 V=“0” digitally





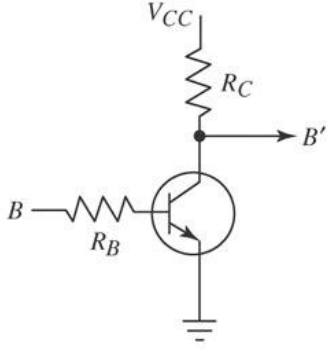
Logic gate (Inverter)



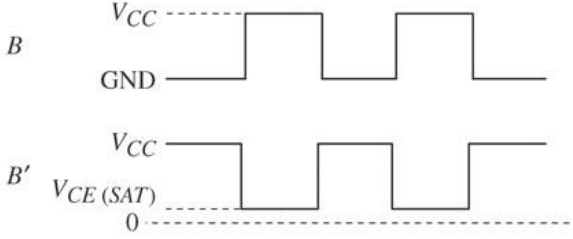
Logic symbol

Input	Output
B	B'
0	1
1	0

Truth table



A transistor logic inverter



Input and output waveforms of a transistor logic inverter

Figure 5.9 The NOT (or inverter) gate.

TTL and CMOS

- TTL: Bipolar transistor family
- CMOS: FET (Field Effect Transistor) family

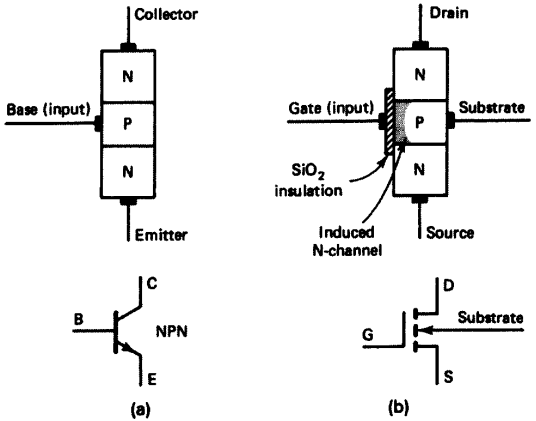
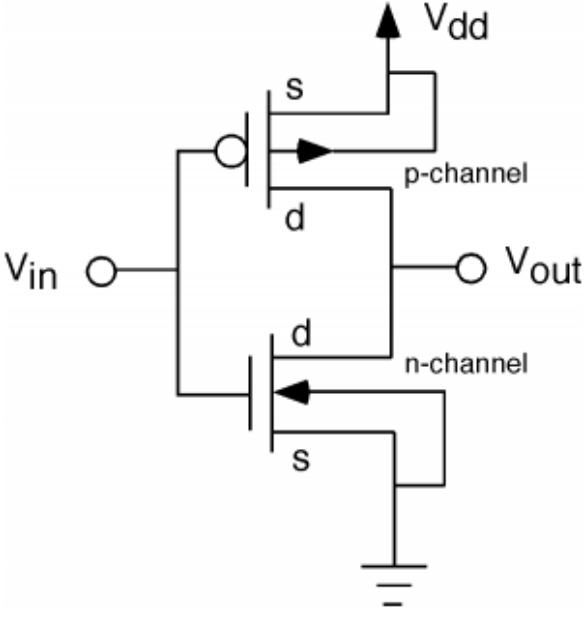


Figure 2–69 Simplified diagrams of bipolar and field-effect transistors: (a) *NPN* bipolar transistor used in TTL ICs; (b) *N*-channel MOSFET used in CMOS ICs.

TTL and CMOS

- Gate level: H=> N channel On, P channel Off
- Gate level: L=> N channel Off, P channel On



CMOS Gate

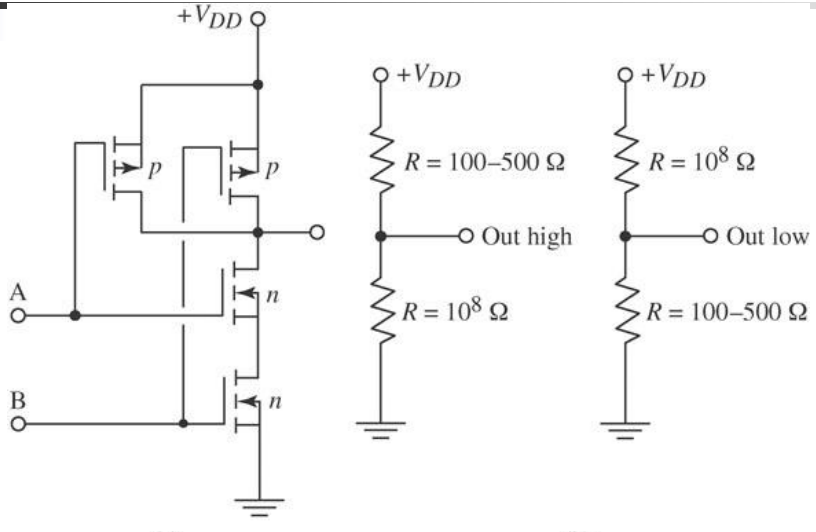


Figure 5.24 CMOS NAND gate (a) and its equivalent output circuit (b).

CMOS gate Logic
High input: P-ch Off
N-ch On
Low Input: P-ch On
N-ch Off

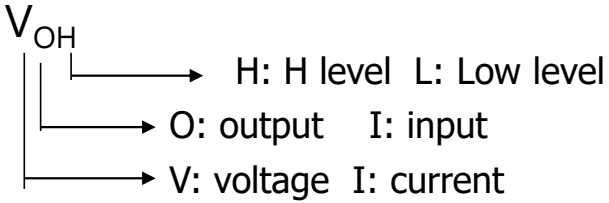
A=H, B=H : Vout=L
A=H, B=L: Vout=H
A=L, B=H: Vout=H
A=L, B=L: Vout=H

TTL level

1. **TTL** 레벨

H level: 5V , L level: 0V

2. Notation



3. TTL level

V_{OL} : L level output voltage $\leq$ 0.4 V

V_{IL} : L level recognized input voltage $\leq$0.8 V

V_{OH} : H level output voltage $\geq$ 2.4 V

V_{IH} : H level recognized input voltage $\geq$2.0 V

TTL level and Noise margin

1. **Noise margin**

   Recognizable Voltage difference between output and input signal

2. Adding noise to a low-level output=> recognizable signal due to noise margin

3. Voltage level

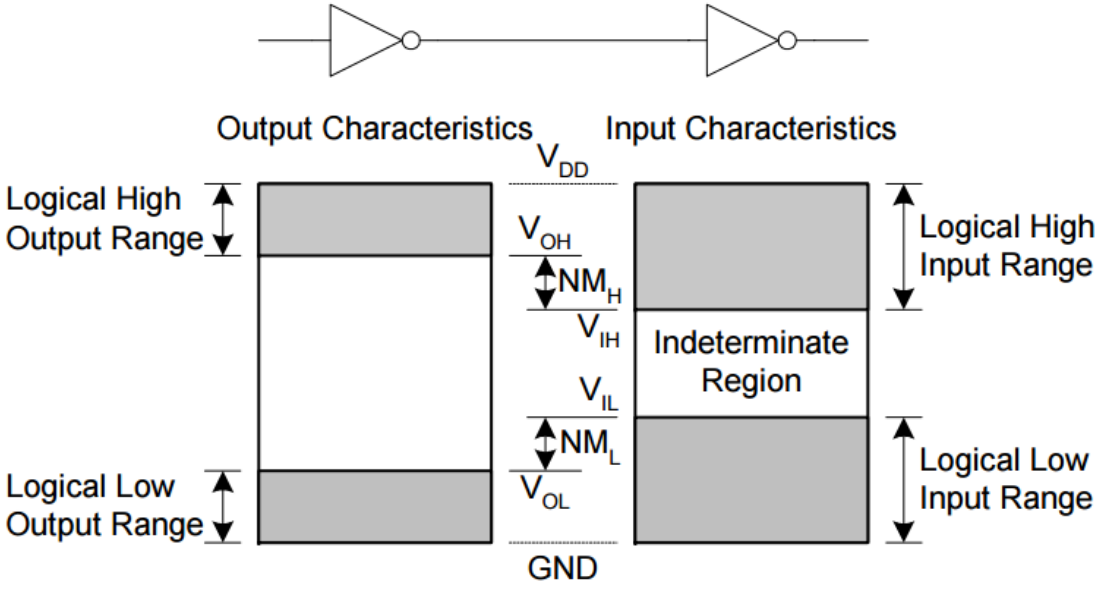
   V_{OL} : L level output voltage ≤ 0.4 V

   V_{IL} : L level recognized input voltage ≤0.8 V

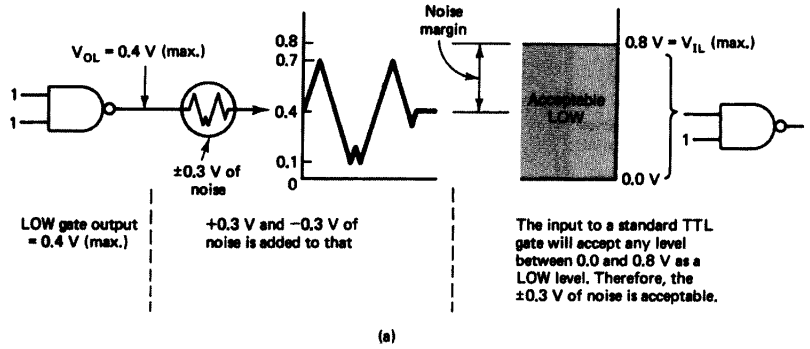
   V_{OH} : H level output voltage ≥ 2.4 V

   V_{IH} : H level recognized input voltage ≥2.0 V

Noise margin



TTL voltage level



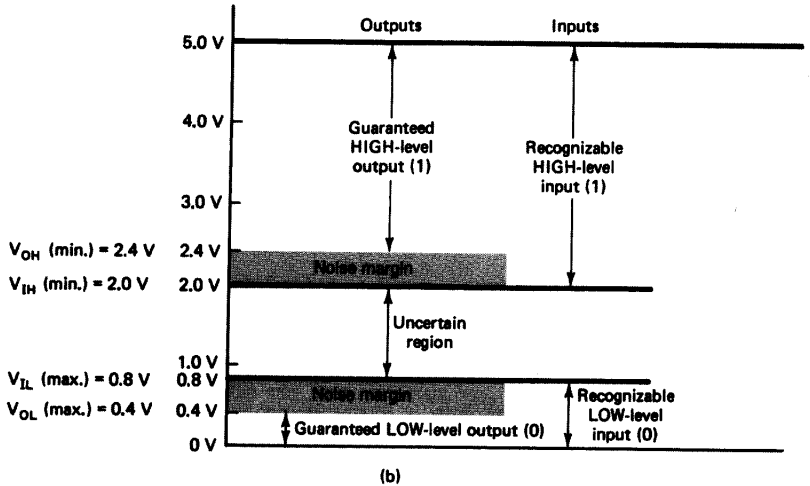


Figure 2–60 (a) Adding noise to a LOW-level output; (b) graphical illustration of the input/output voltage levels for the standard 74XX TTL series.

TTL & CMOS voltage level

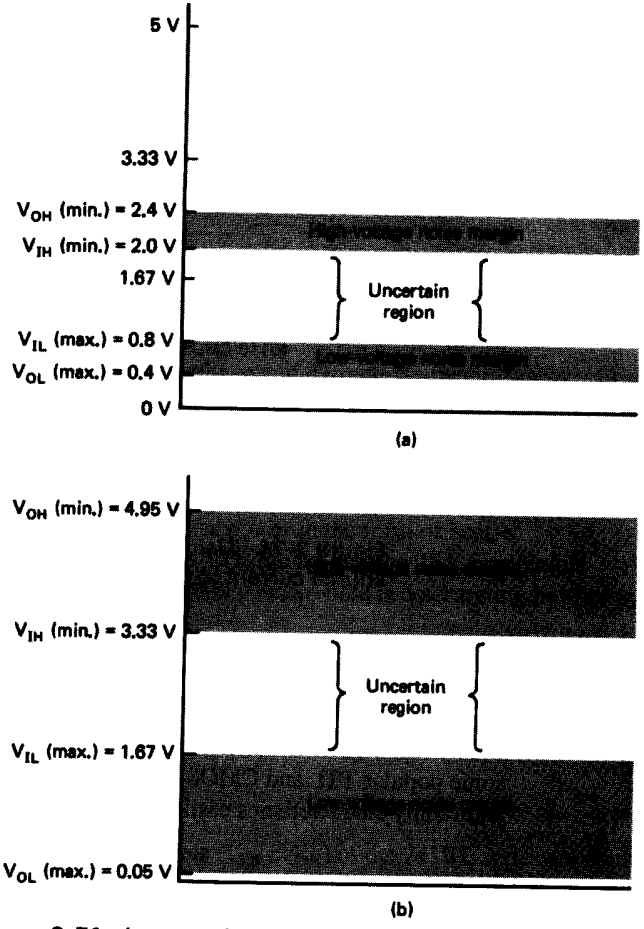


Figure 2–71 Input and output voltage specifications: (a) 7400 series TTL; (b) 4000B series CMOS (5-V supply).

TTL Input Output Current

1. Output current: Source or sink current from TTL output gate in High or Low-level Output

   $I_{OH} \leq$ 0.4 mA (source)

   $I_{OL} \leq$16 mA (sink)

2. Input Current: Source or sink current from TTL output gate in High or Low-level Output

   $I_{IH} \leq$ 0.04 mA, (sink)

   $I_{IL} \leq$1.6 mA (source)

TTL Input Output Current

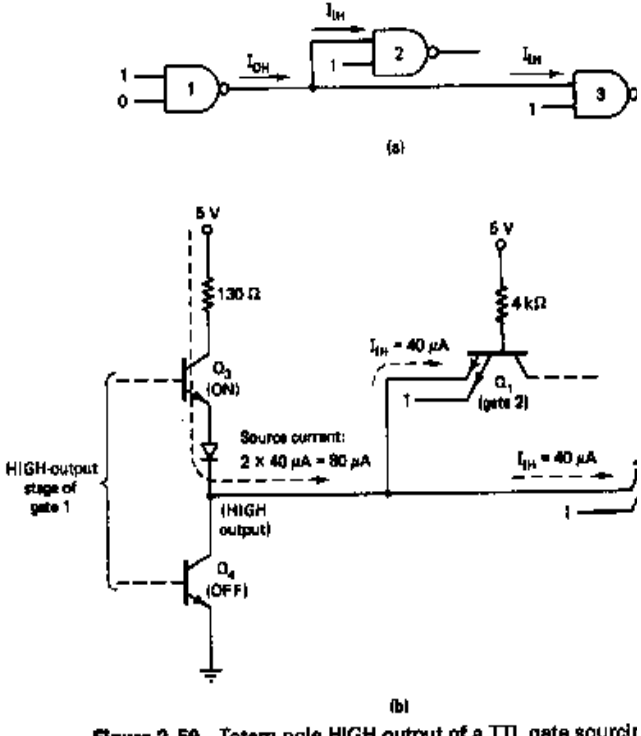
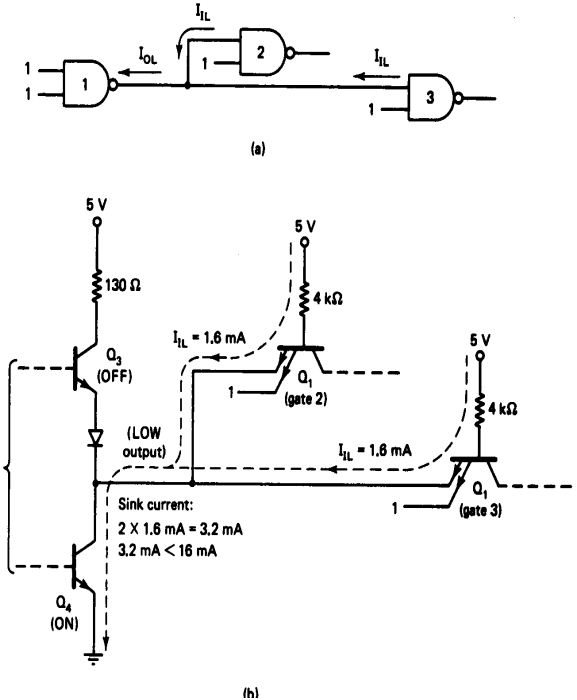
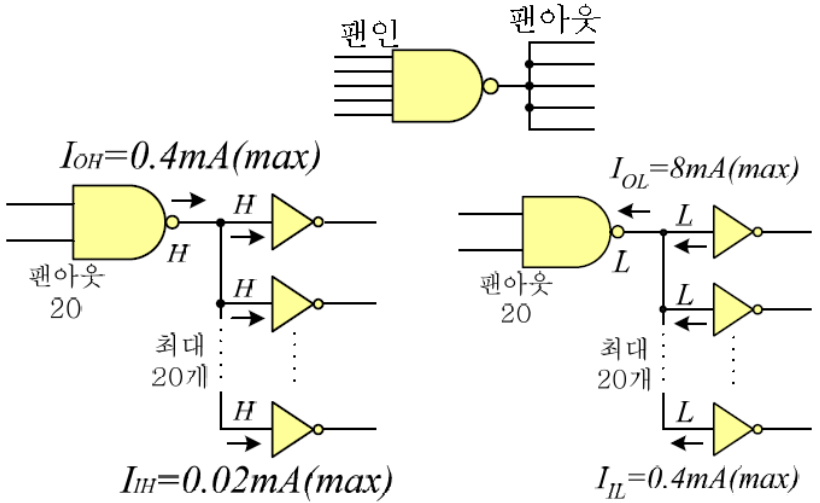


Figure 2–59 Totem pole HIGH output of a TTL gate sourcing current to two gate inputs.



Fan-in, Fan-out

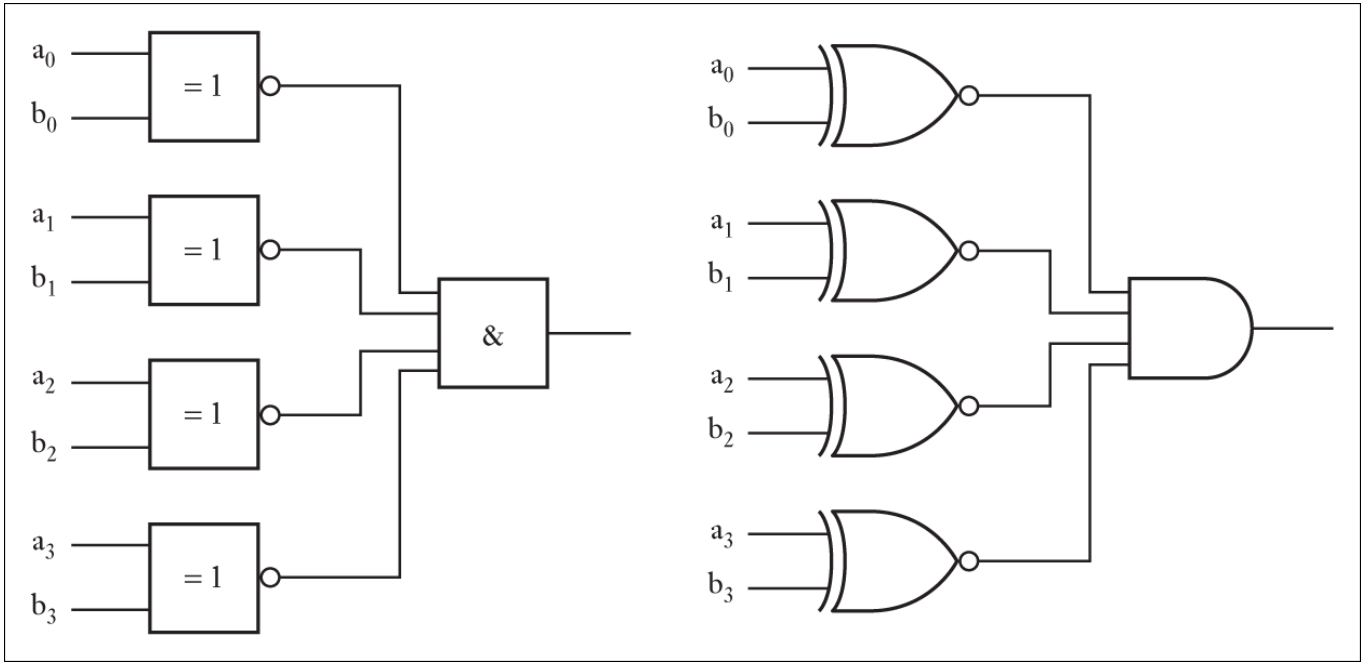
- Fan-out: 1 개의 게이트에서 다른 게이트의 입력으로 연결 가능한 최대 출력 게이트 수
- Fan-in : 1 개의 게이트에 입력으로 접속할 수 있는 게이트 수



Fan-out

$$\frac{I_{OH}(\max)}{I_{IH}(\max)} = \frac{0.4mA}{0.02mA} = 20$$

4 bits comparator



XOR operation
If A=B output=0

Logic gate: Flip flop

- S–R Flip–Flop
  - Used for latch or memory

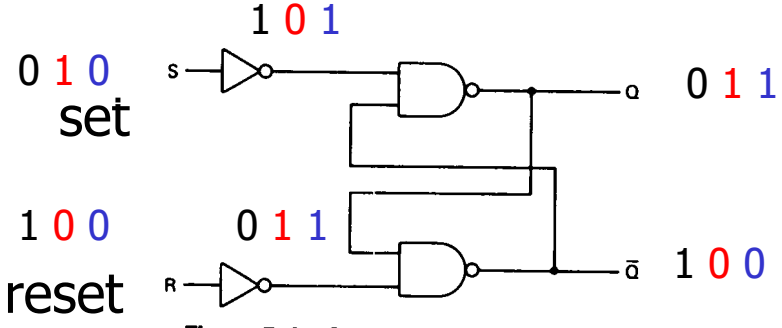


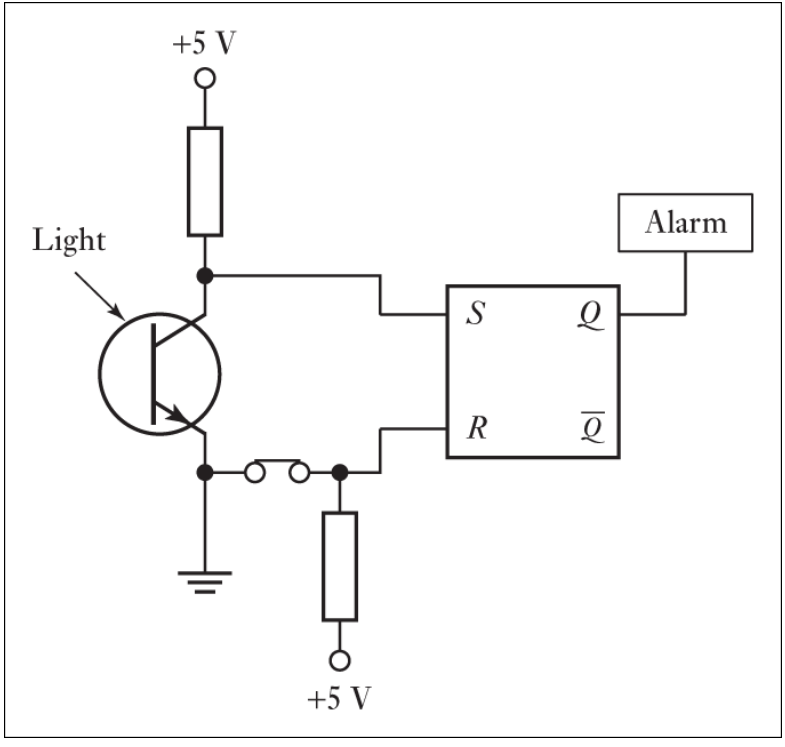
Figure 5–2 Cross-NAND *S-R* flip-flop.

TABLE 5–2
Function Table for Figure 5–2

S	*R*	*Q*	$\overline{Q}$	*Comments*
0	0	*Q*	$\overline{Q}$	Hold condition
1	0	1	0	Flip-flop Set
0	1	0	1	Flip-flop Reset
1	1	1	1	Not used

Eg. SN74L71
74HC74

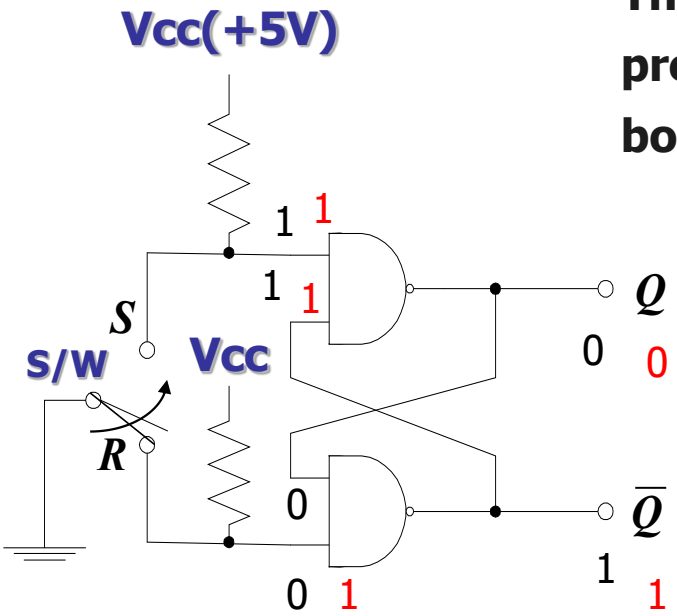
RS flip flop application: Alarm circuit



(Flip-Flop:FF)

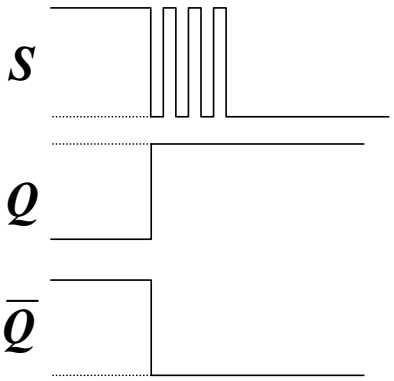
Application of RS FF

- Chattering Free Circuit



After S/W is on

The output signal keeps previous level even under the bounding of switch



D–Latch (7475)

- Latch input signal while enable signal is on

Function Table for a 7475[a]

	Inputs		Outputs	
Operating mode	*E*	*D*	*Q*	$\overline{Q}$
Data enabled	H	L	L	H
	H	H	H	L
Data latched	L	×	*q*	$\overline{q}$

[a] *q* = State of *Q* before the HIGH-to-LOW edge of *E*; × = don't care.

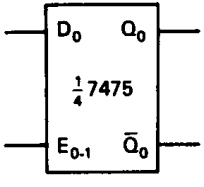
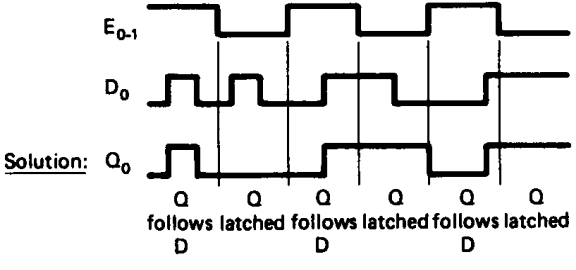
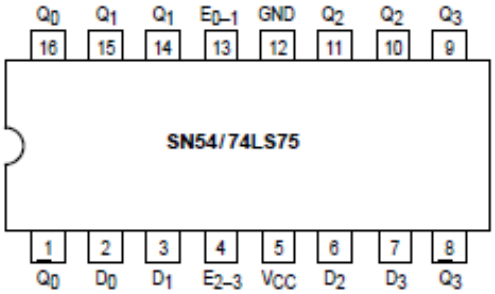


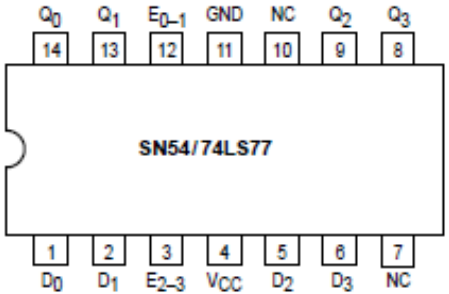
Figure 5–13



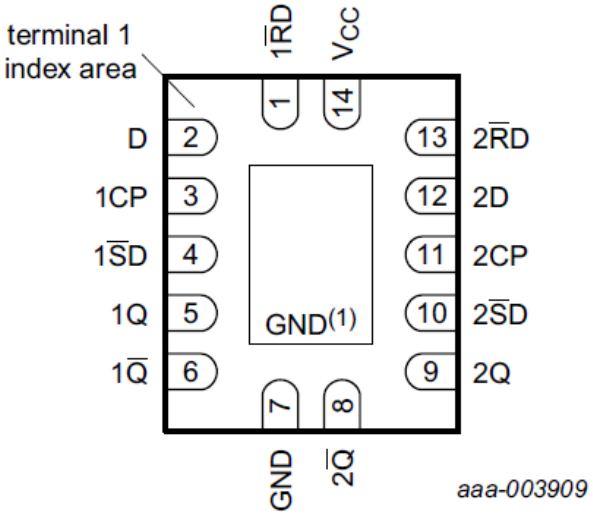
D-latch examples

CONNECTION DIAGRAMS DIP (TOP VIEW)





74HC74
74HCT74

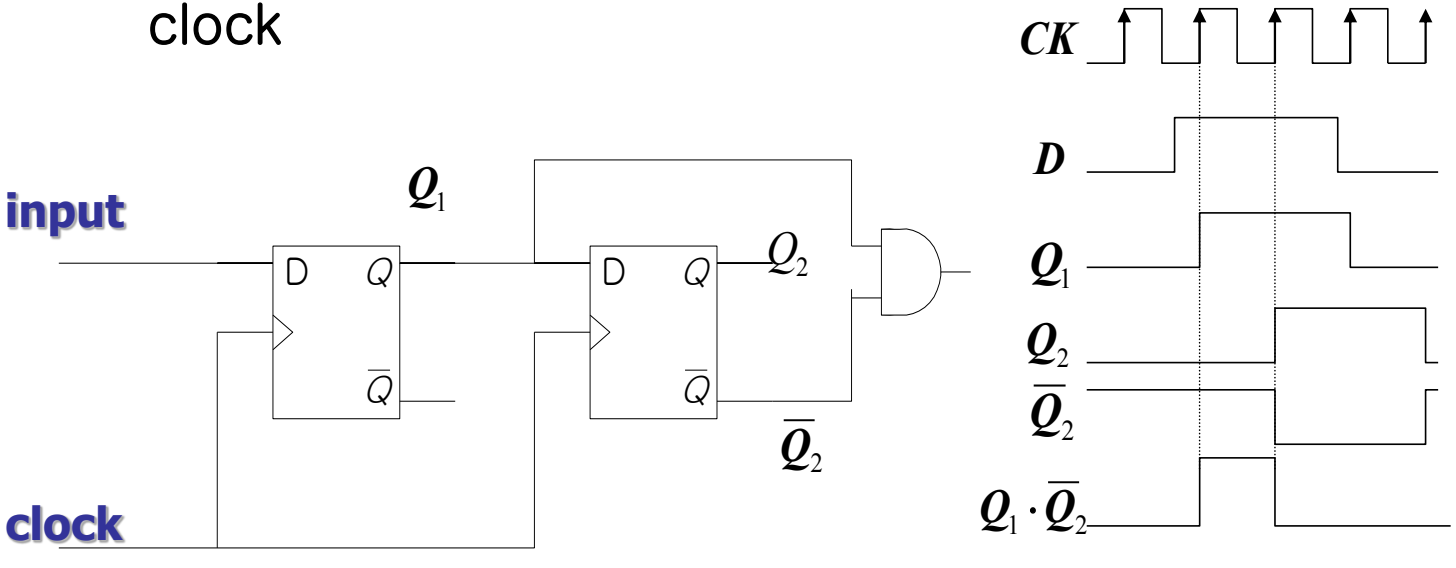


Transparent top view

Flip-Flop:FF

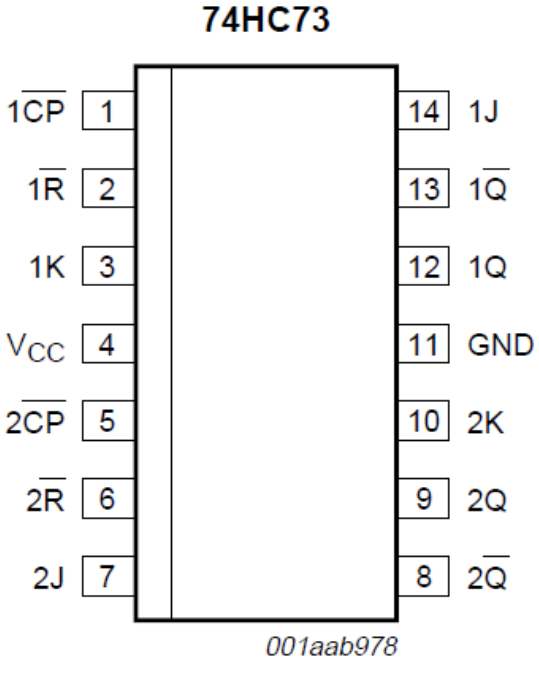
D flip flop Application

- Pulse edge detection by synchronized clock



J–K Flip–Flop

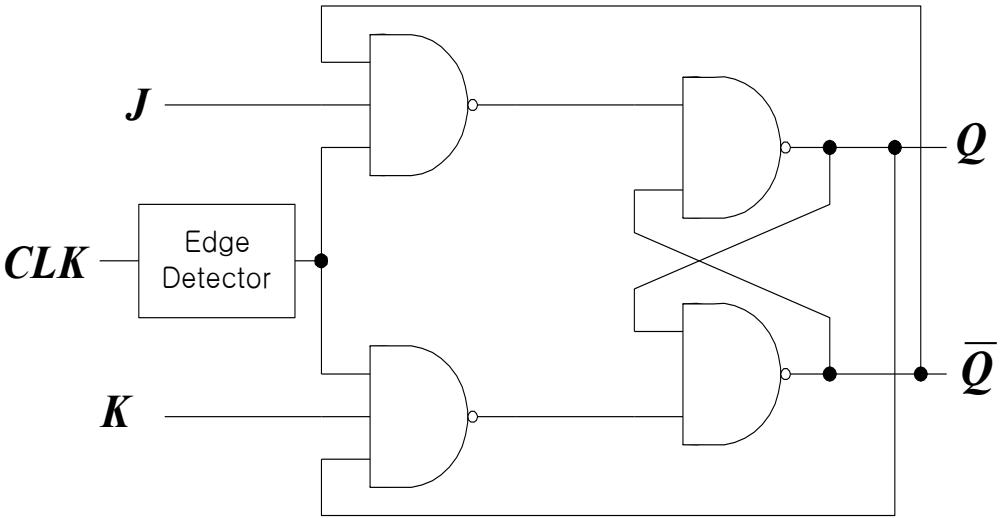
- Toggle the output at J=K=High signal
- Operating Modes
  - J=0, K=0 => Data Hold
  - J=1, K=0 => Set
  - J=0, K=1 =>Reset
  - J=1, K=1 =>Toggle
    (output switch to opposite state)



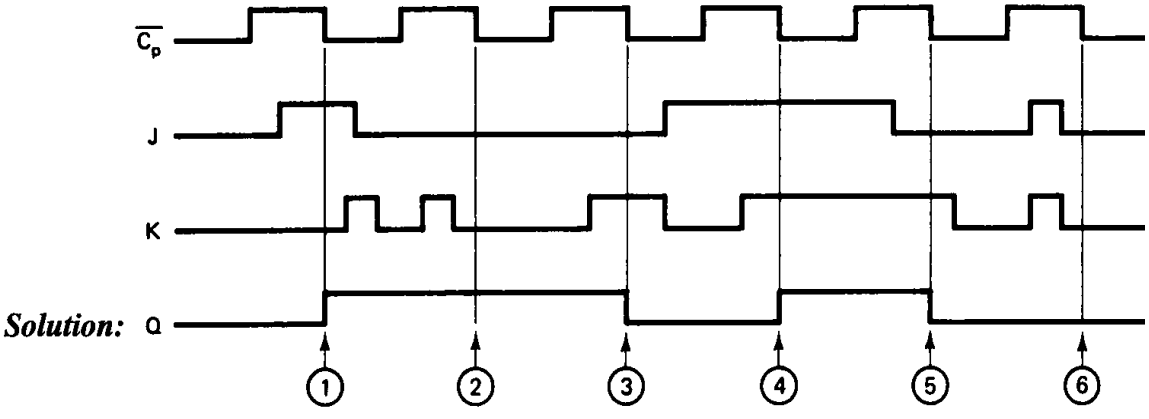
Flip-Flop:FF

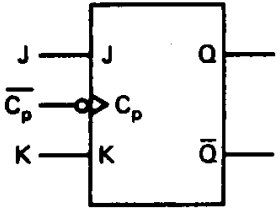
J-K FF (2)

- J-K structure



J–K Flip–Flop





Solution:

(1) J = 1, K = 0 at the negative clock edge; Q is Set

(2) J = 0, K = 0 at the negative clock edge; Q is held
(transitions in K before the edge are ignored)

(3) J = 0, K = 1 at the negative clock edge; Q is Reset

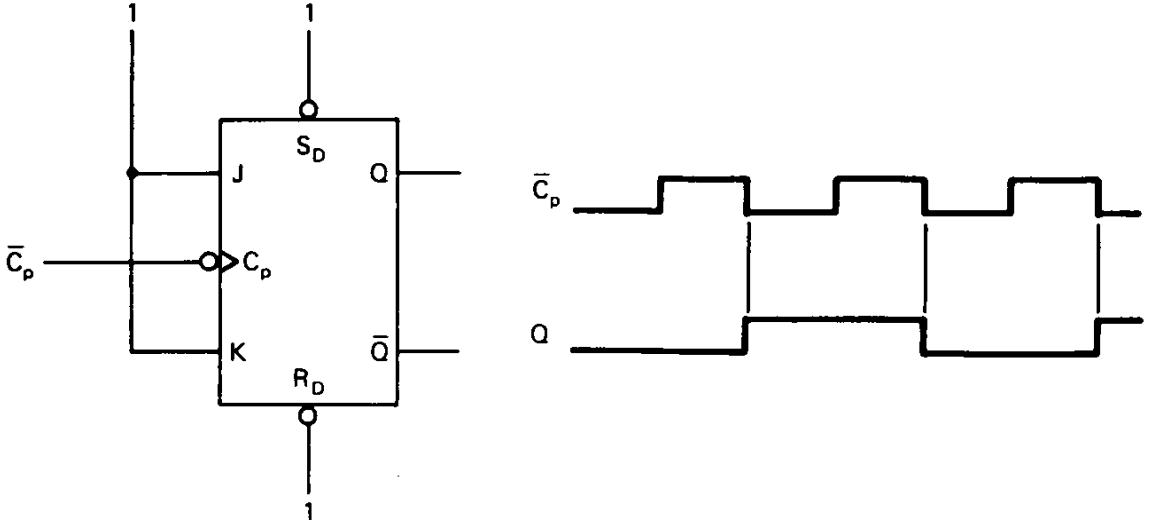
(4) J = 1, K = 1 at the negative clock edge; Q toggles

(5) J = 0, K = 1 at the negative clock edge; Q is Reset

(6) J = 0, K = 0 at the negative clock edge; Q is held

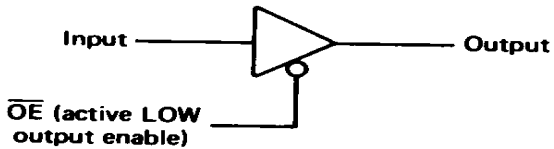
J–K Flip–Flop

- Toggle flip flop by J-K flip flop
- Used for a Frequency divider

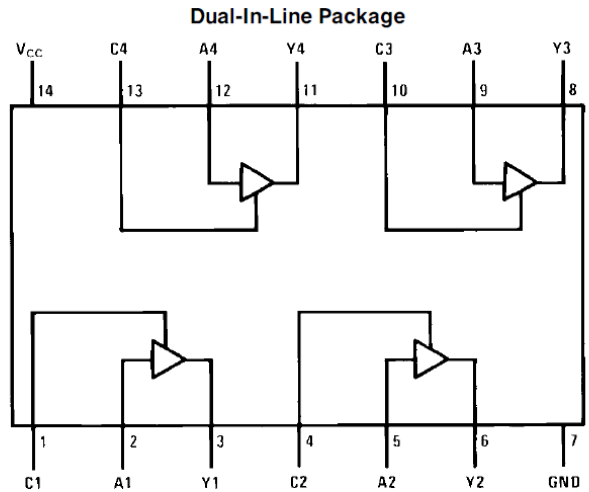


Three state buffers, Latches, and Transcivers

- Three state buffers: sharing same data lines
- Buffer: data isolation without changing logic level



Input	$\overline{OE}$	Output
1	0	1
0	0	0
1	1	Float
0	1	Float



TL/F/6388–1

Order Number DM74LS126AM or DM74LS126AN
See NS Package Number M14A or N14A

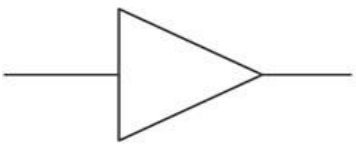
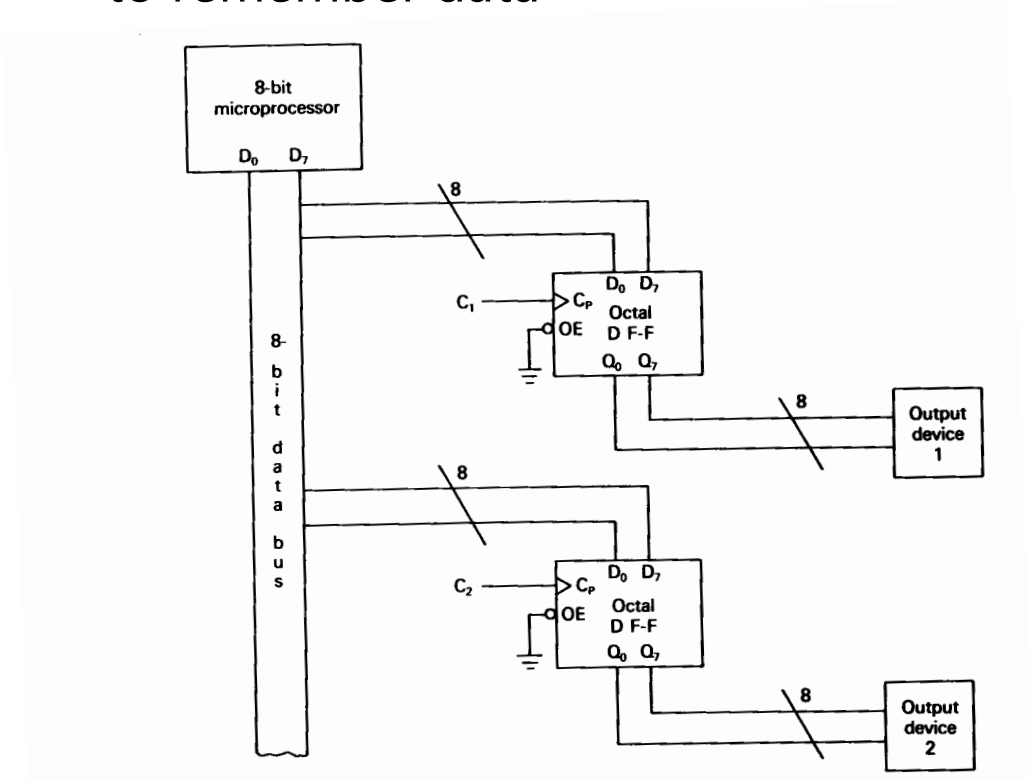


Figure 5.33 A two-state noninverting buffer.

Three state buffers, Latches, and Transcivers

- Octal Latches and flip flops: used in microprocessor to remember data

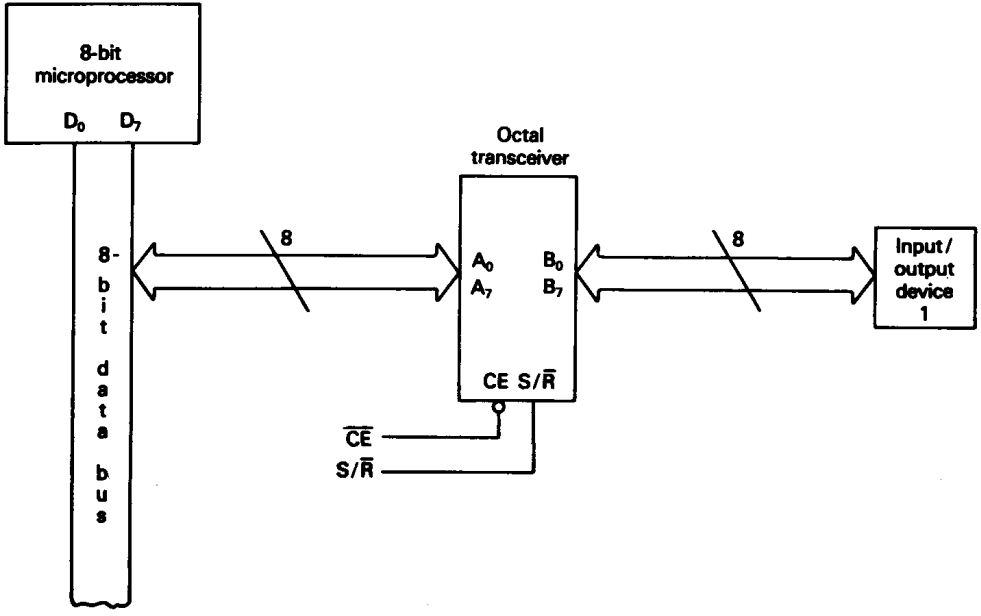


74LS374

(Octal data flip flops)

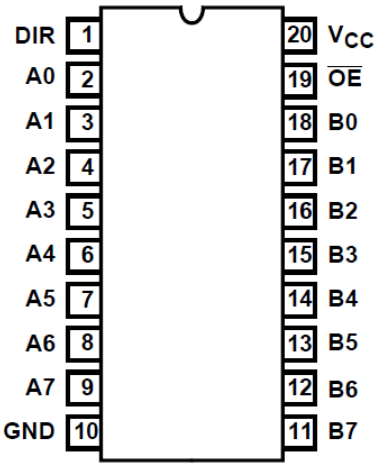
Three state buffers, Latches, and Transcivers

- Transcivers: transmitter and receiver, bidirectional

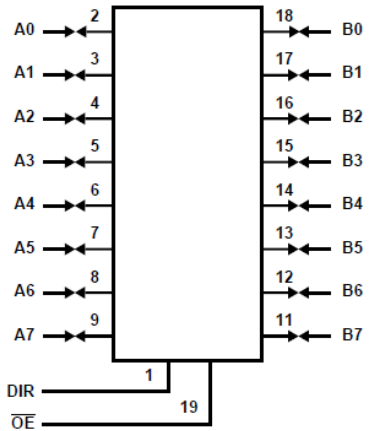


Octal–Bus Transceiver

CD54AC245, CD54ACT245
(CERDIP)
CD74AC245, CD74ACT245
(PDIP, SOIC, SSOP)
TOP VIEW



Functional Diagram



TRUTH TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = High Level, L = Low Level, X = Irrelevant

Decoders

- **Decoder**: Convert some code into some number or character

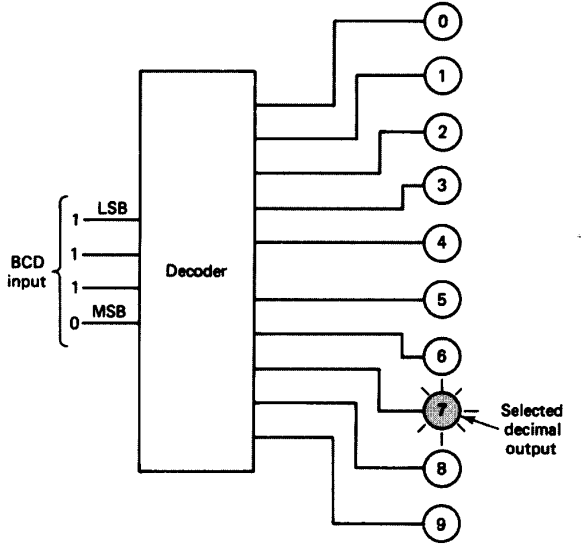


Figure 4–4 A BCD decoder selects the correct decimal indicating lamp based on the BCD input.

Decoders

- Output of an Octal Decoder

Truth Tables for an Octal Decoder

(a) Active-HIGH outputs

Input			Output							
2^2	2^1	2^0	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

(b) Active-LOW outputs

Input			Output							
2^2	2^1	2^0	0	1	2	3	4	5	6	7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Decoders

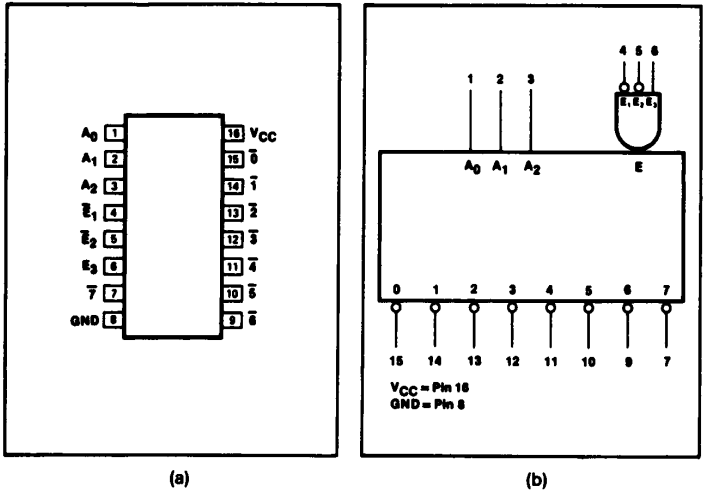
- Decoder ICs

  74138: 1 0f 8 octal decoder

  7442 : 1 0f 10 BCD decoder

  74154: 1 of 16 hex decoder

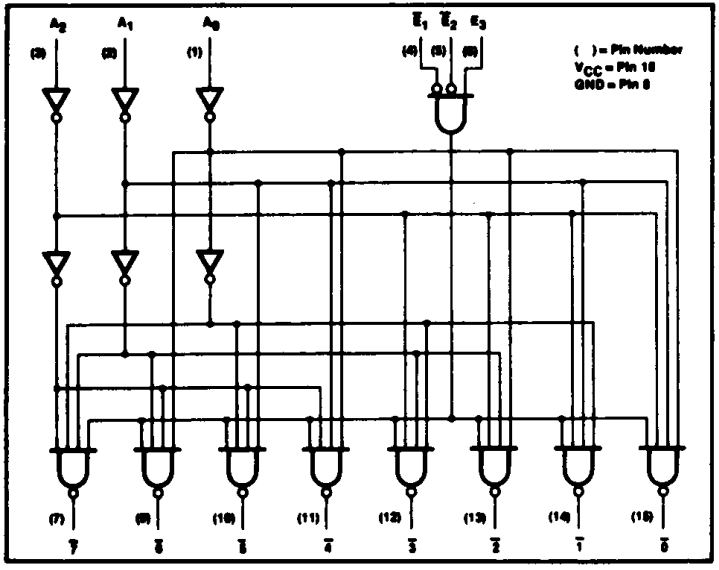
  7447 : BCD to seven segment decoder



74138 decoder: 3 bits decoding

Decoders

Control bits



(c)

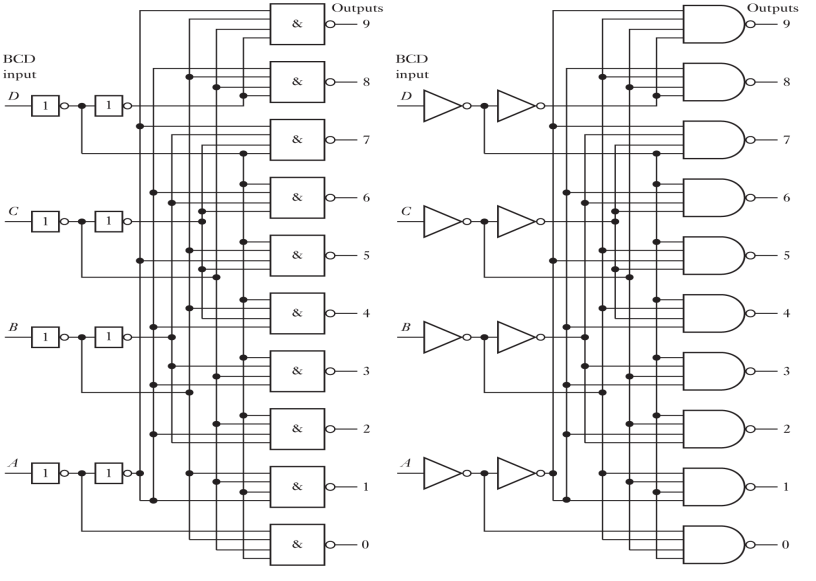
INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care

(d)

Function Table of 74138 decoder

BCD-to-decimal decoder



Inputs				Outputs									
A	*B*	*C*	*D*	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Encoders

- **Encoder:** generate a coded output from a numeric input

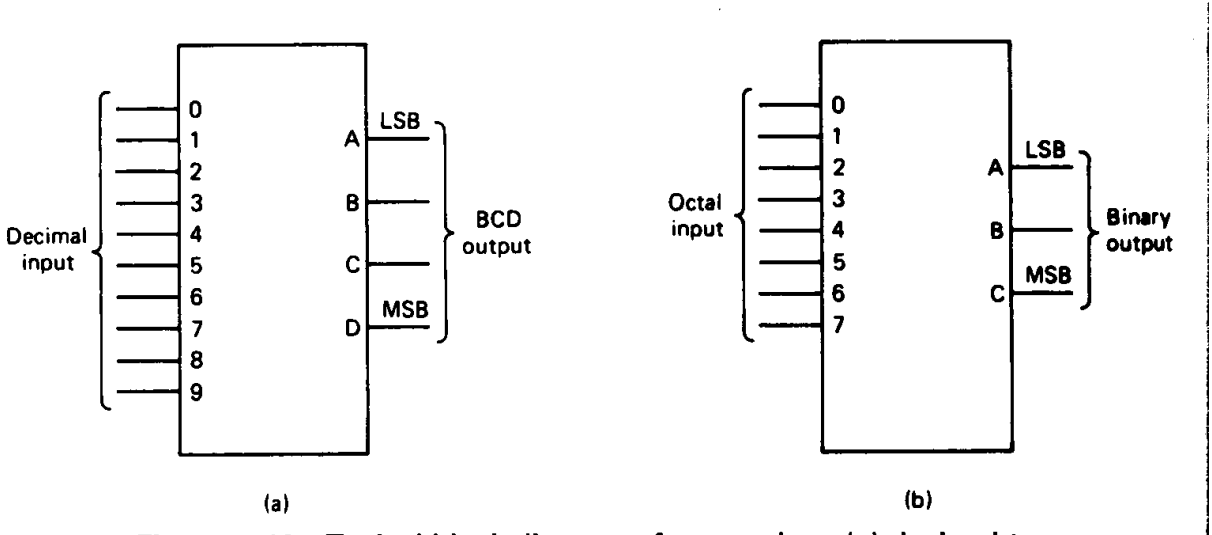
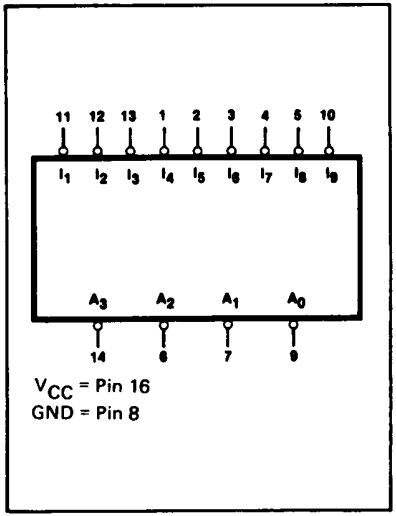


Figure 4–10 Typical block diagrams for encoders: (a) decimal-to-BCD encoder; (b) octal-to-binary encoder.

Encoders

- 74147 decimal-to-BCD encoder



(a)

INPUT									OUTPUT			
$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	$\bar{I}_8$	$\bar{I}_9$	$\bar{A}_3$	$\bar{A}_2$	$\bar{A}_1$	$\bar{A}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

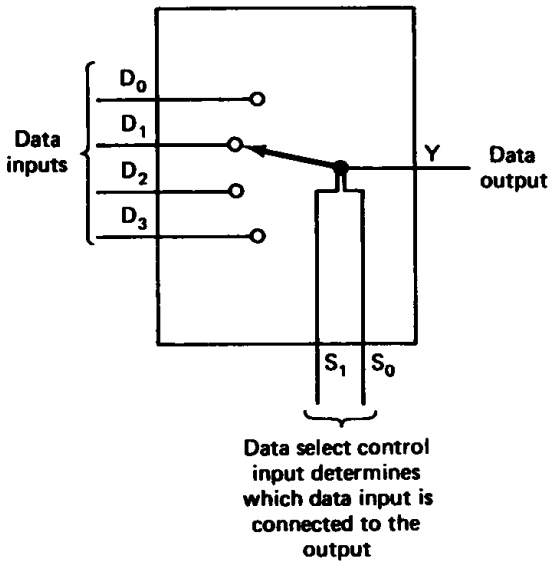
H = HIGH voltage level
L = LOW voltage level
X = Don't care

(b)

Figure 4–11 The 74147 decimal-to-BCD (10-line-to-4-line) encoder: (a) logic symbol; (b) function table.

Multiplex

- **Multiplex**: Funnel several data lines into a single line for transmission



S1=0, S0=0 => Do selected

S1=0, S0=1 => D1 selected

S1=1, S0=0 => D2 selected

S1=1, S0=1 => D3 selected

Multiplex

- E.g. 16-line multiplexer (74151) design: use 2 mutiplexers connected serially

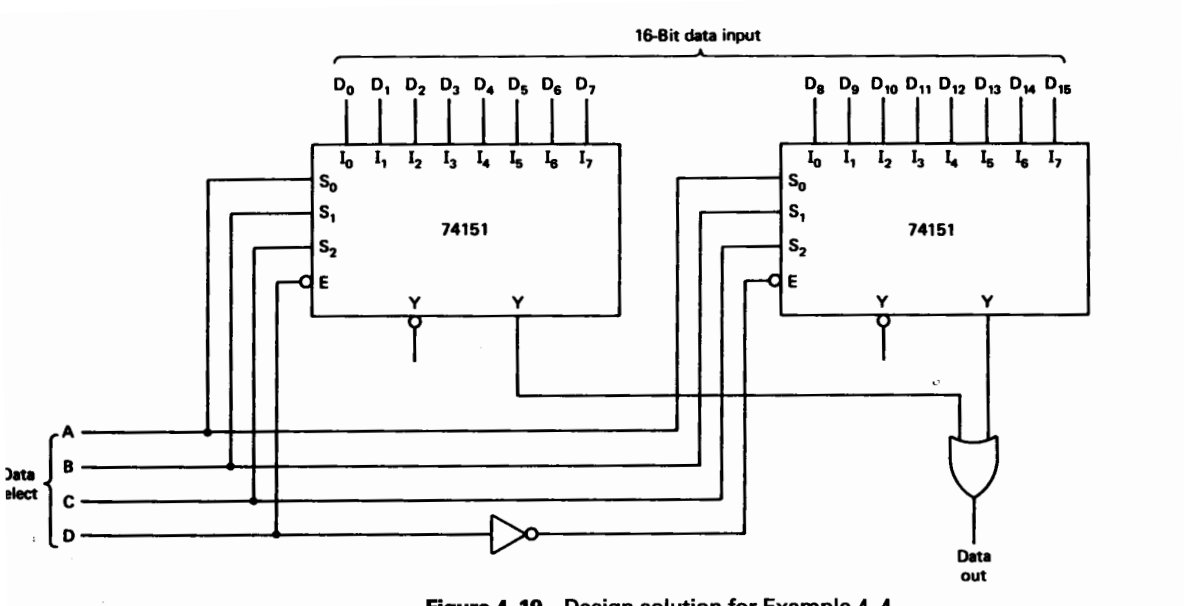


Figure 4–19 Design solution for Example 4–4.

Eg. ABCD

1111

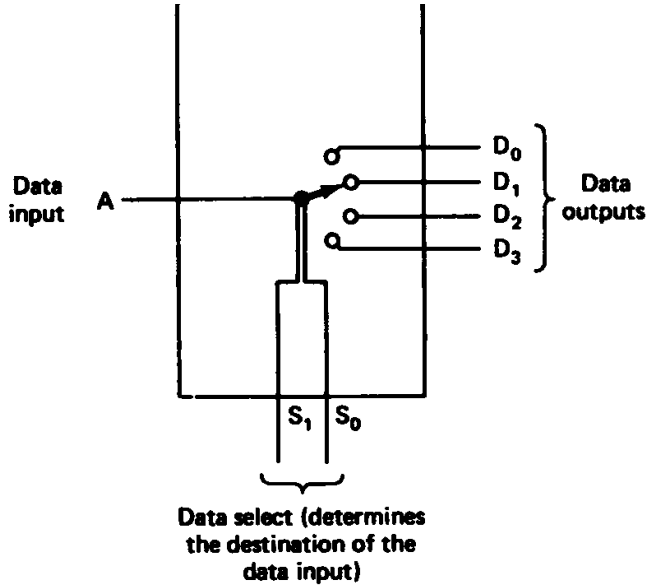
Low byte=disable

High byte=enable

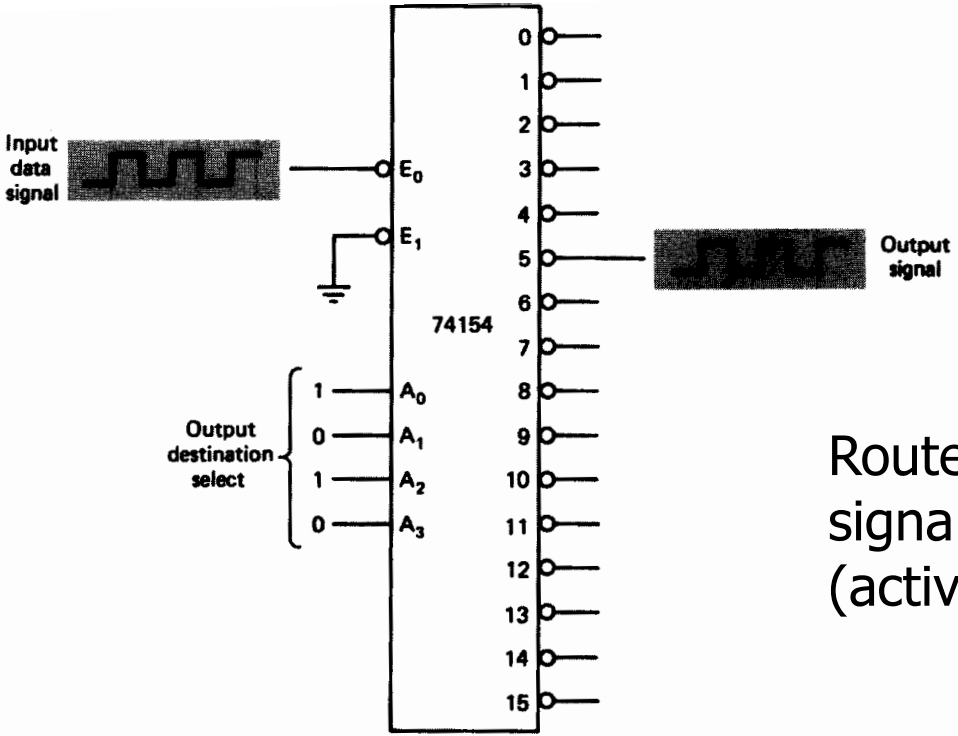
D15 selected

Demutiplexers

- **Demutiplexer**: data distributor, opposite of multiplexer



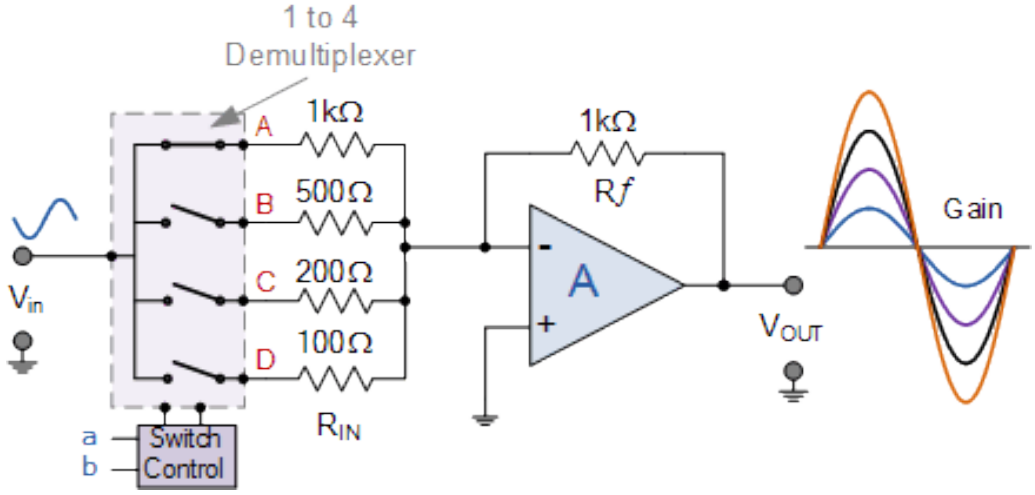
Demultiplexer



Route an input signal to 5 output (active low)

Demultiplexer 응용 회로

디지털 앰프 게인 조정

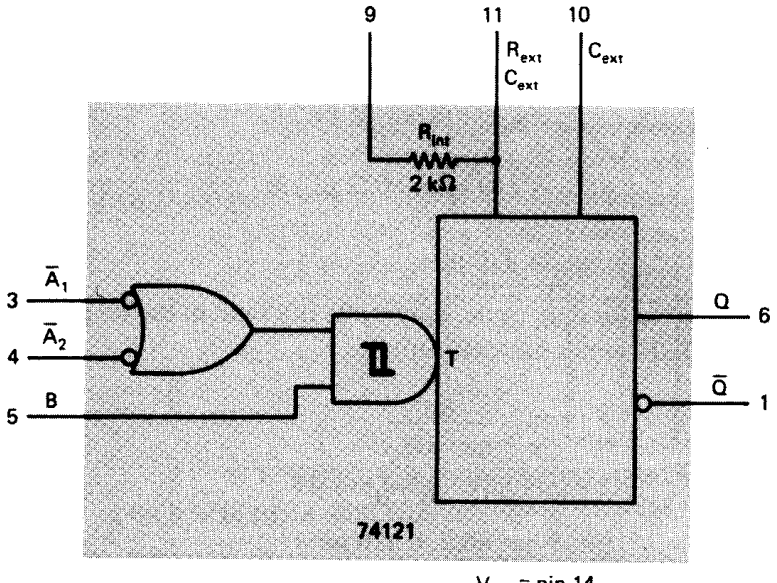


One-shot multivibrator

- To fulfill Electric circuit timing requirement
  - Bistable: triggered by external source and remains in state, eg. R-S flip flop
  - Astable: free running oscillator, e.g. duty cycle
  - Monostable: one shot pulse

One-shot multivibrator

- One-shot monostable Multivibrator



INPUTS			OUTPUTS	
$\bar{A}_1$	$\bar{A}_2$	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

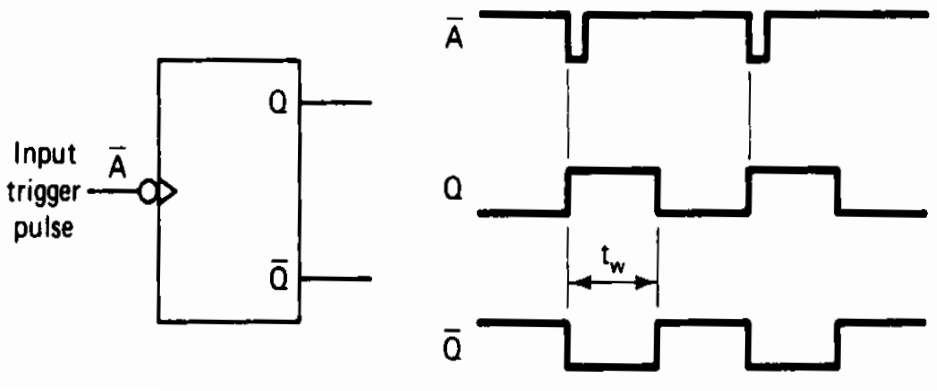
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

(b)

One-shot multivibrator

One-shot monostable Multivibrator

Input-output waveforms and those determination



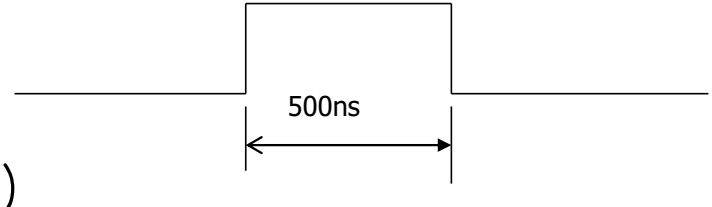
Pulse width: $t_w = R_{ext} * C_{ext} * \ln 2$

One-shot multivibrator

One-shot monostable Multivibrator

e.g. Generate pulse satisfying the conditions

- Circuit for generating output of 500ns



Sol.)

$t_w = R_{ext} * C_{ext} * \ln 2 = 500ns$

So $R_{ext} * C_{ext} = 0.722\ \mu s$

Pick $C_{ext} = 100\ pF$;

then

$R_{ext} = 0.722 / 0.0001\ \mu F = 7.22\ k\Omega$

Astable mode pulse generator

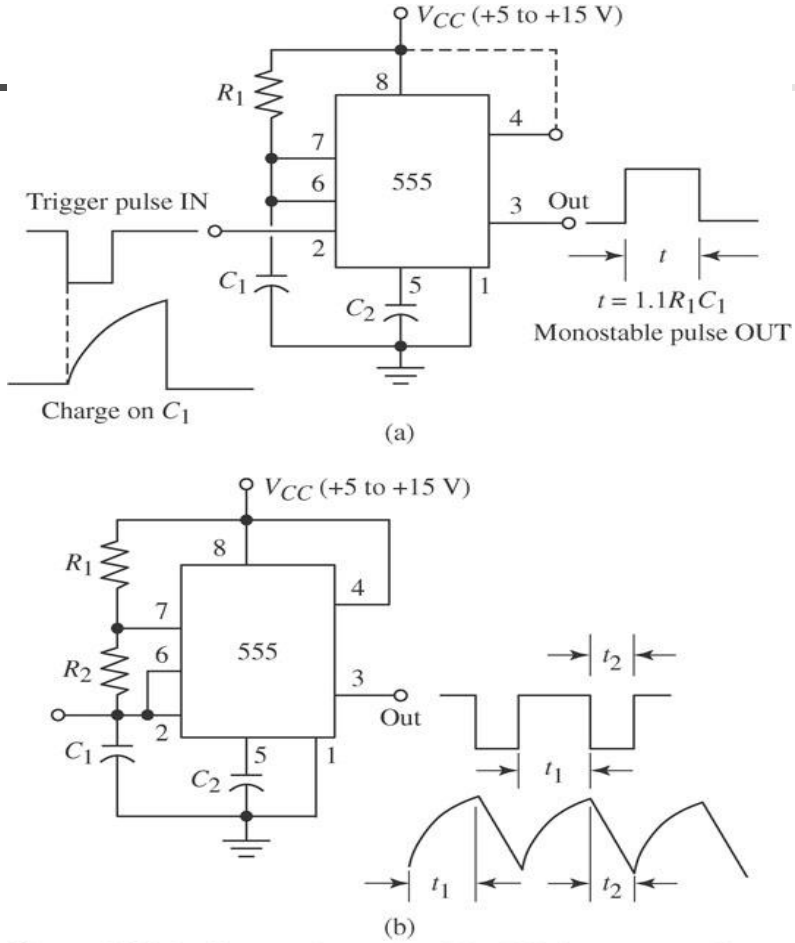


Figure 5.39 Basic operating modes of the 555 timer: monostable mode (a) and astable mode (b)

- Period

$$T = t_1 + t_2 = [0.693(R_1 + R_2)C_1] + [0.693R_2C_1] = 0.693(R_1 + 2R_2)C_1$$

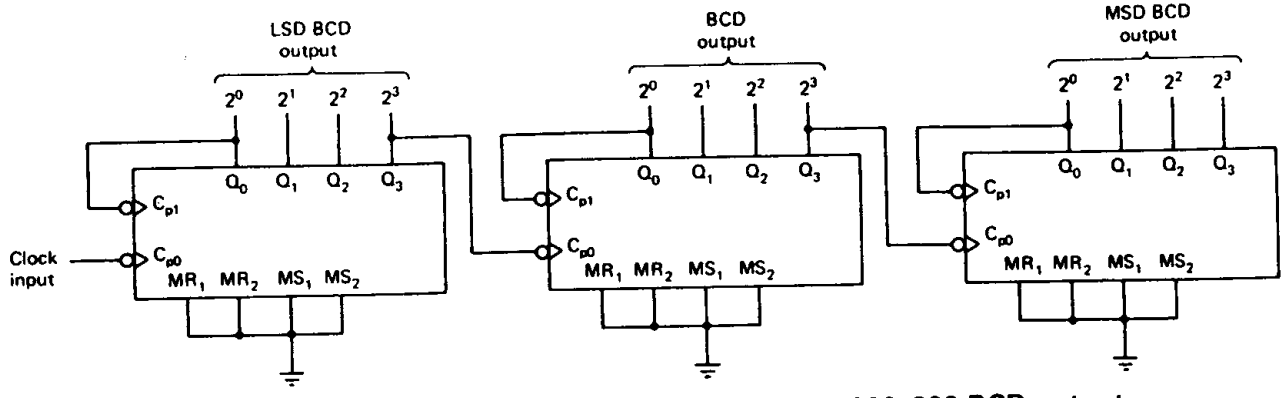
Duty cycle= $\frac{t_1}{T} = \frac{1 + R_2/R_1}{1 + 2R_2/R_1}$

Frequency $f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C_1}$

3 digits (BCD output) counter

Reset

Counting order:
0,1,2,3,4,5,6,7,8,9,0,1,2 ….

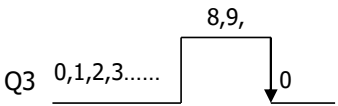


1st digit

10^{th} digit

100^{th} digit

At 1000->1001, reset, transit to next digit

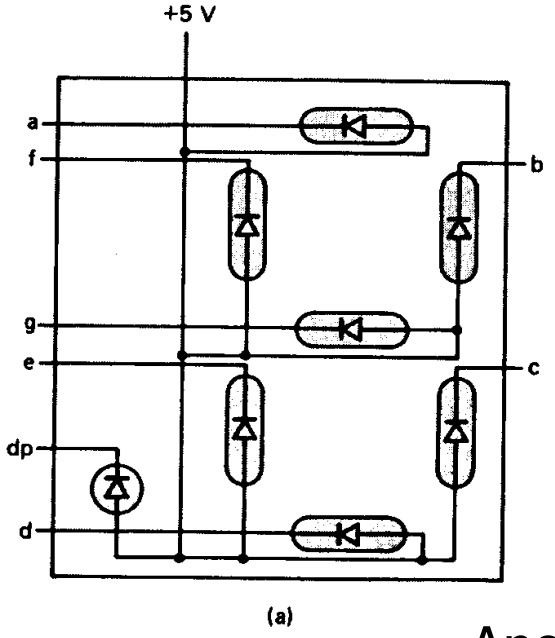


7490: decimal counters

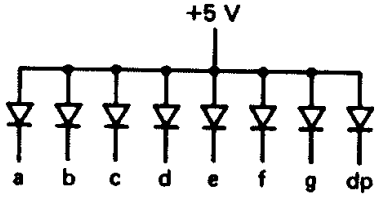
7 segment LED display

-seven separate LED in a single pack

-convert 4bit BCD code into 7-segment code



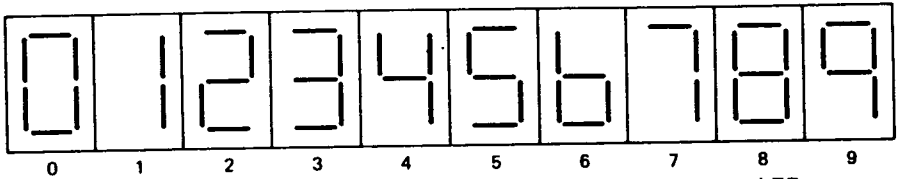
(a)



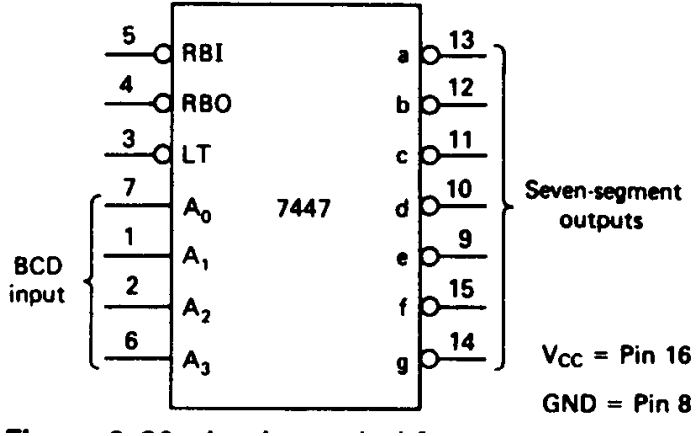
(b)

Anode common LED

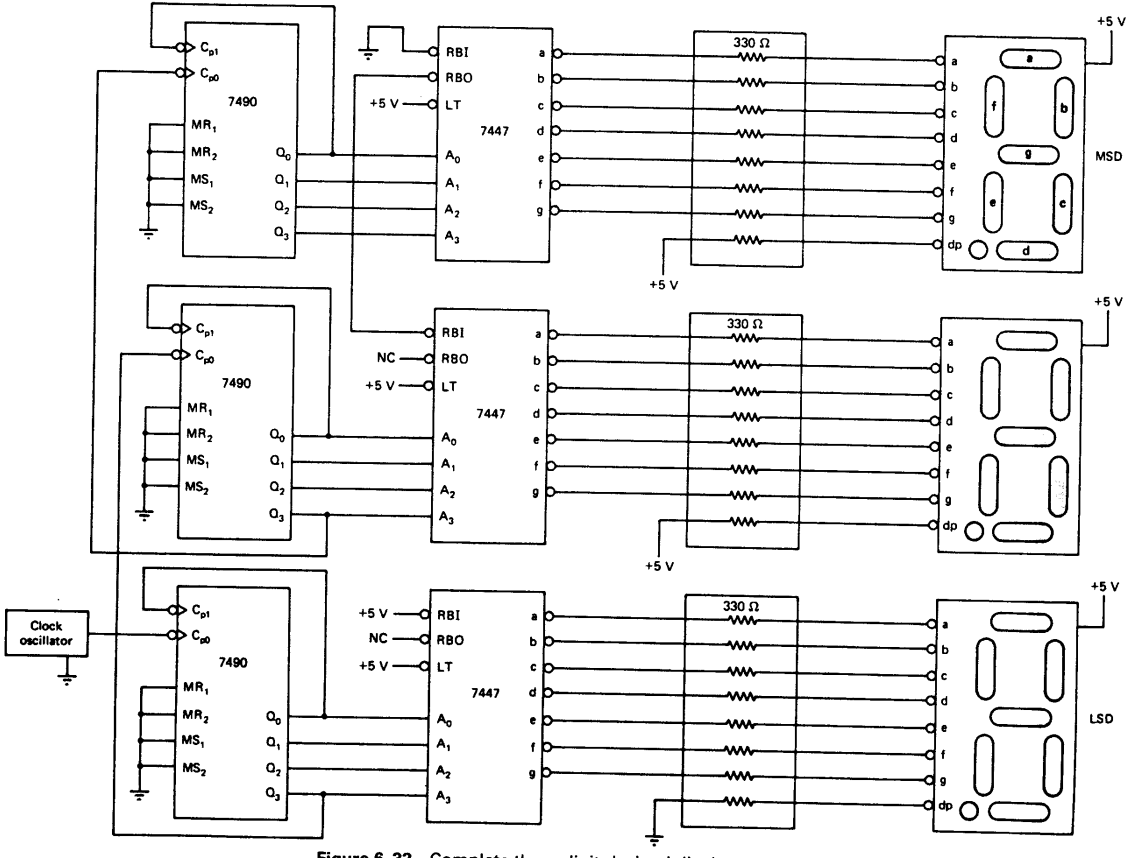
Numerical representation by LED



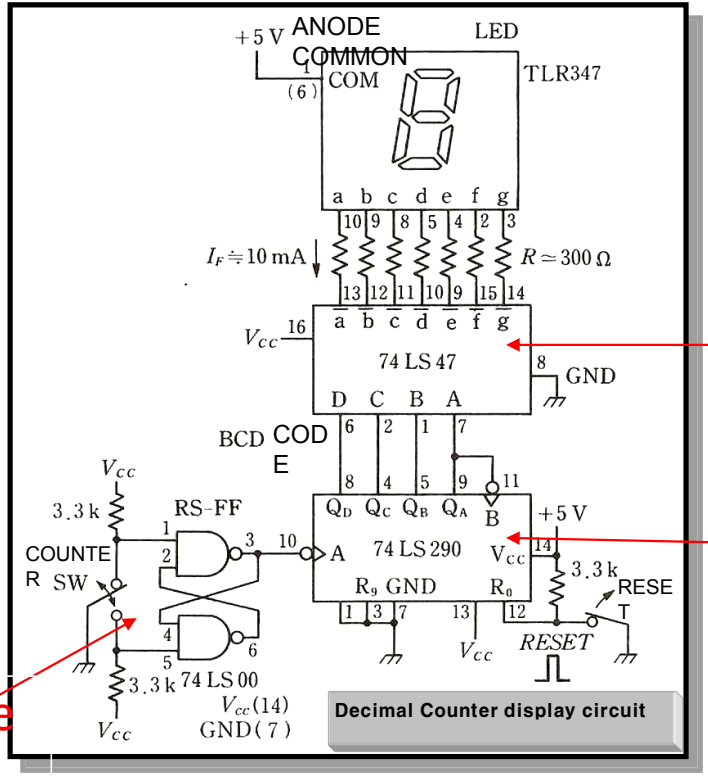
BCD to 7-segment decoder IC: 7447



3 digits decimal display



COUNTER / DECODER Application circuit



Decoder

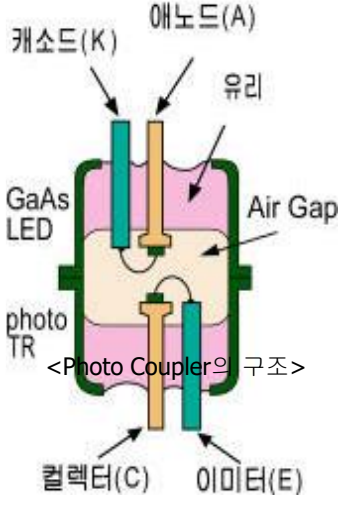
Decimal counter

Chattering free circuit

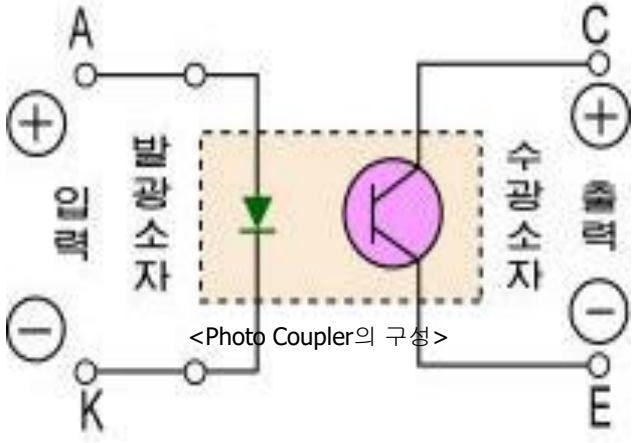
PHOTO COUPLER

: Photo Coupler입력 전기 신호와 출력 전기 신**호**를 "빛"으로써 전달하는 역할
: 일반적으로 발광소자와 수광 소자를 하나의 **Package** 에 결합하여 입출력 간을 전기적으로 절연시켜 광으로 신호를 전달하는 광결합 소자

Photo Coupler의 구조 및 구성



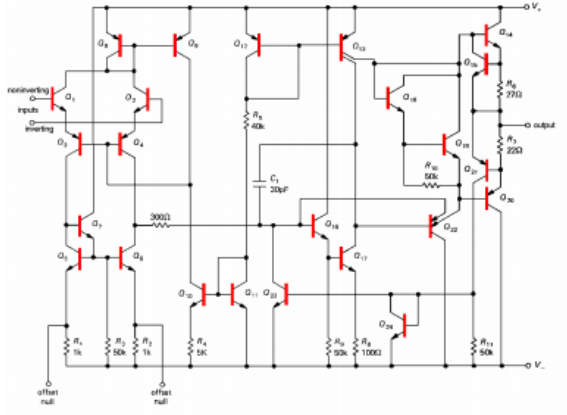
<Photo Coupler의 구조>

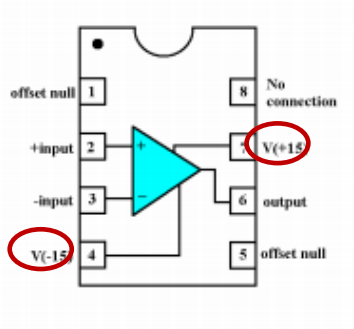


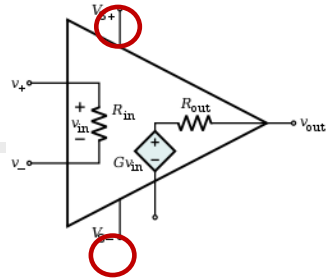
<Photo Coupler의 구성>

OP AMP (Operational Amplifier)

:연산 증폭기 또는 차동 증폭기로 불리며 두 단자의 전압을 뺄셈하여 증폭해주는 역할
즉, 작은 전압을 큰 전압으로 증폭해주는 용도로 사용







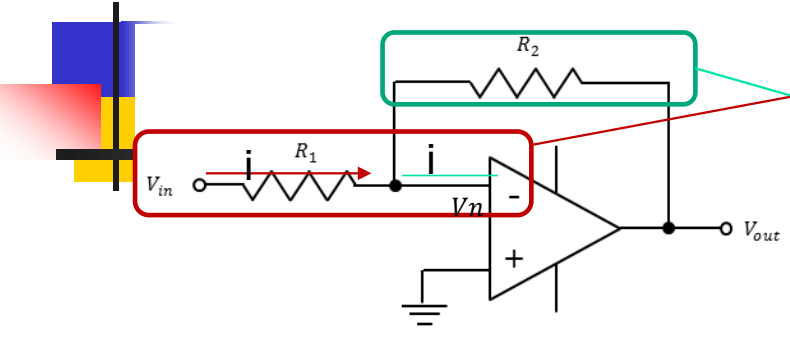
$V_{s\pm}$ = ±12V or ± 15V or ±20V

OP AMP의 전체 회로도
: 수 십개의 트렌지스터로 구성되어 있다.

OP AMP (Operational Amplifier)

Op Amp의 회로

1. 반전 증폭기(Inverting Amplifier)



$$V_{in} = iR_1 \quad (1)$$

$$V_{out} = -iR_2 \quad (2)$$

$$V_{out} = A(V_{in} - Vn) \quad (3) \qquad Vn = 0$$

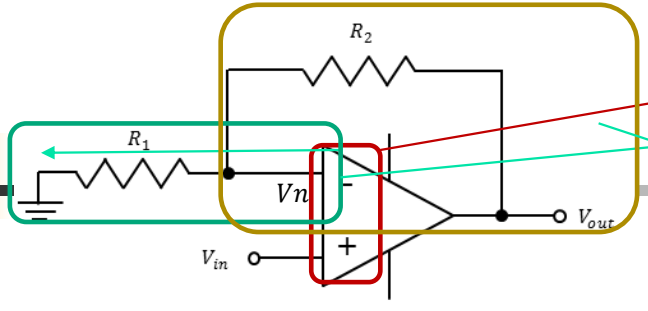
$$A = \frac{V_{out}}{V_{in}} = \frac{-iR_2}{iR_1} = -\frac{R_2}{R_1} \quad (4)$$

$$\therefore V_{out} = -\frac{R_2}{R_1} V_{in}$$

OP AMP (Operational Amplifier)

Op Amp의 회로

2. 비반전 증폭기(Non-Inverting Amplifier)



$$V_n = V_{in} \quad (1)$$

$$i = \frac{V_{in}}{R_1} \quad (2)$$

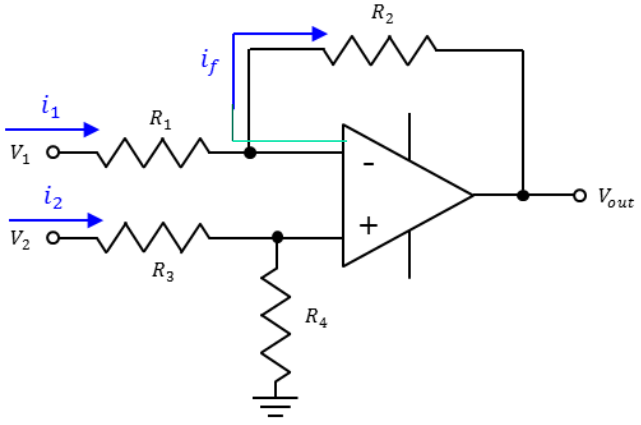
$$V_{out} - V_{in} = iR_2 \quad (3)$$

$$\therefore V_{out} = (1 + \frac{R_2}{R_1})V_{in} \quad (4)$$

OP AMP (Operational Amplifier)

Op Amp의 회로

3. 차동 증폭기(Differential Amplifier)



$$i_1 = \frac{V_1 - V_-}{R_1},\ i_2 = \frac{V_2 - V_+}{R_3},\ i_f = \frac{V_- - V_{out}}{R_2} \quad \text{(1)}$$

$$V_+ = V_2 \frac{R_4}{R_3 + R_4} \quad \text{(2)}$$

$$V_+ \cong V_- \quad \text{(3)}$$

$$I_1 = I_f = \frac{V_1 - V_-}{R_1} = \frac{V_- - V_{out}}{R_2} \quad \text{(4)}$$

$$V_{out} = -\frac{R_2}{R_1} V_1 + \frac{R_4}{R_3 + R_4} \frac{R_1 + R_2}{R_1} V_2 \quad \text{(5)}$$

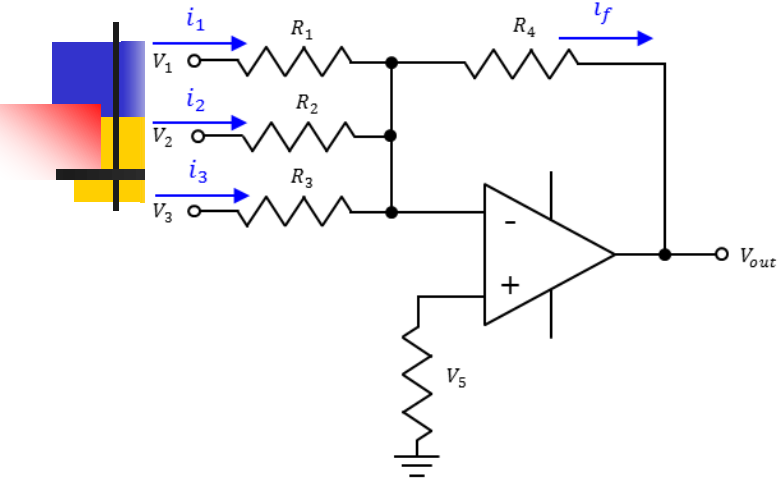
If $R_1 = R_3$, $R_2 = R_4$

$$V_{out} = \frac{R_2}{R_1}(V_2 - V_1) \quad \text{(5)}$$

OP AMP (Operational Amplifier)

Op Amp의 회로

4. 반전 가산기(Inverting Summing Amplifier)



$$i_f = i_1 + i_2 + i_3 = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \quad (1)$$

$$V_{out} = i_f R_4 = -\left(\frac{R_4}{R_1}V_1 + \frac{R_4}{R_2}V_2 + \frac{R_4}{R_3}V_3\right) \quad (2)$$

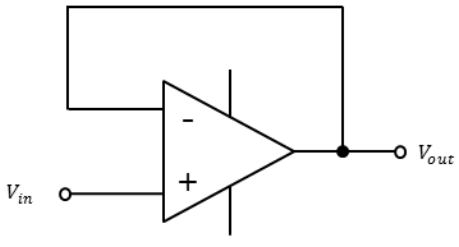
If $R_1 = R_2 = R_3 = R_4$

$$V_{out} = -(V_1 + V_2 + V_3) \quad (3)$$

OP AMP (Operational Amplifier)

Op Amp의 회로

5. 전압 팔로워(Voltage Follower) or 버퍼(buffer)



$$V_{in} = V_n = V_p \quad (1)$$

$$V_{in} = V_{out} \quad (2)$$

왜 Voltage Follower를 사용하는가?

1. 입력단과 출력단의 분리
2. 출력단이 새로운 전압원이 되기 때문에 노이즈로 부터 분리
3. 신호의 전류가 약할 때, 버퍼를 통해 강한 전류를 생성