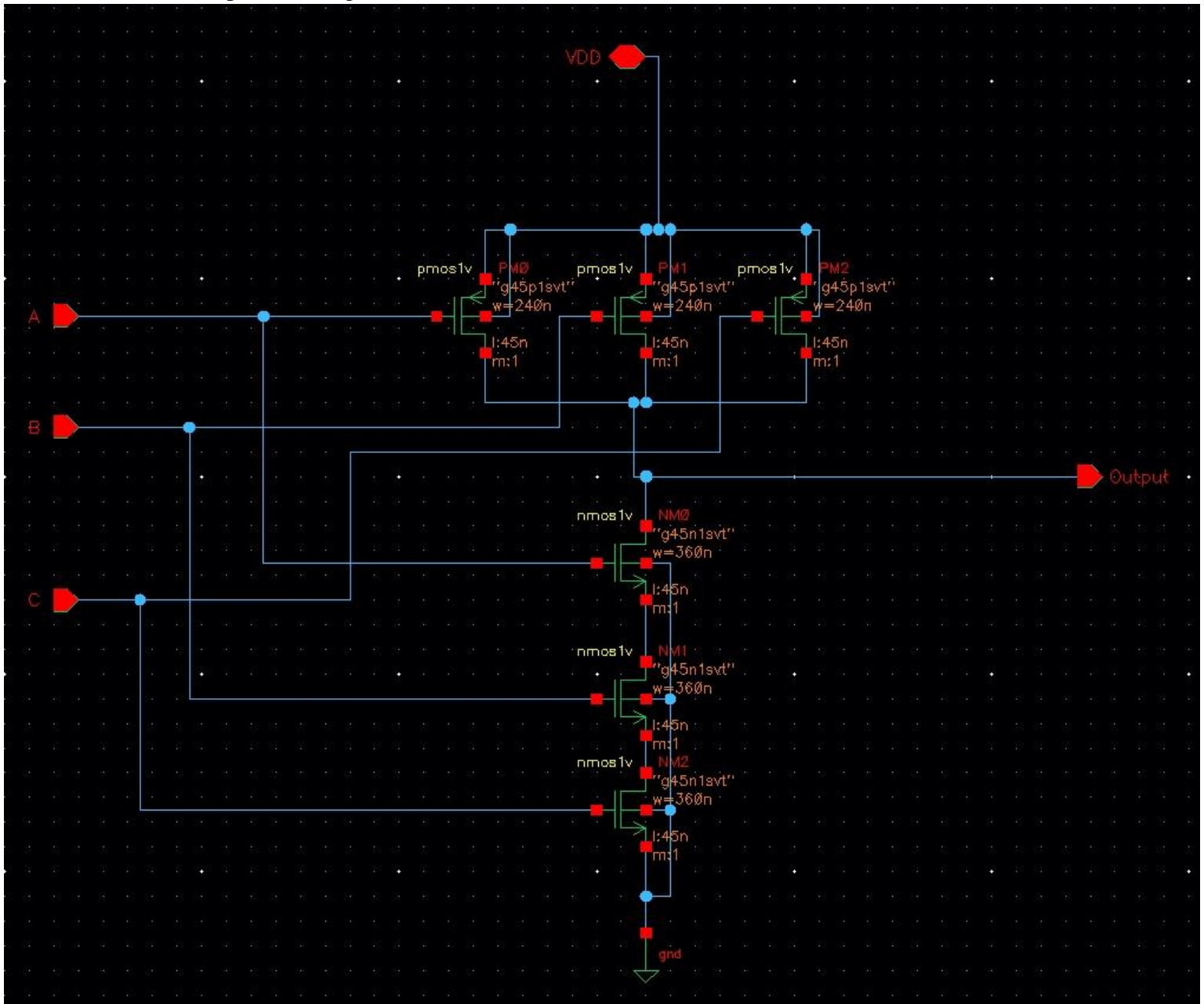


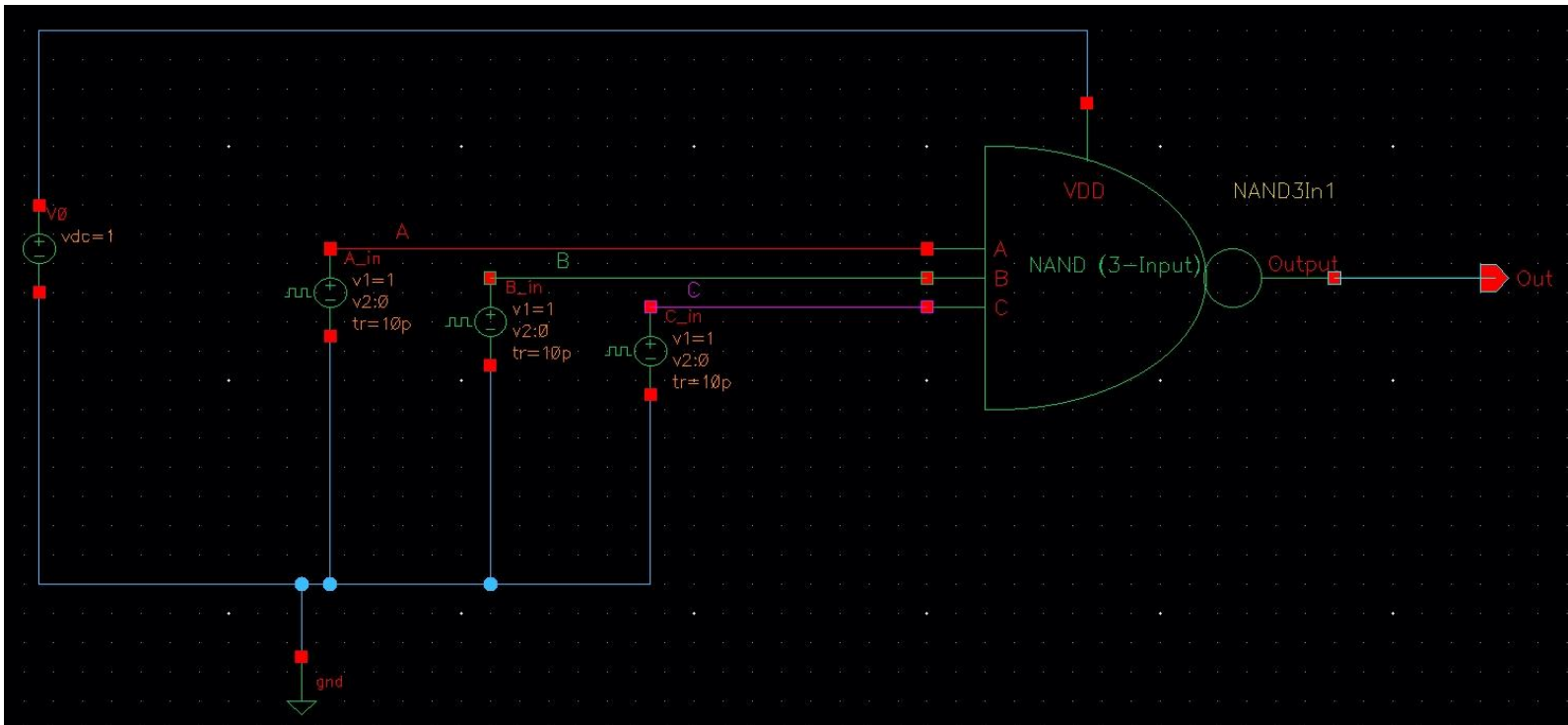
Cadence Project

Schematics for Simple Combinational Logic Functions

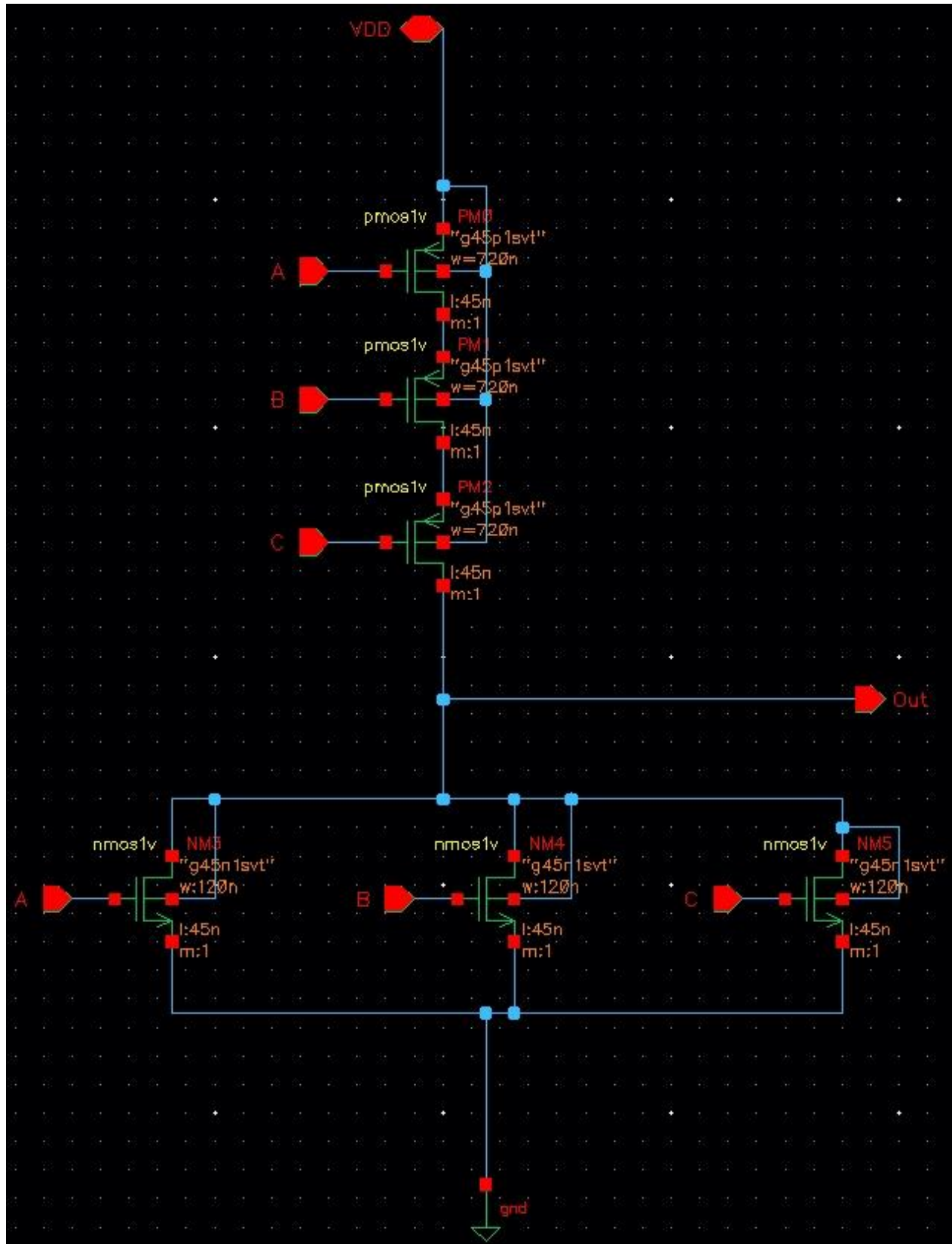
Step-1: For each of the following, create schematics and simulate to verify operation.

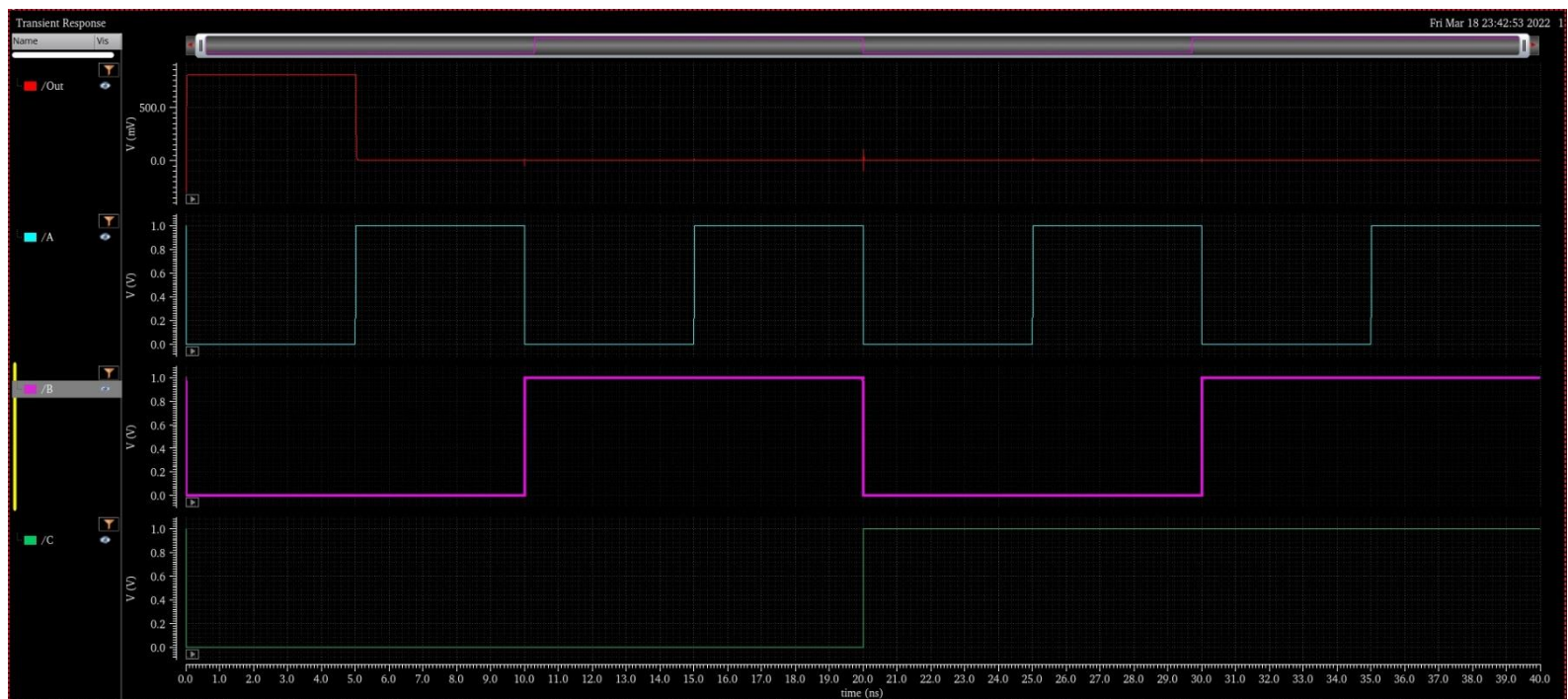
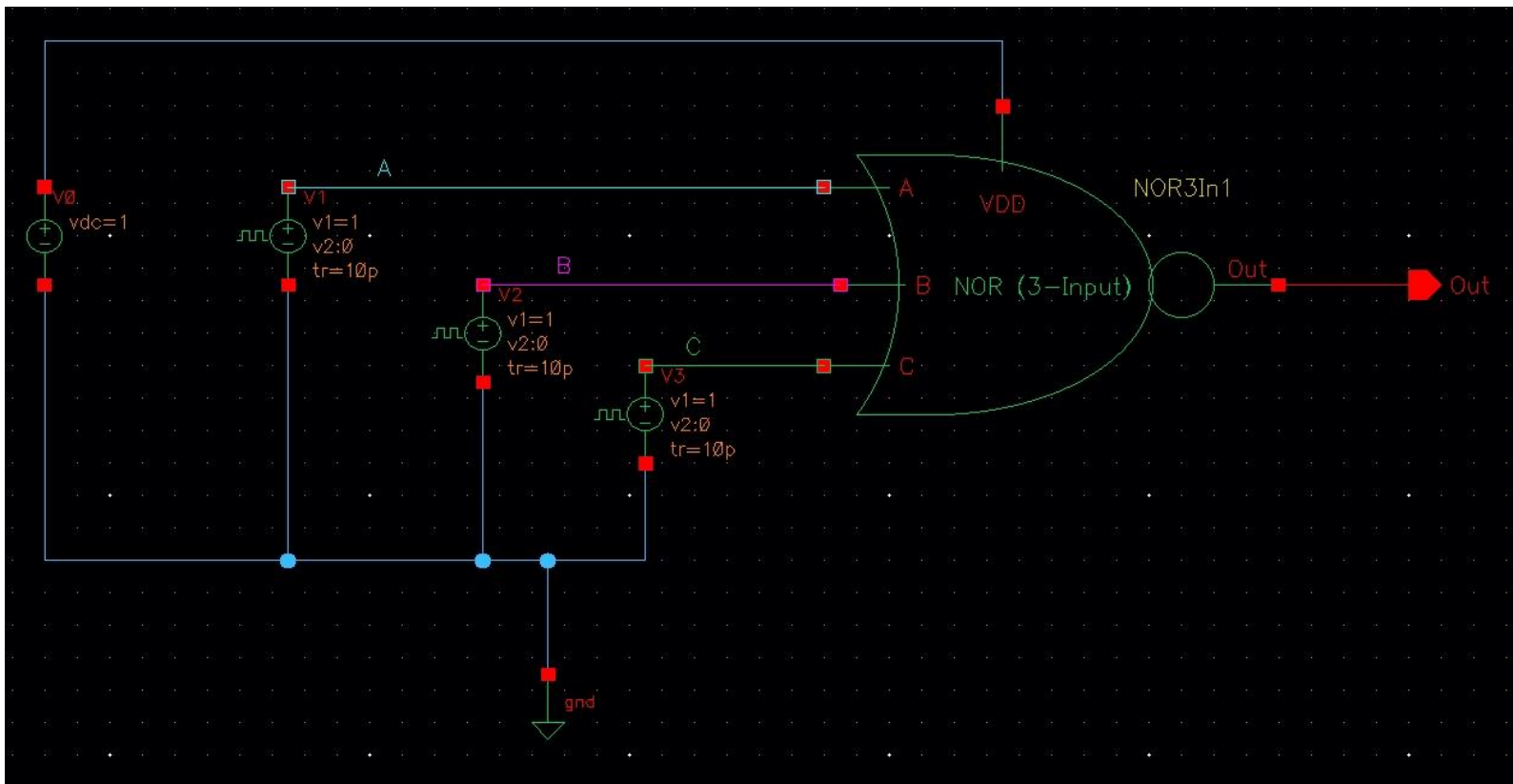
A. 3 input NAND gate





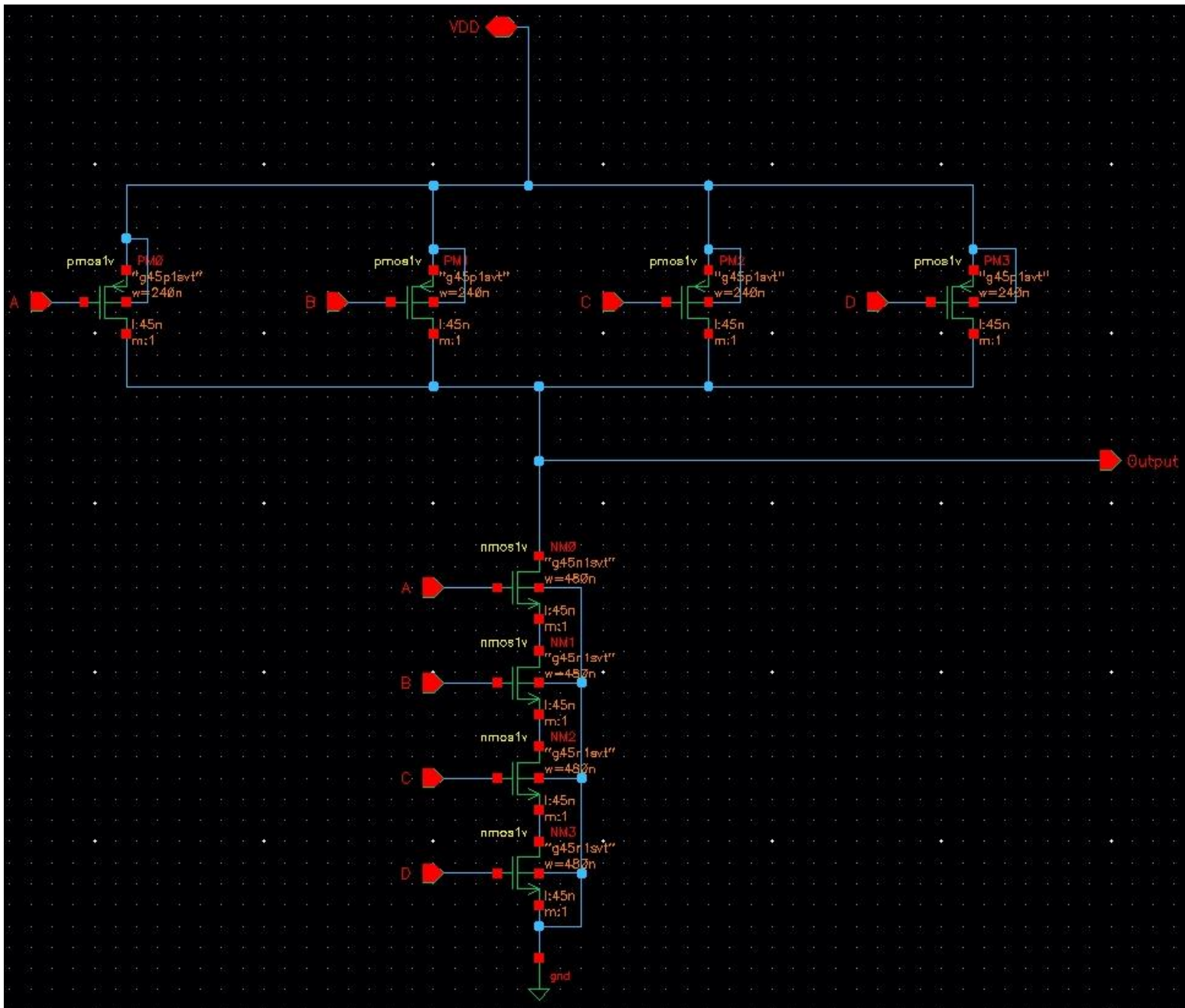
B. 3 input NOR gate

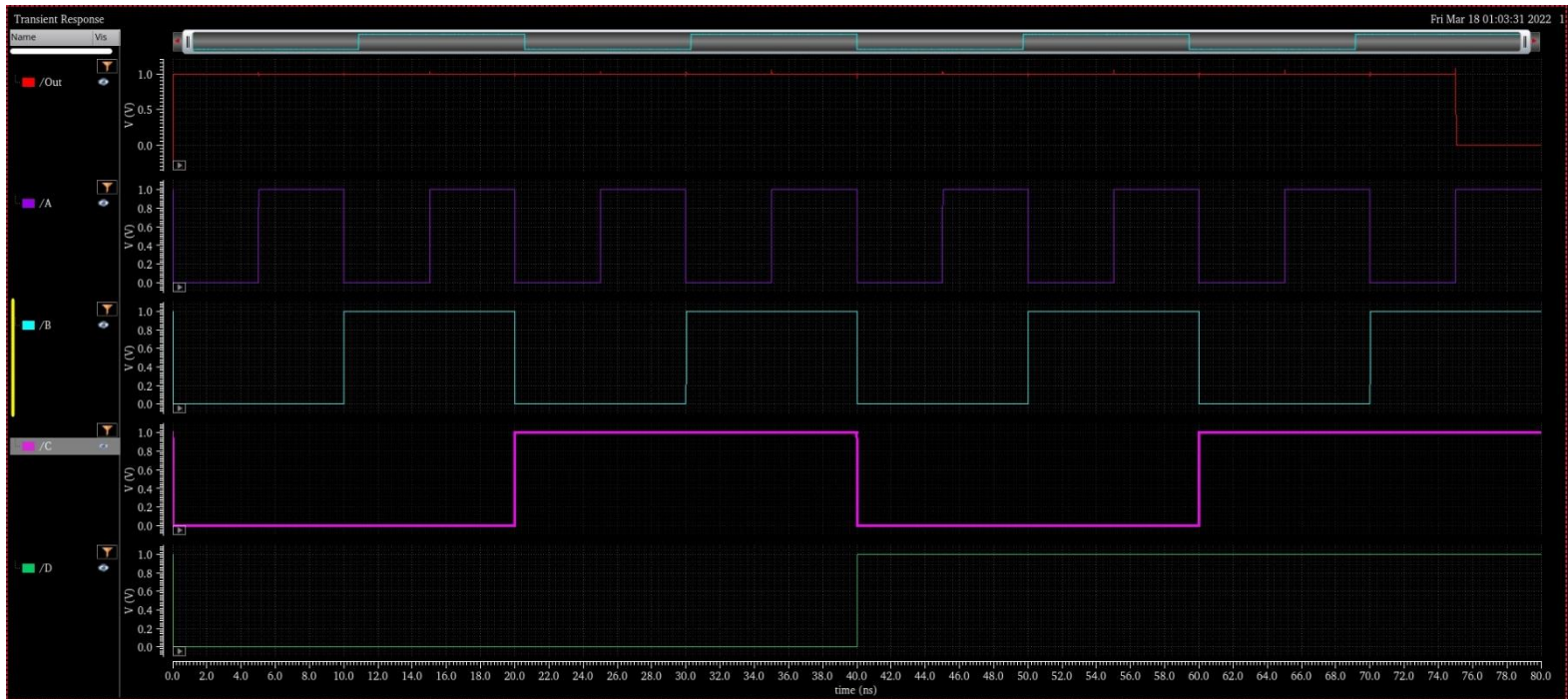
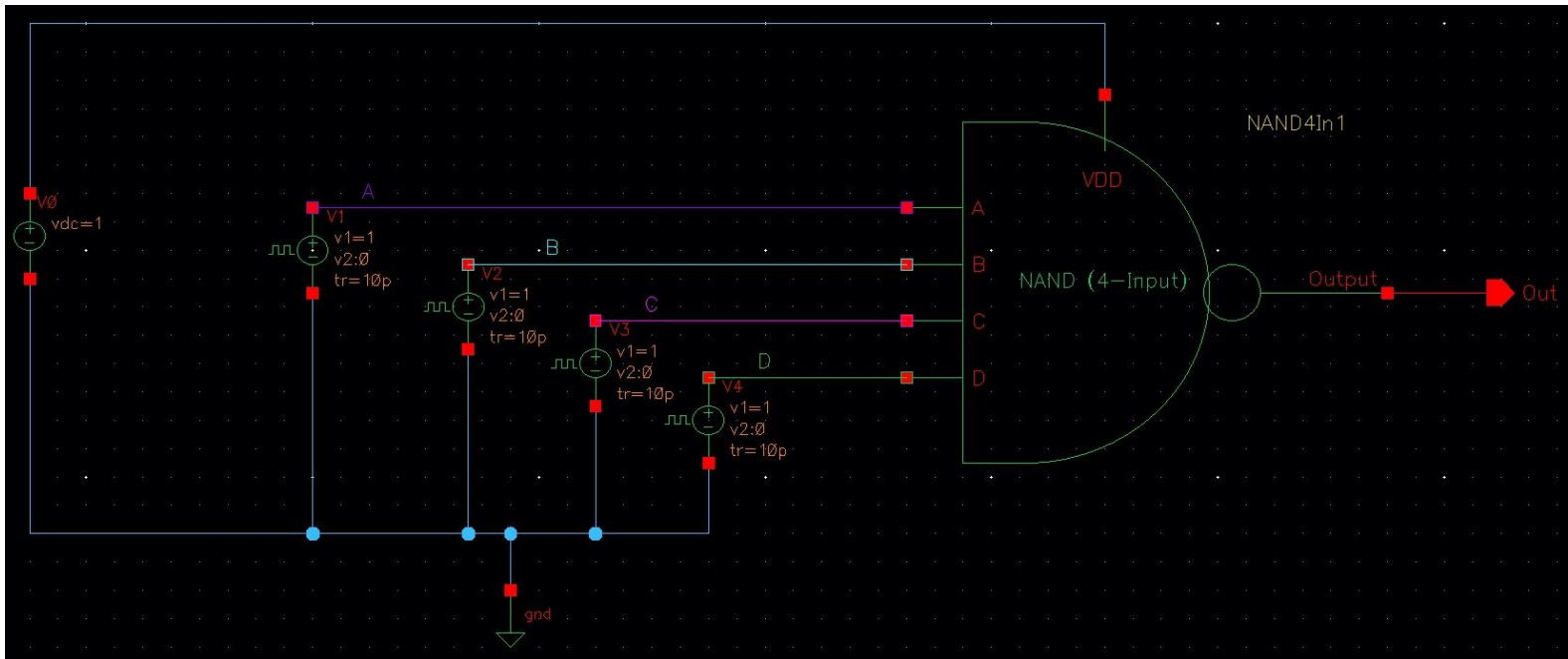




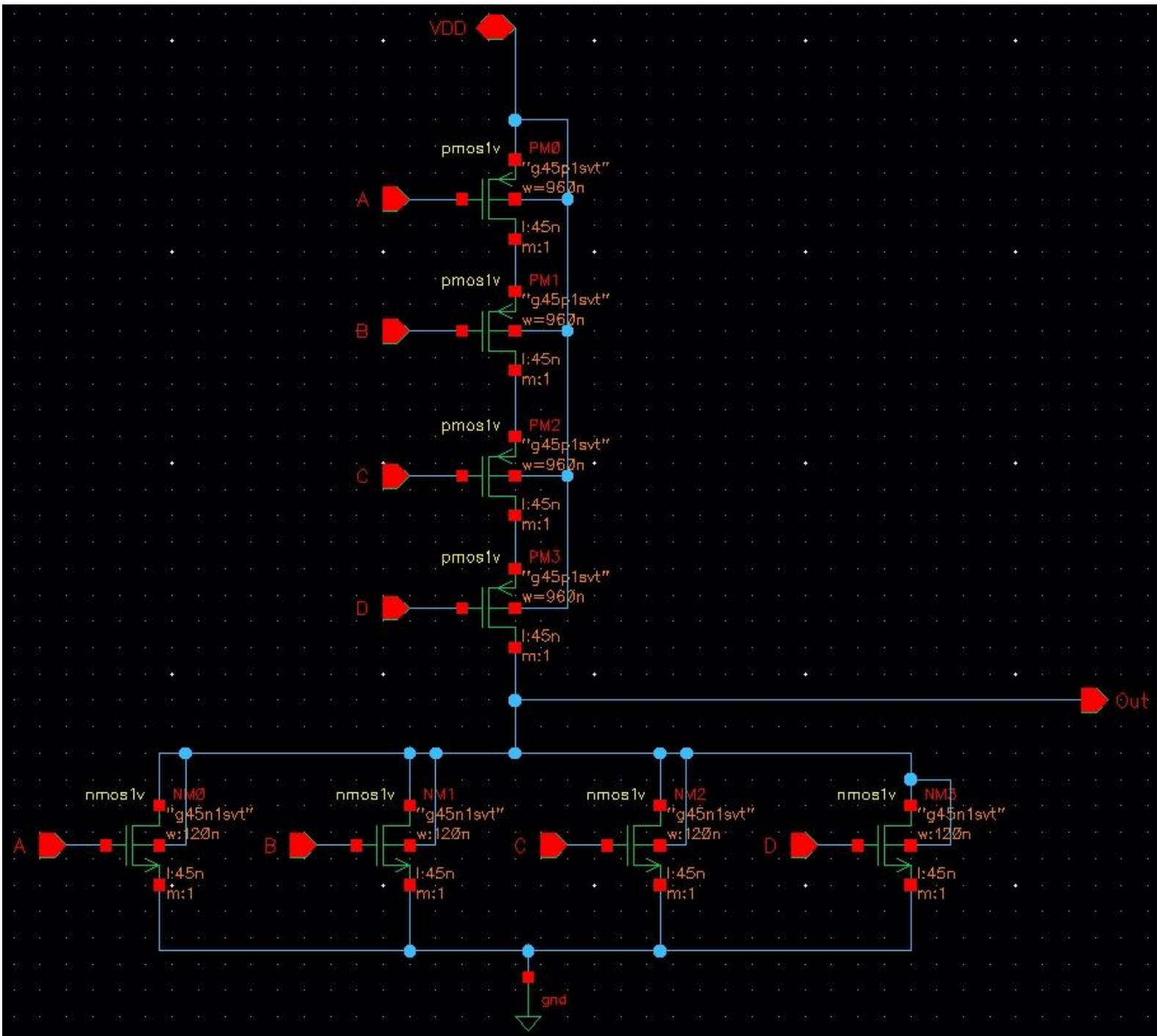


C. 4 input NAND Gate

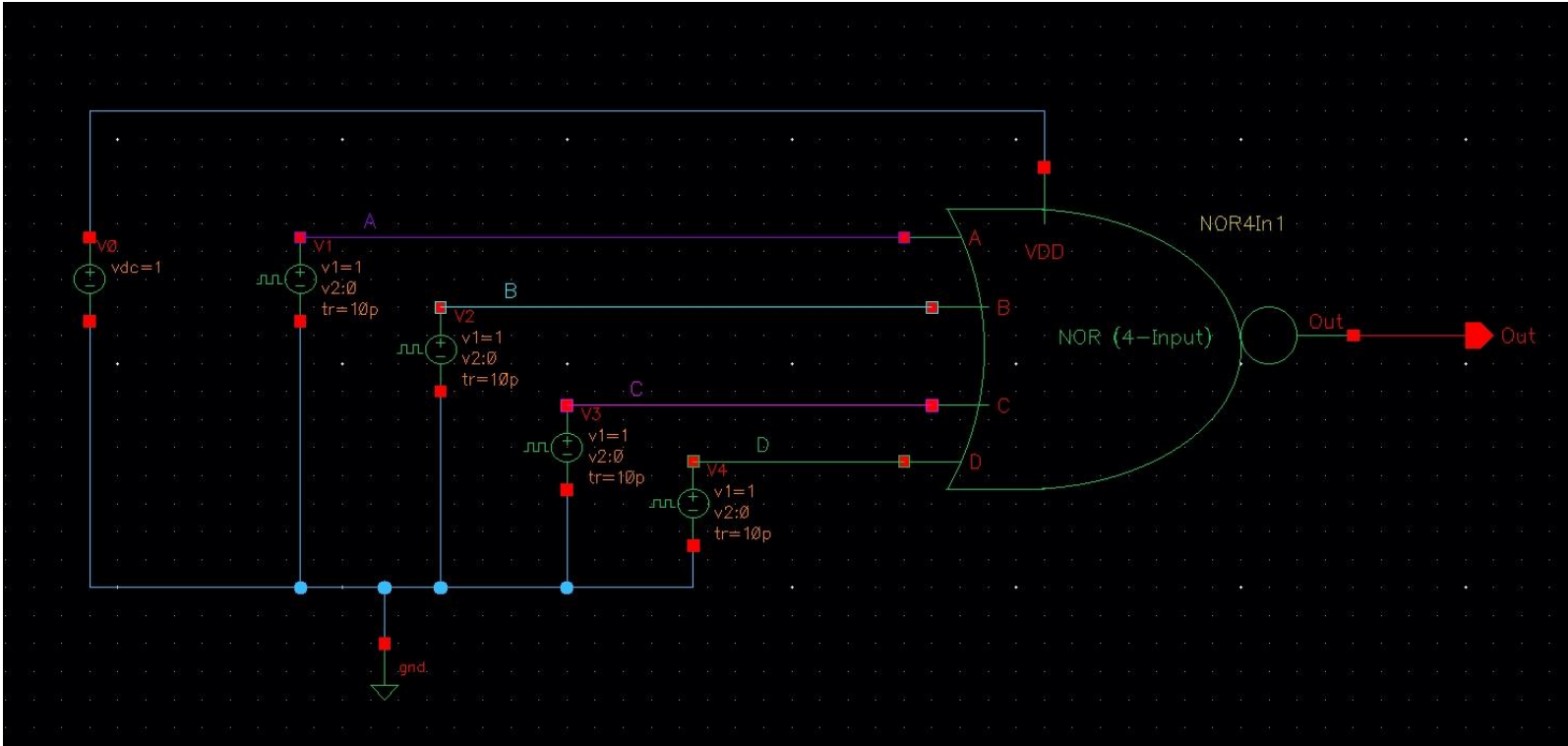




D. 4 input NOR gate

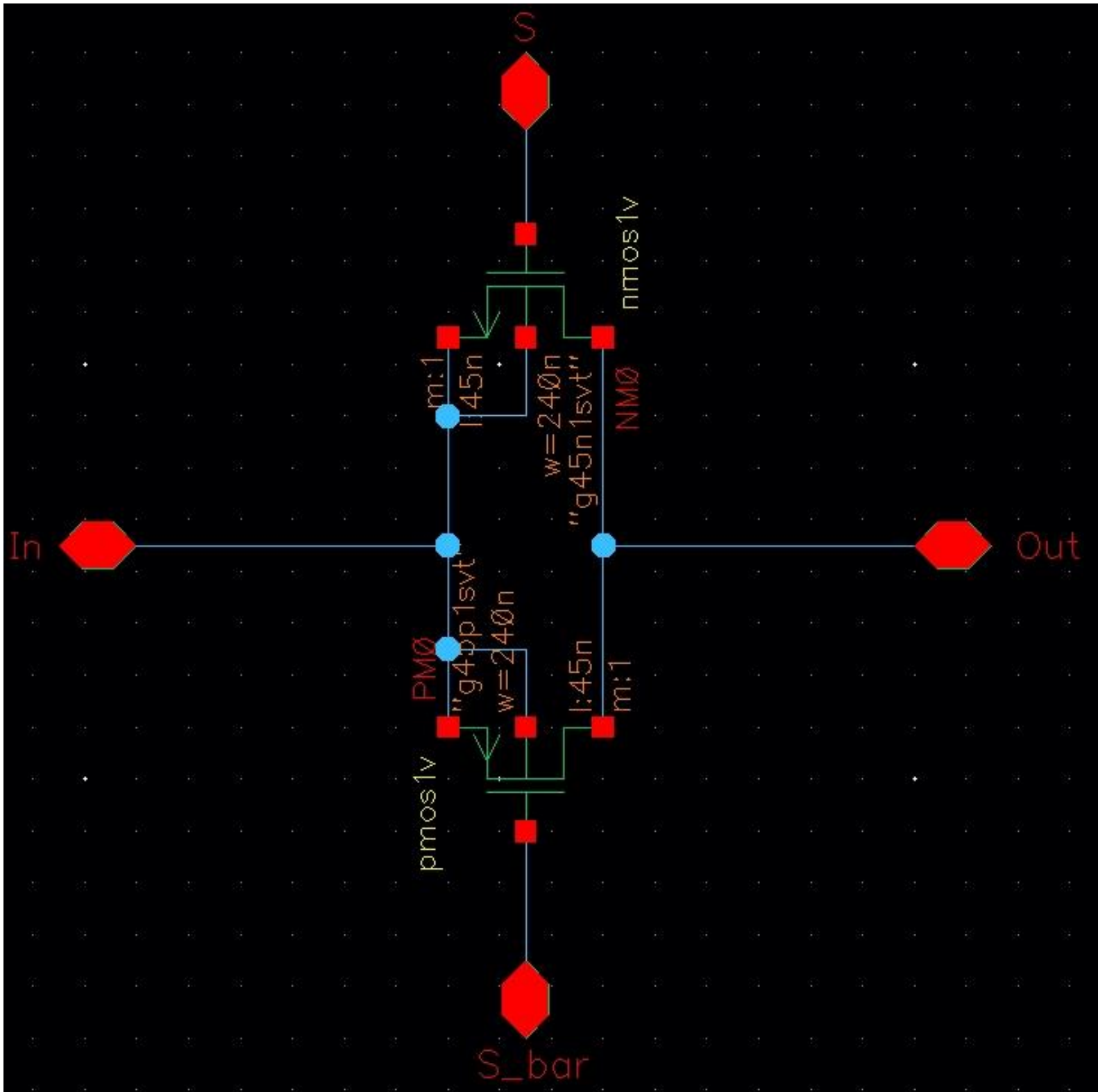


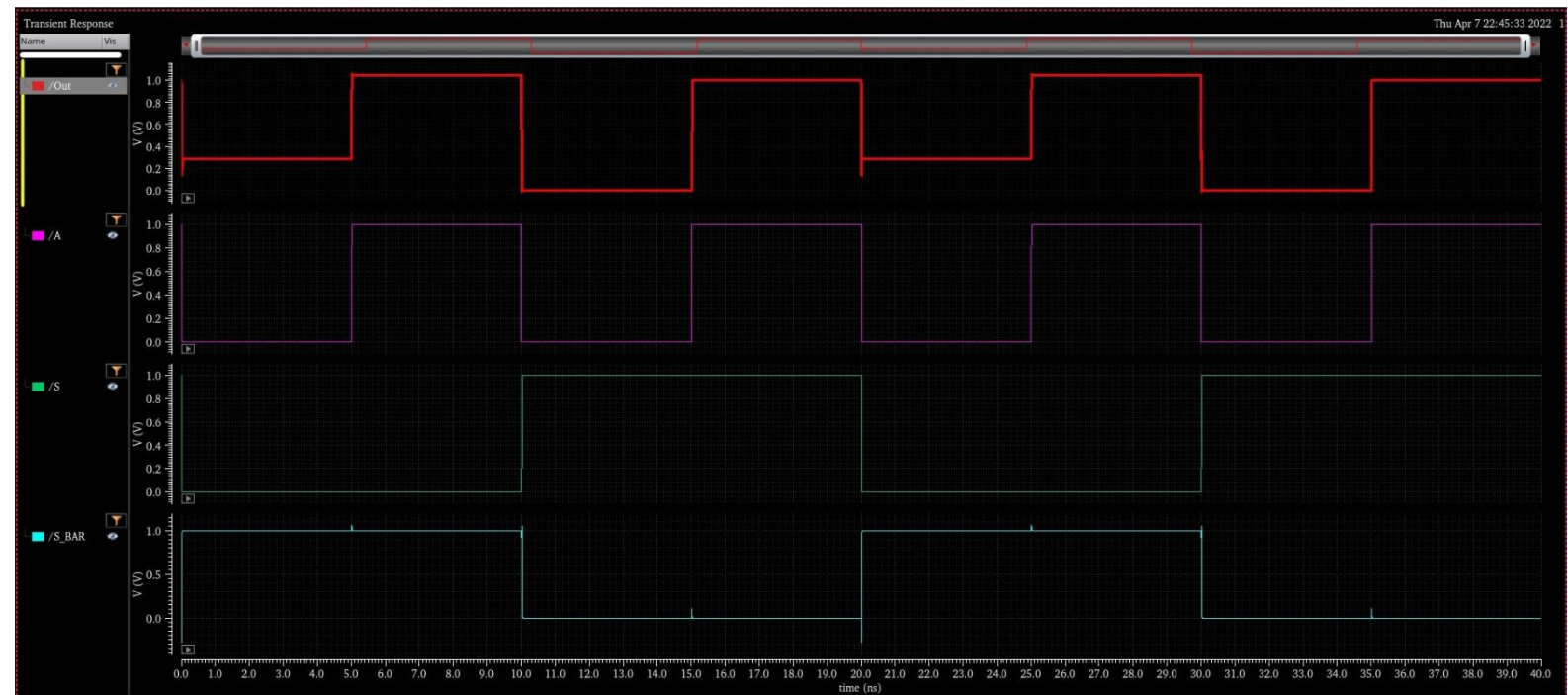
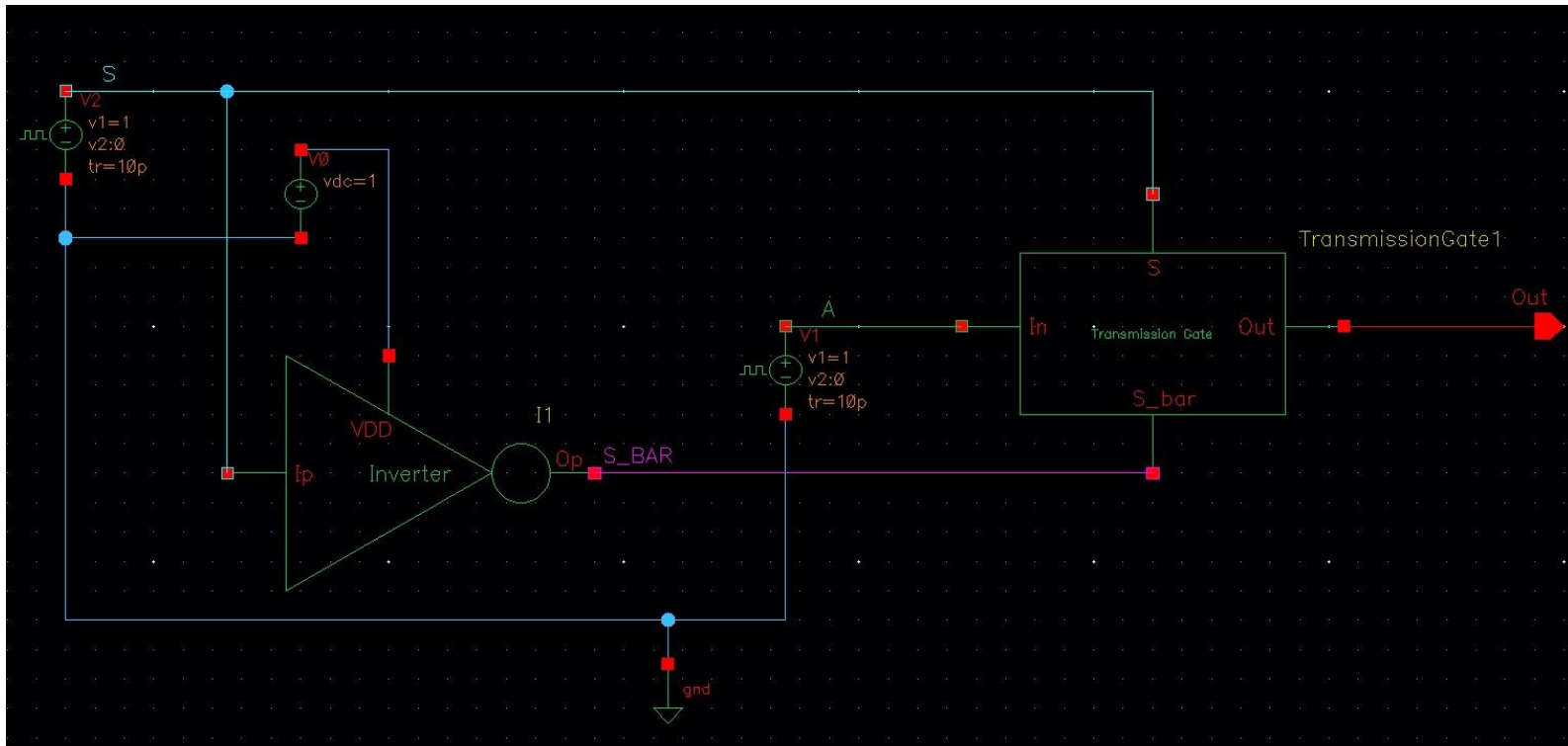




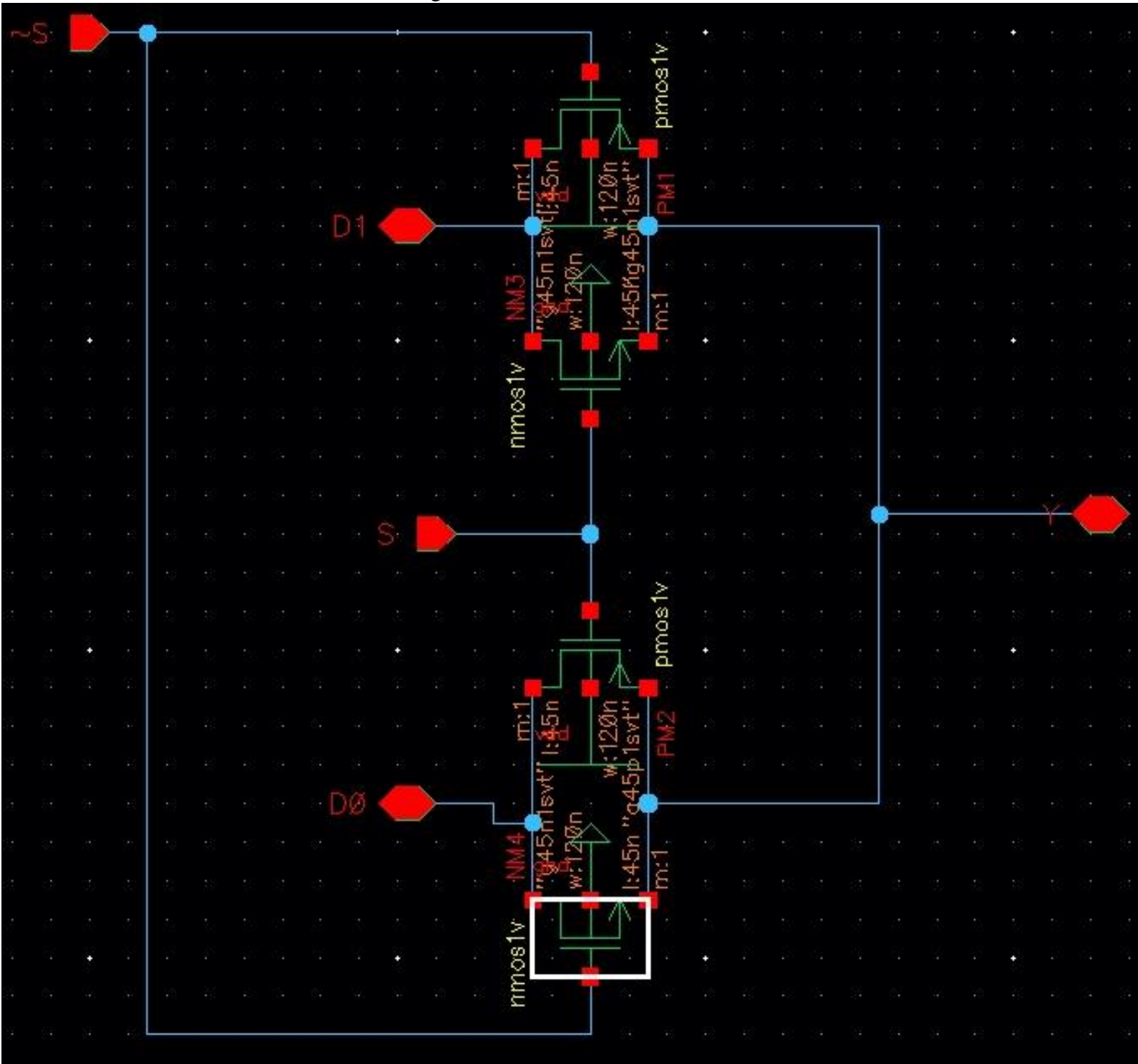


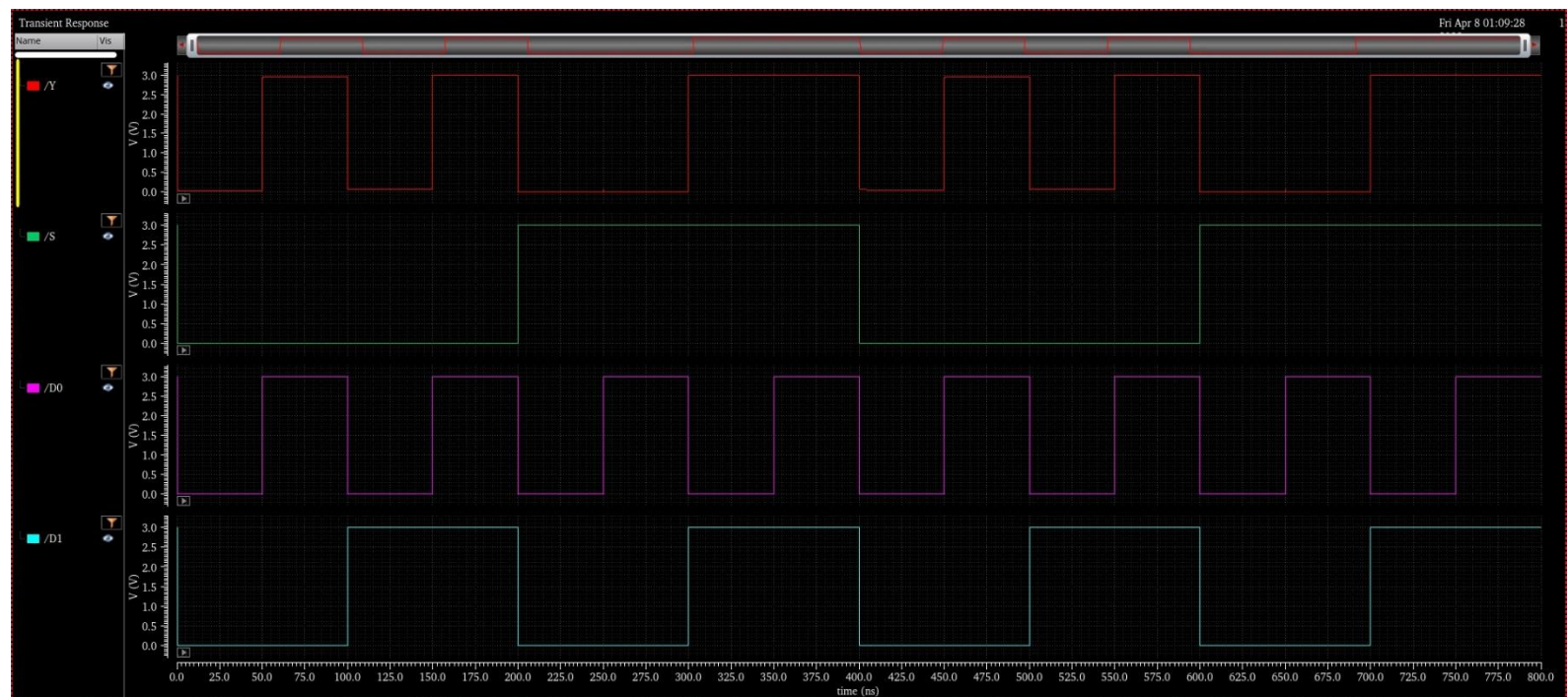
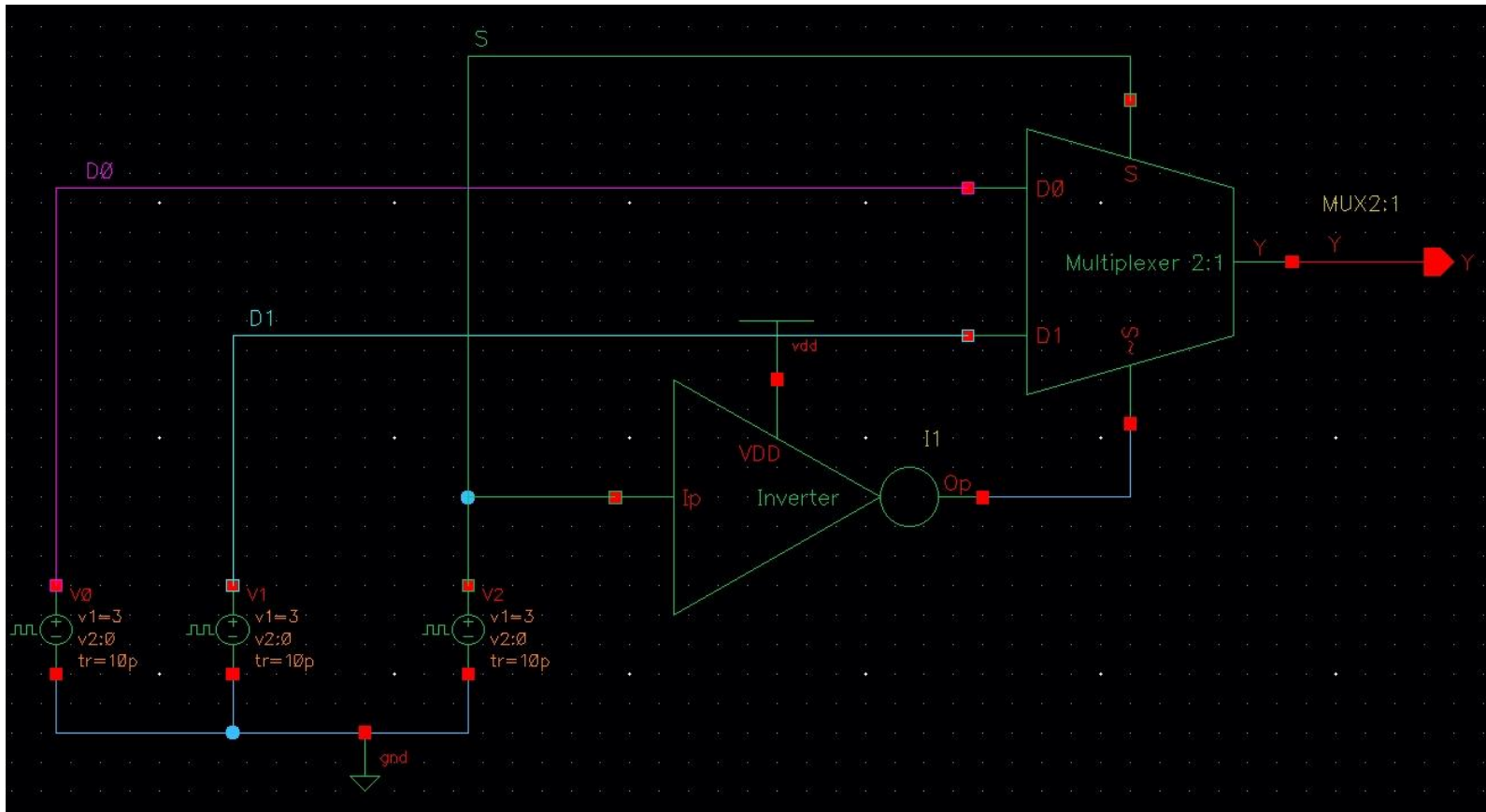
E. Transmission Gate





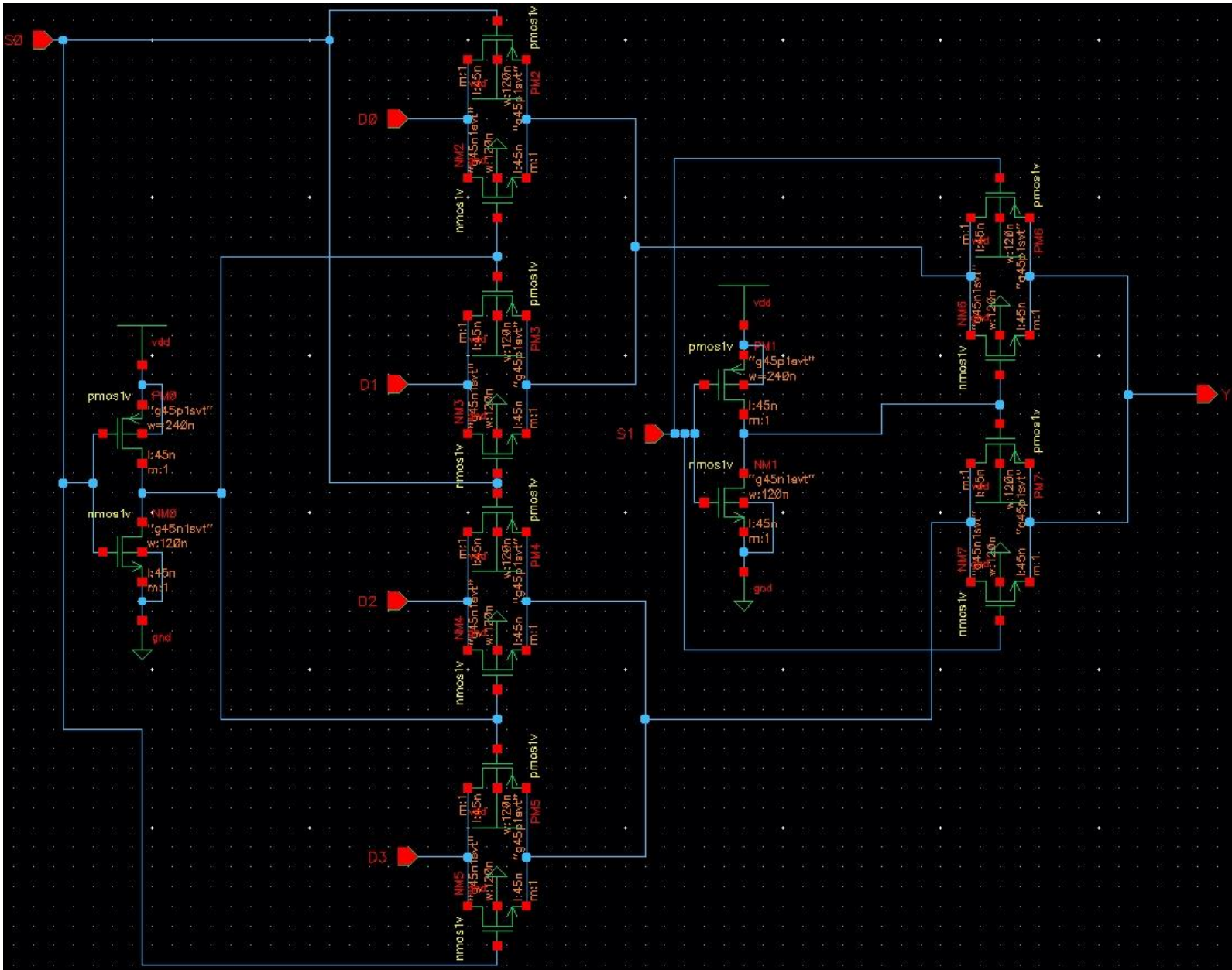
F. 2 to 1 MUX transmission gates

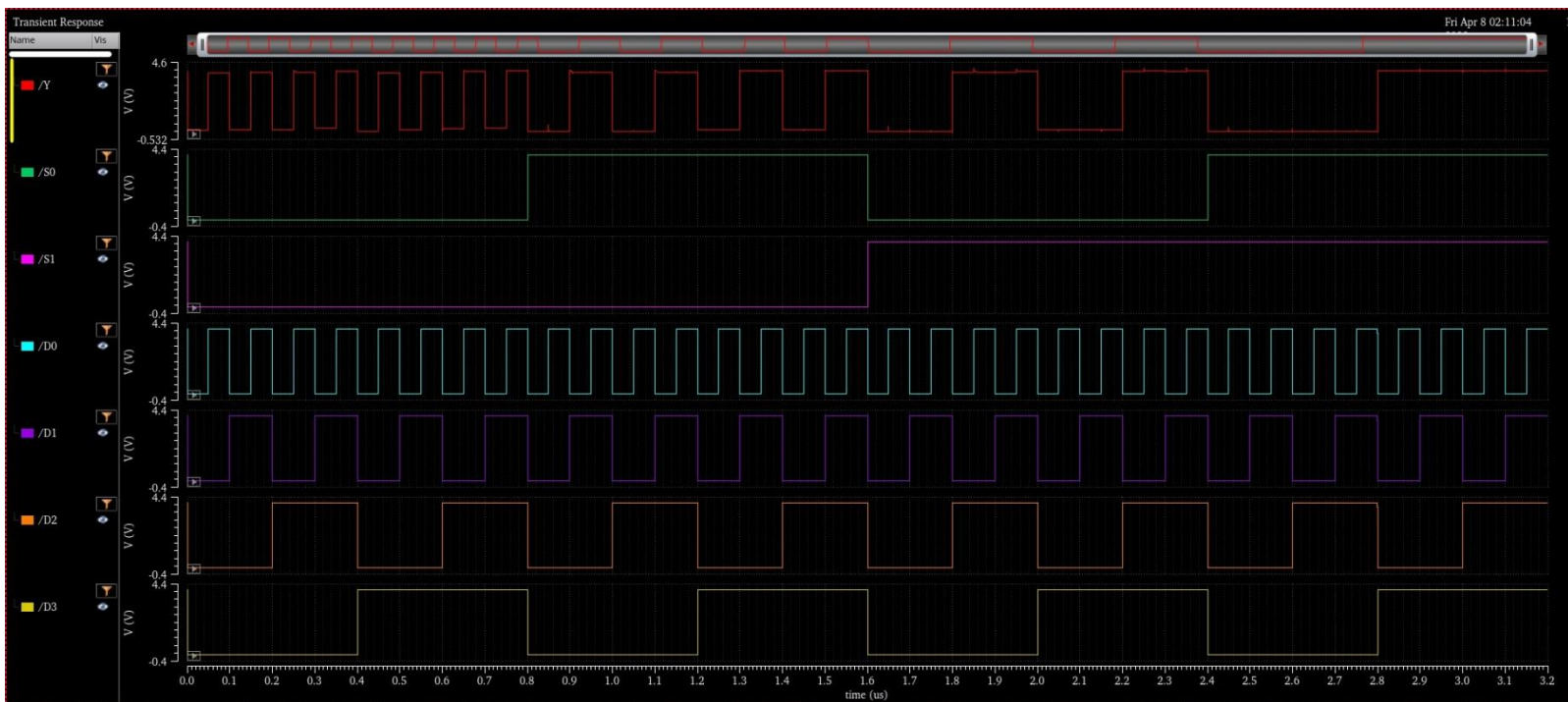
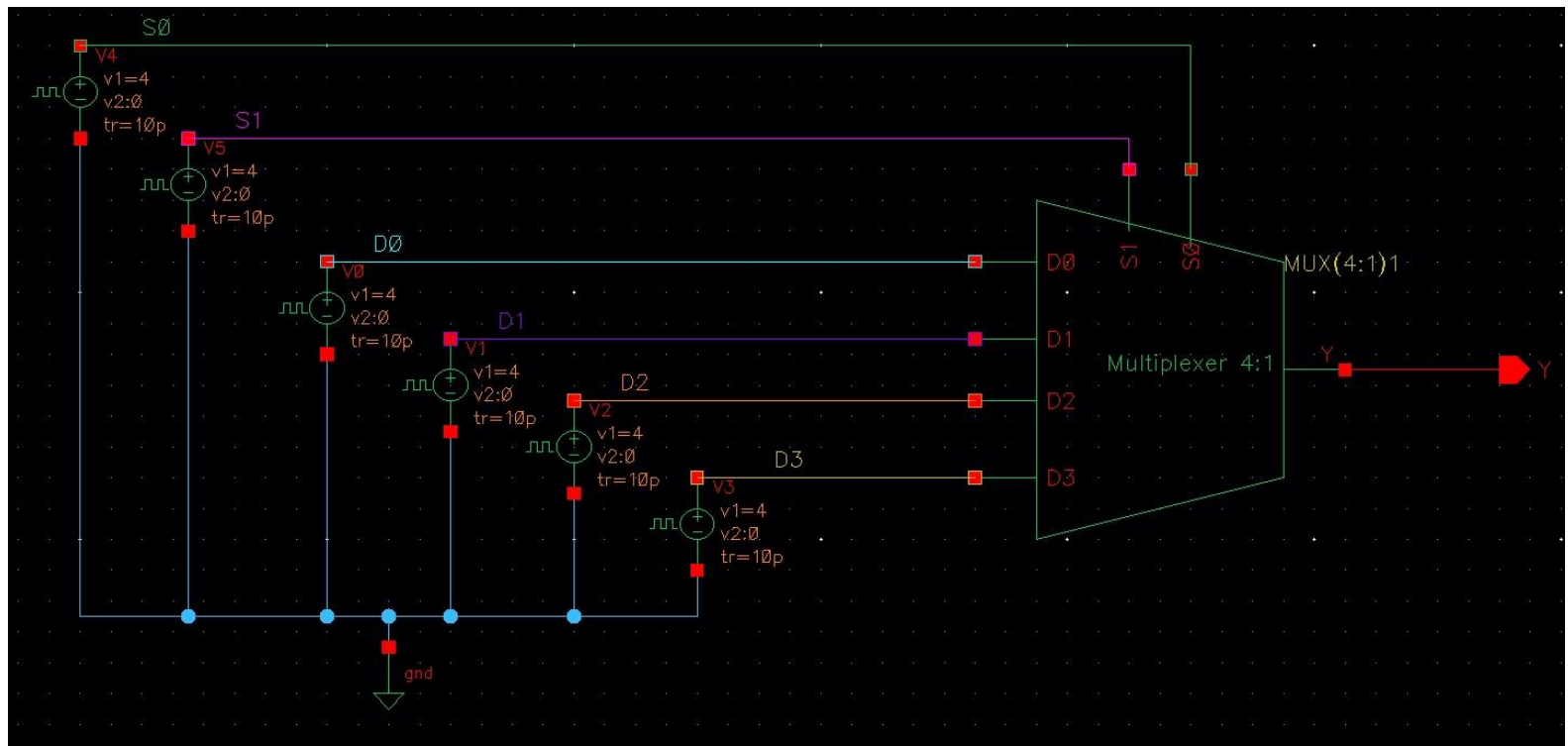




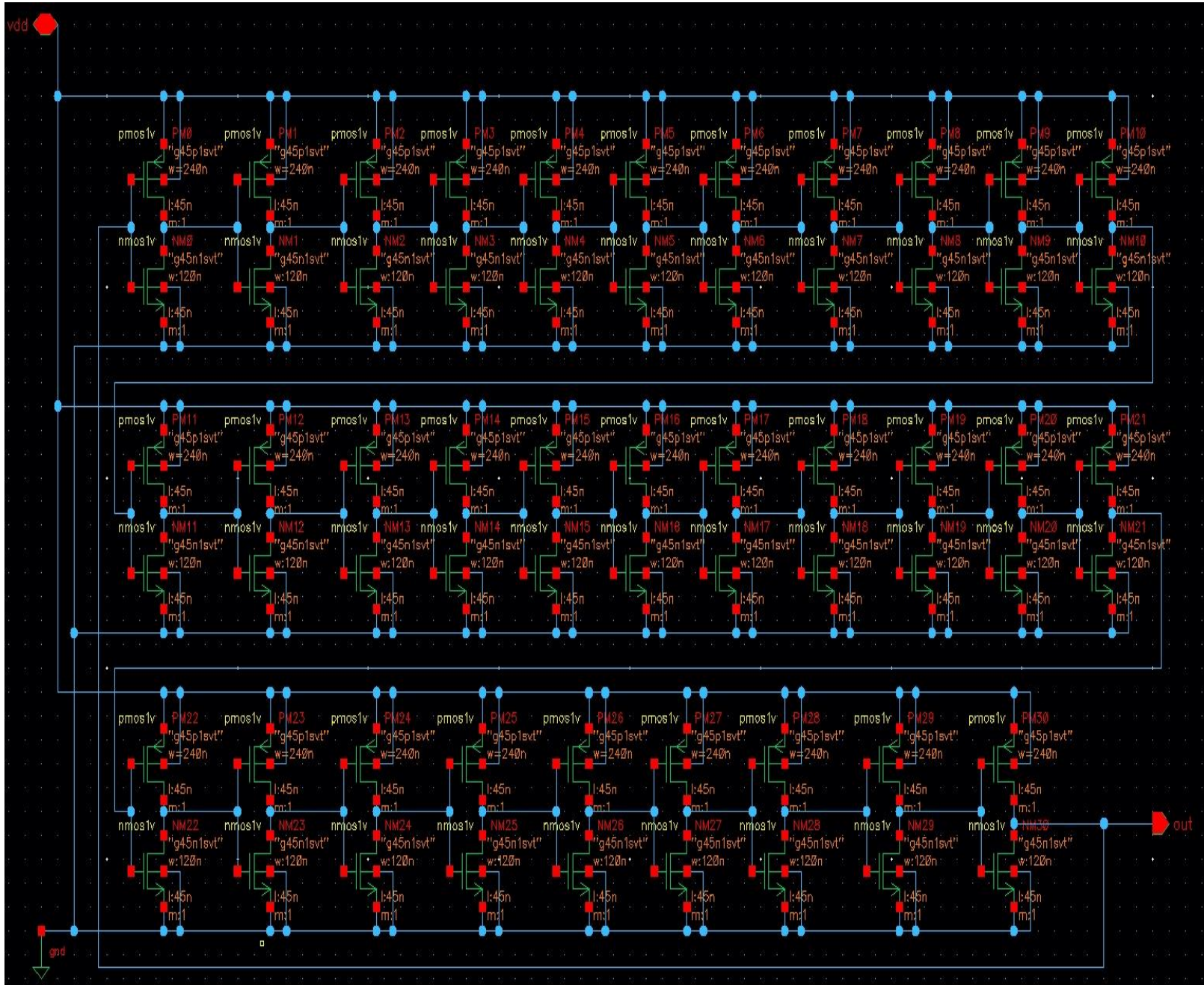


G. 4 to 1 MUX using Transmission gates

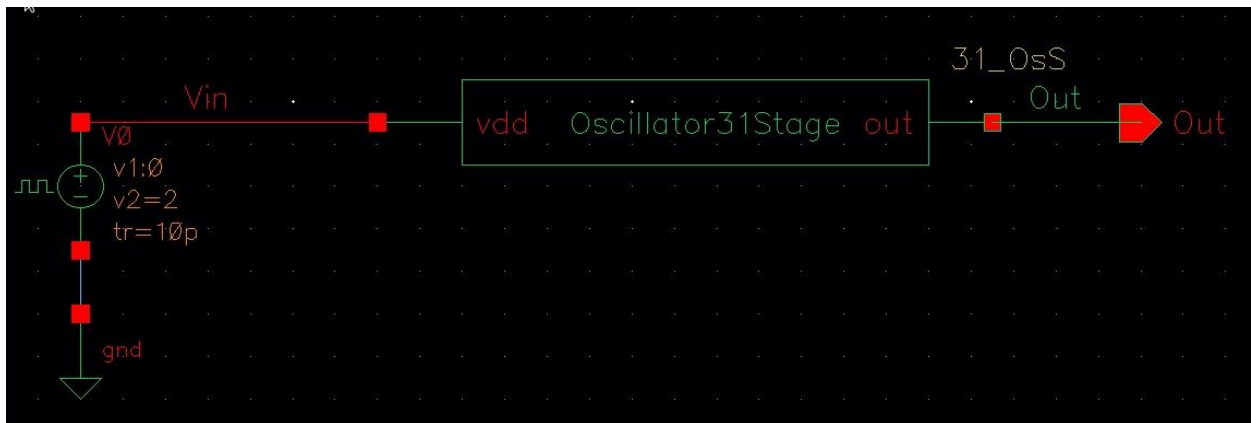




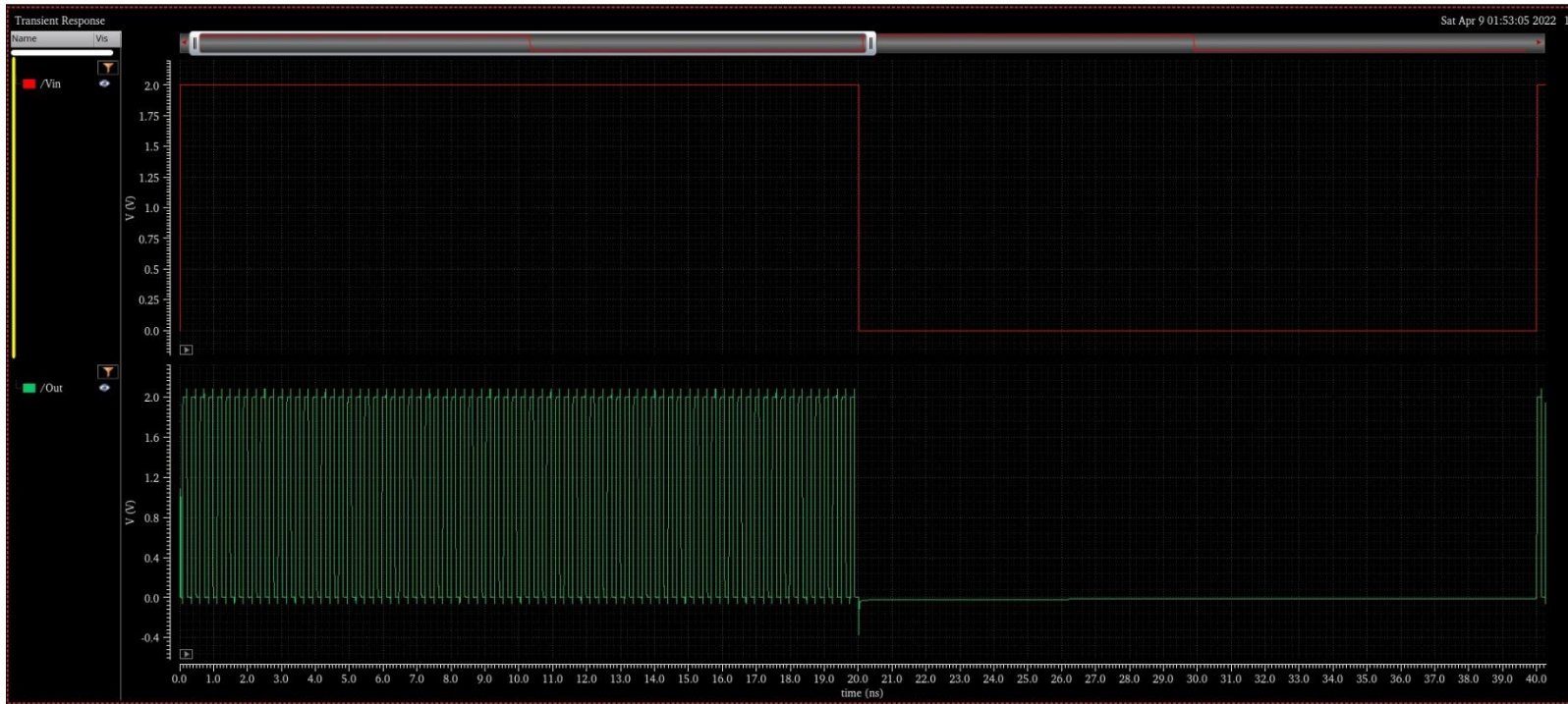
### H. 31 Stage Ring Oscillator











Step-2: DC Characteristics of an Inverter

