Kong Meng Vang
CPE 151-01 SP22

CADENCE PROJECT-3

SEQUENTIAL CIRCUITS, SPRING 2022

CPE 151 SP22

Student: Kong Meng Vang

Instructor: Professor Praveen Meduri

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Part – 1 D-FF Schematic: Design the following D Flip Flop in Cadence and show proper operation through transient simulations.

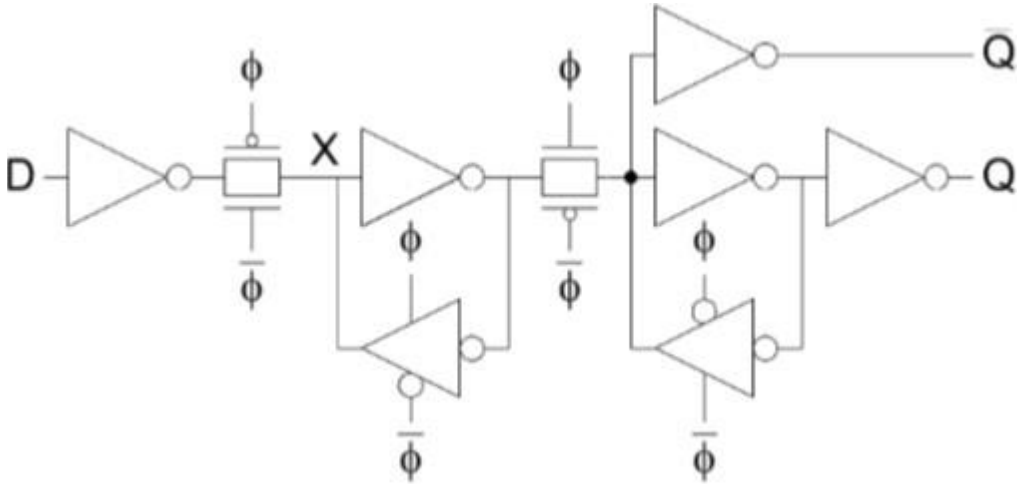

Figure – 1 DFF Schematic

A. Schematics, test bench and appropriate transient analysis wave forms for Inverter.

B. Schematics, test bench and appropriate transient analysis wave forms for Transmission gate.

C. Schematics, test bench and appropriate transient analysis wave forms for tri-state Inverter.

D. Schematics, test bench and appropriate transient analysis wave forms for the overall DFF circuit, also called top-level design, figure - 1.

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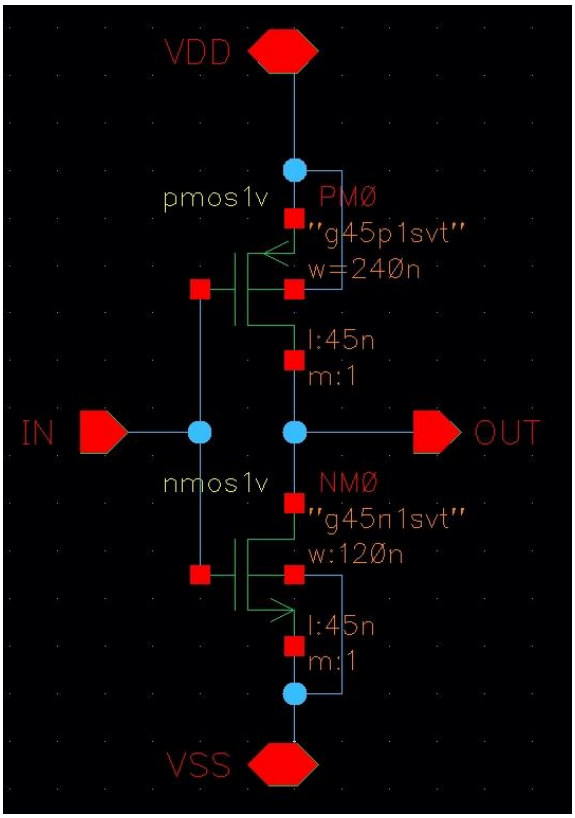
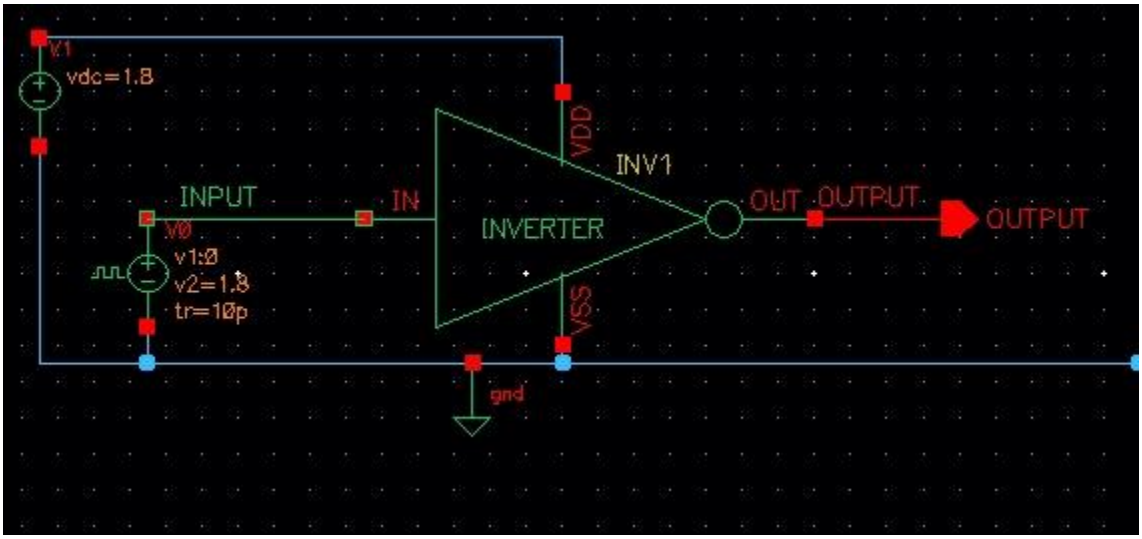
A. Inverter

Schematic:





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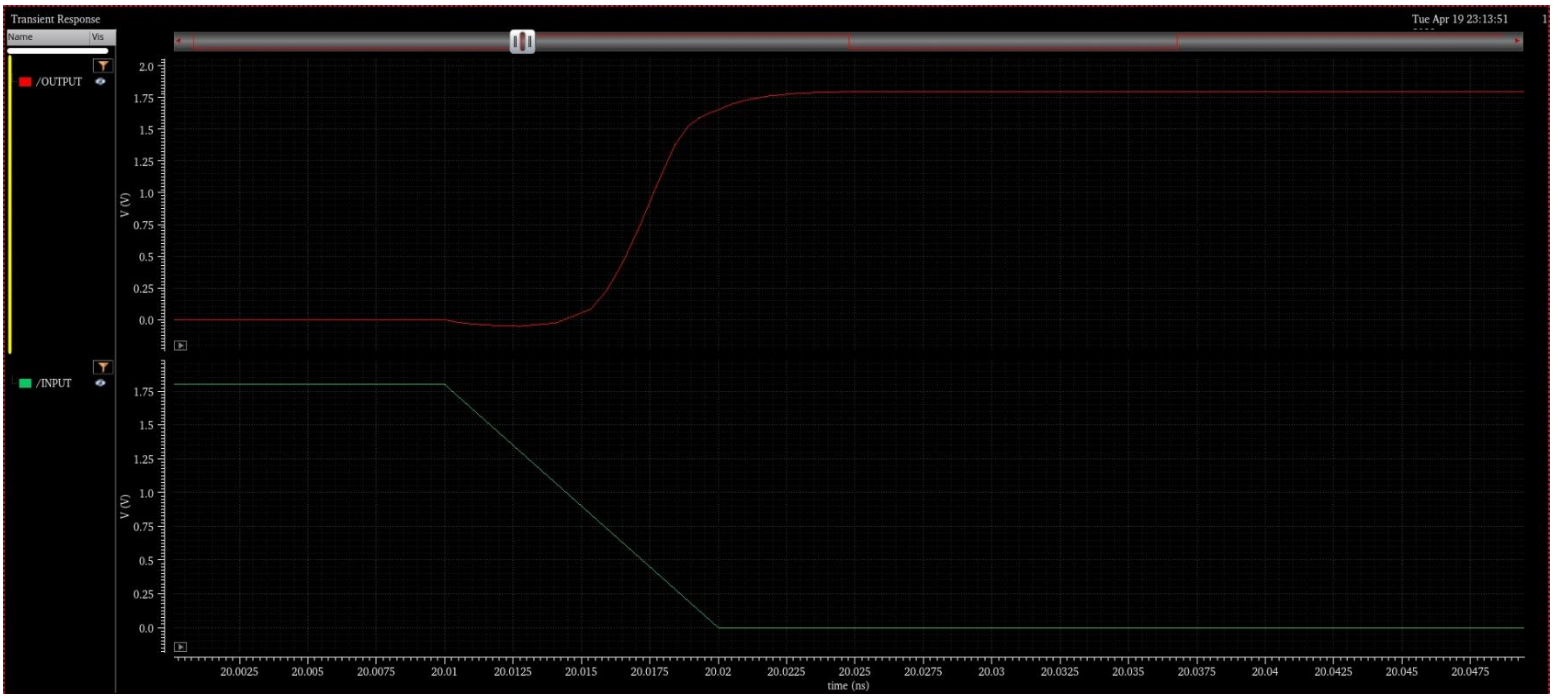
Transient Analysis:



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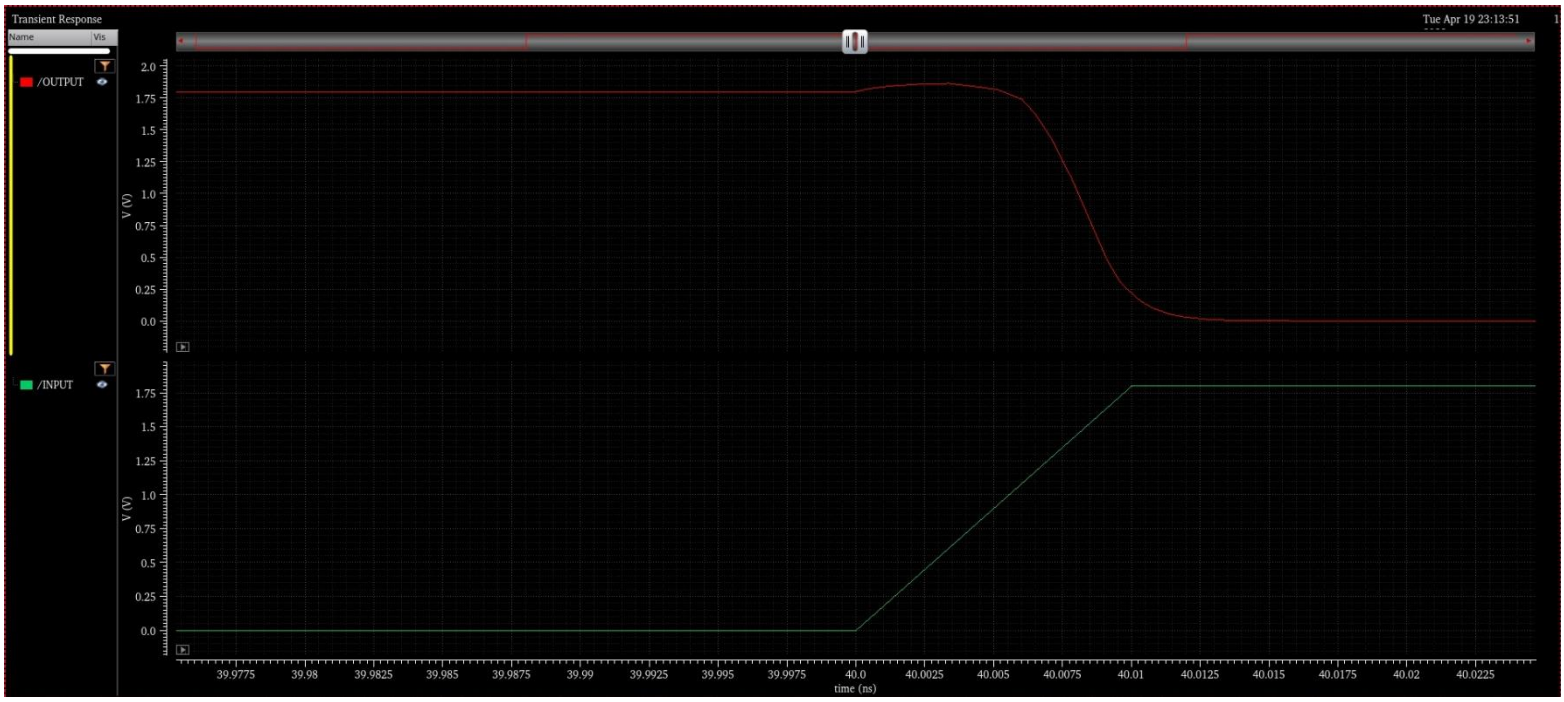
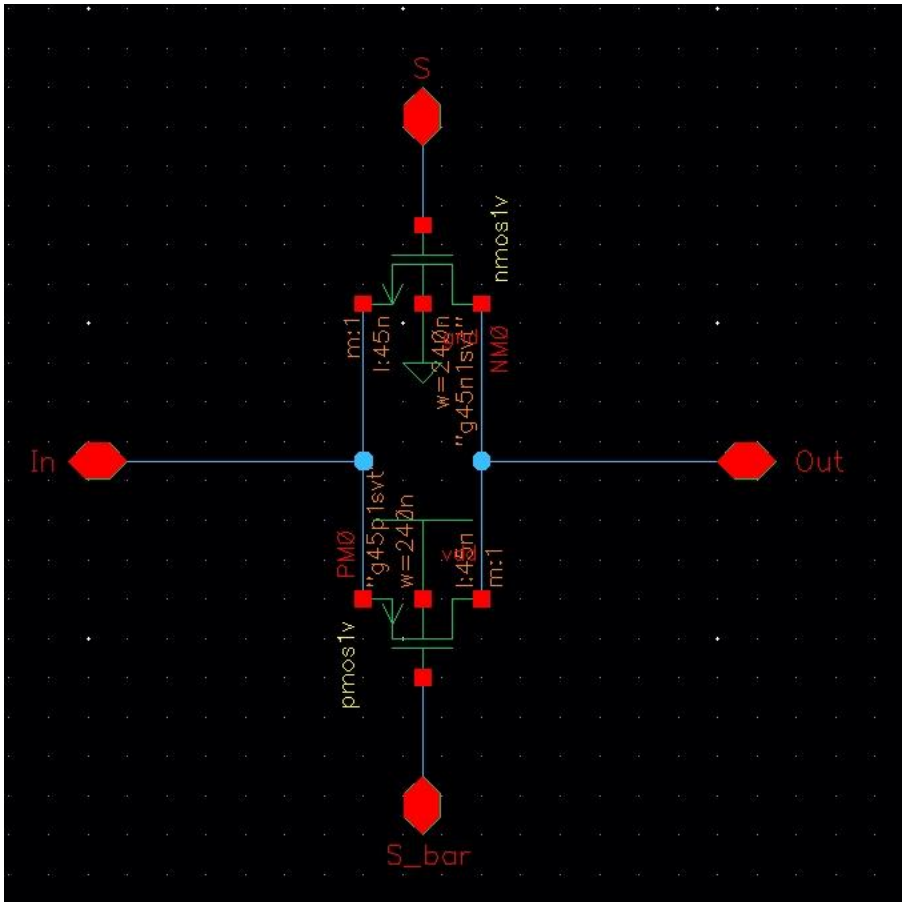


B. Transmission Gate
Schematic:



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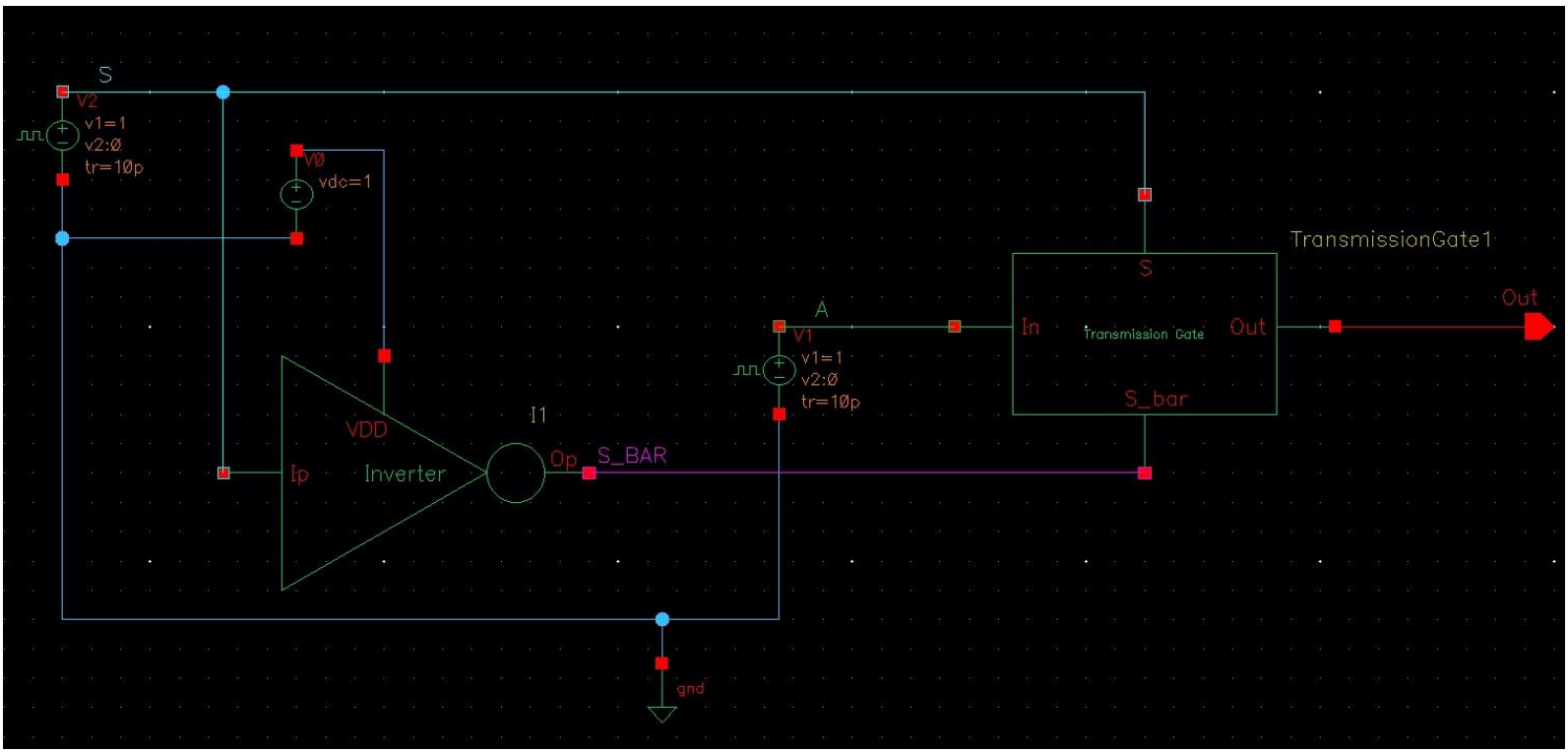

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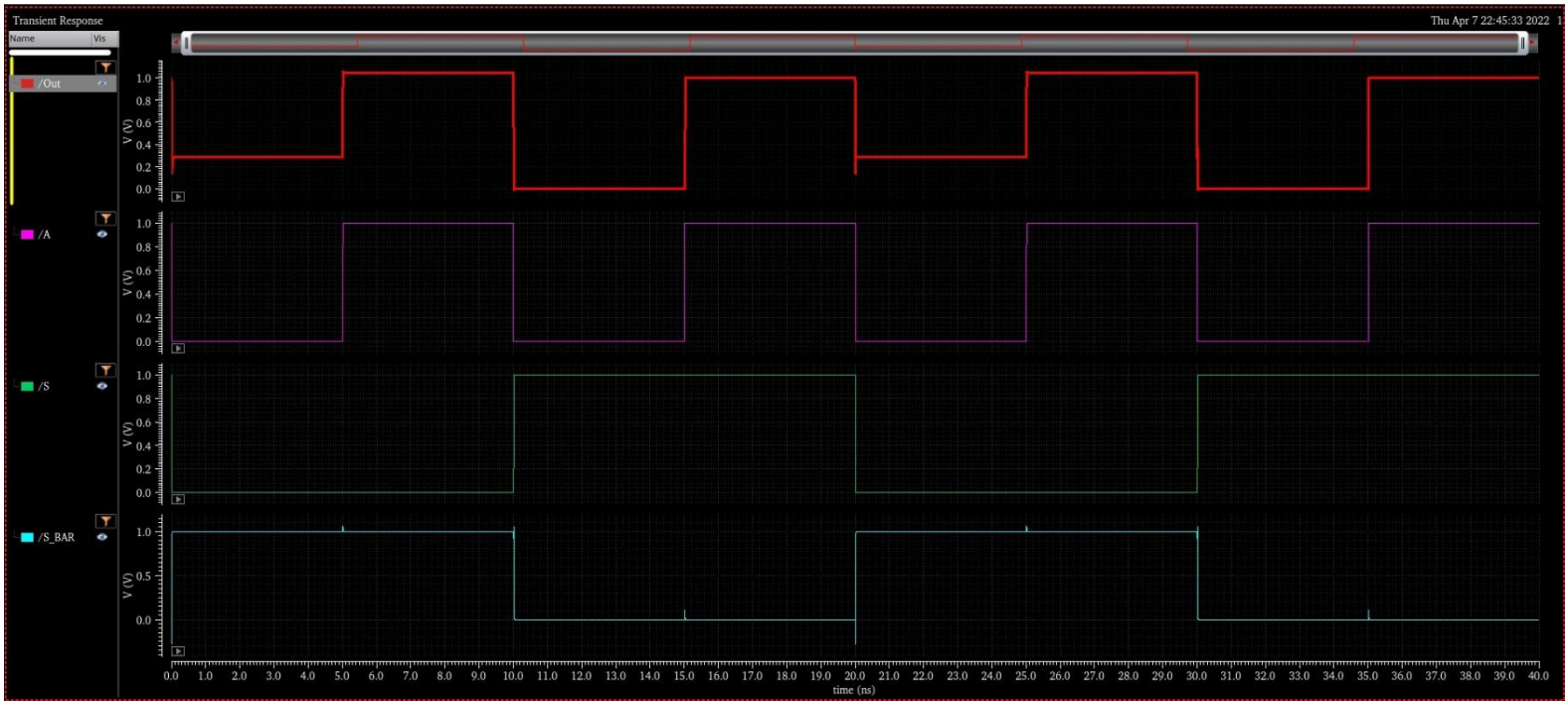
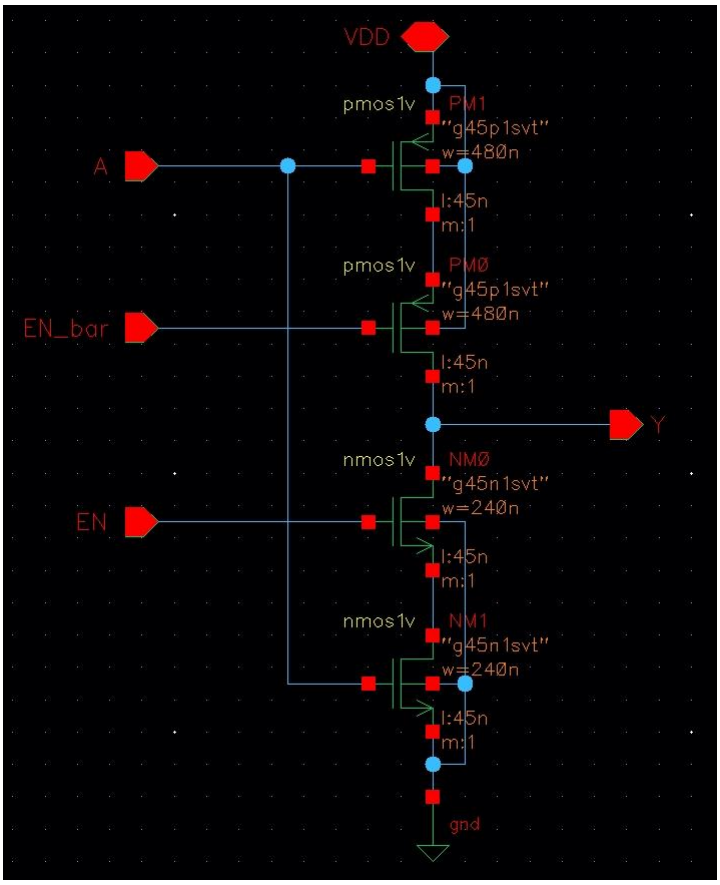
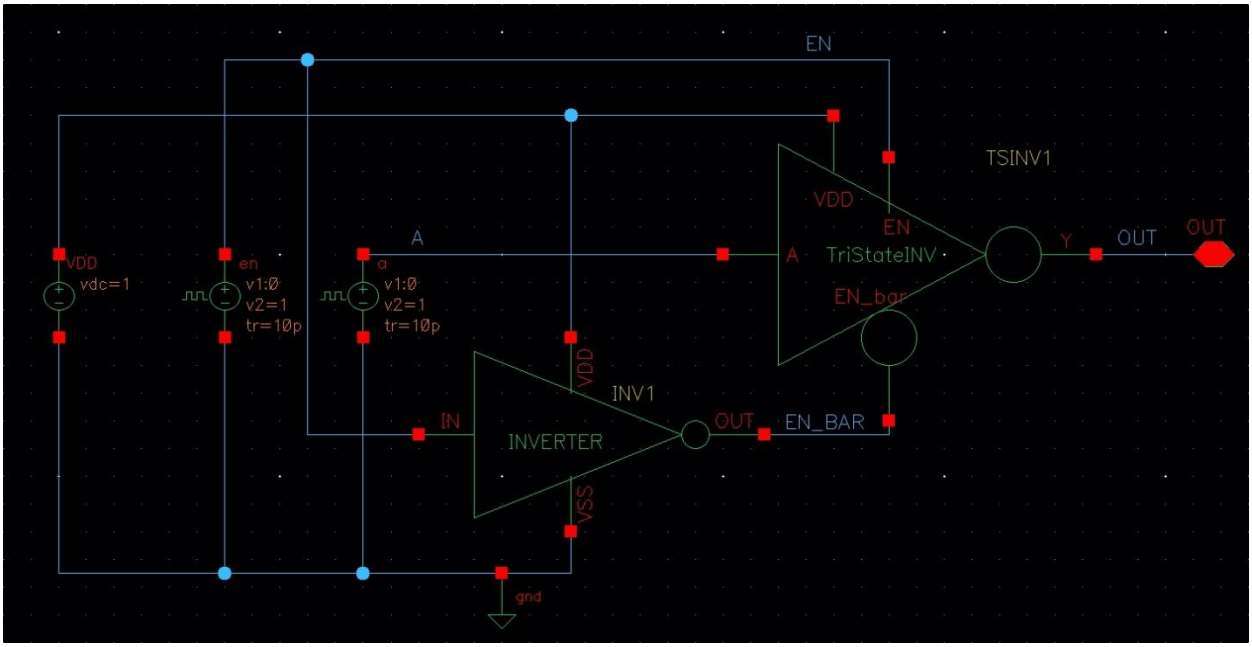
Transient Analysis:



C. Tri-State Inverter
Schematic:





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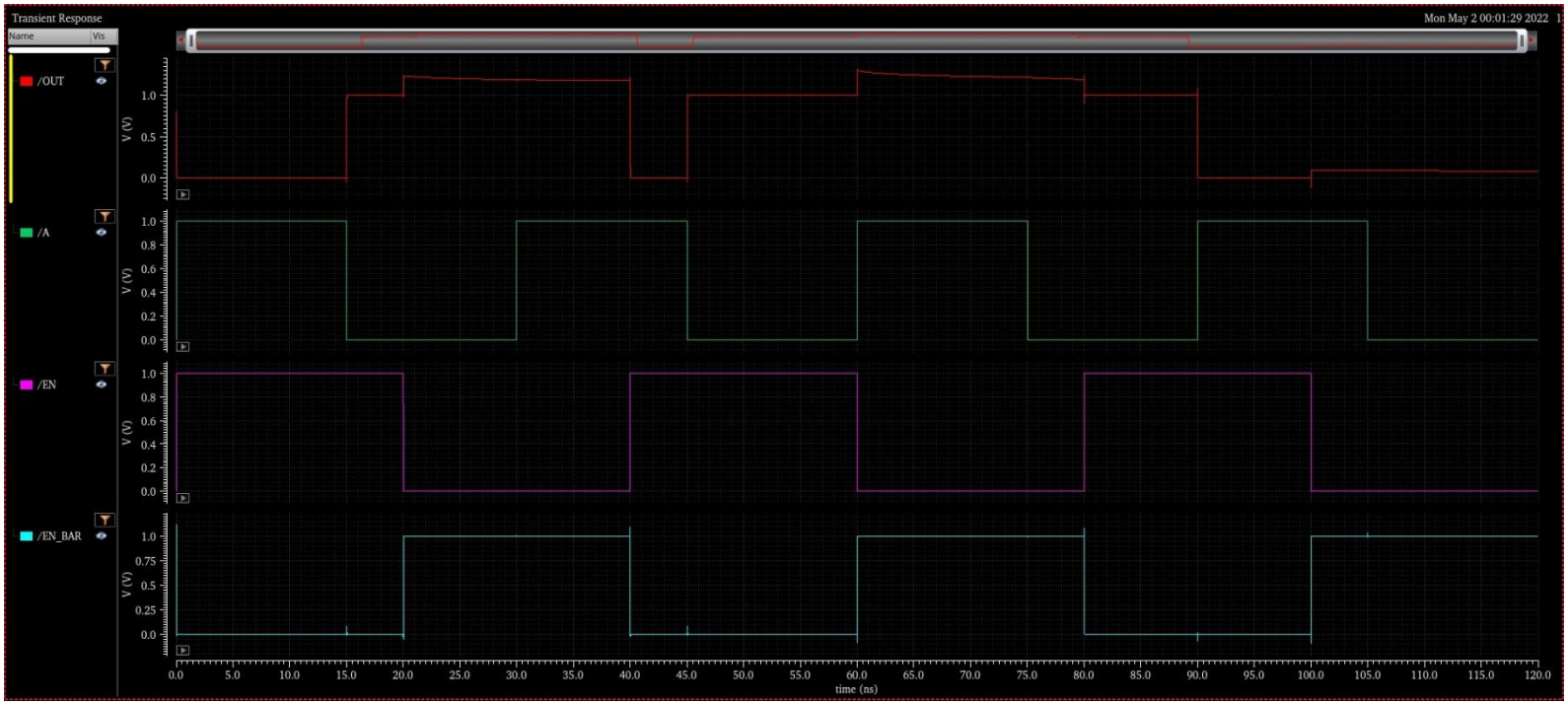

Transient Analysis:

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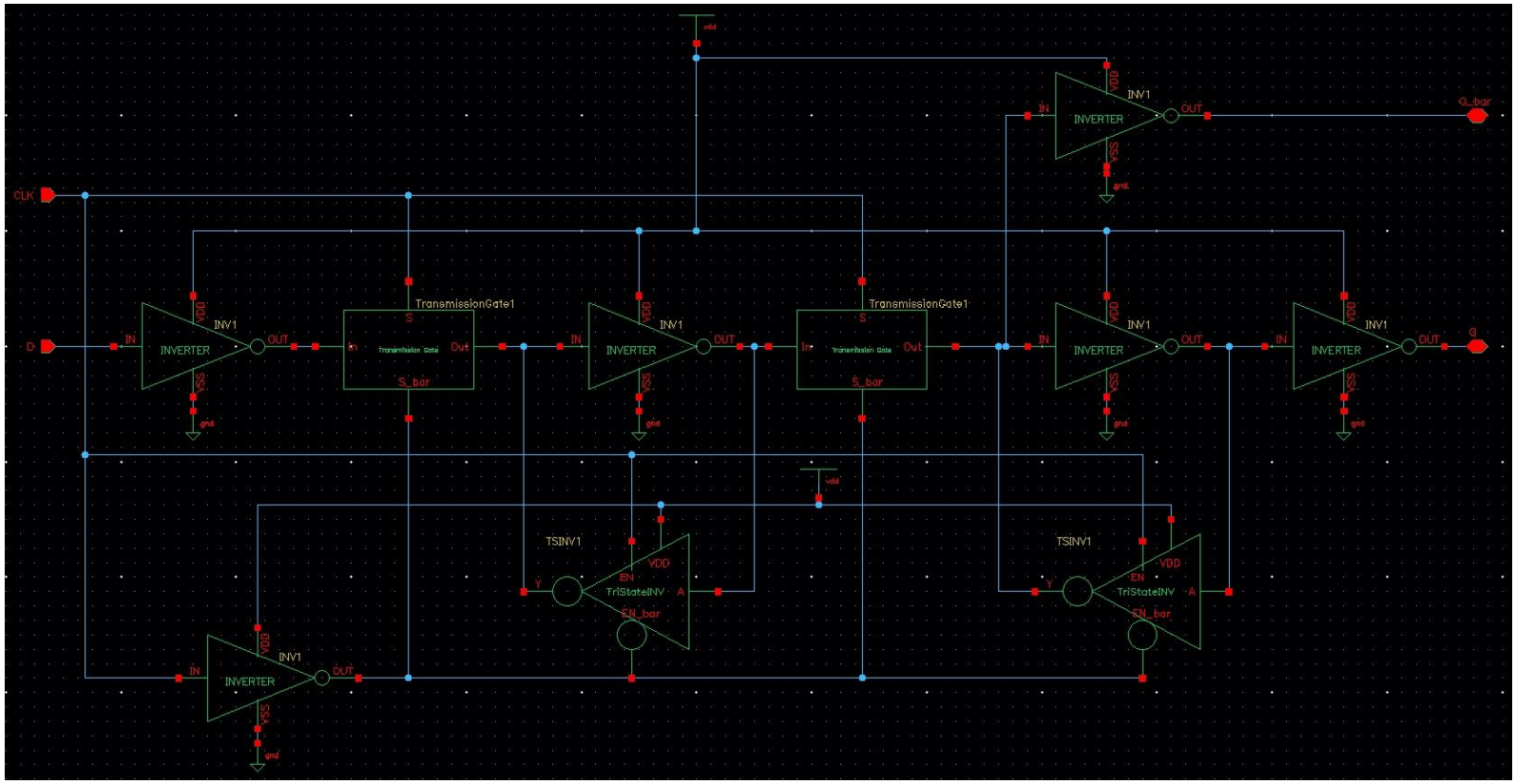
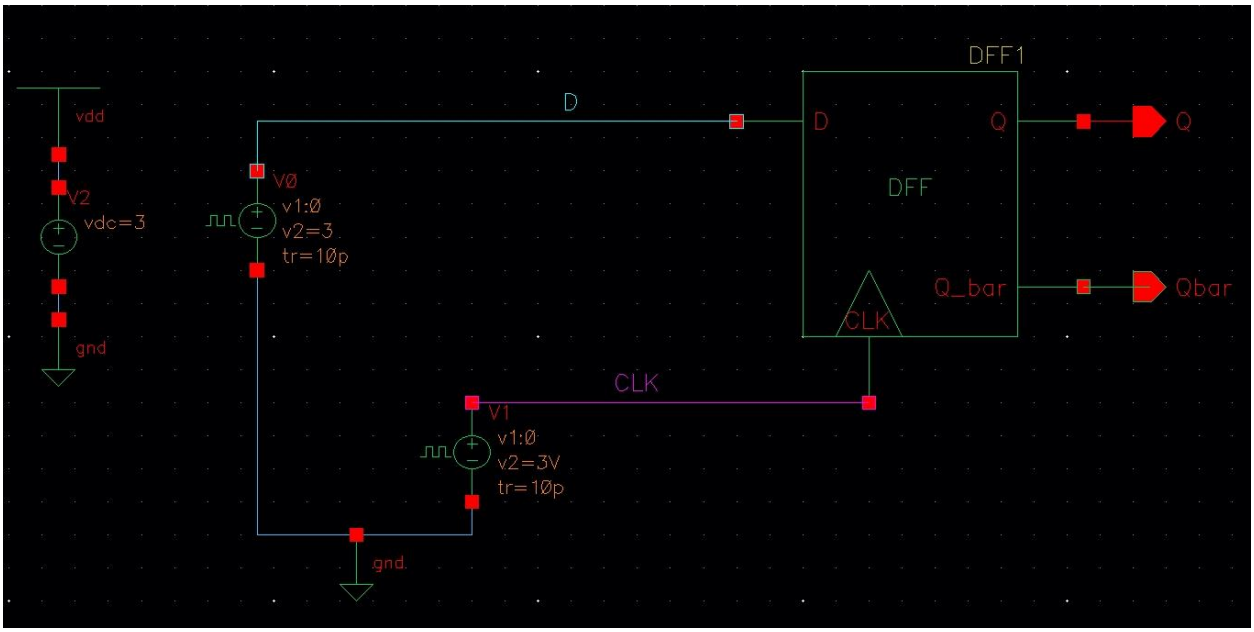
D. DFF
Schematics:





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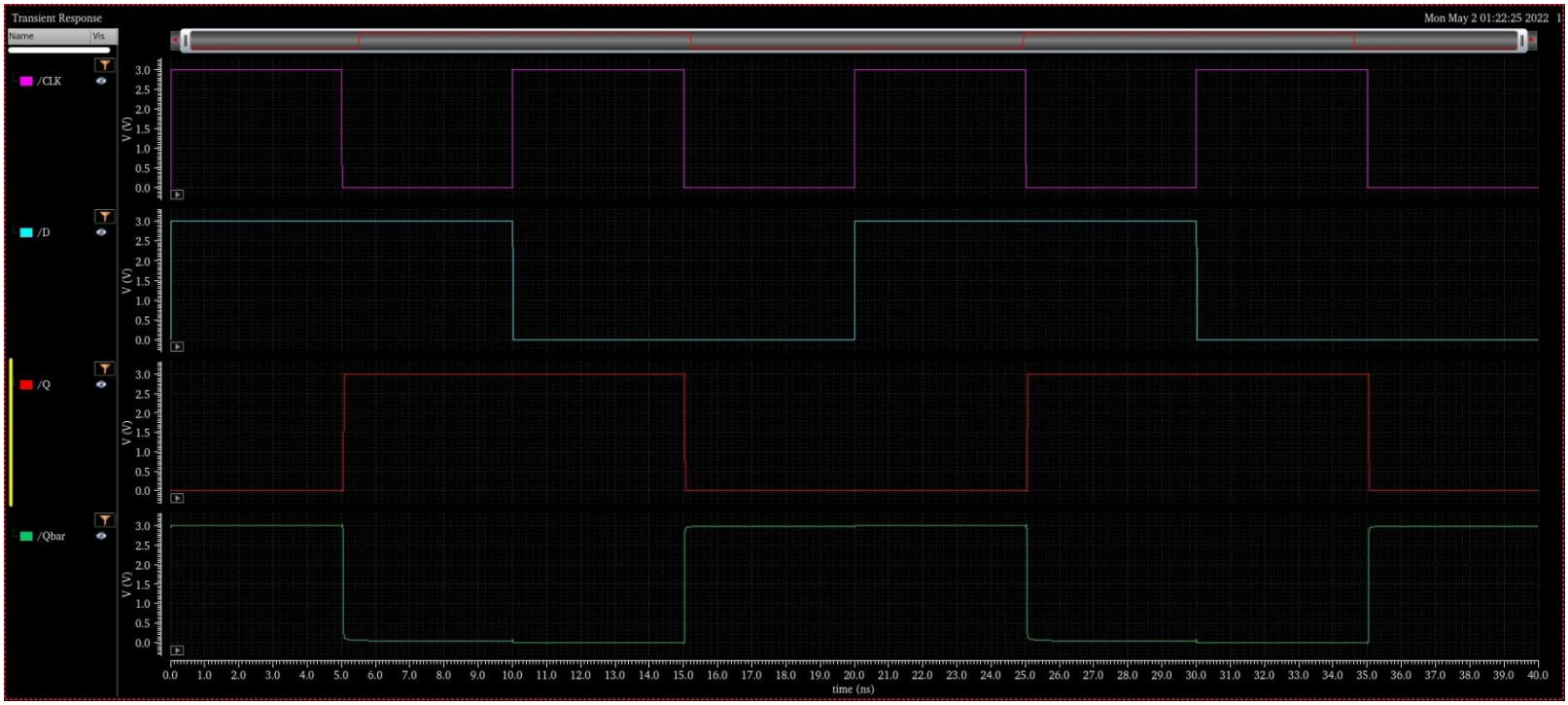
Transient Analysis:



Discussion:

Everything seems good. All created designs are working as expected. The only thing I may need to change or revise and test again would be incorporating an inverter within the tri-state inverter design.

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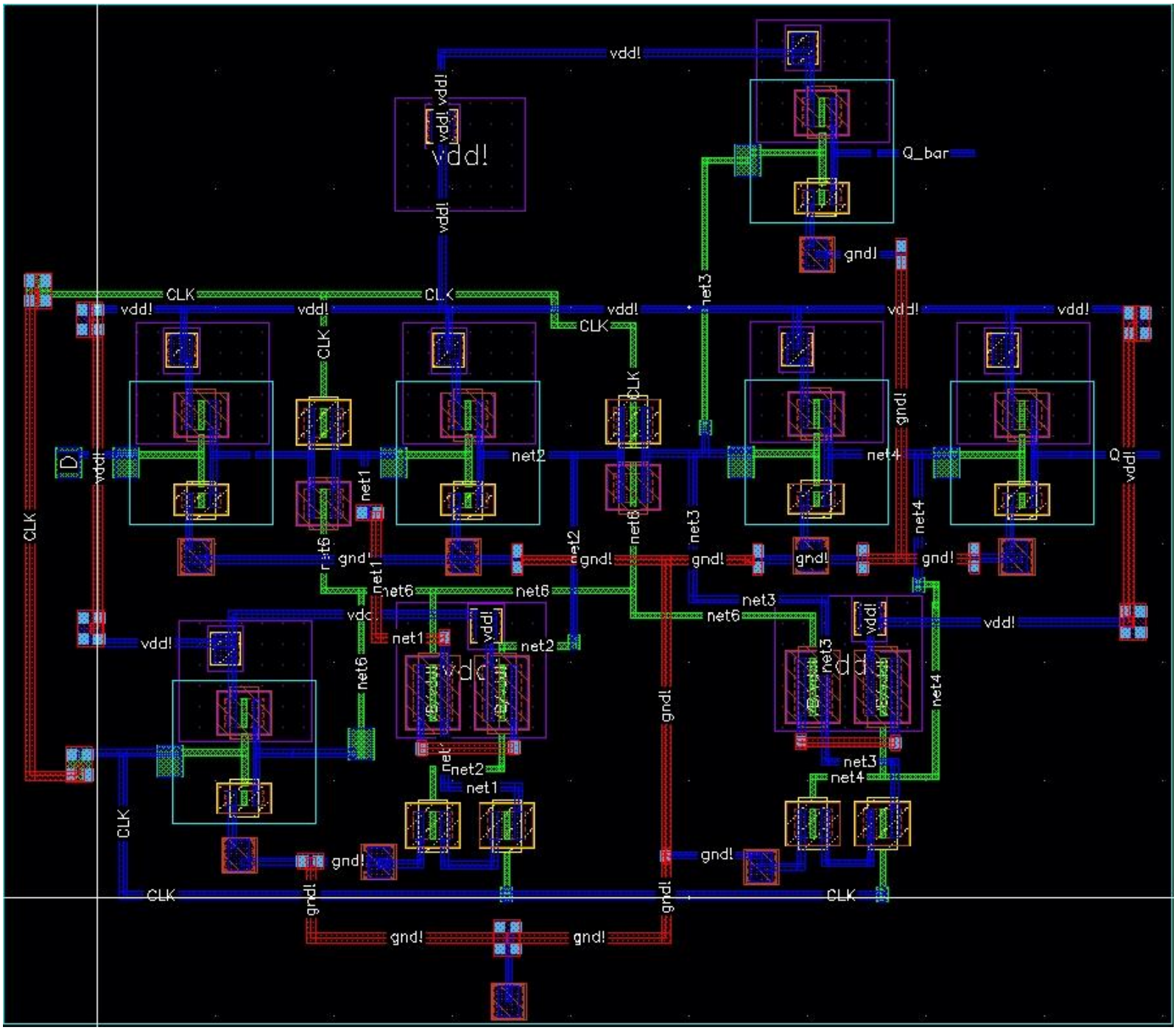
Part 2 – DFF Layout:

Design the layout of a D-Flip Flop and perform DRC, LVS checks on the layout. Conduct Post-Layout extraction and simulation procedures on the final layout.

DFF Layout:



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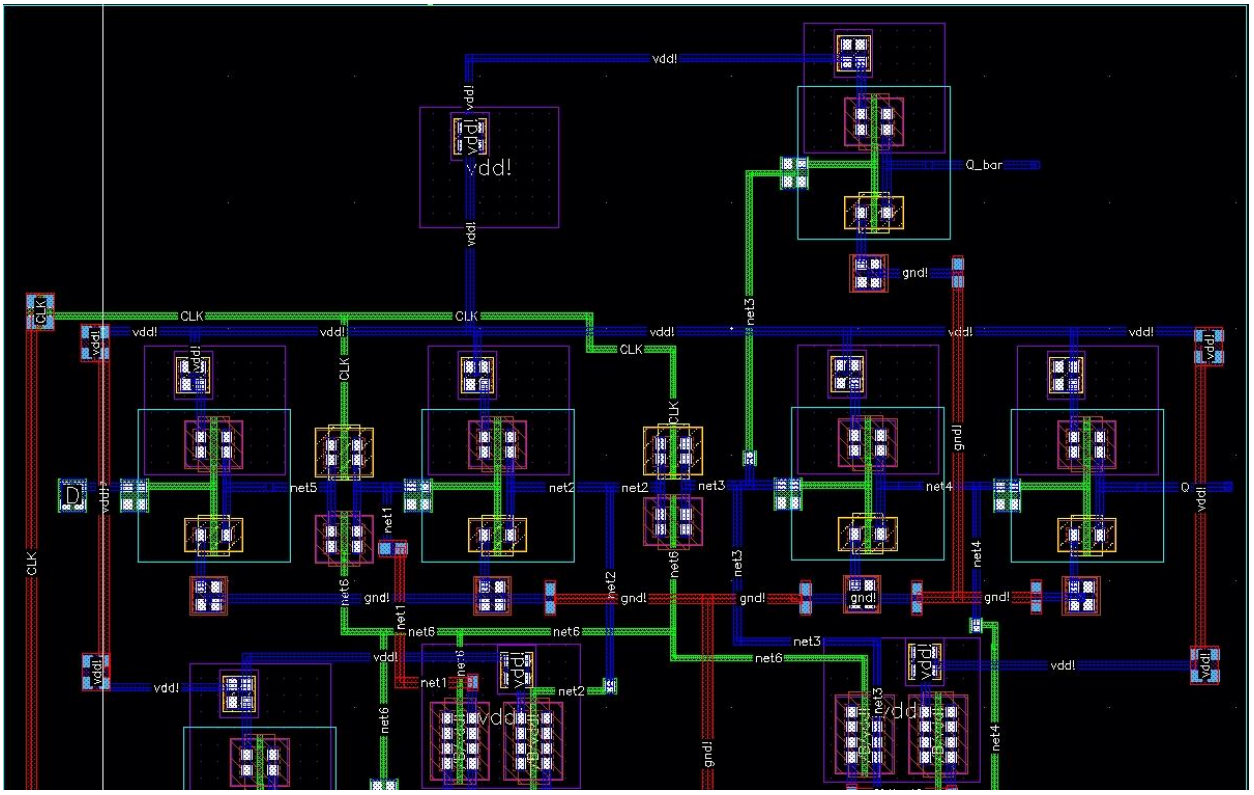

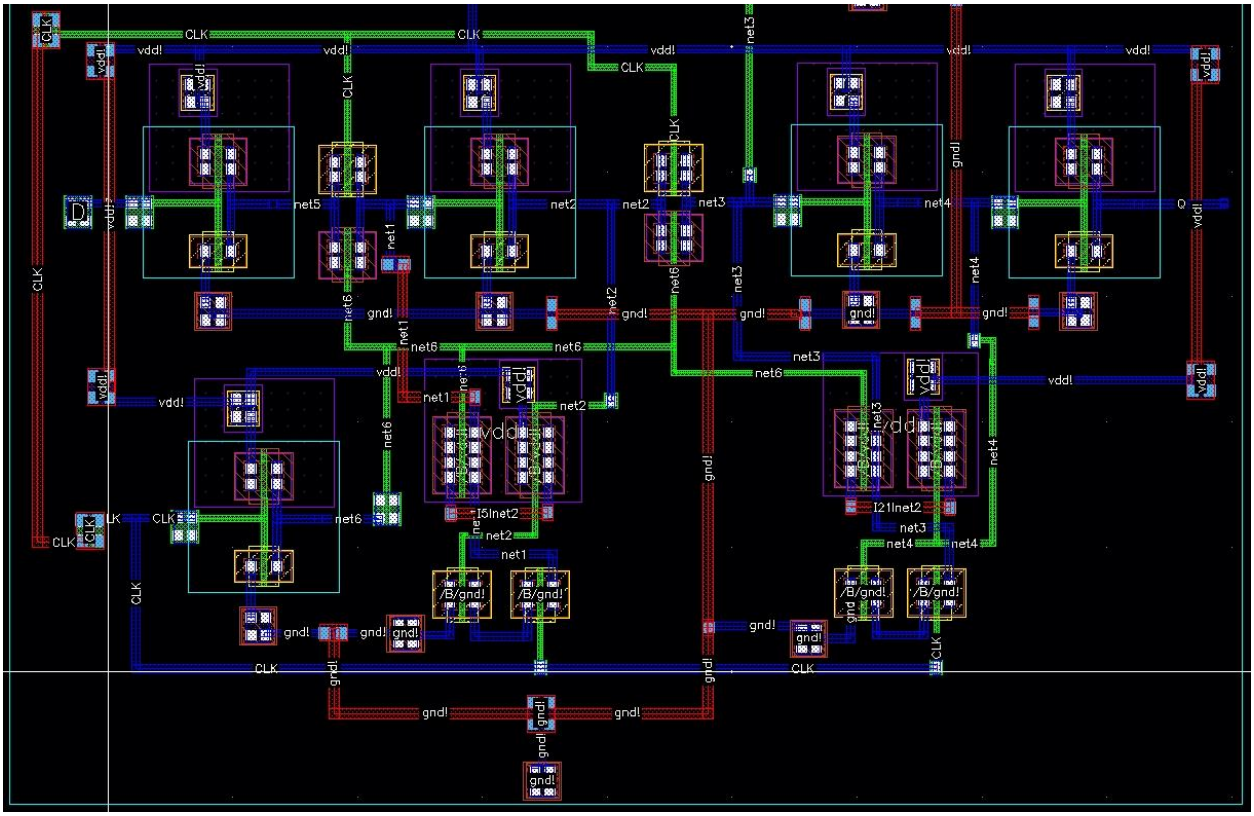

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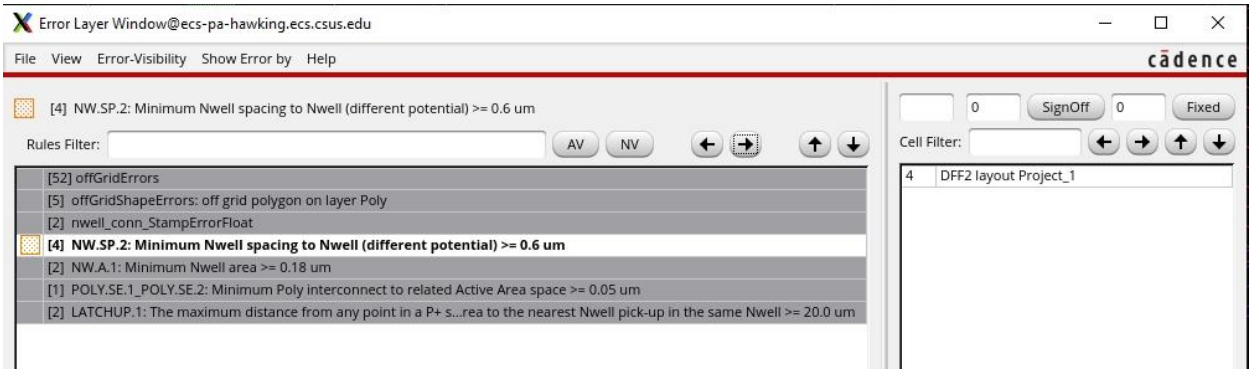
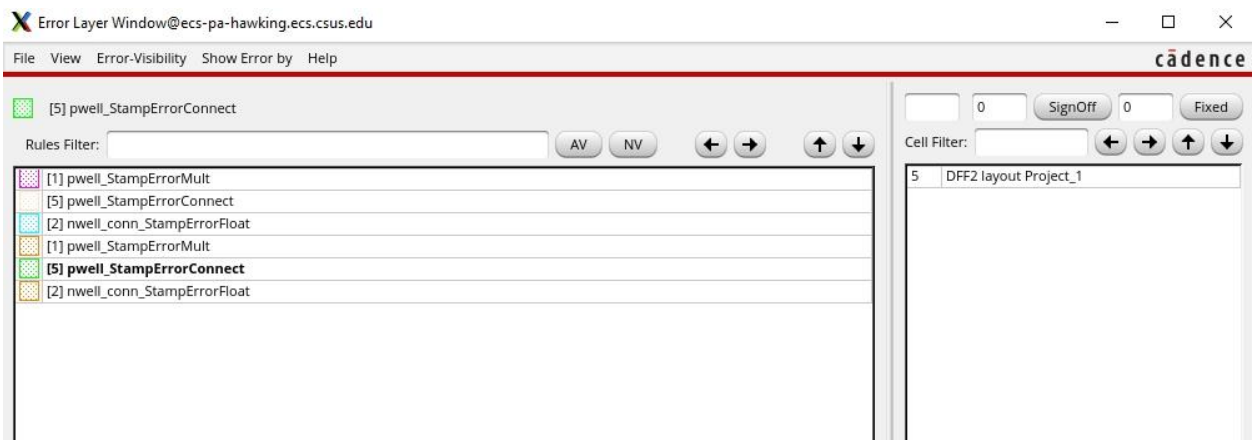
DRC and LVS checks:

I couldn’t get zero error for the DRC and LVS checks.





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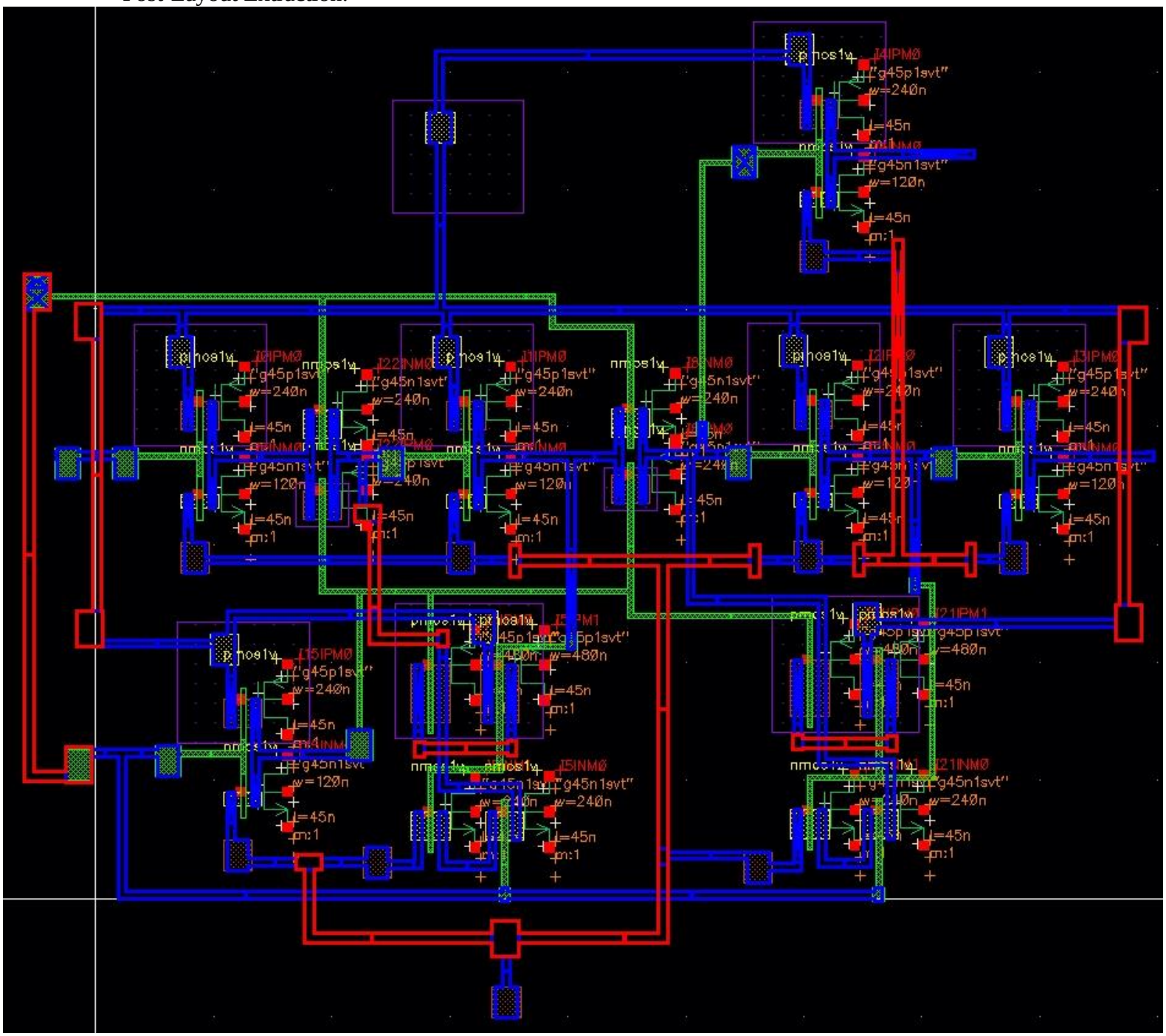
Post-Layout Extraction:



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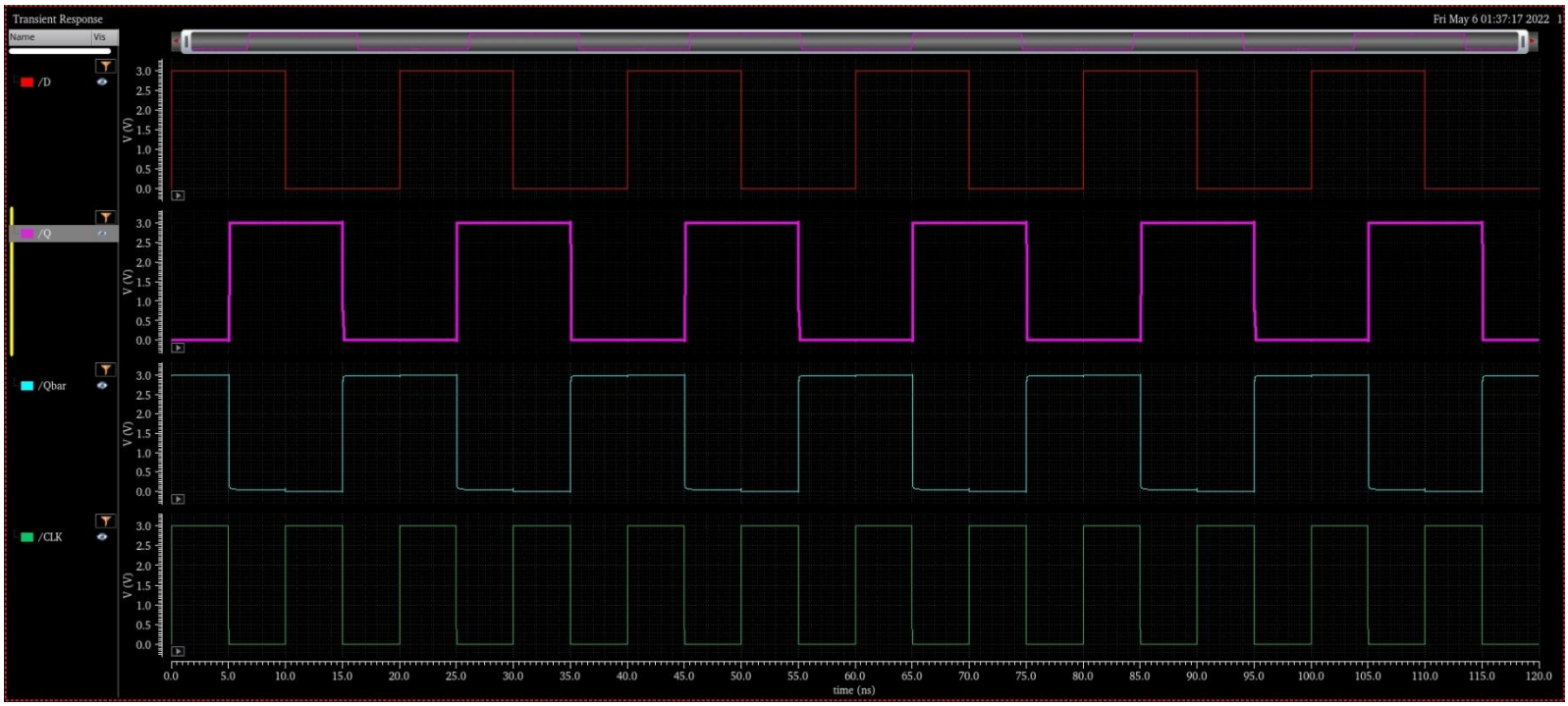
Simulation:



Discussion:

The DFF seems to be generating the desired results but without getting zero errors for the DRC and LVS check, I'm not too confident if everything is laid out correctly. If I were to re-do this project, I would re-do this tri-state inverter as stated earlier. Also, I should design and test all the layouts for the inverter, transmission gate, and tri-state inverter before redoing the DFF to ensure each circuit is performing correctly and generating the expected results. This may also make the DFF layout less complicated and allow me to place and connect each circuit in a more linear side-by-side connection to not look as messy and complicated in comparison to what I have designed and laid out so far.