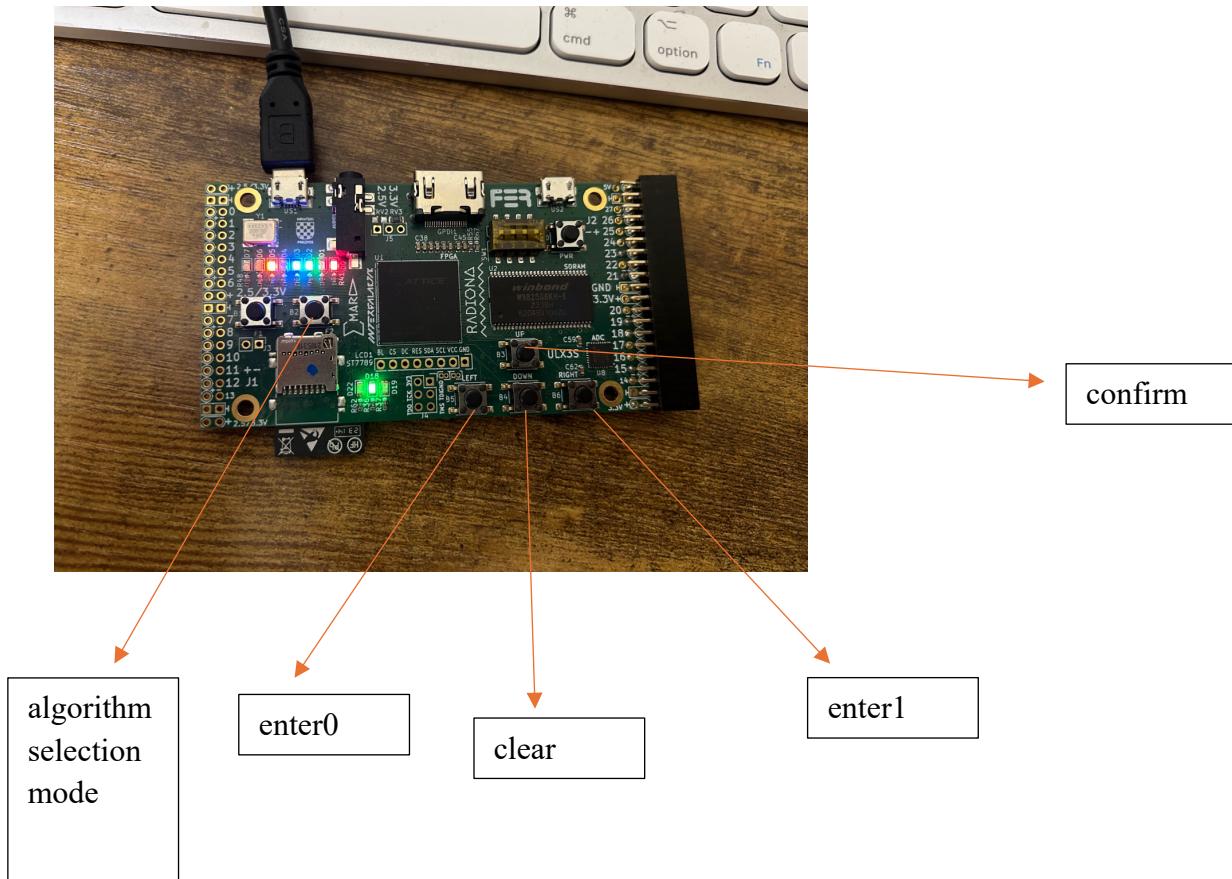
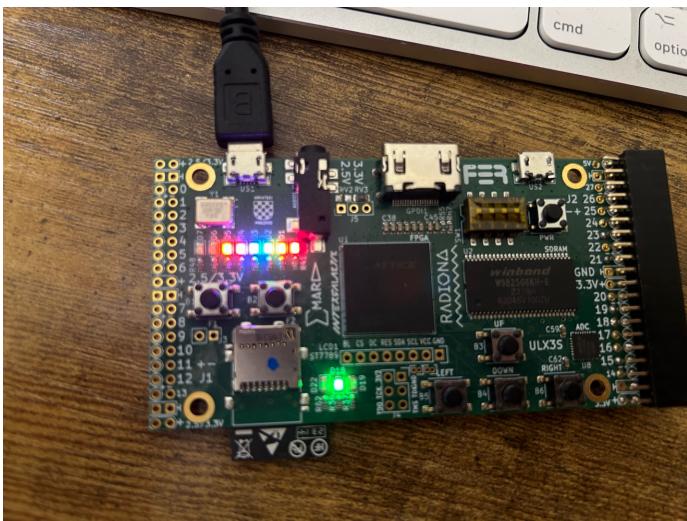


FPGA testing

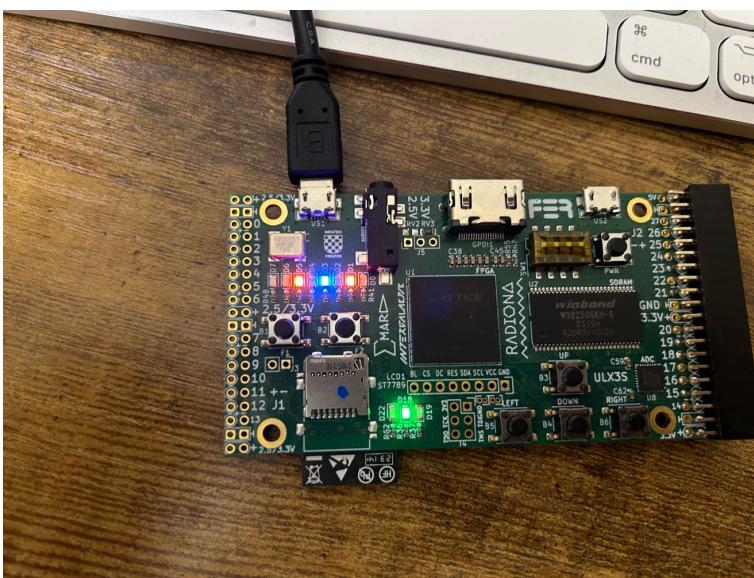
The initial state



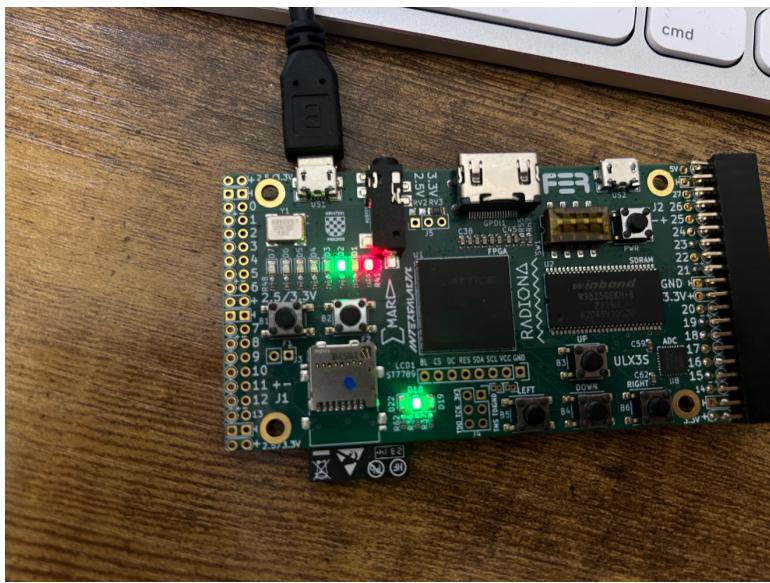
The lock is opened, in the PASS state. All LEDs are on



The password is wrong, the device is in the LOCK state.



The algorithm selection mode, the input algorithm ID is 3'd5(3'b101)



In addition, I used Timer on my phone to measure the time in the design.

To solve the Button Debounce issue, only button is pressed for more than 0.01s then it can be regarded as a valid press. All tests listed in the README are completed on the FPGA and no problem is found.