1. Description

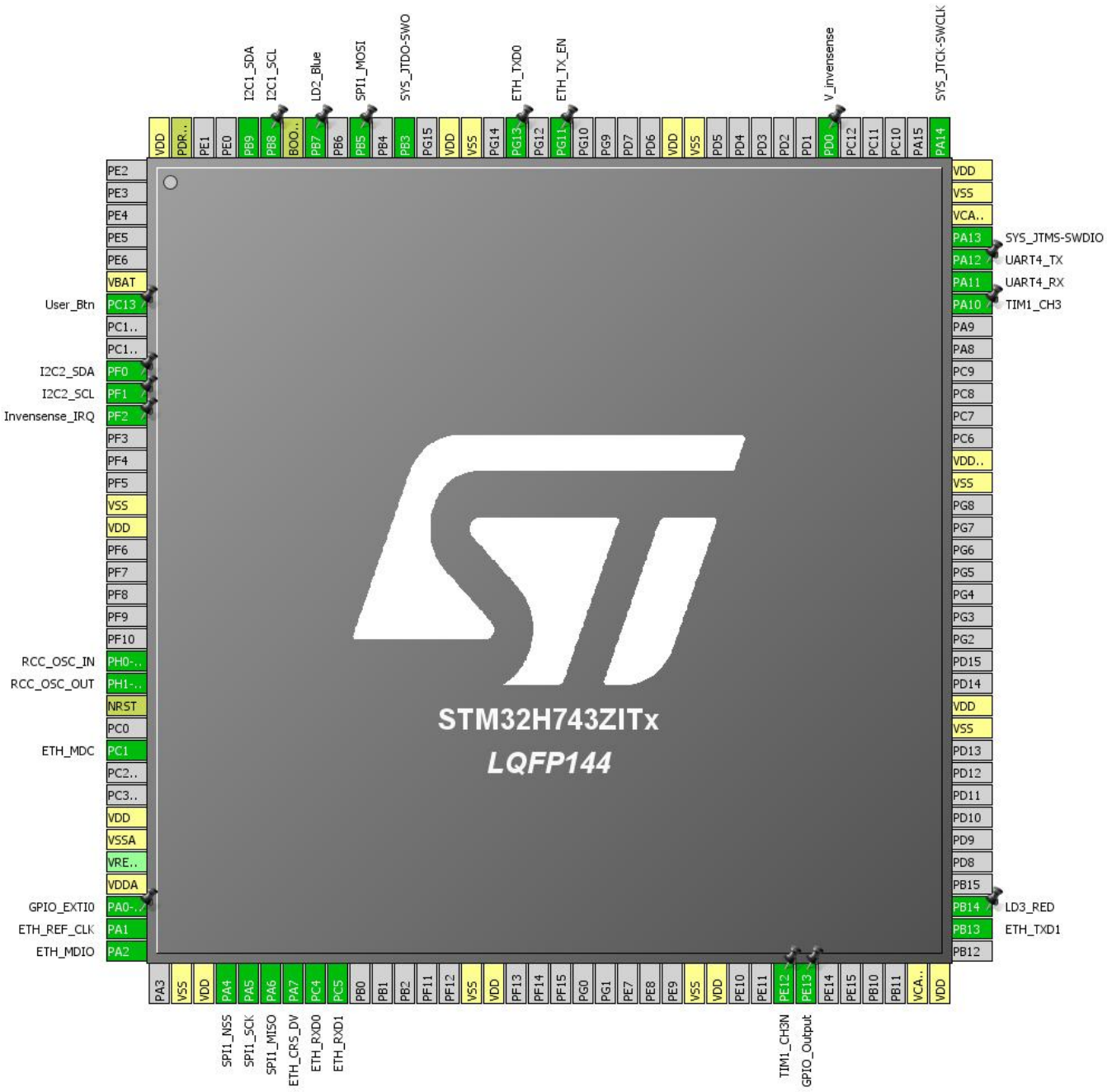
1.1. Project

Project Name	STCubeGenerated
Board Name	STCubeGenerated
Generated with:	STM32CubeMX 4.26.1
Date	09/03/2018

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



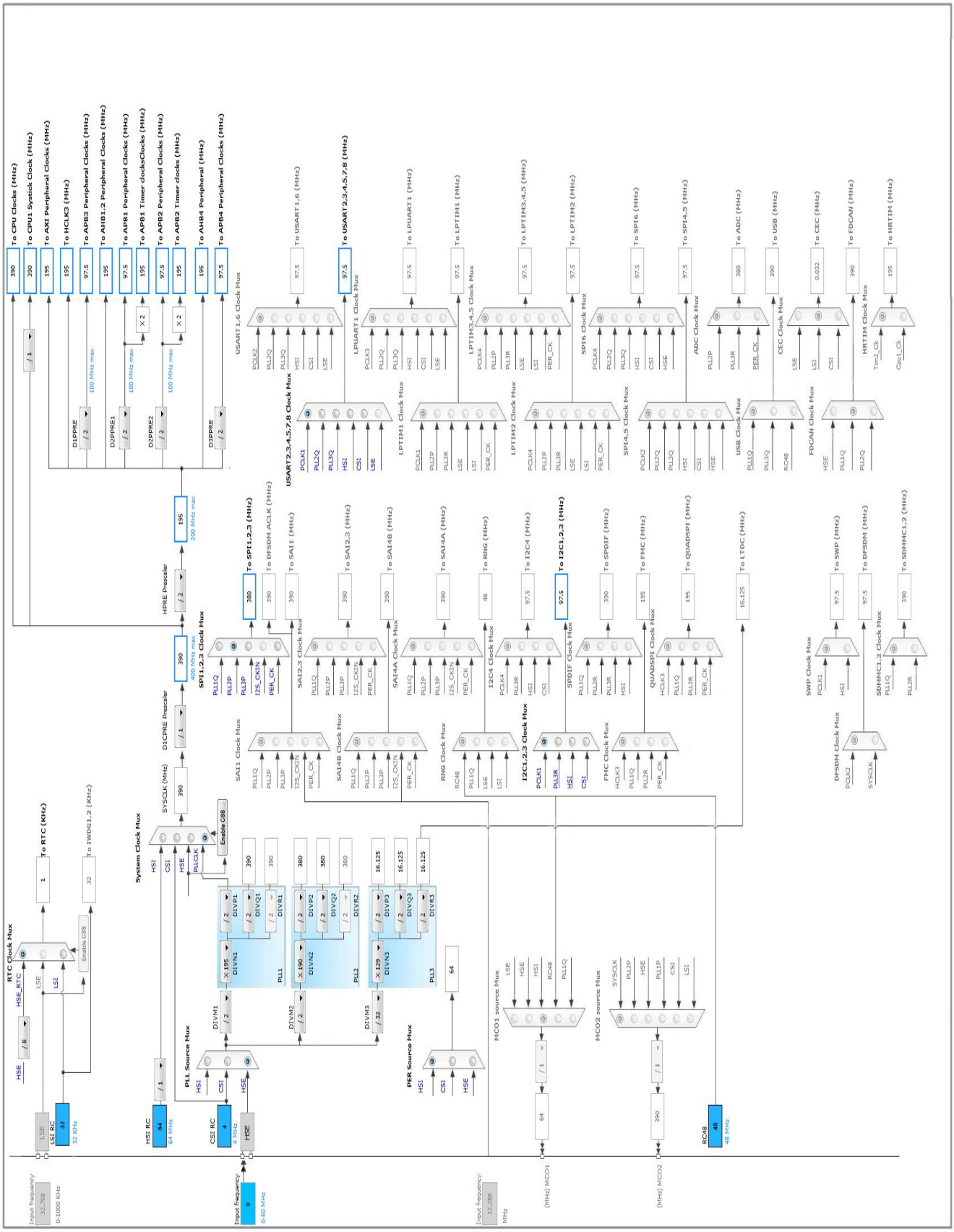
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	User_Btn
10	PF0	I/O	I2C2_SDA	
11	PF1	I/O	I2C2_SCL	
12	PF2	I/O	GPIO_EXTI2	Invensense_IRQ
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	GPIO_EXTI0	
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	SPI1_NSS	
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
65	PE12	I/O	TIM1_CH3N	
66	PE13 *	I/O	GPIO_Output	
71	VCAP1	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	
75	PB14 *	I/O	GPIO_Output	LD3_RED
83	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
84	VDD	Power		
94	VSS	Power		
95	VDD33_USB	Power		
102	PA10	I/O	TIM1_CH3	
103	PA11	I/O	UART4_RX	
104	PA12	I/O	UART4_TX	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
114	PD0 *	I/O	GPIO_Output	V_invensense
120	VSS	Power		
121	VDD	Power		
126	PG11	I/O	ETH_TX_EN	
128	PG13	I/O	ETH_TXD0	
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SYS_JTDO-SWO	
135	PB5	I/O	SPI1_MOSI	
137	PB7 *	I/O	GPIO_Output	LD2_Blue
138	BOOT0	Boot		
139	PB8	I/O	I2C1_SCL	
140	PB9	I/O	I2C1_SDA	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ETH

Mode: RMII

5.1.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30040060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Address	**0x30040200 ***
Rx Buffers Length	1524

5.2. I2C1

I2C: I2C

5.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x009033B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.3. I2C2

I2C: I2C

5.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x009033B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.4. RCC

High Speed Clock (HSE): BYPASS Clock Source

5.4.1. Parameter Settings:

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	16

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 4 and 8 MHz
PLL1 clock Output range	Wide VCO range

PLL2 clock Output range	Wide VCO range
PLL Fractional Part	0
PLL2 Fractional Part	0

5.5. RTC

mode: Activate Clock Source

mode: Activate Calendar

5.5.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	**99 ***
Synchronous Predivider value	**9999 ***

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	**Storeoperation Set ***

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

5.6. SPI1

Mode: Full-Duplex Slave

Hardware NSS Signal: Hardware NSS Input Signal

5.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Input Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

5.7. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM8

5.8. TIM1

Channel3: PWM Generation CH3 CH3N

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	

- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	**Enable ***
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	**3 ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

5.9. UART4

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**1000000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	**FIFO mode enable ***
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	**Enable ***
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA4	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
TIM1	PE12	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
UART4	PA11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	User_Btn
	PF2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	Invensense_IRQ
	PA0-WKUP	GPIO_EXTI0	**External Interrupt Mode with Rising/Falling edge**	**Pull-down ***	n/a	
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LD3_RED
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	V_invensense
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LD2_Blue

6.2. DMA configuration

DMA request	Stream	Direction	Priority
UART4_RX	DMA1_Stream4	Peripheral To Memory	**Medium ***
UART4_TX	DMA1_Stream5	Memory To Peripheral	**Medium ***
I2C1_RX	DMA2_Stream1	Peripheral To Memory	**Medium ***
I2C1_TX	DMA2_Stream0	Memory To Peripheral	**Medium ***
TIM1_CH3	DMA1_Stream0	Memory To Peripheral	**Very High ***
I2C2_RX	DMA1_Stream6	Peripheral To Memory	**Medium ***
I2C2_TX	DMA1_Stream7	Memory To Peripheral	**Medium ***
SPI1_RX	DMA1_Stream2	Peripheral To Memory	**High ***
SPI1_TX	DMA1_Stream3	Memory To Peripheral	**High ***

UART4_RX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_TX: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C1_RX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte

Memory Data Width:	Byte

I2C1_TX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

TIM1_CH3: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

I2C2_RX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C2_TX: DMA1_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_RX: DMA1_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

SPI1_TX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

6.3. BDMA configuration

nothing configured in DMA service

6.4. MDMA configuration

nothing configured in DMA service

6.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	14	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line0 interrupt	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream2 global interrupt	true	0	0
DMA1 stream3 global interrupt	true	0	0
DMA1 stream4 global interrupt	true	0	0
DMA1 stream5 global interrupt	true	0	0
DMA1 stream6 global interrupt	true	0	0
TIM1 break interrupt	true	2	0
TIM1 update interrupt	true	2	0
TIM1 trigger and commutation interrupts	true	2	0
TIM1 capture compare interrupt	true	2	0
I2C1 event interrupt	true	2	0
I2C1 error interrupt	true	2	0
I2C2 event interrupt	true	2	0
I2C2 error interrupt	true	2	0
SPI1 global interrupt	true	2	0
TIM8 update interrupt and TIM13 global interrupt	true	2	0
DMA1 stream7 global interrupt	true	2	0
UART4 global interrupt	true	2	0
DMA2 stream0 global interrupt	true	1	0
DMA2 stream1 global interrupt	true	1	0
Ethernet global interrupt	true	3	0
Ethernet wake-up interrupt through EXTI line 86	true	3	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line2 interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
HSEM1 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	030538_Rev1

7.2. Parameter Selection

Temperature	25
Vdd	3.0

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STCubeGenerated
Project Folder	E:\SVN\Project\USBL_ETH\RTE\Device\STM32H743ZITx\STCubeGenerated
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_H7 V1.3.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report