Lab Report 3
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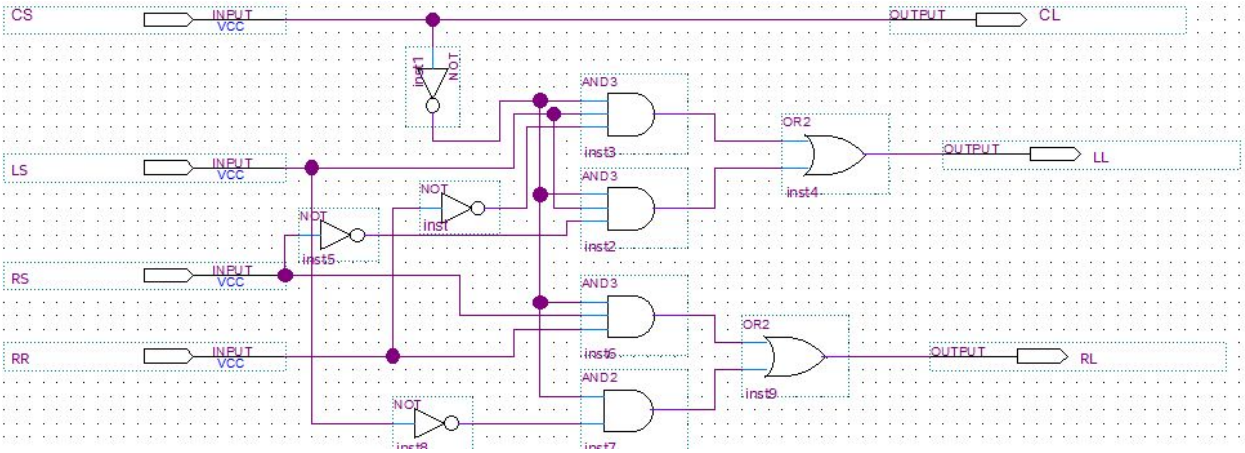
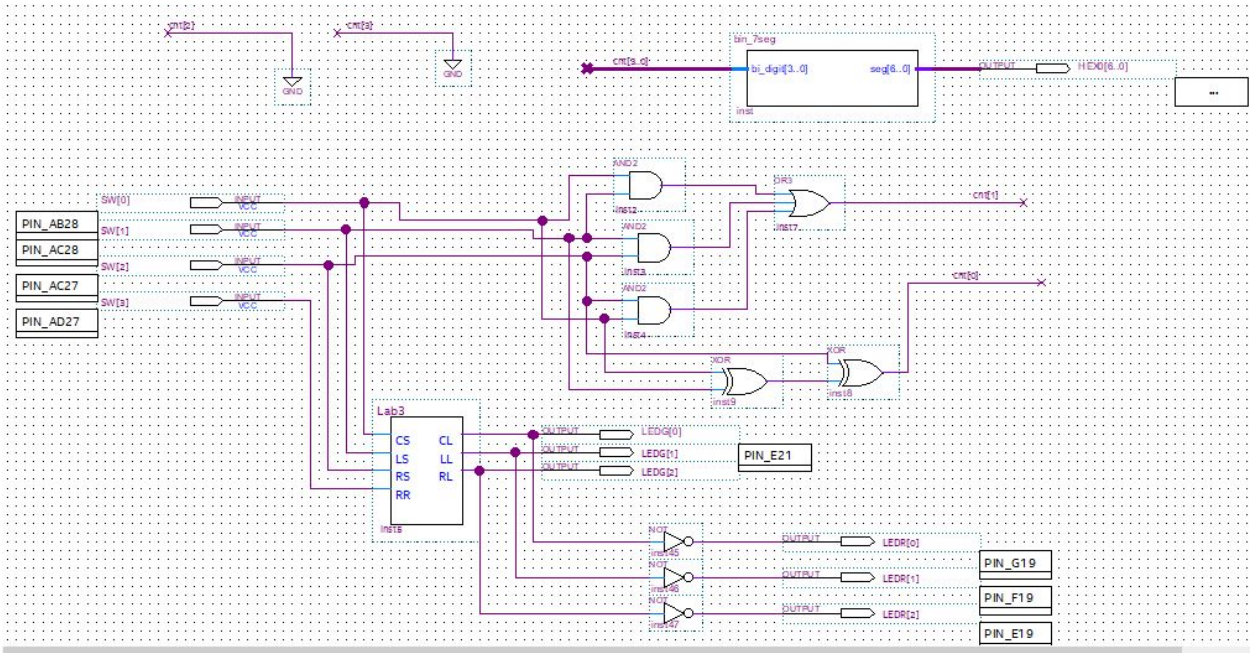
Introduction:
In this lab, we simulated how traffic signals would work using logic gates and on the DE2115 board. First, we designed the circuit in Quartus. We first designed an SOP logic circuit that would control the lights. Later, we minimized into its own gate to simplify the whole circuit. We also made a 7 segment block that would control the counter on the board, which represents how many cars are waiting. In the end, you should have red lights and green lights turning on in each situation and a counter that has a max value of 3.

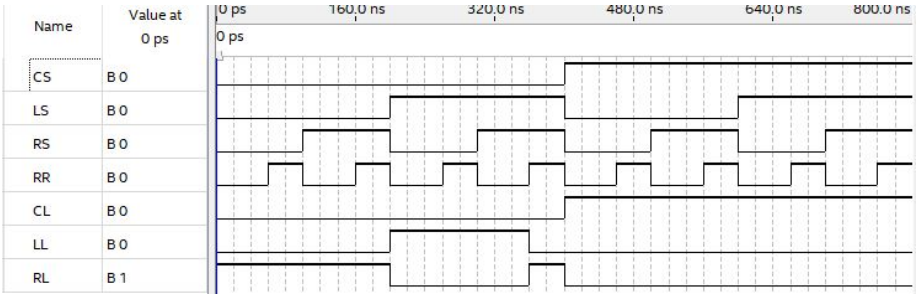
Schematic of switches (input) and Lights (output)



Schematic with simplified circuit from above and 7 segment display



Simulation Results



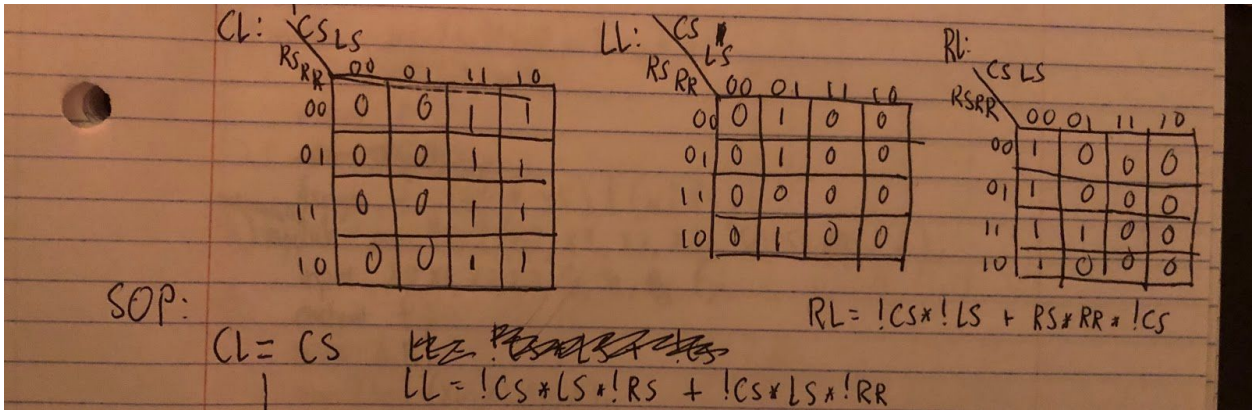
Pin Assignments

	tatu	From	To	Assignment Name	Value	Enabled	Entity
1	✓		SW[1]	Location	PIN_AC28	Yes	
2	✓		SW[2]	Location	PIN_AC27	Yes	
3	✓		SW[3]	Location	PIN_AD27	Yes	
4	✓		SW[0]	Location	PIN_AB28	Yes	
5	✓		LEDR[0]	Location	PIN_G19	Yes	
6	✓		LEDR[1]	Location	PIN_F19	Yes	
7	✓		LEDR[2]	Location	PIN_E19	Yes	
8	✓		HEX0[0]	Location	PIN_G18	Yes	
9	✓		HEX0[1]	Location	PIN_F22	Yes	
10	✓		HEX0[2]	Location	PIN_E17	Yes	
11	✓		HEX0[3]	Location	PIN_L26	Yes	
12	✓		HEX0[4]	Location	PIN_L25	Yes	
13	✓		HEX0[5]	Location	PIN_J22	Yes	
14	✓		HEX0[6]	Location	PIN_H22	Yes	
15	✓		LEDG[0]	Location	PIN_E21	Yes	
16	?		*LEDG[1]	Location	PIN_E22	Yes	
17	?		*LEDG[2]	Location	PIN_E25	Yes	

Simulation Design:

When designing the circuit, we both built our circuits individually so that we could both learn everything about this lab. Also, if one of us makes a mistake, it would be easy to address the problem. One of our designs actually had an error during our attempt. There was an extra line connecting all of the inputs to each other, which completely messed up the outputs. Once we deleted the line, both designs worked. I think that this strategy is extremely effective because it gives us an opportunity to check to make sure both of us are going down the right path. If one of us makes a mistake, it would be easy to find the error because we can just simply compare the two circuits. In the end, it would be the same as both of us working on one circuit because we are still communicating, asking questions, and cooperating.

K-Maps:



We chose these mainly because we did not get any points off from the pre-lab based on these equations.

FPGA Testing:
When we first loaded the circuit onto the FPGA, we realized that we had the green and red lights reversed. There were two green lights on and one red light on when we wanted the reverse. To fix this, we simply switched the positions of all LEDG and LEDR in the “Schematic with simplified circuit from above and 7 segment display”. The simulation did not show compensate for this detail because we only had the outputs labeled as “Center Light” and assumed that it handled both green and red lights. In reality, green lights and red lights are two separate LEDs.

Advantages and disadvantages of different implementation methodologies:
For us, we implemented our circuit to be as simple as possible to create and read. Specifically when choosing how to implement our light circuit. We chose to use the sum of products equation and did not overly simplify the equation which would have made it more difficult to read and understand. While doing this may have required us to use more gates and wires, we thought that it’d be better to keep the schematic easiest to read as possible.

Any problems with the circuit that required correction and a new download?
For us, we did not observe any major problems that required a major correction or new download. The majority of the work that we put into this lab was just trying to figure out how to accomplish what we wanted to do in Quartas.

Conclusion:
The primary takeaway from this lab for us is how to create higher level circuits that can use the other circuits that we created. In this lab, we created the schematic that we made in the pre-lab and then created a higher level circuit that utilized that circuit and combined it with the seven segment display.