Konstantin Okunev

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Professional Summary

Hardware-focused Software Engineer with 15+ years of experience in **FPGA design, verification, embedded systems, and electronic board bring-up**. Proven track record in **diagnostics, test systems, and production support** across leading semiconductor companies. Skilled at bridging hardware and software domains to deliver high-performance, cost-efficient solutions.

Core Skills

Programming & Scripting: C++, Python, TCL
FPGA & Hardware: SystemVerilog, RTL design, Quartus, ModelSim, FPGA validation
Tools & Platforms: Logic/protocol analyzers, oscilloscopes, MSVS, Windows environment
Domains: Digital design verification, embedded systems, board design & bring-up

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Professional Experience

Intel Corporation – San Jose, CA

Software Engineer | Dec 2015 – Present

- Designed and implemented **diagnostics subsystems** for HDMT Gen3 tester instruments (HECC, HECC Cal, BP MTB), optimizing test coverage and improving reliability.
- Developed unit tests and integrated diagnostics software into production toolchain, ensuring system-level quality validation.
- Supported HDMT Gen2 tester in production; implemented enhancements for HPCCx instruments, reducing debug turnaround time.
- Debugged and resolved high-priority field issues, maintaining uptime and improving customer satisfaction.

- Contributed as FPGA designer/verification engineer for **HDBI tester** platform:
    - Designed and verified RTL code for custom IP modules on **Arria 10** and **Stratix 10** FPGAs.
    - Delivered test instruction processing and event engine modules, enabling successful rollout into production.

Altera Corporation – San Jose, CA

Member of Technical Staff, Test Engineer | Nov 2006 – Dec 2015

- Key contributor to **ATS7 proprietary IC tester**, digital subsystems (backend processor, bridge board, DUT data processor).
- Authored **functional/device specifications** and board schematics for backend and bridge board subsystems.
- Designed and debugged FPGA configurations for **Stratix II, III, Cyclone III** platforms.
- Developed RTL simulation testbenches, improving design validation coverage.
- Led software development for ATS7 upgrade: partitioned tester into subtesters, delivering **significant test cost savings**.
- Ported tester software from 32-bit to 64-bit Windows, extending tool lifecycle.
- Provided ongoing debug and production support across multiple product lines.

Guzik Technical Corporation – Mountain View, CA

Software Engineer | Sep 2001 – Nov 2006

- Developed and deployed software for **Signal Generator module** in the ReadWrite Analyzer platform, enhancing test capability for storage devices.
- Contributed to FPGA design and RTL simulation, ensuring robust system integration.
- Built application-level media test modules (Media Scan, PRML Error), expanding test coverage for disk drive analysis.

Education

Master of Science in Applied Mathematics
Novosibirsk State University – Novosibirsk, Russia