```
ADC AVR
                  Χ
                              Timers
                                  Ε
                                           Μ
              K
                       K
                                                          \Delta
                                 , el 21045
                                                  Μ
                                                                  , el 21170
                                    29 O
                                                2024
0.1 Z
           3.1
\sum
                                                               duty cycle
                          cseg
DC_VALUE. \Theta
                                        PORTD
                                                                        TCCR1A, TCCR1B
                     PORTB
                        Fast PWM, 8 bit, non-inverting output
       TMR1A
                                                              N = 256,
                                                                            BOTTOM = 0
  TOP = 0x00ff = 255. \Gamma
                                             PD3, PD4
                                                                        PCINT19 (PD3)
PCINT20 (PD4)
                         PCMSK2,
                                             o Pin Change Interrupt 2
                                                                         PCICR. A
                                               duty cycle 50%)
 i
           6 (
                           6
                                                                          \mathbf{Z}
                                                                                      i-
                                       ,
                                                                       . \Sigma
                       . T
                                              Ζ
  duty cycle
                                                                          . H
                                                          10 \mathrm{ms}
                               PD3
                                      PD4. E
     pc2isr
                   PIND
                                                   PD3, PD4
                                                                           . \Sigma
                                                                                      PD3
cur_PIND AND (NOT prev_PIND)
                                           bit
                                                 PIND
                                                                 1
                                                                           0. A
                                       \mathbf{Z}
                                            1
                                                                         PD4
                                 i
                     i
                           Ζ
                                1
; Ex3_1.asm
; Created: 10/25/2024 5:06:29 PM
; Author : User
.include "m328PBdef.inc"
org 0x0
     rjmp reset
.org 0xA
     rjmp pc2isr
.def temp = r16
.def DC VALUE = r17
.def DC_INC = r18; DC_INC = 1 -> DC_VALUE increasing, DC_INC = 0 -> DC_VALUE

→ decreasing

.def i = r19
.def prev_PIND = r20
.def cur\_PIND = r21
```

6

10

11 12

13

14 15

16

17

18

19

20

21 22

```
DUTY: .DB 5, 26, 46, 66, 87, 107, 128, 148, 168, 189, 209, 230, 250; 255*(2+8k)/100, k = 0 \dots 12.
    \rightarrow Initial k = 6.
   .equ DUTY LAST = 12
24
   .equ DUTY_START = 6
25
   pc2isr:
          push temp
28
         in temp, SREG
29
         push temp
30
         in cur_PIND, PIND
                                           ; Get the current set PIND bits
31
         mov temp, prev_PIND
32
         com temp
                                            ; Get the previous clear PIND bits
33
                                            ; Get the 1 bit that was just set and caused the PCINT2
         and temp, cur_PIND
34

    interrupt

                                         ; Skip next instruction if PD3 was not pressed
         sbrc temp, 3
35
         rjmp increase
36
         sbrc temp, 4
                                         ; Skip next instruction if PD4 was not pressed
37
         rjmp decrease
38
         rjmp end
   increase:
40
         cpi i, DUTY_LAST
41
         breq end
42
         inc i
43
         adiw Z, 1
         rjmp end
45
   decrease:
         cpi i, 0
         breq end
48
         dec i
49
         sbiw Z, 1
50
   end:
51
         mov prev_PIND, cur_PIND
          pop temp
53
          out SREG, temp
54
         pop temp
55
         rjmp reset
56
57
   reset:
58
          ; Init stack pointer
         ldi temp, high(RAMEND)
          out SPH, temp
61
         ldi temp, low(RAMEND)
62
         out SPL, temp
63
64
         ; Set PORTB as output
65
         ser temp
          out DDRB, temp
67
68
          ; Set PORTD as input
69
          clr temp
70
         out DDRD, temp
71
```

```
72
          ; Fast PWM, 8 bit, non-inverting output, N = 256. BOTTOM = 0, TOP = 0 \times 000ff = 255
73
          ldi temp, (1<<WGM10) | (1<<COM1A1)
74
          sts TCCR1A, temp
75
          ldi temp, (1<<WGM12) | (1<<CS12)
          sts TCCR1B, temp
78
          ; Enable PCINT19 (PD3), PCINT20 (PD4) interrupts
79
          ldi temp, (1<<PCINT19) | (1<<PCINT20)
80
          sts PCMSK2, temp
82
          ; Enable Pin Change Interrupt 2: PCINT[23:16]
          ldi temp, (1 << PCIE2)
          sts PCICR, temp
85
86
          ; Set previous state of PIND = 0
87
          ldi prev_PIND, 0
89
          ; Initialize i to duty cycle starting position: 6 (50%)
          ldi i, DUTY_START
91
92
          ; Load the starting address of the duty cycle value into Z
93
          LDI ZH, HIGH(2*DUTY+DUTY_START)
94
          LDI ZL, LOW(2*DUTY+DUTY_START)
          sei
    ; Replace with your application code
99
100
          lpm DC_VALUE, Z
101
          sts OCR1AL, DC_VALUE
102
103
          ldi r24, LOW(10*16)
104
          ldi r25, HIGH(10*16)
                                     ; Set delay (10ms * 16)
105
          rcall delay_mS
                                           ; Delay for 10ms
106
107
          rjmp start
108
109
    ; delay of 1000*F1+6 cycles (almost equal to 1000*F1 cycles)
    delay mS:
    ; total delay of next 4 instruction group = 1+(249*4-1) = 996 cycles
112
          ldi r23, 249
                                       ; (1 cycle)
113
    loop inn:
114
                                               ; 1 cycle
          dec r23
115
                                                  ; 1 cycle
          nop
          brne loop_inn
                                          ; 1 or 2 cycles
118
          sbiw r24, 1
                                             ; 2 cycles
119
          brne delay_mS
                                           ; 1 or 2 cycles
120
121
          ret
                                                 ; 4 cycles
122
```

- 0.2 Z 3.2
- 0.3 Z 3.3