1. Source code directory structure

TOP LEVEL GSENSE400BSI_top

SECOND LEVEL

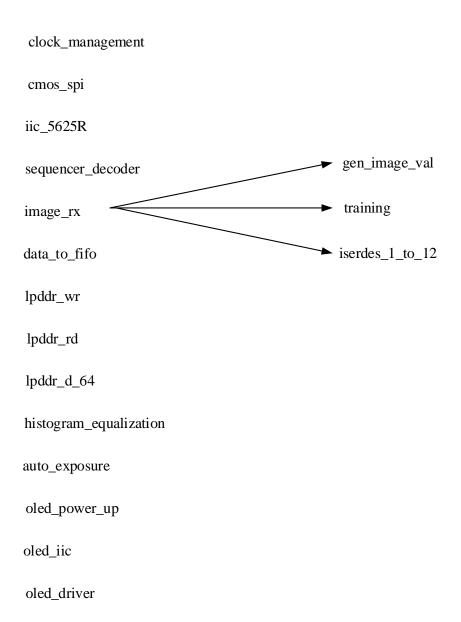


Fig.1 Source code module hierarchy

Figure 1 shows the source code module hierarchy. The entire top-level module is divided into 14 sub-modules, which are clock_management, cmos_spi, iic_5625R, sequencer_decoder, image_rx, data_to_fifo, lpddr_wr, lpddr_rd, lpddr_d_64, histogram_equalization, auto_exposure, oled_power_up, oled_iic and oled_driver. Each module function is described below.

clock_management: Complete each module clock management cmos spi: Complete CMOS image sensor SPI configuration for configuring sensor

operating mode, PGA, etc.

iic 5625: Power-on timing of the sensor through the IIC configuration AD5625

sequencer decoder: Control sensor on-chip AD decoding and exposure time

image rx: Decode and train received digital images

gen image val: Generate image sync signal

training: Image training module, including bit training, word training and channel training

iserdes 1 to 12: 1-12 serial to parallel conversion module

data_to_fifo: Complete image stitching

lpddr_wr: LPDDR write buffer lpddr rd: LPDDR read buffer

lpddr_d_64: MIG core provided by xilinx

auto_exposure: Automatic exposure control based on luminance mean and histogram distribution

histogram_equalization: Implementation of adaptive platform histogram equalization algorithm

oled power up: Complete OLED power-on sequencing

oled iic: Complete OLED register configuration

oled driver: Complete OLED drive timing

2. Compiler version

ISE 14.7

3. How to start the work

Power-on self-starting through a FLASH of S25FL256SAGNFI001