Use Vivado to Build an Embedded System

CECS 461: Hardware and Software Co-design

Spring 2021

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1. After which step we finished building the hardware platform for the embedded system?

We finished building the hardware platform in step 3. Specifically, after step 3-1-5 in which we launch SDK and click ok.

2. Briefly describe the major components in the hardware platform.

In the ZYNQ7 Processing System, there are two major components that are used. One is memory DDR, which is used to store and compute data. Second is UART, which is used to transmit and receive data.

3. What is the top-level description file for hardware platform in SDK? Copy the contents in this file that support the answer you provide in the previous question.

The top-level description file is system.hdf.

Design Information

Target FPGA Device:	7z010
Part:	xc7z010clg400-1
Created With:	Vivado 2018.3
Created On:	Fri Feb 5 13:56:50 2021

Address Map for processor ps7_cortexa9_[0-1]

Cell	Base Addr	High Addr	Slave I/f	Mem/Reg
ps7_xadc_0	0xf8007100	0xf8007120		REGISTER
ps7_uart_1	0xe0001000	0xe0001fff		REGISTER
ps7_slcr_0	0xf8000000	0xf8000fff		REGISTER
ps7_scuwdt_0	0xf8f00620	0xf8f006ff		REGISTER
ps7_scutimer_0	0xf8f00600	0xf8f0061f		REGISTER
ps7_scugic_0	0xf8f00100	0xf8f001ff		REGISTER
ps7_scuc_0	0xf8f00000	0xf8f000fc		REGISTER
ps7_ram_1	0xffff0000	0xffffffdff		MEMORY
ps7_ram_0	0x00000000	0x0002ffff		MEMORY
ps7_pmu_0	0xf8893000	0xf8893fff		REGISTER
ps7_pl310_0	0xf8f02000	0xf8f02fff		REGISTER
ps7_ocmc_0	0xf800c000	0xf800cfff		REGISTER
ps7_l2cachec_0	0xf8f02000	0xf8f02fff		REGISTER
ps7_iop_bus_config_0	0xe0200000	0xe0200fff		REGISTER
ps7_intc_dist_0	0xf8f01000	0xf8f01fff		REGISTER
ps7_gpv_0	0xf8900000	0xf89fffff		REGISTER
ps7_globaltimer_0	0xf8f00200	0xf8f002ff		REGISTER
ps7_dma_s	0xf8003000	0xf8003fff		REGISTER
ps7_dma_ns	0xf8004000	0xf8004fff		REGISTER
ps7_dev_cfg_0	0xf8007000	0xf80070ff		REGISTER
ps7_ddrc_0	0xf8006000	0xf8006fff		REGISTER
ps7_ddr_0	0x00100000	0x3fffffff		MEMORY
ps7_coresight_comp_0	0xf8800000	0xf88fffff		REGISTER
ps7_afi_3	0xf800b000	0xf800bfff		REGISTER
ps7_afi_2	0xf800a000	0xf800afff		REGISTER
ps7_afi_1	0xf8009000	0xf8009fff		REGISTER
ps7_afi_0	0xf8008000	0xf8008fff		REGISTER

IP blocks present in the design

ps7_intc_dist_0	ps7_intc_dist	1.00.a
ps7_scutimer_0	ps7_scutimer	1.00.a
ps7_slcr_0	ps7_slcr	1.00.a
ps7_scuwdt_0	ps7_scuwdt	1.00.a
ps7_l2cachec_0	ps7_l2cachec	1.00.a
ps7_scuc_0	ps7_scuc	1.00.a
ps7_pmu_0	ps7_pmu	1.00.a
ps7_afi_1	ps7_afi	1.00.a
ps7_afi_0	ps7_afi	1.00.a
ps7_afi_3	ps7_afi	1.00.a
ps7_axi_interconnect_0	ps7_axi_interconnect	1.00.a
ps7_globaltimer_0	ps7_globaltimer	1.00.a
ps7_afi_2	ps7_afi	1.00.a
ps7_dma_s	ps7_dma	1.00.a
ps7_xadc_0	ps7_xadc	1.00.a
ps7_iop_bus_config_0	ps7_iop_bus_config	1.00.a
ps7_ddr_0	ps7_ddr	1.00.a
ps7_pl310_0	ps7_pl310	1.00.a
ps7_ddrc_0	ps7_ddrc	1.00.a
ps7_ocmc_0	ps7_ocmc	1.00.a
ps7_uart_1	ps7_uart	1.00.a
ps7_coresight_comp_0	ps7_coresight_comp	1.00.a
ps7_cortexa9_1	ps7_cortexa9	5.2
ps7_scugic_0	ps7_scugic	1.00.a
processing_system7_0	processing_system7	5.5
ps7_cortexa9_0	ps7_cortexa9	5.2
ps7_clockc_0	ps7_clockc	1.00.a
ps7_dev_cfg_0	ps7_dev_cfg	1.00.a
ps7_dma_ns	ps7_dma	1.00.a
ps7_gpv_0	ps7_gpv	1.00.a
ps7_ram_1	ps7_ram	1.00.a
ps7_ram_0	ps7_ram	1.00.a

4. What does a bit stream file do? Is there a bit stream file generated for the hardware platform we built in this lab?

The bit stream file is used to design and configure an FPGA, but no bit stream file was generated in this lab.

5. What is the step that transitions our design from hardware platform to software platform? What are the tools used for hardware design and software design respectively? What information are passed from hardware design tool to software design tool?

The export hardware step is when the transition from hardware to software platform occurs. The tool used for hardware design is Vivado and IP integrator, while for software design, it is Xilinx SDK. All the information regarding the specific hardware components which are used is sent to Xilinx SDK.

6. How many projects are created for building the software platform? Briefly describe the key design information provided in each one of them and the role each one of them play in the software platform.

Three total projects are created for building the software platform. One was "design_1_wrapper_hw_platform_0," which initializes the PS as part of the first stage bootloader. Second was "mem_test," which is the application that is used to verify the functionality of the design. Third was "mem_test_bsp," which is used to store drivers and libraries that form the lowest layer of application software stack.

7. What is a BSP? What information does it provide and what role does it play in building the software platform?

As described previously, Board Support Package (BSP) is collection of libraries and drivers that form the lowest layer of application software. The software application runs on top of a given software platform using APIs, so a BSP must be created to be able to create, use, and run software application.

8. What is the top-level description file for software platform in SDK? Briefly describe the key information in this file and support your answer by copying the related contents in this file.

The top-level description file for software platform is system.mss. This is used to store information regarding peripheral drivers and libraries used in the software platform as seen in the picture below.

Target Information

This Board Support Package is compiled to run on the following target.

Hardware Specification: C:\Users\KuldeepGohil\Desktop\Spring2021\CECS461\Labs\Lab1\project_1\project_1.sdk\design_1_wrapper_hw_platform_0\system.hdf
Target Processor: ps7_cortexa9_0

Operating System

Board Support Package OS.

Name: standalone
Version: 6.8
Description: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic
Documentation: standalone_v6_8

Peripheral Drivers

Drivers present in the Board Support Package.

ps7_afi_0	generic		
ps7_afi_1	generic		
ps7_afi_2	generic		
ps7_afi_3	generic		
ps7_coresight_comp_0	coresightps_dcc	Documentation	
ps7_ddr_0	ddrps	Documentation	
ps7_ddrc_0	generic		
ps7_dev_cfg_0	devcfg	Documentation	Import Examples
ps7_dma_ns	dmaps	Documentation	Import Examples
ps7_dma_s	dmaps	Documentation	Import Examples
ps7_globaltimer_0	generic		
ps7_gpv_0	generic		
ps7_intc_dist_0	generic		
ps7_iop_bus_config_0	generic		
ps7_l2cachec_0	generic		
ps7_ocmc_0	generic		
ps7_pl310_0	generic		
ps7_pmu_0	generic		
ps7_ram_0	generic		
ps7_ram_1	generic		
ps7_scuc_0	generic		
ps7_scugic_0	scugic	Documentation	Import Examples
ps7_scutimer_0	scutimer	Documentation	Import Examples
ps7_scuwdt_0	scuwdt	Documentation	Import Examples
ps7_slcr_0	generic		
ps7_uart_1	uartps	Documentation	Import Examples
ps7_xadc_0	xadcps	Documentation	Import Examples

Libraries

Libraries present in the Board Support Package.

No libraries in the Board Support Package

9. What is an .elf file? Is there an .elf file generated in this lab?

The .elf file is the linkable executable file which is the final machine code of our software. Yes, there is an .elf file that is generated in this lab.

10. Please provide a screenshot of your embedded system output and block diagram of your hardware platform.