Hardware/Software Codesign Lab 3

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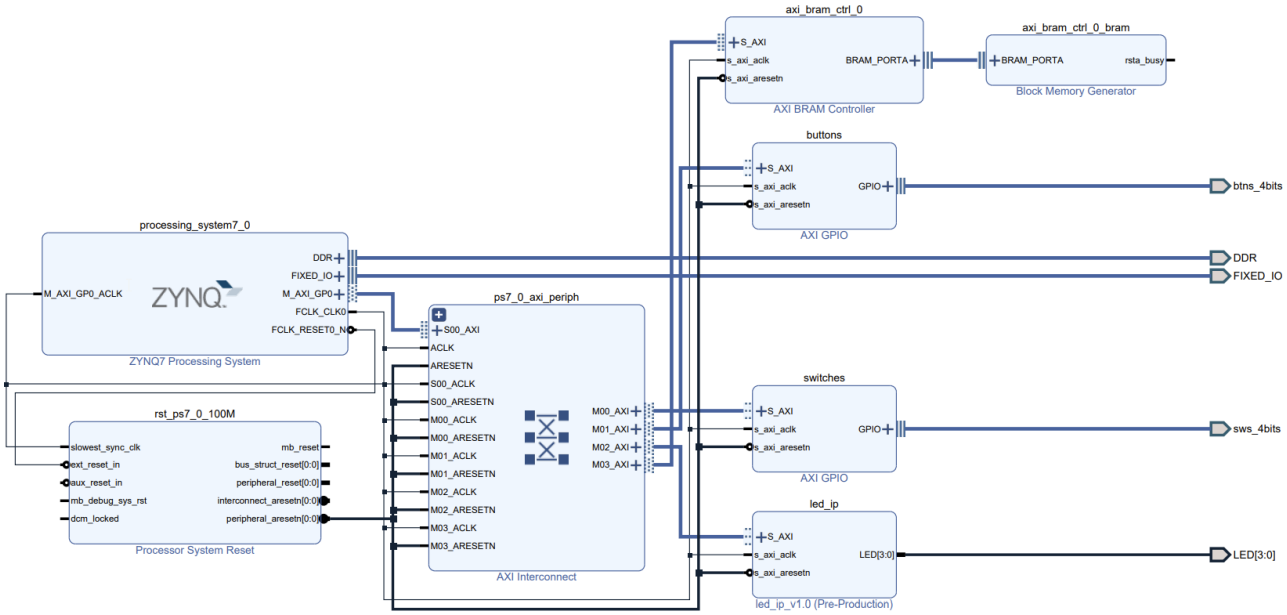
1. Follow the Lab 3 manual finish Lab 3.
2. Copy and paste the following information to the end of this document and submit this document:
   1) Block diagram for your hardware platform.



   2) peripheral memory map

processing_system7_0

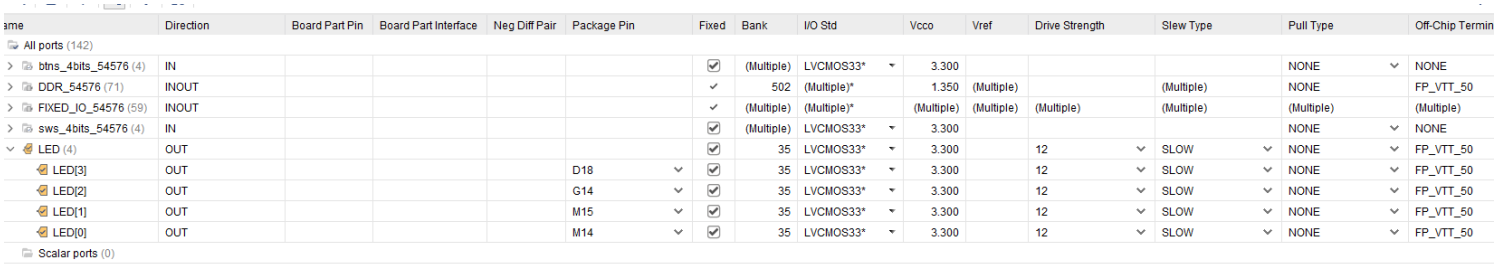
Data (32 address bits : 0x40000000 [1G])

axi_bram_ctrl_0	S_AXI	Mem0	0x4000_0000	8K	0x4000_1FFF
buttons	S_AXI	Reg	0x4121_0000	64K	0x4121_FFFF
led_ip	S_AXI	S_AXI_reg	0x43C0_0000	64K	0x43C0_FFFF
switches	S_AXI	Reg	0x4120_0000	64K	0x4120_FFFF

3) system.hdf: highlight information for the custom IP added and BRAM and BRAM controller.

axi_bram_ctrl_0	0x40000000	0x40001fff	S_AXI	MEMORY
switches	0x41200000	0x4120ffff	S_AXI	REGISTER
buttons	0x41210000	0x4121ffff	S_AXI	REGISTER
led_ip	0x43c00000	0x43c0ffff	S_AXI	REGISTER

4) Pin assignment for the four LEDs



ame	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termin
All ports (142)														
btns_4bits_54576 (4)	IN					☑	(Multiple)	LVCMOS33*	3.300				NONE	NONE
DDR_54576 (71)	INOUT					✓	502	(Multiple)*	1.350	(Multiple)		(Multiple)	NONE	FP_VTT_50
FIXED_IO_54576 (59)	INOUT					✓	(Multiple)	(Multiple)*	(Multiple)	(Multiple)	(Multiple)	(Multiple)	(Multiple)	(Multiple)
sws_4bits_54576 (4)	IN					☑	(Multiple)	LVCMOS33*	3.300				NONE	NONE
LED (4)	OUT					☑	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[3]	OUT				D18	☑	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[2]	OUT				G14	☑	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[1]	OUT				M15	☑	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
LED[0]	OUT				M14	☑	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50
Scalar ports (0)														

3. Answer the following question:
   1) Which register in the custom IP is used to control the leds? Can we use a different one? Show the modified code to use a different register to control the leds.
   Register 0 is used to control the leds. Since there are three other registers able to control the leds, yes we can use different register.

   2) Can we move the instantiation of lab3_user_logic from led_ip_v1_0_S_AXI.v to led_ip_v1_0, why or why not?

   Since led_ip_v1_0 is a wrapper that is top level for led IP, yes we can.