EE341: Project 4

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1 Problem 6.147

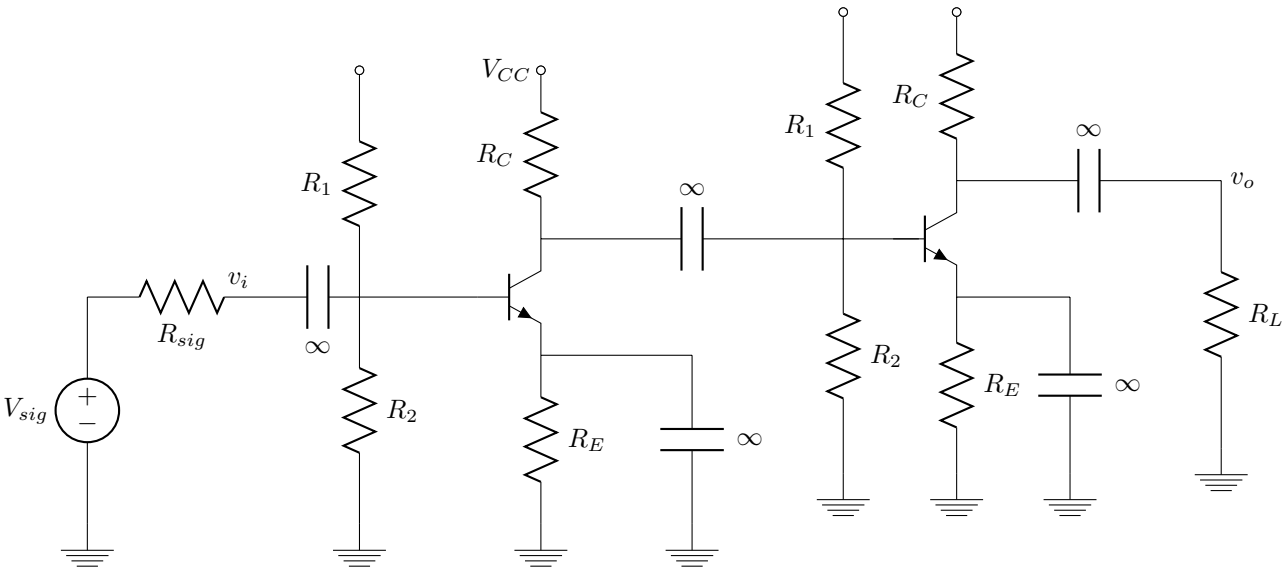


Figure 1: Large Signal Model

The problem is given as two of the amplifiers shown in Fig 1 connected with a load resistance R_L. The problem states $V_{CC} = 9V$, $R_1 = 100k\Omega$, $R_2 = 47k\Omega$, $R_E = 3.9k\Omega$, $R_C = 6.8k\Omega$, $\beta = 100$, $R_{sig} = 5k\Omega$, and $R_L = 2k\Omega$.

1.1 Hand Calculations

DC Bias: Part *a* asks for the DC collector current I_C and the DC collector voltage V_C of both transistors. For the first transistor, we replace R_1 and R_2 with their Thevinin equivalent resistance, $R_B = R_1||R_2 = 32k\Omega$, and voltage $V_B = \frac{R_2}{R_1+R_2}V_{BB} = 2.88V$. We then write the KVL using the large signal model, solve for I_B, and use β to find I_C.

$$V_{BB} = R_{B_1}I_{B_1} + 0.7V + R_{E_1}I_{B_1}(\beta + 1) \tag{1}$$

$$I_{B_1} = 5.12\mu A I_{C_1} = \beta I_{B_1} \tag{2}$$

$$I_{C_1} = 512\mu A \tag{3}$$

We then find V_{C_1} as follows. $V_{C_1} = V_{CC} - R_{C_1} I_{C_1} = 5.5V$. For the second transistor, we observe that the connecting signal is shunted out with a large capacitance. Since the second transistor has the same parameters and associated resistances and voltages as the first, we can conclude that $I_{C_1} = I_{C_2}$ and $V_{C_1} = V_{C_2}$.

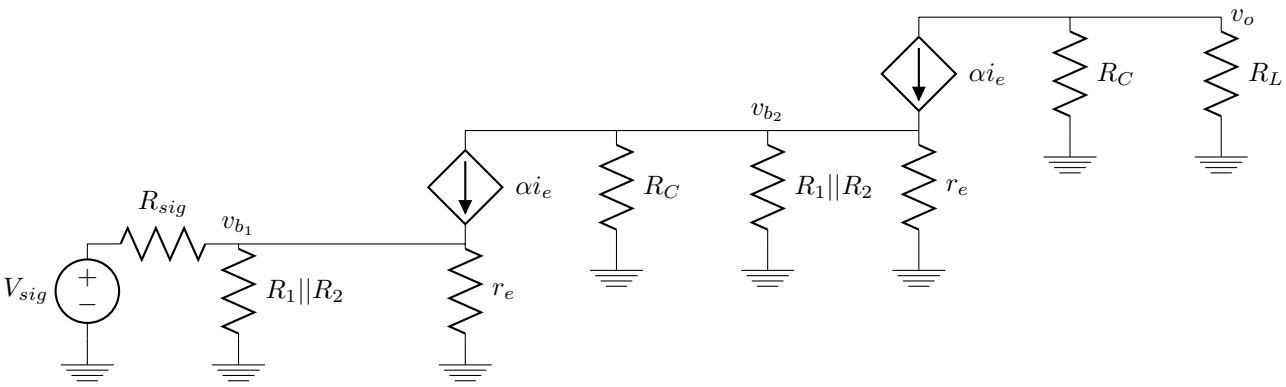


Figure 2: Small Signal Model

Small Signal Equivalent Circuit: Part b asks for the small signal equivalent circuit. Fig. 2 shows the small signal model for the entire circuit. R_{sig} is given as $5k\Omega$, R_C as $6.8k\Omega$, R_L as $2k\Omega$. R_1 and R_2 are given, so $R_1||R_2$ is calculated as $32k\Omega$. $r_e = \frac{V_T \alpha}{I_C} = 48\Omega$.

Input Resistances & Gains: Part c asks for the input resistance R_{in_1} and gain $\frac{v_{b_1}}{v_{sig}}$. R_{in_1} is the input resistance to the first stage, not including the signal resistance R_{sig}. The input resistance is calculated as follows.

$$R_{in_1} = (R_1||R_2)||((\beta + 1)r_e) \tag{4}$$

$$R_{in_1} = 4.24k\Omega \tag{5}$$

The gain for the first stage can be calculated as follows using R_{in_1}.

$$\frac{v_{b_1}}{v_{sig}} = \frac{R_{in_1}}{R_{sig} + R_{in_1}} \tag{6}$$

$$\frac{v_{b_1}}{v_{sig}} = 459\frac{mV}{V} \tag{7}$$

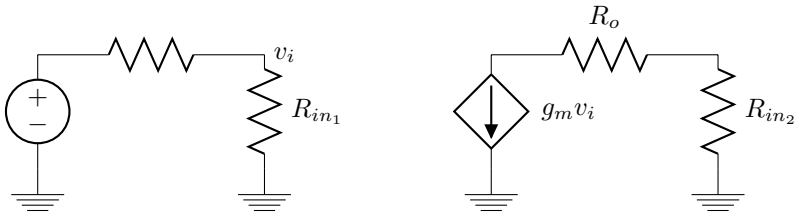


Figure 3: Model

Part d asks for the input resistance R_{in_2} and gain from transistor one $\frac{v_{b_2}}{v_{b_1}}$. By inspection it is clear that $R_{in_2} = R_{in_1} = 4.24k\Omega$. To calculate the gain, the transistor model shown in Fig. 3 was used. To complete

the model, g_m is calculated. $g_m = \frac{\alpha}{r_e} = 20.6\frac{mA}{V}$. R_o is simply R_C, as R_{in} of the following stage is not included. It is then simple to calculate the gain as $\frac{v_{b_2}}{v_{b_1}} = -g_m(R_{in_2}||R_{out_1}) = -51.9\frac{V}{V}$.

Part *e* asks for the gain $\frac{v_o}{v_{b_2}}$. Using the model in Fig. 3, we find that $\frac{v_o}{v_i} = g_m(R_{out_2}||R_L) = -31.8\frac{V}{V}$.

Part *f* asks for the total gain $\frac{v_o}{v_{sig}}$. This value is calculated by simply multiplying the gains from parts *c*, *d*, and *e*. We find that $\frac{v_o}{v_{sig}} = 758\frac{V}{V}$.

1.2 Spice Verification

DC Bias: It was observed that with the used model, spice produced a V_{BE} of $756.2mV$. This was a source of error for the theoretical calculations, which were based off the assumed V_{BE} of $0.7V$.

With this value across the transistor's pins, $V_C = 5.611V$ and $I_C = 498.38\mu A$. This was the same as theoretical calculations when the different V_{BE} was accounted for.

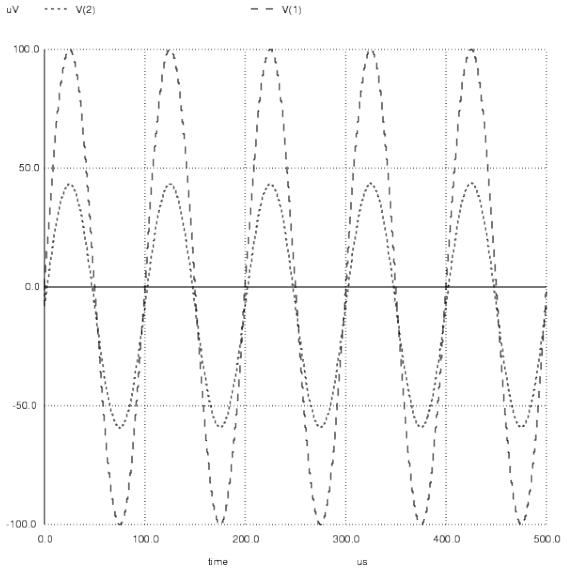
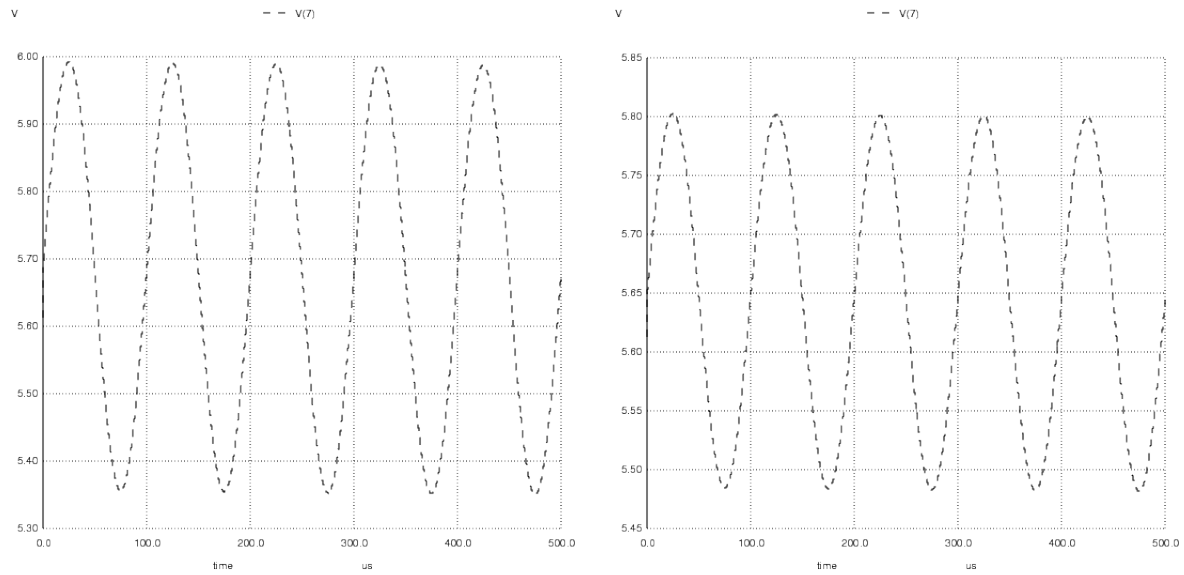


Figure 4: Input to First Stage with $v_{sig} = 100\mu V$

Input & Output Resistances: R_{in} was found to be $4.2k\Omega$, where the input voltage halved in spice, as shown in Fig. 4. *Rout* was found to be $6.8k\Omega$, where the input voltage halved in spice, as shown in Fig. 5.



(a) $R_l = \infty$ (b) $R_l = 6.8k\Omega$

Figure 5: Output

Gains: The gains and the errors are shown in the below table. The low error indicates that a proper analysis was made.

Table 1: Gain and Error From Spice

Name	Value	Error
Input Loss	472mV/V	2.75%
First Stage	-52.67V/V	1.46%
Second Stage	-29.15V/V	9.09%
Overall Gain	786.46V/V	3.618%

2 SPICE Source Code Listings

Listing 1: Verification of Amplifier

```
* 2 Stage Common Emitter Amplifier

*Input
vcc   10 0  DC 9
vsig 1   0  AC SIN(0 100u 10k 0 0 0)
rsig 1   2  5k

ca    2   3  100u

*First Stage
r1a   10 3  100k
r2a   3   0  47k
```

```
Qa    4   3   5   ntran
rea   5   0   3.9k
cea   5   0   100u
rca   4   10  6.8k

cb    4   6   100u

*Second stage
r1b   10  6   100k
r2b   6   0   47k
Qb    7   6   8   ntran
reb   8   0   3.9k
ceb   8   0   100u
rcb   7   10  6.8k

cc    7   9   100u

*Load
rl    9   0   2k

.model ntran npn (bf=100)
```