KOPPULA PETER

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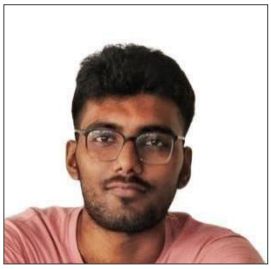

OBJECTIVE

Highly motivated and detail-oriented RTL Design Engineer with 1 year of hands-on experience in designing digital circuits using Verilog. Eager to leverage a strong foundation in RTL coding, logic synthesis, and timing analysis to contribute to innovative projects in a collaborative team environment. Committed to enhancing design efficiency, ensuring high-quality deliverables, and continually expanding technical skills in FPGA and ASIC design.

RELEVANT EXPERIENCE

RTL Engineer February 2023 – Present
KALKI TECH Hyderabad

- Designed the **Bad Block Management** logic for **Nand Flash Controller** in collaboration with team of developers and performed functional verification of sub system in LEO satellite (Anvesha) for DRDO.
- Designed the **UDP SPF** (secure packet forwarding) with client specifications and contributed for verification.
- Supported designing of logic components by designing related specifications for Post Quantum Cryptographic Algorithm **(CPA-PKE).**
- Designed **SSS** algorithm for cryptography application.

PROFESSIONAL TRAINING

- **RTL DESIGN AND VERIFICATION Training**

  From **VLSI FIRST RTL Design & Verification** training institute for VLSI, Hyderabad July 2023 to January 2023.

PROJECTS

- MIPS based 64-bit Single Cycle Processor.
- Single precision Floating point unit
- APB Protocol.
- Published in IEEE through 5Nano - Reduced size and Power efficient Level Shifter using MTCMOS & SC-CMOS.

EDUCATIONAL QUALIFICATIONS

- **Bachelor of Technology (B. Tech)** in Electronics & Communication Engineering (2020-2023)

  Lakireddy Bali Reddy college of Engineering, Mylavaram. **CGPA** - 7.6

- **DIPLOMA** in Electronics and communication engineering (2017-2020)

  AANM & VVRSR polytechnic, Gudlavalleru. **CGPA** – 9.6

- **SSC** from Nava Bharat High school (2016-2017). **CGPA** - 9.5

TECHNICAL SKILLS

- **Digital Design domain**
  - **Logical Designing**
  - **Digital System design**
  - **Computer Organization and Architecture**
- **VLSI domain**
  - **System & Micro Architecture**
  - **IP Development**
  - **RTL integration**
  - **FPGA Design**
  - **Static Timing Analysis**
  - **Clock Domain Crossing** (Basics).
- **RTL Designing**
  - **Verilog Programming:** Fork-join blocks, looping & branching construct. System tasks & Functions, compiler directives, Races in simulation, pipelining RTL & TB Coding, Abstractions,Regions of Verilog, memory designing, FSM designing, Synthesis issues.
- **Verification**
  - **System Verilog (Basics):** Data types, Arrays, OOPS, Randomization, Program block, Inter Process Communication, Interface, Coverage, Assertions.
- **Protocols**
  - APB, AXI, MIL-1553, UART, SPI.

SKILLS SUMMARY

- **Programming Languages:** Verilog, System Verilog, C.
- **Firsthand experience with EDA tools:** Xilinx Vivado, Intel Quartus(basic), Cadence virtuoso, Questa Sim, Visual Studio.
- **Familiar with:** FPGA (Zynq-7000, Kria), Arduino.
- **Version control:** GIT, GitHub.
- **Scripting:** TCL.
- **Soft Skills:** Focus, Creative thinking, Listening, Public Speaking, Adaptability.

CERTIFICATIONS

- Certified in RTL Designing by Entuple (RTL to GDSII).

WORKSHOPS

- On Analog Schematic Design and Layout conducted by LBRCE.
- On RTL Designing by ENTUPLE (RTL to GDSII).
- FPGA designing by Kalki-Tech.

EXTRA-CURRICULAR ACTIVITIES

- Digital design and Verilog classes teacher in Kalki Tech training institute.
- Project making in VLSI (digital & analog) and FPGA for MTech, MS and free lancing.
- Organized Workshops in VLSI and FPGA in Colleges
- Badminton tournaments.

INTERESTS & HOBBIES

- Project Making.
- Badminton, Chess.
- Podcast, Long rides.

DECLARATION

I, **KOPPULA PETER,** hereby declare that all the details mentioned above are in accordance with the truth and fact as per my knowledge and I hold the responsibility for the correctness of the above-mentioned particular