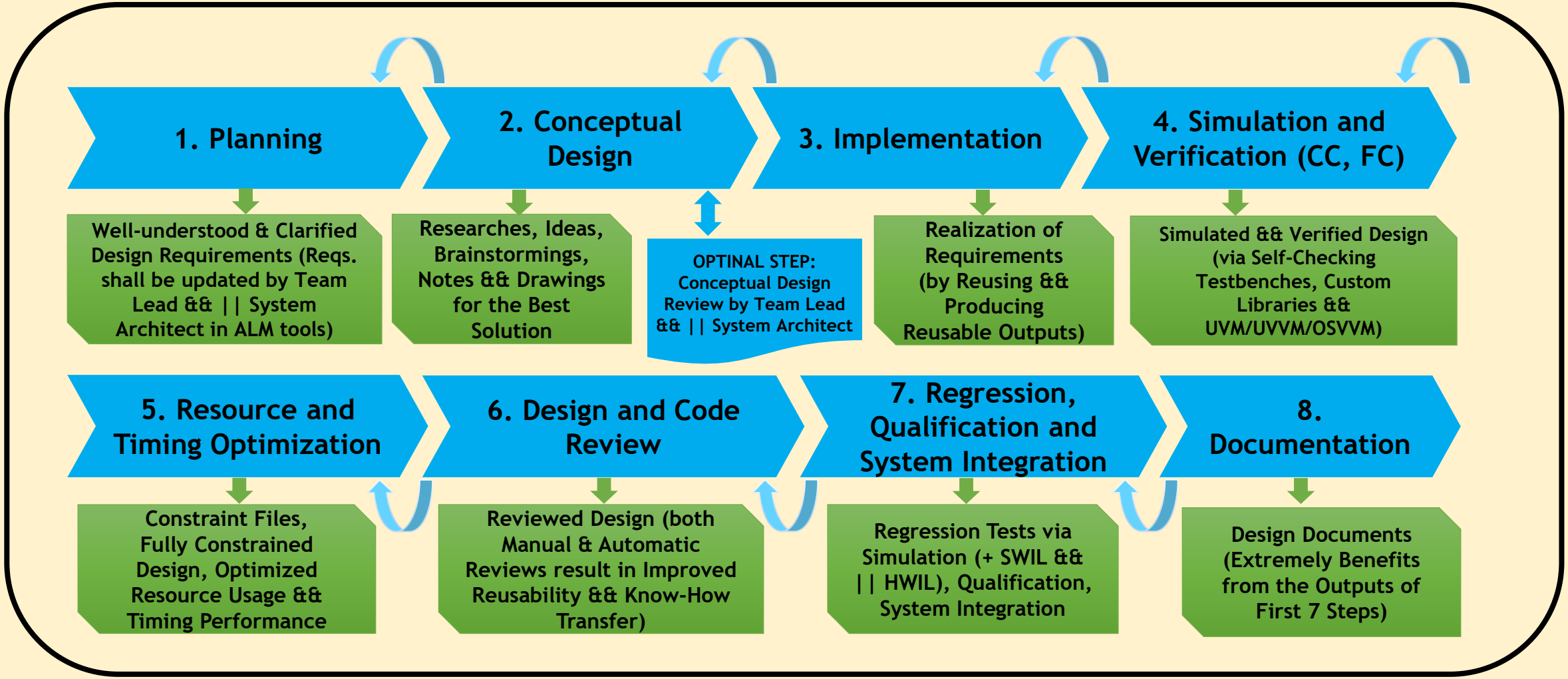
Notes:

- Each blue box is a step of the flow, and each green box shows the outputs of related design step.

FPGA DESIGN & VERIFICATION FLOW



TASK MANAGEMENT TOOL: Project A

TASK 1 ← → **DESIGN TASK**

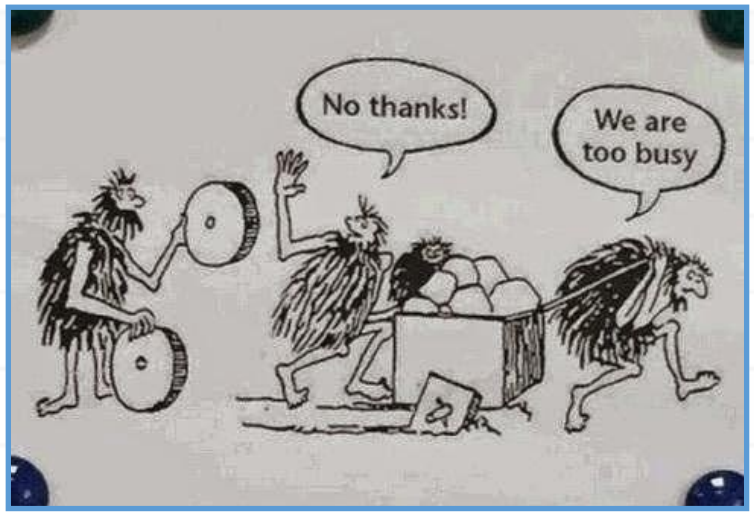
Status: open
Priority: 0

Swimlane: Default swimlane
Column: Working on currently
Position:

Assignee:
Creator:

▼ Description

▼ Sub-Tasks



Title	Assignee	Time tracking
planning		Start timer
concept design		Start timer
implementation		Start timer
simulation		Start timer
optimization		Start timer
testing		Start timer
review		Start timer
documentation		Start timer

DESIGN SUB-TASKS