Summary of Xilinx WP272

In this summary, it is mentioned that using a global reset does not make much sense and why it should be avoided.

Global Reset Isn't Timing-Critical

There are three methods to generate a global reset signal, and the resulting global reset signal is generally slow. Even if the Global Set/Reset (GSR) meets the necessary requirements, it should still be considered a timing-critical event. The document defines the requirements of GSR as ensuring that all flip-flops in the system are reset and that the reset duration is longer than the clock period. It is important to note that GSR operates as a high fan-out network. Due to the presence of multiple clocks and clock phases in the system, synchronization becomes difficult. In summary, there is a potential issue between the moment the GSR signal is generated and the synchronization of the system, making the GSR signal a timing-critical event.

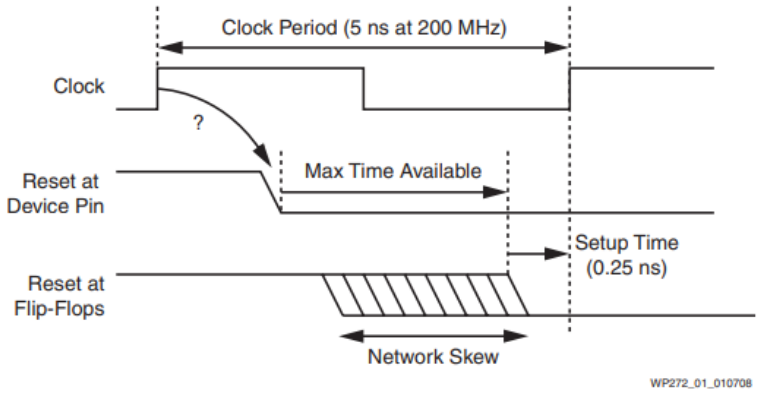

Figure 1: **Reset Timing Diagram - Asserted Between Clock Edges**

The reset signal activates in an active-low state between the clock edges and propagates to flip-flops. As it propagates, network skew occurs, and setup time constraints determine when the reset is deactivated. From the illustrated example, it is evident that resetting all flip-flops within a clock period is difficult due to network skew and setup time constraints. This problem worsens as clock rates increase because there is less time for the GSR signal to propagate.

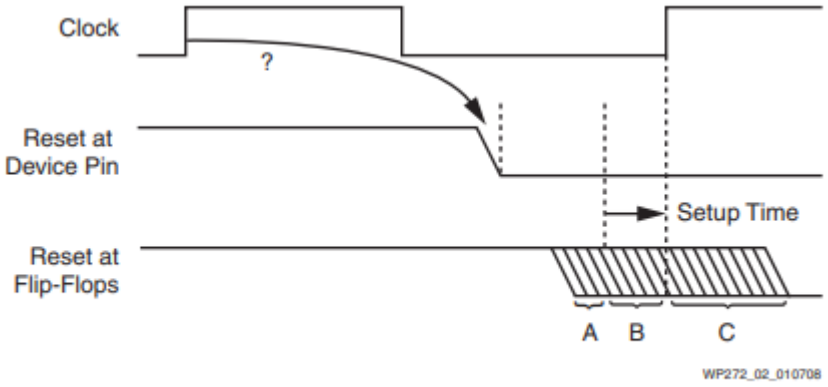

Figure 2: **Reset Timing Diagram - Asserted Asynchronously to the Clock**

From this illustration, we can see that Flip-Flop A can receive the reset easily, but it is uncertain whether Flip-Flop B will reset correctly, and Flip-Flop C has to wait for the next clock edge to reset.

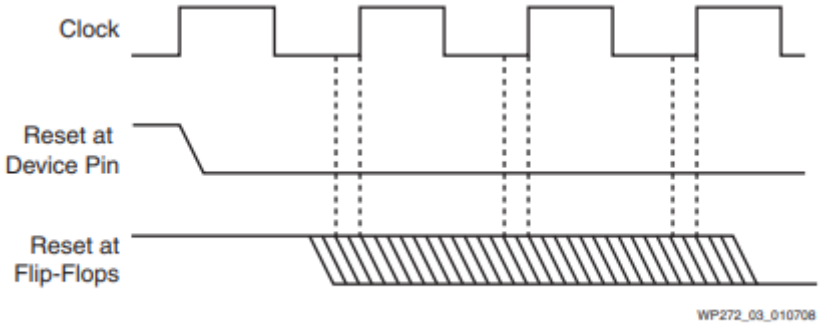

Figure 3: **Reset Timing Diagram - High Clock Rate**

The increasing clock rate and its effects on flip-flops receiving reset signals at different times can be clearly observed in the above illustration.

Does It Really Matter?

In most cases, the probability of reset failure is given as 0.01%, which means that reset release is not critical.

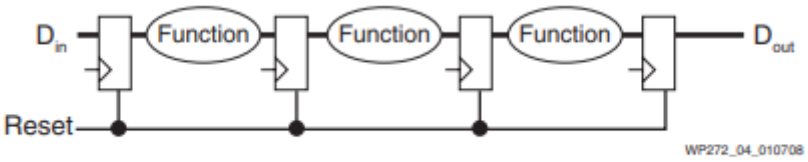

Figure 4: **Reset for a Pipeline**

For pipelined systems, reset release is not significant because the pipeline naturally flushes incorrect data from the system.

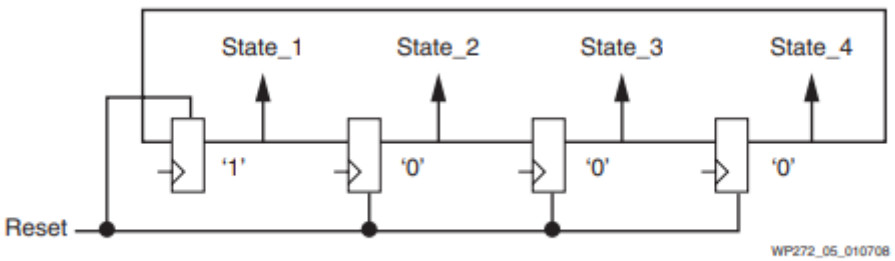

Figure 5: **Reset for a One-Hot State Machine**

However, in systems with feedback loops, such as the one-hot state machine example shown in the illustration, reset release is important because these systems operate synchronously. If the reset release occurs at the wrong time, synchronization is disrupted. The probability of this

occurring is inversely proportional to the proximity of the flip-flops to each other, as closer flip-flops reduce network skew.

Automatic Coverage of the 99.99% of Cases

This section explains that in Xilinx FPGAs, the configuration process automatically initializes flip-flops and even RAMs to a defined initial state. Since no extra data erasure occurs during this process, the need for an additional reset is reduced.

Strategy for the 0.01% of Cases

For critical parts of a design that require reset, local reset networks should be used to control the flip-flops requiring reset.

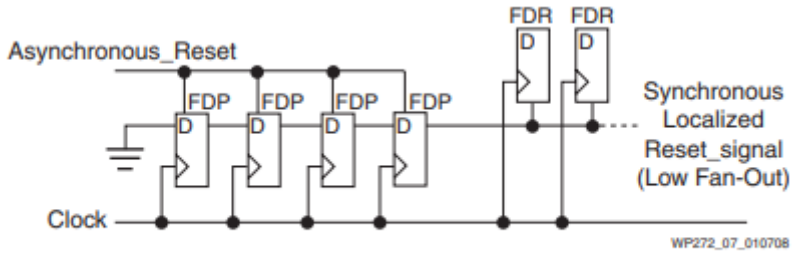

Figure 7: **Localized Reset**

During the Configuration Process or When an Asynchronous Reset Signal is Used, all flip-flops in the chain are initially set to 1 (High). Almost immediately, the flip-flop at the end of the chain sends an active reset signal to the local reset network. When the GSR (Global Set/Reset) or Asynchronous Reset Signal is Released: The shift register begins to be filled with 0s every clock cycle. The number of flip-flops in the chain determines how long this local reset signal will last. The Flip-Flop at the End of the Chain Transitions from High to Low: This transition occurs synchronously with the clock signal and the local reset signal is terminated.

Reset Costs More Than You Think!

The impact of using a global reset in design should not be overlooked, as it can cause more harm than expected.

Summary

For Xilinx FPGAs, there is no need to add a global reset network. Even if a system truly requires a reset, the critical components should be identified and carefully controlled during the reset process. When creating a system, it's important to consider if this specific part should be reset before putting a reset mechanism into place..