GFIR-55: WP272 Summary

Global Reset

Global reset is a type of reset application that resets all flip-flops and registers simultaneously. It transmits only one reset signal to other modules generally via the GSR(Global Set/Reset) network. With global reset, initial values can be controlled easily, and after configuration, the initial values are set automatically.

Pros	Cons
The system can be controlled with only one reset signal.	That may cause the flip-flops in different clocks to operate at different times when the reset is released. (Timing problems)
It's useful to reset all flip-flops in simulations and debug.	Distributing the same signal to many modules could cause routing delays.
It's easy to implement for small systems that contain a couple of modules.	Creating a reset connection for each flip-flop consumes FPGA routing resources.

Local Reset

Local reset is a type of reset application where only specific components or modules are reset individually. Unlike global reset, this is distributed only to the required modules. And it's often synchronized with each clock domain to avoid timing problems.

Pros	Cons
The reset signal is distributed only to the necessary components.	It may cause complexity, so the Designer should determine which modules need reset signal carefully.
Resource usage is efficient. Unnecessary routing resources are not spent.	It may cause synchronization problems. Reset synchronization in different clock domains should be implemented carefully.
Since each module releases reset synchronously with its clock signal, timing problems are minimized.	

Conclusion

The global reset signal is useful for simple and small systems, but it may cause timing problems and inefficient resource usage in bigger systems. On the other hand, local reset is more advantageous in multi-clock domain systems especially because each module releases a reset signal synchronously with their clock signals, so it prevents timing problems. Additionally, since modern FPGA devices already initialize the value of flip-flops during configuration, global reset is generally unnecessary. Therefore, in complex, and high-performance FPGA designs, local reset should be preferred for better synchronization.