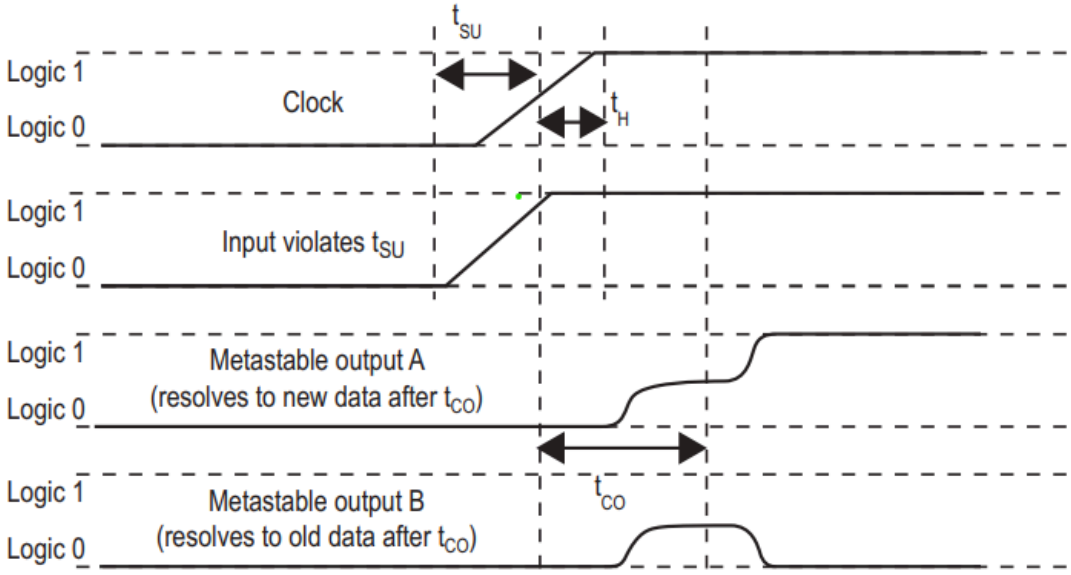
WP1082 Metastability

- If a data signal transition violates a register's tSU(set up time) or tH(hold time) requirements, the output of the register may go into a metastable state
- Defined output high or low state is delayed beyond the specified tCO(clock to output delay)
- MTBF indicates the regularity of failure due to metastability

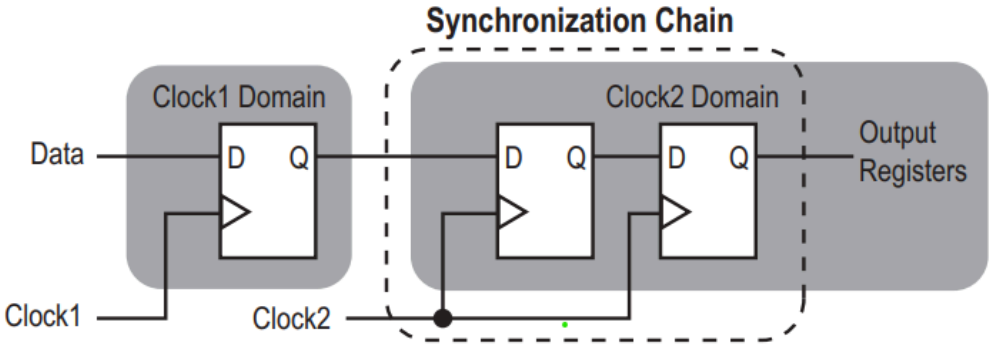
Figure 2. Examples of Metastable Output Signals



Synchronization Register

- To reducing metastability errors in asynchronous signal, synchronization registers or synchronizer is used
- This creates a additional time to settle down metastability

Figure 3. Sample Synchronization Register Chain



- Don't forget that, the first register in the chain is driven from an unrelated clock domain, or asynchronously

- A bus of asynchronous signal could send betweern clock domains and that causes incorrect bus data. In this case we may use DCFIFO or hand-shaking logic.
- **DCFIFO**: Data stored in a dual-port memory
- **Hand-shake:** It sends a control signal between clocks to make them inform about eachothers

Calculating MTBF

- Required MTBF depends on the system application (a medical device requires higher MTBF than a consumer video-display)

$$MTBF = \frac{e^{t_{MET}/C_2}}{C_1 \cdot f_{CLK} \cdot f_{DATA}}$$

  C1 and C2 constants depend on the device process and operating conditions
  fCLK is the clock frequency, fDATA is the toggling frequency of the asynchronous input data signal
- Faster clock frequencies and faster-toggling data reduce (or worsen) the MTBF
  tMET parameter is the available metastability settling time
- The tMET for a synchronization chain is the sum of the output timing slacks for each register in the chain

$$failure\_rate_{design} = \frac{1}{MTBF_{design}} = \sum_{i=1}^{number\ of\ chains} \frac{1}{MTBF_i}$$

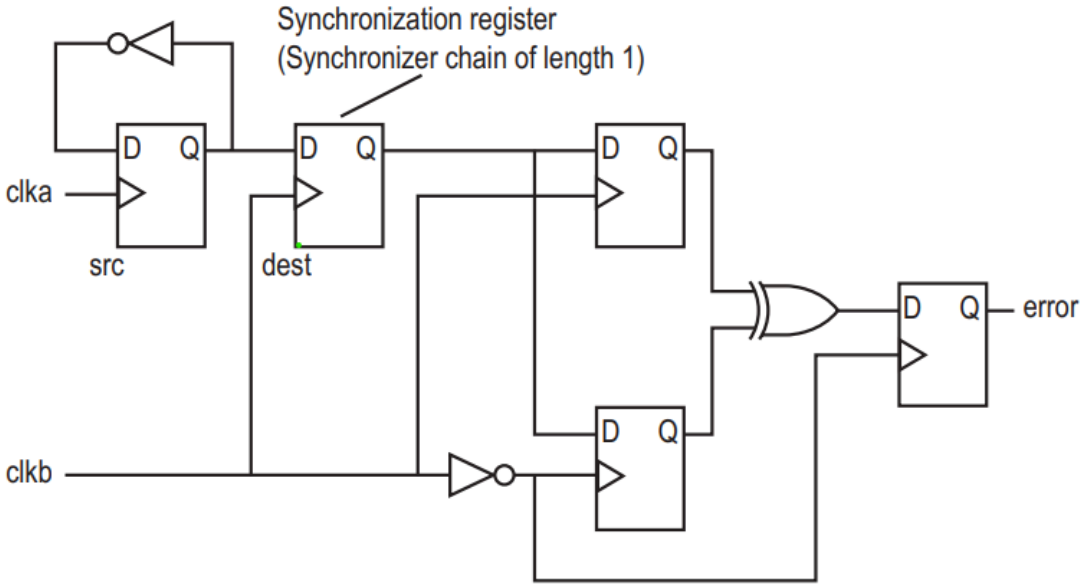
- The failure rate for a synchronizer is 1/MTBF

Characterizing Metastability Constants

- The difficulty with this characterization is that MTBFs for typical FPGA designs are in years, so measuring the time between metastability events using real designs under real operating

conditions is impractical

Figure 4. Test Circuit Structure for Metastability Characterization



- The destination registers capture the output of the synchronizer one clock cycle later and one half-clock cycle later. If the signal goes metastable before resolving at the next clock edge, the circuit detects that the sampled signals are different, and outputs an error signal
- The test is performed at different clock frequencies, and the MTBF versus tMET results are plotted on a logarithmic scale. The C2 constant corresponds to the slope of the trend line for the experimental results, and the C1 constant scales the line linearly

Improving Metastability MTBF

- Due to exponential equation, lowering the C2 is makes the largest effect
- Small increments in tMET significantly impact MTBF
- Additional registration stages in registration chains can increase tMET.
- Two registers are typically used, but Altera recommends using three registers for better metastability preservation.