Global Reset Isn't Timing-Critical

```
Assumption of the global reset is not timing-critical is not true. And this
assumption getting worst when it comes to clock rates increase.
```

*%99.99 of the time it does not really matter

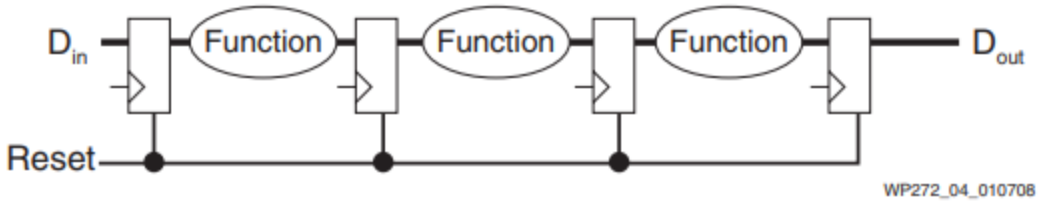

Figure 4: **Reset for a Pipeline**

*%0.01 case it may reset at wrong time

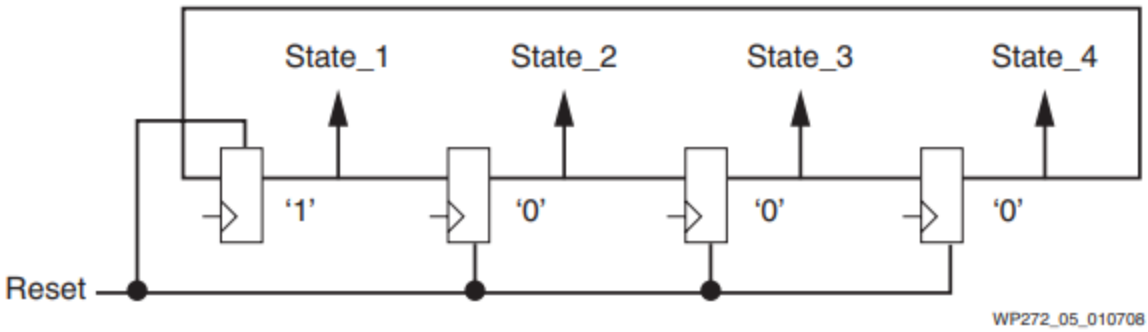

Figure 5: **Reset for a One-Hot State Machine**

- The timing of reset signals is crucial in state machines, particularly those with feedback loops.
- Similarly, encoded state machines risk transitioning to unexpected or illegal states if flip-flops aren't reset synchronously.
- Precise synchronization of reset signals is essential to prevent state machine failures.
- Circuits without feedback, like Finite Impulse Response (FIR) filters, are less sensitive to reset timing. Because FIR filters need to have all of the taps filled with valid data, resetting the tap registers before this point has no value.

Strategy for the 0.01% of Cases

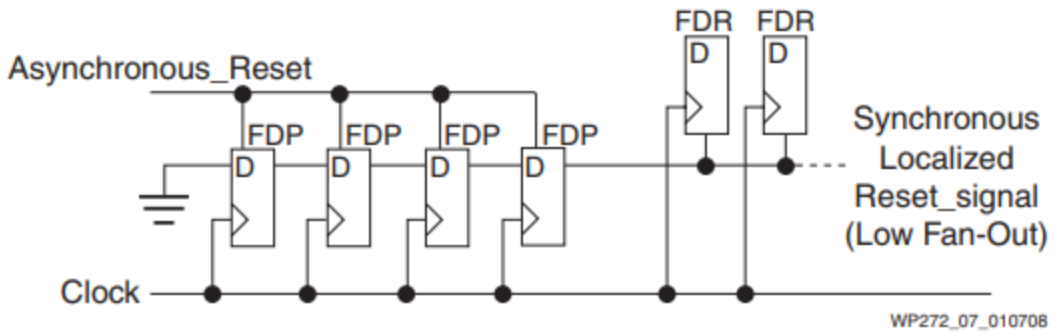

Figure 7: **Localized Reset**

- Prioritize comprehensive reset strategy development and ensure thorough design reviews to mitigate rare but critical reset-related failures.
- Localized reset networks to achieve precise control over critical flip-flops, ensuring synchronous reset release and enhancing overall system reliability.
- Upon the release of an asynchronous reset signal or device configuration, the shift register fills with zeros, delaying the release of the localized reset.
- Utilize shift register chains to generate timed, synchronous reset pulses, ensuring that critical flip-flops are released in sync with the clock, leading to a more reliable and predictable system.