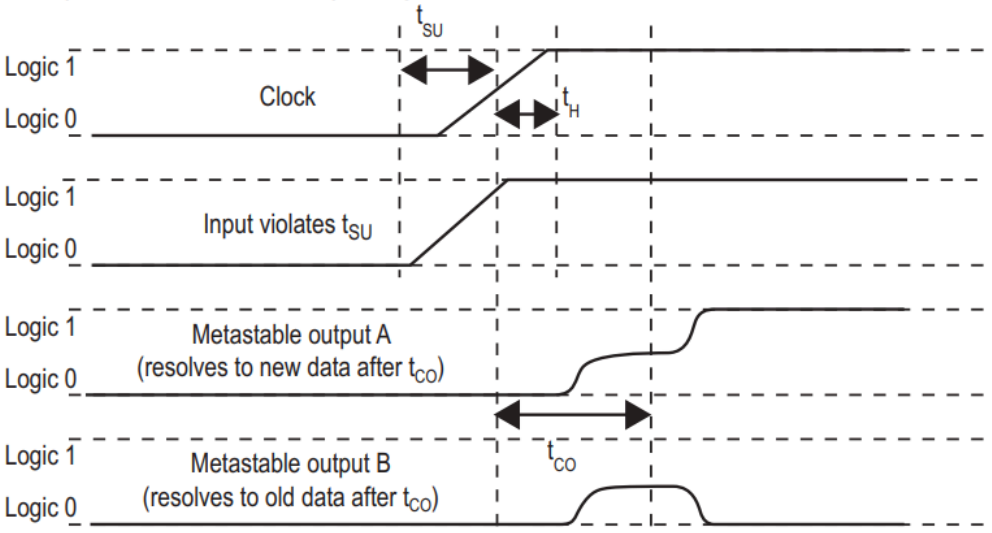
Metastability

What's Metastability?

- Metastability is a condition where a register's output is temporarily undefined between 0 and 1.
- This occurs due to setup/hold time violations.
    - **tsu(Setup Time):** The data must be stable for a certain period before the clock edge.
    - **th(Hold time):** The data must be stable for a certain period after the clock edge.
    - **Setup/hold time violation:** If the data is not stable for a certain period as setup/hold time, it may cause metastability.

Figure 2. Examples of Metastable Output Signals



Why is it a problem?

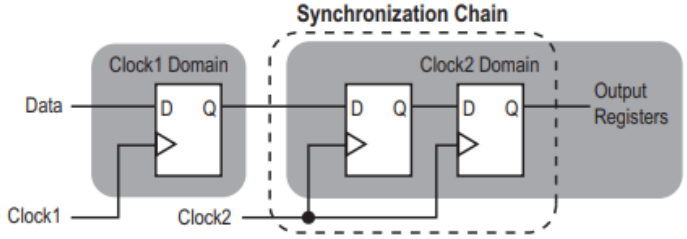
- A metastable signal may spread incorrect or inconsistent logic values.
- That can cause **system-level failures**, especially if the unstable signal is captured by downstream logic before resolving.

When does it happen?

- **Multiple clock domains:** Crossing the signals between different clock domains.
- **Asynchronous external inputs:** Mechanical buttons, or external peripherals

How to reduce this hazard?

- Using **synchronization register chains** (2 or more flip-flops in series.)
    - Increase the available settling time by using two or more registers clocked by the destination clock.



Mean Time Between Failures (MTBF)

Formula

tMET: Settling time (for metastability resolution)
C1 and **C2:** Device-specific process constants
fCLK: Destination clock frequency
fDATA: Data toggle frequency

$$MTBF = \frac{e^{t_{MET}/C_2}}{C_1 \cdot f_{CLK} \cdot f_{DATA}}$$

Factors affecting MTBF

- Longer synchronization chain →**Higher MTBF**
- Lower data toggle and clock frequencies →**Higher MTBF**
- FPGA process technology (C1 and C2 constants)

Best Practices

- Place synchronizer registers inside the same CLB to reduce routing delays.
- Consider 2-3 stage synchronizers for critical signals like resets.

Example:

Parameters:
fCLK: 100 MHz, fDATA: 1kHz, C1: 0.1ns, C2: 1, tMET (depends on synchronizer chain)

1. Scenario: 2 Flip-flop chain
Assume tMET (metastability settling time) is 0.5ns between registers

MTBF = e^(tMET / C1) / (C2* fCLK * fDATA)

MTBF = e^(0.5 / 0.1) / (1e3 * 100e7 * 1)
MTBF = e^5 / 1e11
MTBF = 148.4 / 1e11 == 1.48µs

This means there might be a metastability error approximately every 1.48µs. It's too low and unacceptable.

2. Scenario: 3 Flip-flop chain and optimized routing (tMET = 2ns)
Assume tMET is optimized by reducing routing delays (registers placed inside the same CLB), so tMET = 2ns for 3 flip-flops.

MTBF = e^(2 / 0.1) / (1e3 * 100e7 * 1)
MTBF = e^20 / 1e11 = 4850s ≈ 1.35 hours

This means there might be a metastability error approximately every 1.35 hours. It's better.

2. Scenario: 4 Flip-flop chain and lower clock frequency
Assume we reduced clock frequency to 25MHz, add 1 more flip-flop, so make the tMET = 3ns (3 flip-flop * 1 (settling time))

MTBF = e^(3 / 0.1) / (1e3 * 25e7 * 1)
MTBF = e^20 / 1e11 = 428000s ≈ 119 hours ≈ 5 days

This means there might be a metastability error approximately every 5 days. It's more better.