Gowin DSP

User Guide

UG287-1.1E,10/9/2017

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Revision History

Date	Version	Description
10/9/2017	1.1E	Initial version.

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1 About This Guide

1.1 Purpose

This manual provides a main description of DSP architecture, signal definition, and user calling methods, etc., which helps in getting used to Gowin DSP and enhancing design efficiency.

1.2 Supported Products

The information in the guide applies to the following products:

1. GW1N series FPGA products: GW1N-2, GW1N-4, GW1N-6, GW1N-9.
2. GW1NR series FPGA products: GW1NR-4, GW1NR-9;
3. GW2A series FPGA products: GW2A-55, GW2A-18.
4. GW2AR series FPGA products: GW2AR-18.

1.3 Related Documents

The latest user guides are available on our Website. Refer to the related documents at http://www.gowinsemi.com.cn:

1. GW2A series FPGA Products Data Sheet
2. GW1N series FPGA Products Data Sheet
3. GW2AR series FPGA Products Data Sheet
4. GW1NR series FPGA Products Data Sheet

1.4 Abbreviation and Terminology

Table 1-1 shows the abbreviations and terminologies used in this manual.

Table 1-1 Abbreviations and Terminologies

Abbreviation and Terminology	Full Name	Meaning
DSP	Digital Signal Processing	-
FPGA	Field Programmable Gate Array	-
FIR	Finite Impulse Response	-
FFT	Fast Fourier Transformation	-
CFU	Configurable Function Unit	-
MULT	Multiplier	-
PADD	Pre-adder	-
ALU	Arithmetic Logic Unit	-

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If any questions, comments, or suggestions, please feel free to contact us directly.

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2 Overview

GOWINSEMI FPGA products (except GW1N-1) have abundant DSP blocks. GOWINSEMI DSP solutions can meet user demands for high performance digital signal processing, such as FIR and FFT designs, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power. This manual mainly helps users to be familiar with DSP architecture and usage quickly. Please refer to *Gowin FPGA Primitives Guide* for the details. Primitives library locates in the installation directory of Gowin Yunyuan software: GOWIN/x.x/Pnr/lib/gwxx, of which "x.x" is the software version, and "gwxx" is the device series, such as gw1n and gw2a.

DSP blocks functions and features are as follows:

- Multiplier with 3 width: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data
- Barrel Shifter
- Adaptive filtering through signal feedback
- Support registers pipeline and bypass

The number of GOWINSEMI FPGA products 18-bit multiplier MULT18×18 is listed in Table 2-1. The configuration modes supported by DSP blocks are listed in Table 2-2.

Table 2-1 MULT18 x 18 Resources

Device		MULT18 x 18 Qty.
GW1N series FPGA Products	GW1N-2	16
	GW1N-4	16
	GW1N-6	20
	GW1N-9	20
GW1NR series FPGA Products	GW1NR-4	16
	GW1NR-9	20
GW2A series FPGA Products	GW2A-18	48
	GW2A-55	40
GW2AR series FPGA Products	GW2AR-18	48

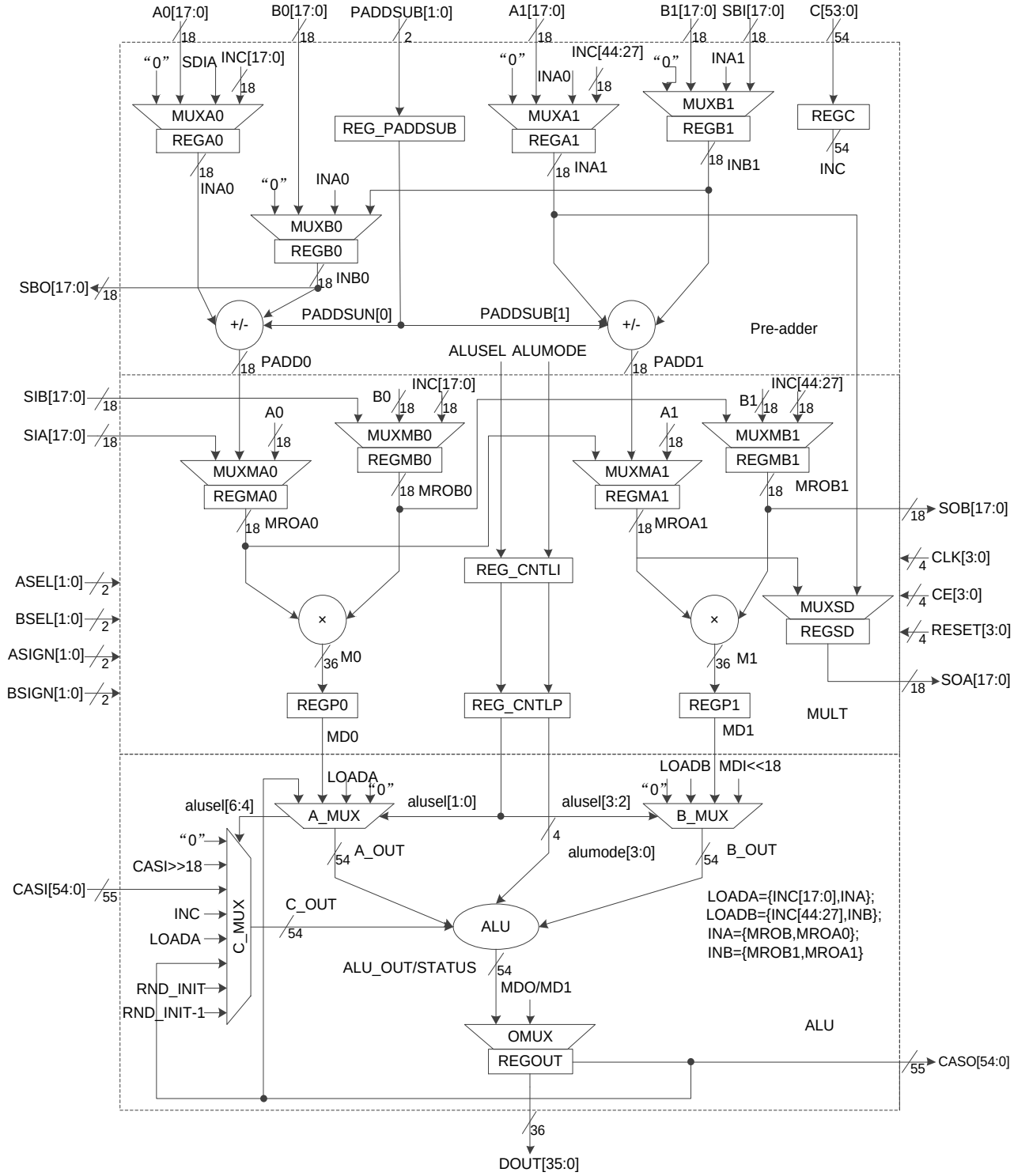
Table 2-2 Configuration Modes Supported by DSP

Mode	Primitives Name	Description
PADD	PADD9	9-bit pre-adder
	PADD18	18-bit pre-adder
ALU	ALU54	54-bit ALU
MULT	MULT9 x 9	9-bit Multiplier
	MULT18 x 18	18-bit Multiplier
	MULT36 x 36	36-bit Multiplier
MULTALU	MULTALU18 x 18	MULTALU 18X18: 18-bit MULTALU
	MULTALU36 x 18	MULTALU 36X18: 36X18-bit MULTALU
MULTADDALU	MULTADDALU18 x 18	Accumulation or reloading of two 18-bit MULTADD

3 DSP Architecture

GOWINSEMI DSP blocks are arranged in horizontal rows in the FPGA array. DSP block contains 2 Macro, and each Macro contains two pre-adders, two 18 x 18 bit multipliers, and one 3 input ALU54. Figure 3-1 shows the architecture of a GOWINSEMI DSP macro.

Figure 3-1 DSP Architecture



GOWINSEMI DSP block contains pre-adder, multiplier, ALU, and internal staged registers. Table 3-1 shows DSP ports description. The internal staged registers are as shown in Table 3-2. In addition, input signals CLK, CE, and RESET are used to control the registers.

Table 3-1 DSP Ports Description

Ports Name	I/O	Description
A0[17:0]	I	18-bit data input A0
B0[17:0]	I	18-bit data input B0
A1[17:0]	I	18-bit data input A1
B1[17:0]	I	18-bit data input B1
C[53:0]	I	54-bit data input C
SIA[17:0]	I	Shift data input A, used for CASCADE connection. The input signal SIA is directly connected to the output signal SOA of previously adjacent DSP and the delay from SIA to SOA inside a DSP is one clock cycle.
SIB[17:0]	I	Shift data input B, used for CASCADE connection. The input signal SIB is directly connected to the output signal SOB of previously adjacent DSP and the delay from SIB to SOB inside a DSP is one clock cycle.
SBI[17:0]	I	Pre‑adder logic shift input, backward direction.
CASI[54:0]	I	ALU input from previous DSP block, used for cascade connection.
ASEL[1:0]	I	Source select for Multiplier or pre-adder input A
BSEL[1:0]	I	Source select for Multiplier input B
ASIGN [1:0]	I	Sign bit for input A
BSIGN[1:0]	I	Sign bit for input B
PADDSUB[1:0]	I	Operation control signals of pre-adder, used for pre-adder logic add/subtract selection
CLK[3:0]	I	Clock input
CE[3:0]	I	Clock Enable
RESET[3:0]	I	Reset input, synchronous or asynchronous
SOA[17:0]	O	Shift data output A
SOB[17:0]	O	Shift data output B
SBO[17:0]	O	Pre‑adder logic shift output, backward direction.
DOUT[35:0]	O	DSP output data
CASO[54:0]	O	ALU output to next DSP block for cascade connection, the highest bit is sign extended.

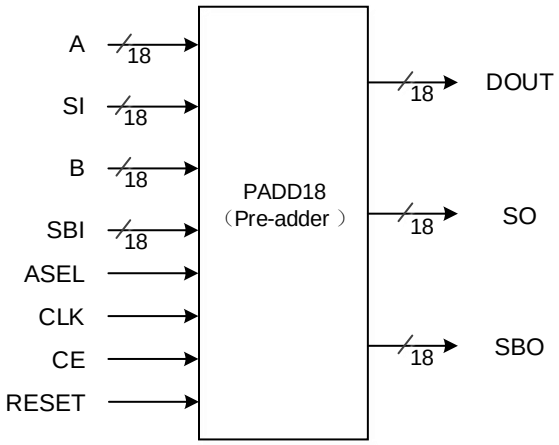
Table 3-2 Internal Registers Description

Register	Description and Associated Attribute
A0 register	Registers for A0 input
A1 register	Registers for A1 input
B0 register	Registers for B0 input
B1 register	Registers for B1 input
C register	Registers for C input
P1_A0 register	Registers for A0 input of left multiplier
P1_A1 register	Registers for A1 input of right multiplier
P1_B0 register	Registers for B0 input of left multiplier
P1_B1 register	Registers for B1 input of right multiplier
P2_0 register	Registers for pipeline of left multiplier
P2_1 register	Registers for pipeline of right multiplier
OUT register	Registers for DOUT output
OPMODE register	Registers for operation mode control
SOA register	Registers for shift output at port SOA

3.1 PADD

Each DSP macro features two units of pre-adders to implement pre-add, pre-subtraction, and shifting. PADD locates at the first stage with two inputs. One is parallel 18-bit input B or SBI, and the other is either parallel 18-bit input A or SIA. A register chain is used for each input to enhance timing performance. The stage registers can also be bypassed to directly feed multiplier. GOWINSEMI PADD can be used as function block independently. PADD contains 9-bit PADD9 and 18-bit PADD18. The two PADDs have the same structure, registers, and parameters attribute. See Figure 3-2 for PADD18 architecture.

Figure 3-2 PADD18 Architecture



The port signals and description for PADD18 are listed in Table 3-3. PADD18 registers and attributes are listed in Table 3-4.

Table 3-3 PADD18 Port Signals

Ports Name	I/O	Description
A[17:0]	I	18-bit data input A
B[17:0]	I	18-bit data input B
SI[17:0]	I	18-bit shift data input A
SBI[17:0]	I	Pre-adder shift input, backward direction
ASEL	I	Source select for pre-adder
CLK	I	Clock input
CE	I	Clock Enable
RESET	I	Reset input
SO[17:0]	O	Shift data output A
SBO[17:0]	O	Pre‐adder shift output, backward direction
DOUT[17:0]	O	Data output

PADD registers and parameter attribute are listed in Table 3-4. The parameters can be configured according to user demands to implement expected functions by selecting different inputs.

Table 3-4 PADD18 Attribute Description

Attribute Name	Values(default)	Description
AREG	1’b0,1’b1（1’b0）	Registers for A input (A or SI) ● 1’b0: bypass mode ● 1’b1: registered mode

Attribute Name	Values(default)	Description
BREG	1’b0,1’b1(1’b0)	Registers for B input(B or SBI) ● 1’b0: bypass mode ● 1’b1: registered mode
ADD_SUB	1’b0,1’b1(1’b0)	Pre-adder add/subtract selection ● 1’b0: add ● 1’b1: sub
PADD_RESET_MODE	SYNC,ASYNC(SYNC)	synchronous or asynchronous
SOREG	1’b0,1’b1(1’b0)	Registers for shift output at port SO. ● 1’b0: bypass mode ● 1’b1: registered mode
BSEL_MODE	1’b0,1’b1(1’b1)	B input selection ● 1'b1: input SBI ● 1'b0: input B

PADD9 can be used for 9-bit pre-adding, pre-subtraction, and shifting. Figure 3-3 shows PADD9 architecture. PADD9 Port signals and description are listed in Table 3-5.

Figure 3-3 PADD9 Architecture

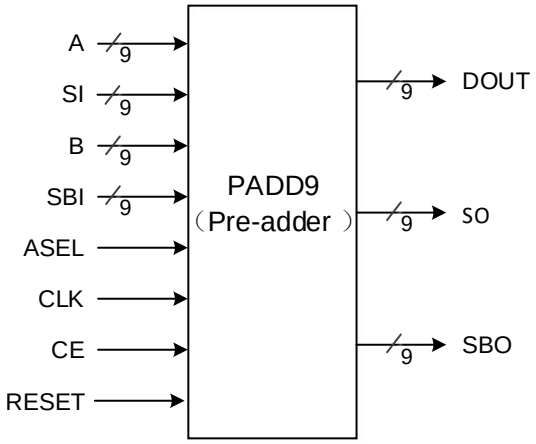


Table 3-5 PADD9 Port Signals

Ports Name	I/O	Description
A[8:0]	I	9-bit data input A
B[8:0]	I	9-bit data input B
SI[8:0]	I	shift data input A
SBI[8:0]	I	Pre‐adder shift input, backward direction
ASEL	I	Source select for pre-adder
CLK	I	Clock input
CE	I	Clock Enable

Ports Name	I/O	Description
RESET	I	Reset input
SO[8:0]	O	Shift data output A
SBO[8:0]	O	Pre‐adder shift output, backward direction
DOUT[8:0]	O	Data output

Table 3-6 PADD9 Attribute Description

Attribute Name	Values(default)	Description
AREG	1’b0,1’b1(1’b0)	Registers for A input（A or SI） ● 1’b0: bypass mode ● 1’b1: registered mode
BREG	1’b0,1’b1(1’b0)	Registers for B input (B or SBI) ● 1’b0: bypass mode ● 1’b1: registered mode
ADD_SUB	1’b0,1’b1(1’b0)	Pre-adder add/subtract selection ● 1’b0: add ● 1’b1: sub
PADD_RESET_MODE	SYNC,ASYNC(SYNC)	synchronous or asynchronous
SOREG	1’b0,1’b1(1’b0)	Registers for shift output at port SO ● 1’b0: bypass mode ● 1’b1: registered mode
BSEL_MODE	1’b0,1’b1(1’b1)	B input selection ● 1'b1: input SBI ● 1'b0: input B

3.2 MULT

Each DSP macro has two multiplier units to perform the multiplication. Based on the needs of multiplication width, the multipliers can be configured as 9x9, 18x18, 36x18 or 36x36. Based on the needs of multiplication width, the multipliers can be configured as 9x9, 18x18, 36x18 or 36x36. The 36x36 multiplier mode requires one DSP block (two macros) to configure.

Registers at both multiplier input side and output side are optionally available. For each bit of the input signal or the output signal, the user can select to use register or bypass the register. For each DSP macro, there are clock signals, clock enable signals, and reset signals. Each clock

signal can be driven by BUFG, BUFS, or logic. Each clock enable signal or reset signal can be driven by BUFS or logic. Registers can select clock signals, clock enable signals, and reset signals as input. Please refer to *4 DSP Operation Mode > 4.1MULT* for the detailed information.

3.3 Arithmetic Logic Unit

Each DSP macro supports one flexible 54-bit ALU which provides robust extension to MULT part. It can be used independently. Figure 3-4 shows the architecture of ALU54D. The port signals for ALU54D are listed in Table 3-7.

Figure 3-4 ALU54D Architecture

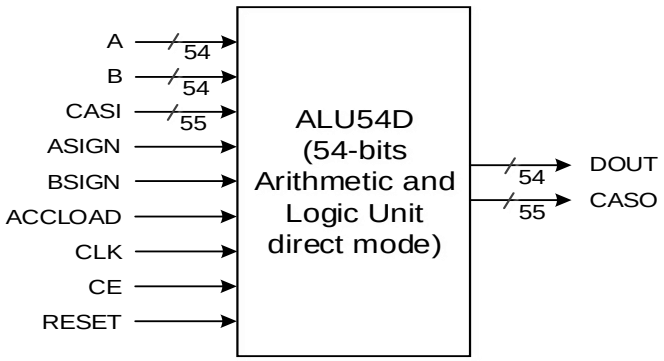


Table 3-7 ALU54D Port Signals

Ports Name	I/O	Description
A[53:0]	I	54-bit data input A
B[53:0]	I	54-bit data input B
ASIGN	I	Sign bit for input A
BSIGN	I	Sign bit for input B
ACCLOAD	I	used for accumulator reload selection
CASI[54:0]	I	55-bit data input B
CLK	I	Clock input
CE	I	Clock Enable
RESET	I	Reset input
DOUT[53:0]	O	54-bit data output
CASO[54:0]	O	55-bit data cascade output

ALU54D Attributes

ALU54D attributes are as shown in Table 3-8.

Table 3-8 ALU54D Attributes Setting

Attribute Name	Values(default)	Description
AREG	1'b0,1'b1(1'b0)	Registers for A input ● 1'b0: bypass mode ● 1'b1: registered mode
BREG	1'b0,1'b1(1'b0)	Registers for B input ● 1'b0: bypass mode ● 1'b1: registered mode
ASIGN_REG	1'b0,1'b1(1'b0)	ASIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
BSIGN_REG	1'b0,1'b1(1'b0)	BSIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
ACCLOAD_REG	1'b0,1'b1(1'b0)	ACCLOAD register ● 1'b0: bypass mode ● 1'b1: registered mode
OUT_REG	1'b0,1'b1(1'b0)	Output register ● 1'b0: bypass mode ● 1'b1: registered mode
B_ADD_SUB	1'b0,1'b1(1'b0)	B_OUT add/subtract selection ● 1'b0: add ● 1'b1: sub
C_ADD_SUB	1'b0,1'b1(1'b0)	C_OUT add/subtract selection ● 1'b0: add ● 1'b1: sub
ALU54D_MODE	0,1,2(0)	ALU54D operation mode: ● 0: ACC/0 +/- B +/- A; ● 1: ACC/0 +/- B + CASI; ● 2: A +/- B + CASI;
ALU_RESET_MODE	SYNC,ASYNC(SYNC)	Synchronous or asynchronous reset

4 DSP Operation Mode

GOWINSEMI DSP supports the following operation modes:

- MULT
- MULTALU
- MULTADDALU

4.1 MULT

Based on the needs of multiplication width, the multipliers can be configured as 9x9, 18x18, 36x36, etc. Each DSP macro have two independent 18 x 18 multipliers.

Each DSP block can be configured with up to 36 bits data-width of DSP supporting modes including 9x9, 18x18, 36x18 and 36x36 multipliers.

4.1.1 MULT 9 x 9

MULT 9 X 9 can be used to implement 9-bit multiplication. The port signals are listed in Table 4-1. The architecture is shown in Figure 4-1.

Figure 4-1 MULT 9 x 9 Architecture

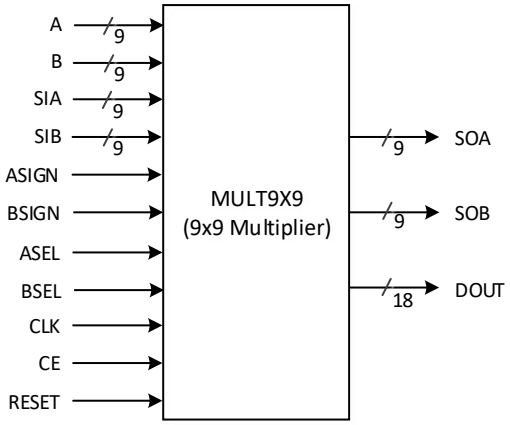


Table 4-1 MULT 9 x 9 Port Signals

Ports Name	I/O	Description
A[8:0]	I	9-bit data input A
SIA[8:0]	I	9-bit shift data input A
B[8:0]	I	9-bit data input B
SIB[8:0]	I	9-bit shift data input B
ASIGN	I	Sign bit for input A
BSIGN	I	Sign bit for input B
ASEL	I	Source select for Multiplier input A (A/SIA)
BSEL	I	Source select for Multiplier input A (A/SIA)
CLK	I	Clock input
CE	I	Clock Enable
RESET	I	Reset input
DOUT[17:0]	O	Multiplier output data
SOA[8:0]	O	Shift data output A
SOB[8:0]	O	Shift data output B

MULT 9 x 9 Attribute

MULT 9 x 9 attributes are listed in Table 4-2

Table 4-2 MULT 9 x 9 Attributes Setting

Attribute Name	Values(default)	Description
AREG	1'b0,1'b1(1'b0)	Registers for A（A/SIA）input ● 1'b0: bypass mode ● 1'b1: registered mode
BREG	1'b0,1'b1(1'b0)	Registers for B (B/SIB)input ● 1'b0: bypass mode ● 1'b1: registered mode
ASIGN_REG	1'b0,1'b1(1'b0)	ASIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
BSIGN_REG	1'b0,1'b1(1'b0)	BSIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
SOA_REG	1'b0,1'b1(1'b0)	SOA register ● 1'b0: bypass mode ● 1'b1: registered mode
OUT_REG	1'b0,1'b1(1'b0)	Output register ● 1'b0: bypass mode ● 1'b1: registered mode
PIPE_REG	1'b0,1'b1(1'b0)	Pipeline registers ● 1'b0: bypass mode ● 1'b1: registered mode
MULT_RESET_MODE	SYNC,ASYNC(SYNC)	Synchronous or asynchronous reset

4.1.2 MULT 18 x 18

MULT 18 X 18 can be used to implement 18-bit multiplication. The port signals are listed in Table 4-3. The architecture is shown in Figure 4-2.

Figure 4-2 MULT 18 x 18 Architecture

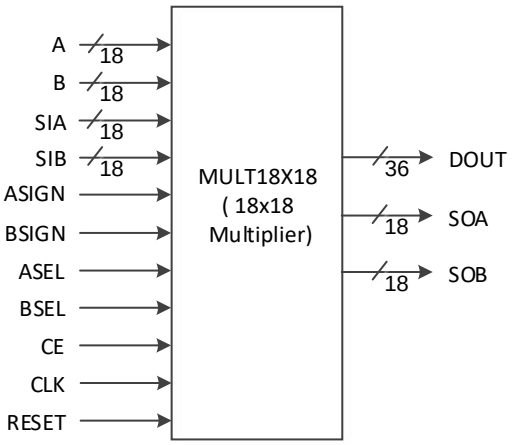


Table 4-3 MULT 18 x 18 Port Signals

Ports Name	I/O	Description
A[17:0]	I	18-bit data input A
SIA[17:0]	I	18-bit shift data input A
B[17:0]	I	18-bit data input B
SIB[17:0]	I	18-bit shift data input B
ASIGN	I	Sign bit for input A
BSIGN	I	Sign bit for input B
ASEL	I	Source select for Multiplier input A (A/SIA)
BSEL	I	Source select for Multiplier input A (A/SIA)
CLK	I	Clock input
CE	I	Clock Enable
RESET	I	Reset input
DOUT[35:0]	O	Multiplier output data
SOA[17:0]	O	Shift data output A
SOB[17:0]	O	Shift data output B

MULT 18 x 18 Attribute

MULT 9 x 18 attributes are listed in Table 4-4

Table 4-4 MULT 18 x 18 Attributes Setting

Attribute Name	Values(default)	Description
AREG	1'b0,1'b1(1'b0)	Registers for A (A/SIA) input ● 1'b0: bypass mode ● 1'b1: registered mode
BREG	1'b0,1'b1(1'b0)	Registers for B (B/SIB)input

Attribute Name	Values(default)	Description
		● 1’b0: bypass mode ● 1’b1: registered mode
ASIGN_REG	1’b0,1’b1(1’b0)	ASIGN input register ● 1’b0: bypass mode ● 1’b1: registered mode
BSIGN_REG	1’b0,1’b1(1’b0)	BSIGN input register ● 1’b0: bypass mode ● 1’b1: registered mode
SOA_REG	1’b0,1’b1(1’b0)	SOA register ● 1’b0: bypass mode ● 1’b1: registered mode
OUT_REG	1’b0,1’b1(1’b0)	Output register ● 1’b0: bypass mode ● 1’b1: registered mode
PIPE_REG	1’b0,1’b1(1’b0)	Pipeline registers ● 1’b0: bypass mode ● 1’b1: registered mode
MULT_RESET_MODE	SYNC,ASYNC(SYNC)	Synchronous or asynchronous reset

4.1.3 MULT 36 x 36

MULT 36 x 36 can be used to implement 36-bit multiplication. A 36x36 multiplier is constructed with one DSP block. The port signals are listed in Table 4-5.The architecture is shown in Figure 4-3.

Figure 4-3 MULT 36 x 36 Architecture

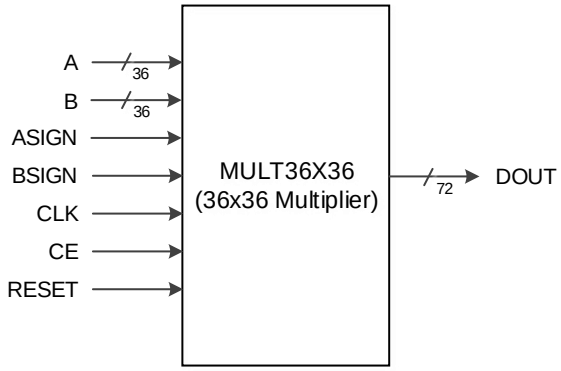


Table 4-5 MULT 36 x 36 Port Signals

Ports Name	I/O	Description
A[35:0]	I	36-bit data input A
B[35:0]	I	36-bit data input B
ASIGN	I	Sign bit for input A
BSIGN	I	Sign bit for input B
CLK	I	Clock input
CE	I	Clock Enable
RESET	I	Reset input
DOUT[71:0]	O	Multiplier output data

MULT 36 x 36 Attribute

MULT 36 x 36 attributes are listed in Table 4-6

Table 4-6 MULT 36 x 36 Attributes Setting

Attribute Name	Values(default)	Description
AREG	1'b0,1'b1(1'b0)	Registers for A input ● 1'b0: bypass mode ● 1'b1: registered mode
BREG	1'b0,1'b1(1'b0)	Registers for B input ● 1'b0: bypass mode ● 1'b1: registered mode
OUT0_REG	1'b0,1'b1(1'b0)	Output0 register ● 1'b0: bypass mode ● 1'b1: registered mode
OUT1_REG	1'b0,1'b1(1'b0)	Output1 register ● 1'b0: bypass mode ● 1'b1: registered mode
PIPE_REG	1'b0,1'b1(1'b0)	Pipeline registers ● 1'b0: bypass mode ● 1'b1: registered mode
ASIGN_REG	1'b0,1'b1(1'b0)	ASIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
BSIGN_REG	1'b0,1'b1(1'b0)	BSIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
MULT_RESET_MODE	SYNC,ASYNC(SYNC)	Synchronous or asynchronous reset

4.2 MULTALU

MULTALU contains 36 x 18 MULTALU and 18 x 18 MULTALU.

MULTALU36 x 18 has three operation modes:

$$DOUT = A*B \pm C$$

$$DOUT = \sum (A*B)$$

$$DOUT = A*B + CASI$$

MULTALU18 x 18 has three operation modes:

$$DOUT = \sum (A*B) \pm C$$

$$DOUT = \sum (A*B) + CASI$$

$$DOUT = A*B \pm D + CASI$$

4.2.1 MULTALU 36 x 18

The port signals of MULTALU 36 x 18 are listed in Table 4-7. The architecture for MULTALU 36 x 18 is shown in Figure 4-4. It can be composed of two 18x18 multipliers and an ALU.

Figure 4-4 MULT 36 x 18 Architecture

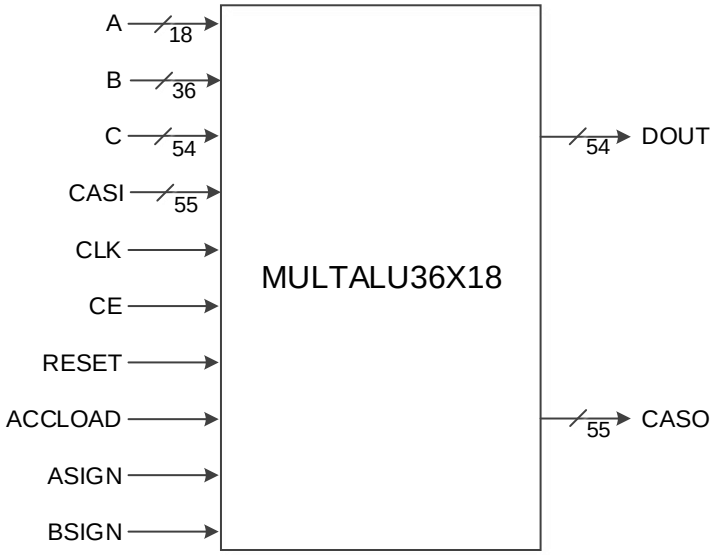


Table 4-7 MULT 36 x 18 Port Signals

Ports Name	I/O	Description
A[17:0]	I	18-bit data input A
B[35:0]	I	36-bit data input B
C[53:0]	I	54-bit data input C
ASIGN	I	Sign bit for input A
BSIGN	I	Sign bit for input B
CLK	I	Clock input
CE	I	Clock Enable
RESET	I	Reset input
ACCLOAD	I	used for accumulator reload selection
CASI[54:0]	I	ALU input from previous DSP block, used for cascade connection
DOUT[53:0]	O	54-bit data output
CASO[54:0]	O	ALU output to next DSP block for cascade connection

MULT 36 x 18 Attribute

MULT 36 x 18 attributes are listed in Table 4-8.

Table 4-8 MULT 36 x 18 Attributes Setting

Attribute Name	Values(default)	Description
AREG	1'b0,1'b1(1'b0)	Registers for A input ● 1'b0: bypass mode ● 1'b1: registered mode
BREG	1'b0,1'b1(1'b0)	Registers for B input ● 1'b0: bypass mode ● 1'b1: registered mode
CREG	1'b0,1'b1(1'b0)	Registers for C input ● 1'b0: bypass mode ● 1'b1: registered mode
ASIGN_REG	1'b0,1'b1(1'b0)	ASIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
BSIGN_REG	1'b0,1'b1(1'b0)	BSIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
ACCLOAD_REG0	1'b0,1'b1(1'b0)	The first stage register of ACCLOAD ● 1'b0: bypass mode ● 1'b1: registered mode
ACCLOAD_REG1	1'b0,1'b1(1'b0)	The second stage register of ACCLOAD ● 1'b0: bypass mode ● 1'b1: registered mode
PIPE_REG	1'b0,1'b1(1'b0)	Pipeline registers ● 1'b0: bypass mode ● 1'b1: registered mode
OUT_REG	1'b0,1'b1(1'b0)	Output register ● 1'b0: bypass mode ● 1'b1: registered mode
C_ADD_SUB	1'b0,1'b1(1'b0)	C_OUT add/subtract selection ● 1'b0: add ● 1'b1: sub
MULTALU36X18_MODE	0,1,2(0)	MULTALU36 operation mode: ● 0：36x18 +/- INC ● 1：ACC/0 + 36x18

Attribute Name	Values(default)	Description
		● 2：36x18 + CASI
MULT_RESET_MODE	SYNC,ASYNC(SYNC)	synchronous or asynchronous

4.2.2 MULTALU 18 x 18

MULTALU 18 x 18 is 18-bit MULTALU. The architecture for MULTALU 18 x 18 is shown in Figure 4-5. The port signals of MULTALU 18 x 18 are listed in Table 4-9.

Figure 4-5 MULT 18 x 18 Architecture

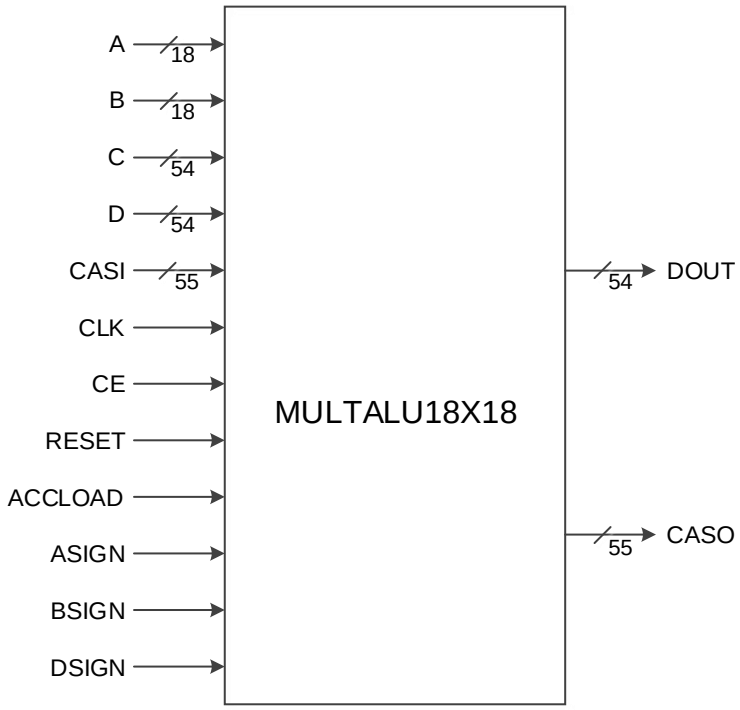


Table 4-9 MULT 18 x 18 Port Signals

Ports Name	I/O	Description
A[17:0]	I	18-bit data input A
B[17:0]	I	18-bit data input B
C[53:0]	I	54-bit data input C
D[53:0]	I	54-bit data input D
ASIGN	I	Sign bit for input A
BSIGN	I	Sign bit for input B
DSIGN	I	Sign bit for input D
CASI[54:0]	I	ALU input from previous DSP block, used for cascade connection
ACCLOAD	I	used for accumulator reload selection

Ports Name	I/O	Description
CLK	I	Clock input
CE	I	Clock Enable
RESET	I	Reset input
DOUT[53:0]	O	Data output
CASO[54:0]	O	ALU output to next DSP block for cascade connection

MULT 18 x 18 Attribute

MULT 18 x 18 attributes are listed in Table 4-10.

Table 4-10 MULT 18 x 18 Attributes Setting

Attribute Name	Values(default)	Description
AREG	1'b0,1'b1(1'b0)	Registers for A input ● 1'b0: bypass mode ● 1'b1: registered mode
BREG	1'b0,1'b1(1'b0)	Registers for B input ● 1'b0: bypass mode ● 1'b1: registered mode
CREG	1'b0,1'b1(1'b0)	Registers for C input ● 1'b0: bypass mode ● 1'b1: registered mode
DREG	1'b0,1'b1(1'b0)	Registers for D input ● 1'b0: bypass mode ● 1'b1: registered mode
DSIGN_REG	1'b0,1'b1(1'b0)	DSIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
ASIGN_REG	1'b0,1'b1(1'b0)	ASIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
BSIGN_REG	1'b0,1'b1(1'b0)	BSIGN input register ● 1'b0: bypass mode ● 1'b1: registered mode
ACCLOAD_REG0	1'b0,1'b1(1'b0)	The first stage register of ACCLOAD ● 1'b0: bypass mode ● 1'b1: registered mode
ACCLOAD_REG1	1'b0,1'b1(1'b0)	The second stage register of ACCLOAD

Attribute Name	Values(default)	Description
		● 1'b0: bypass mode ● 1'b1: registered mode
OUT_REG	1'b0,1'b1(1'b0)	Output register ● 1'b0: bypass mode ● 1'b1: registered mode
PIPE_REG	1'b0,1'b1(1'b0)	Pipeline registers ● 1'b0: bypass mode ● 1'b1: registered mode
MULTALU18X18_MODE	0,1,2(0)	MULTALU18X18 Mode ● 0：ACC/0 +/- 18x18 +/- C ● 1：ACC/0 +/- 18x18 + CASI ● 2：18x18 +/- D + CASI
B_ADD_SUB	1'b0,1'b1(1'b0)	add/subtract selection ● 1'b0: add ● 1'b1: sub
C_ADD_SUB	1'b0,1'b1(1'b0)	add/subtract selection ● 1'b0: add ● 1'b1: sub
MULT_RESET_MODE	SYNC,ASYNC(SYNC)	Synchronous or asynchronous reset

4.3 MULTADDALU

MULTADDALU mode can implement the operation of MULTADD accumulation or reloading. The architecture of MULTADDALU 18 x 18 is shown in Figure 4-6, and the port signals are listed in Table 4-11.

The three operation modes are as follows:

$$DOUT = A0 * B0 \pm A1 * B1 \pm C$$

$$DOUT = \sum (A0 * B0 \pm A1 * B1)$$

$$DOUT = A0 * B0 \pm A1 * B1 + CASI$$

Figure 4-6 MULTADDALU 18 x 18 Architecture

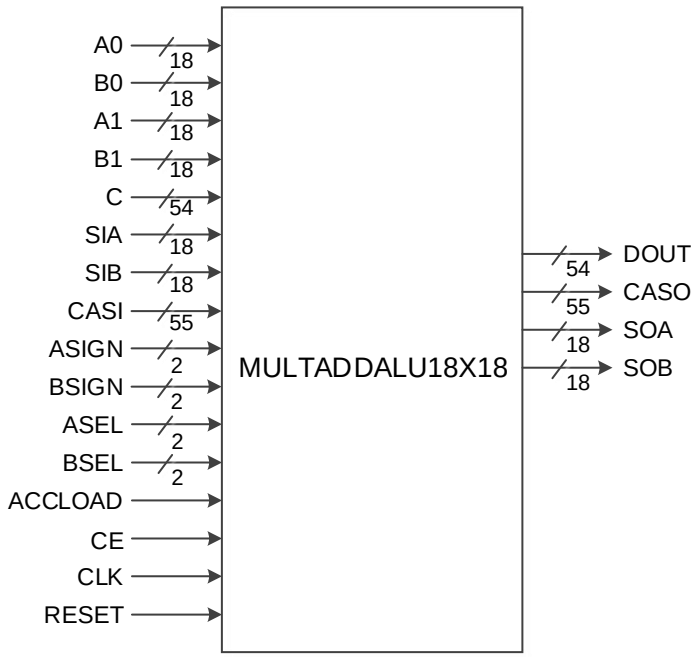


Table 4-11 MULTADDALU 18 x 18 Port Signals

Ports Name	I/O	Description
A0[17:0]	I	18-bit data input A0
B0[17:0]	I	18-bit data input B0
A1[17:0]	I	18-bit data input A1
B1[17:0]	I	18-bit data input B1
C[53:0]	I	54-bit data input C
SIA[17:0]	I	18-bit shift data input A
SIB[17:0]	I	18-bit shift data input B
ASIGN [1:0]	I	Sign bit for input A1/A0
BSIGN[1:0]	I	Sign bit for input B1/B0
ASEL[1:0]	I	Source select for input
BSEL[1:0]	I	Source select for input
CASI[54:0]	I	ALU input from previous DSP block, used for cascade connection
ACCLOAD	I	Used for accumulator reload selection
CLK	I	Clock input
CE	I	Clock Enable
RESET	I	Reset input
DOUT[53:0]	O	Data output

Ports Name	I/O	Description
CASO[54:0]	O	ALU output to next DSP block for cascade connection
SOA[17:0]	O	Shift data output A
SOB[17:0]	O	Shift data output B

MULT 18 x 18 Attribute

MULT 18 x 18 attributes are listed in Table 4-12.

Table 4-12 MULT 18 x 18 Attributes Setting

Attribute Name	Values(default)	Description
A0REG	1'b0,1'b1(1'b0)	Registers for A0/SIA input ● 1'b0: bypass mode ● 1'b1: registered mode
A1REG	1'b0,1'b1(1'b0)	Input register for A1 or AOREG output ● 1'b0: bypass mode ● 1'b1: registered mode
B0REG	1'b0,1'b1(1'b0)	Registers for B0/SIB input ● 1'b0: bypass mode ● 1'b1: registered mode
B1REG	1'b0,1'b1(1'b0)	Input register for B1 or BOREG output ● 1'b0: bypass mode ● 1'b1: registered mode
CREG	1'b0,1'b1(1'b0)	Registers for C input ● 1'b0: bypass mode ● 1'b1: registered mode
PIPE0_REG	1'b0,1'b1(1'b0)	Pipeline registers for multiplier 0 ● 1'b0: bypass mode ● 1'b1: registered mode
PIPE1_REG	1'b0,1'b1(1'b0)	Pipeline registers for multiplier 1 ● 1'b0: bypass mode ● 1'b1: registered mode
OUT_REG	1'b0,1'b1(1'b0)	Output register ● 1'b0: bypass mode ● 1'b1: registered mode

Attribute Name	Values(default)	Description
ASIGN0_REG	1'b0,1'b1(1'b0)	ASIGN input register 0 ● 1'b0: bypass mode ● 1'b1: registered mode
ASIGN1_REG	1'b0,1'b1(1'b0)	ASIGN input register1 ● 1'b0: bypass mode ● 1'b1: registered mode
BSIGN0_REG	1'b0,1'b1(1'b0)	BSIGN input register 0 ● 1'b0: bypass mode ● 1'b1: registered mode
BSIGN1_REG	1'b0,1'b1(1'b0)	BSIGN input register 1 ● 1'b0: bypass mode ● 1'b1: registered mode
ACCLOAD_REG0	1'b0,1'b1(1'b0)	The first stage register of ACCLOAD ● 1'b0: bypass mode ● 1'b1: registered mode
ACCLOAD_REG1	1'b0,1'b1(1'b0)	The second stage register of ACCLOAD ● 1'b0: bypass mode ● 1'b1: registered mode
SOA_REG	1'b0,1'b1(1'b0)	SOA register ● 1'b0: bypass mode ● 1'b1: registered mode
MULTADDALU18X18_MODE	0,1,2(0)	MULT 18 x 18 mode: ● 0：18 x 18 +/- 18 x 18 +/- C ● 1：ACC/0 + 18 x 18 +/- 18 x 18 ● 2：18 x 18 +/- 18 x 18 + CASI
B_ADD_SUB	1'b0,1'b1(1'b0)	add/subtract selection ● 1'b0: add ● 1'b1: sub
C_ADD_SUB	1'b0,1'b1(1'b0)	add/subtract selection ● 1'b0: add ● 1'b1: sub
MULT_RESET_MODE	SYNC,ASYNC(SYNC)	Synchronous or asynchronous reset

5 DSP Invocation

For the details about DSP configuration and invocation, please refer to *Gowin IP Core Generator User Guide >3 IP Core Generation>3.2 DSP*.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