Understanding Metastability in FPGAs

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Abstract

A condition known as metastability occurs when a signal is passed across circuits in unrelated or asynchronous clock domains, which can lead to system failure in FPGAs. This document abstracts the ALTERA white paper named "Understanding Metastability in FPGAs".

1 Introduction

- Importance of timing in digital circuits
- Definition of metastability
- Why metastability is a concern in FPGAs

To ensure reliable operation, a register's input must be constant for a predetermined period of time before and after the clock edge. If a data signal transition does not satisfy the setup-time or hold-time requirements of the register, the output of the register may enter a metastable situation. A steady, defined state is frequently returned rapidly by registers.[1]

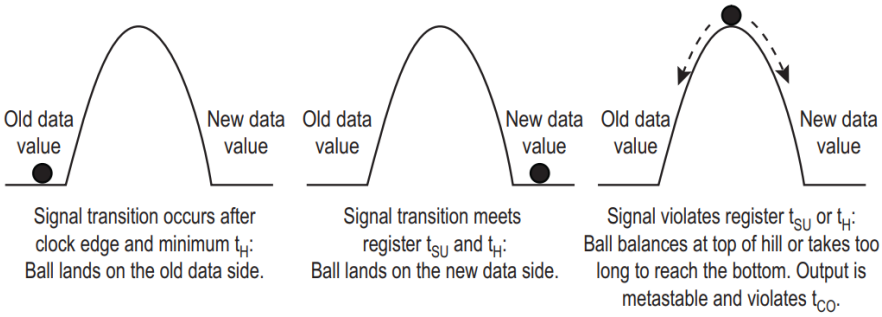

Figure 1: Visualisation of Metastability

2 Metastability in FPGA Designs

- Impact on synchronous and asynchronous designs
- Cross-domain clock transfer challenges
- Examples of metastability issues in FPGA circuits

After beginning in a low state, the data output signal becomes metastable and oscillates between high and low states.

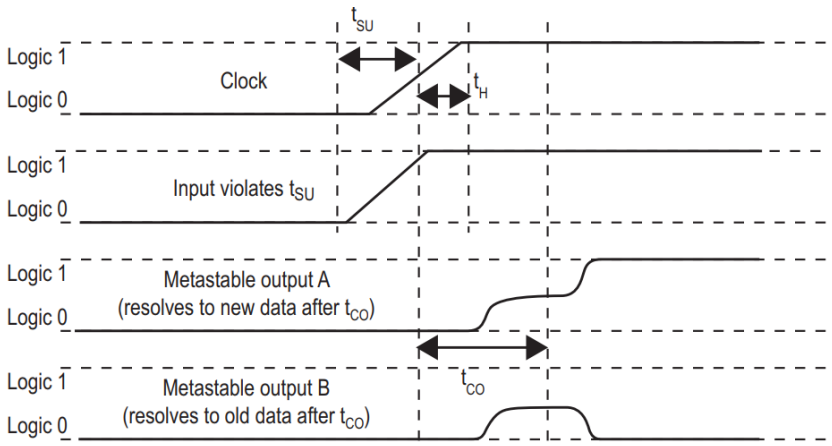

Figure 2: Example of Metastable Output Signals

3 Mitigation Techniques

- Use of multi-stage synchronizers
- Handshaking protocols
- FIFO-based solutions
- CDC (Clock Domain Crossing) design best practices

The metastable signal has no adverse effect on system operation if the data output signal resolves to a legitimate state prior to the subsequent register capturing the data. However, the system may fail if the metastable signal does not resolve to a low or high state before it reaches the next design register.

4 Practical Considerations and Simulations

- Simulation of metastability events
- Measuring MTBF (Mean Time Between Failures)
- FPGA vendor-specific solutions (Xilinx, Intel, etc.)

A signal must be synchronized to a new clock domain before it can be utilized as it moves across circuitry in unrelated or asynchronous clock domains. To overcome failures, a synchronizer chain is employed. The time available for a metastable signal to settle is known as the metastability settling time, and it is found in the timing slack present in the synchronizer register to register routes.

- The registers in the chain are all clocked by the same or phase-related clocks.

- The first register in the chain is driven from an unrelated clock domain, or asynchronously.
- Each register fans out to only one register, except the last register in the chain.

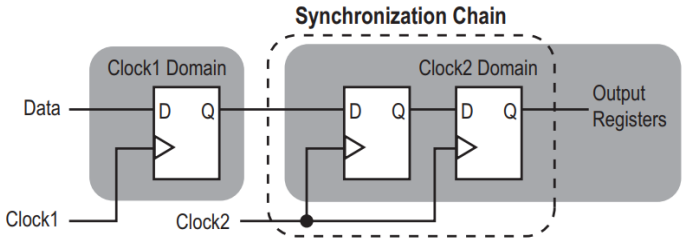

Figure 3: Synchronizer Chain

The calculation of the MTBF is:

$$MTBF = \frac{e^{t_{MET}/C_2}}{C_1 \cdot f_{CLK} \cdot f_{DATA}}$$

Figure 4: Formula for Calculating MTBF

- C_1, C_2 are constants.
- f_{clk} is the clock frequency.
- f_{data} is the toggling frequency of the asynchronous input data signal.
- t_{met} is the available metastability settling time or timing slack available beyond the register's t_{co}.

5 Characterizing Metastability Constants

FPGA vendors can characterize the FPGA for metastability in order to identify the constant parameters in the MTBF equation. When testing MTBF under unrealistic circumstances, a test circuit may be employed. A test circuit is available for the characterizing constants.

There are two separate clocks in this design. Every clock cycle, the synchronizer's data input toggles (f_{data}). There are two locations for the synchronizing register. The output of the synchronizer is recorded in destination registers one

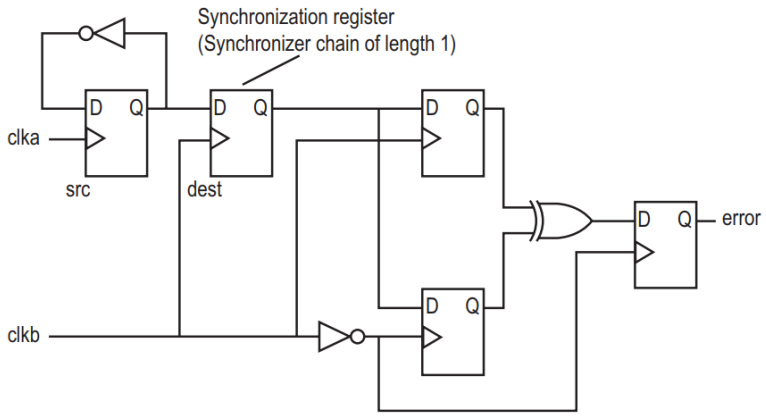

Figure 5: A Test Circuit for Calculating MTBF

clock cycle and one half-clock cycle later. The circuit recognizes that the sample signals are distinct and emits an error signal if the signal becomes metastable before resolving at the subsequent clock edge. A significant percentage of the metastability events that take place at the half-clock cycle time are detected by this circuitry. A logarithmic scale is used to illustrate the MTBF versus t_{met} results of the test conducted with various clock frequencies. The C_1 constant scales linearly, while the C_2 constant responds to the trend line's slope.

6 Conclusion

- Summary of key points
- Best practices for FPGA designers

Due to the exponential term e^{t_{met}/C_2}, it has the largest effect on MTBF. The C_2 constant depends on the technology used to manufacture the device, with faster technologies generally having different characteristics. In most cases, metastability is not the main concern for designers.

To improve metastability MTBF, designers can increase t_{met} by adding extra register stages to the synchronizer chain. A three-stage synchronizer is typically recommended.

References

[1] Altera, "Understanding metastability in fpgas," white paper, Altera Corporation, 2009.