UVVM

- UVVM (Universal VHDL Verification Methodology) offers a structured and simple framework for VHDL testbenches
- Test harnesses using UVVM can be built quickly by connecting verification components (VVCs) to DUT interfaces.
- The UVVM framework leverages global signals for easy connection between test sequencers and verification components.
- UVVM allows parallel command distribution to verification components without time penalties.
- Synchronization of transactions is achieved through commands like `await_value()` and `await_completion()`.
- `await_completion()` helps synchronize events and provides clear visibility of test execution flow.
- VVC Framework allows fine control of timing skew between interfaces for cycle-accurate verification.
- VVCs support buffer management for transmitting and checking data blocks.
- Data coverage goals can be defined to control transmission until desired verification completeness is achieved.
- The core structure of a VVC includes a Command Interpreter, Command Queue, and Command Executor.
- The Executor implements protocol-specific behavior, such as transmit/receive or read/write operations.
- Existing free VVCs include support for UART, AXI4-Lite, Avalon MM, I2C, and SBI interfaces.
- UVVM promotes simplicity and clarity, reducing complexity compared to traditional verification approaches.