

GFIR-55: WP275 Summary

This whitepaper explains the best practices for optimizing the size of FPGA designs. It highlights that optimizing the use of LUTs, and flip-flops can improve performance and reduce device size. The design should use single-level logic because it offers lower latency and a smaller area. Also, using four-input LUTs correctly allows more functions to be performed at one logic level.

Using reset signals unnecessarily can increase design size, and reduce performance. Since FPGAs start in a known state after configuration, a global reset is usually not needed. If a reset is required, an asynchronous reset should be used and connected directly to the flip-flops's reset input. (WP272 in detail)

The priority order of signals is important. Reset signal has the highest priority, followed by set, enable, and data input. Following these rules prevents LUTs from being overloaded with a control logic mechanism.

Coding should follow some rules to save space and improve performance. For example, avoid unnecessary logic levels, and use two-level logic only when necessary. Also, use the internal control signals of flip-flops correctly. As shown in the examples on whitepaper, these techniques can reduce the design size by up to 50%.