**Chapter 8: Names**

Chapter 8 focuses on the concept of names in VHDL, which are identifiers used to refer to objects, types, subprograms, and other design elements. Names ensure clarity, organization, and accessibility in a VHDL design.

**8.1 General**

* Purpose: Names uniquely identify design elements and enable referencing them in expressions, statements, and configurations.
* Types of Names: Includes simple names, selected names, indexed names, slice names, attribute names, and external names.

**8.2 Simple Names**

* Refer to declared entities within a specific scope**.**



**8.3 Selected Names**

* Refer to elements within a hierarchical design or package.
* Syntax: <prefix>.<suffix>

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**8.4 Indexed Names**

* Access individual elements in arrays or vectors using an index.
* Syntax: <array\_name>(<index>)



**8.5 Slice Names**

* Refer to a subset of an array or vector.
* Syntax: <array\_name>(<range>)

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**8.6 Attribute Names**

* Refer to attributes of objects, such as predefined attributes ('event, 'length, etc.) or user-defined attributes.
* Syntax: <object>'<attribute>

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**8.7 External Names**

* Refer to objects or entities external to the current design unit, useful for modular and hierarchical designs.



**From :** <https://adaptivesupport.amd.com/s/question/0D54U00007hX4mrSAC/vhdl-external-name-alias-for-internal-array-signal-not-being-resolved?language=en_US>

**Chapter 9: Expressions**

Chapter 9 focuses on expressions in VHDL, which are combinations of operators and operands used to compute values, control behavior, or specify conditions. Expressions are fundamental for describing hardware behavior.

**9.1 General**

Expressions: Formed by combining operands (constants, variables, signals, or literals) with operators.

Usage: Used in assignments, conditions, and computations throughout a design.

**9.2 Operators**

Operators define operations on operands. They are categorized as:

1. **Arithmetic Operators**:
   * Perform mathematical operations.
   * Examples: +, -, \*, /, mod, rem.
2. **Relational Operators**:
   * Compare two operands and return a boolean.
   * Examples: =, /=, <, <=, >, >=.
3. **Logical Operators**:
   * Perform bitwise or boolean operations.
   * Examples: and, or, nand, nor, xor, not.
4. **Shift Operators**:
   * Shift the bits of operands.
   * Examples: sll, srl, sla, sra, rol, ror.
5. **Concatenation Operator**:
   * Combines elements into an array or string.
   * Example: &.
6. **Miscellaneous Operators**:
   * Include unary operators like + and - for sign operations.

**9.3 Operands**

Operands are the entities acted upon by operators:

* **Literals**: Constant values like 10, '1', or "1010".
* **Names**: References to signals, variables, or constants.
* **Function Calls**: Results of subprogram executions.
* **Qualified Expressions**: Specify the type of a literal or expression.

**9.4 Static Expressions**

* Computed entirely at compile-time.
* Used in constant declarations or constraints.

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**9.5 Universal Expressions**

* Expressions involving universal types like integers or real numbers.
* Automatically converted to specific types when necessary.

**Chapter 10: Sequential Statements**

Chapter 10 describes sequential statements in VHDL, which are used to control the flow of execution in processes, functions, and procedures.

**10.1 General**

* Sequential Statements: Specify the behavior of a design in processes or subprograms.
* Execute in a defined sequence, unlike concurrent statements.

**10.2 Wait Statement**

* Suspends execution of a process until a condition is met.

**10.3 Assertion Statement**

* Verifies conditions during simulation and reports errors or warnings if conditions are false.

**10.4 Report Statement**

* Displays messages during simulation for debugging.

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**From:** <https://peterfab.com/ref/vhdl/vhdl_renerta/mobile/source/vhd00007.htm>

**10.5 Signal Assignment Statement**

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  Description automatically generatedAssigns values to signals

**10.6 Variable Assignment Statement**

* Updates the value of a variable immediately.
* Updates the value of a variable immediately.

**10.7 Procedure Call Statement**

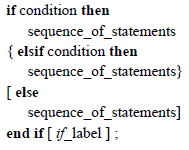
* Invokes a procedure to perform a specific task.

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Description automatically generated

**From:** <https://peterfab.com/ref/vhdl/vhdl_renerta/mobile/source/vhd00052.htm>

**10.8 If Statement**

* Conditional execution of statements.

**10.9 Case Statement**

* A screenshot of a computer program

  Description automatically generatedExecutes one of several branches based on a value.

**10.10 Loop Statement**

* A close up of a text

  Description automatically generatedRepeats a set of statements

**10.11 Next Statement**

* A white screen with black text

  Description automatically generatedSkips the remaining statements in the current iteration of a loop.

**From:** https://ics.uci.edu/~jmoorkan/vhdlref/nexts.html

**10.12 Exit Statement**

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  Description automatically generatedTerminates a loop prematurely.

**From:** <https://peterfab.com/ref/vhdl/vdlande/exits.html>

**10.13 Return Statement**

* Exits a subprogram and optionally returns a value.

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Description automatically generated

**From:** <https://docs.amd.com/r/en-US/ug901-vivado-synthesis/Relaxed-Return-Rules-for-Function-Return-Values>

**10.14 Null Statement**

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  Description automatically generated with medium confidencePlaceholder for no operation.

From: <https://peterfab.com/ref/vhdl/vhdl_renerta/source/vhd00045.htm>