# WP01082 SUMMARY

* MTBF: Mean Time Between Failures
* There are timing requirements for registers to correctly capture data at its inputs and produce an output signal.
* To ensure reliable operation:
* The input must be stable for a minimum time before clock edge (setup time tSU).
* The input must be stable for a minimum time after clock edge (hold time tH).
* After that, the output is available after the clock-to-output delay (tCO).
* If a data signal transition violates a register’s tSU or tH requirements, the output of the register **may** go into a metastable state.
* Metastability problems commonly occur when a signal is transferred between circuitry in unrelated or

asynchronous clock domains.

A diagram of a device

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* If the data output signal resolves to a valid state before the next register captures the data, then the metastable signal does not negatively impact the system operation.
* If the metastable signal does not resolve to a low or high state before it reaches the next design register, it can cause the system to fail.

A diagram of a synchronization scheme

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* The extra synchronization registers allow additional time for a potentially metastable signal to resolve to a known value before the signal is used in the rest of the design. The timing slack available in the synchronizer register-to-register paths is the time available for a metastable signal to settle and is known as the available metastability settling time.
* tMET = TCLK – tCO\_1 – tSU\_2

tMET = Arrival Time of Next Clock Edge - Setup Time of Next Register - Output Time of First Register (assuming path delay between the two registers is negligible)

* The MTBF of a synchronizer chain is calculated with the following formula and parameters: A black text on a white background

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* The C1 and C2 constants depend on the device process and operating conditions.
* fCLK is the clock frequency of the clock domain receiving the asynchronous signal.
* fDATA is the toggling frequency of the asynchronous input data signal.
* The tMET for a synchronization chain is the sum of the output timing slacks for each register in the chain.
* tMET\_total = tMET1 + tMET2 = (TCLK - tCO\_1 - tSU\_2) + (TCLK - tCO\_2 - tSU\_3)

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* The exponential factor in the MTBF equation means that an increase in the design-dependent tMET value increases a synchronizer MTBF exponentially.
* To improve metastability MTBF, designers can increase tMET by adding extra register stages to synchronization register chains. The timing slack on each additional register-to-register connection is added to the tMET value.

# EXTRAS

A diagram of a clock and data

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* *"The window of time relative to the clock edge where metastability will actually be triggered is much smaller than the window defined by the setup and hold times (on the order of femtoseconds in modern FPGAs), however it’s exact location is not known and is a function of a number of variables including temperature and voltage. Meeting the setup and hold requirements guarantees a metastable state will not be triggered."*

A close-up of a newspaper

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* Once a FF goes metastable (due to a setup time violation, say) we can’t say when it will assume a valid logic level or what level it might eventually assume
* If you need to fan out a synchronized signal, synchronize **once** at a single point, then **distribute the synchronized version** to other modules.
* For Bus Synchronization, it is wrong to use single bit synchronizers on each bit.

A diagram of a diagram

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* Handshaking mechanisms can be used, but the bandwidth at the clock domain crossing is reduced since multiple cycles of handshake mechanism are needed for each data package. Dual-port FIFOs can be used to compensate for this problem.