The first sentence of the report seems like the shortest summary of what is left: It is mentioned that the smart thing to do about reset is not global but local.

Although global reset is quite popular in the FPGA community, it is a controversial issue. Therefore, the reasons why local reset is advocated are explained together with the reasons.

Press switch, power supply and microprocessor are typical sources that trigger the global reset signal. When we look at these situations, it is seen that the reset signal is slow. However, this may not be true. Because statistically, with the increase in clock speed, problems can also be seen in global reset. Frankly, triggering a long reset signal from the clock signal may seem logical at first because we think that we are sure that all flip flops are reset. However, the point to consider is the situation of disabling the reset signal.

Although the GSR in the device is in silicon, it cannot be assumed that it works flawlessly. This signal has high fanout and the start sequence can be synchronized to the user clock. However, another point to consider here is that there are multiple clock and clock phase generators in the FPGA. In this case, the global reset cannot be synchronized to all clocks in an FPGA at the same time.