**DSP : Designing for Optimal Results**

**Chapter 1 : Digital Signal Processing Design Challenges**

* Traditional processors cannot provide high performance in designs as algorithm complexity increases. Due to their ability to process in parallel and their flexible architectures, FPGAs can operate at high performance in complex algorithms.
* **XtremeDSP Slice** is a high-speed (500 MHz), low-power (2.3 mW/100 MHz), and efficient DSP processing unit found in Xilinx Virtex-4 FPGAs. With parallel processing and cascade logic, it enables fast and cost-effective execution of complex filters and DSP operations.
  + **High Performance** – Operates at 500 MHz, delivering superior DSP processing power.
  + **Low Power Consumption** – Each slice consumes only 2.3 mW/100 MHz.
  + **Efficient Hardware Design** – Optimized and fast due to its hard-coded IP structure.
  + **Cascade Logic** – Multiple slices can be connected to execute complex filters and operations at high speed.
  + **Smaller FPGA Usage** – Achieves the same functionality with less FPGA resources.
  + **Cost Advantage** – Reduces overall system cost by requiring smaller FPGAs and consuming less power.
  + **Compatibility with Programmable DSP Systems** – Enhances system performance as a pre-processor or co-processor.
* DSP48E is a more advanced and optimized version of the XtremeDSP Slice (DSP48), offering higher processing capacity, lower power consumption, and greater flexibility. (This information is external)

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**Chapter 2 : XtremeDSP Design Considerations**

* Key Features of DSP48 Slices:
* 18x18 bit multiplier, 36-bit result, and 48-bit sign extension
* 3-input 48-bit adder/subtracter with accumulator feedback support
* Dynamic mode control to switch functions between clock cycles
* 18-bit B and 48-bit P buses for cascaded input and output connections
* 17-bit right shift support for high-precision multiplication and arithmetic
* Symmetric rounding, selectable pipelining, and high clock frequency support
* "C" input port for multiply-add, three-operand addition, and rounding operations
* Separate reset and clock enable signals, OPMODE multiplexers
* DSP48 Slice Attributes :

 **AREG, BREG**: Defines the pipeline registers in the A and B input paths

(0, 1, or 2)

 **CREG, MREG, PREG**: Controls the pipeline registers at the multiplier (MREG) and adder (PREG) outputs (0 or 1)

 **CARRYINREG, CARRYINSELREG, OPMODEREG, SUBTRACTREG**: These paths can have pipeline registers set to 0 (none) or 1 (present)

 **B\_INPUT**: Determines whether the B input is routed from the parallel input (DIRECT) or cascaded from the previous slice (CASCADE)

 **LEGACY\_MODE**: Specifies whether the multiplier is "flow-through" and indicates which path is used in the timing analysis. A mismatch with MREG causes an error

* To summarize the timing tools behavior:

 **NONE**: Skips the multiplier, achieving the highest performance (MREG = 1)

 **MULT18x18**: Uses the path through the multiplier (MREG = 0)

 **MULT18x18S**: Uses a pipelined multiplier (MREG = 1)

A diagram of a machine

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* This figure is simplified model of DSP48
* The A and B input can be used directly or multiplied
* The C input can be used addition and substraction process
* The P input is the output from previous DSP48 slice, in this way DSP48 slices can be connected to each other
* The DSP48 slice includes all of the above elements, which makes it ideal to implement digital filter functions.
* Multichannel FIR filters has multiple data input stream. This is used in video streams.
* Direct form FIR filters implementation with adder tree or adder cascade options.

A diagram of a diagram

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**FIR Filter Adder Tree Using DSP48 Slice**

A diagram of a machine

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**FIR Filter With Adder Cascade**

* DSP48 Slices compatible with various size inputs but this is according to performance and resources requirement.
* DSP48 slices provide the various funtion such as multiply, multiply with feedback and accumulation. Function selection is according to OPMODEs.

**Chapter 3 : DSP48 Slice Math Functions**

* DSP48 Slice contains adder/subtracter unit.
* Fallowing the this equation. Output = Z ± (X + Y +CIN). This equation contain the multiplexers in the DSP48 Slice.
* DSP48 Slice can implement add and accumulate functions with up to 36-bit inputs.
* Output = Output + A:B + C
* Output = Shift(P) ± (A:B + C)
* Output = 0 ± (A:B +C)
* The above equations use for accumulate functions. The functions selected by OPMODEs.
* DSP48 slice can multiply two 18-bit numbers and perform addition or subtraction. The result can be processed with the previous product, zero, or a shifted product. Name of this feature is Multiply Accumulate (MAC).
* DSP48 Slice has 3:1 Y mux, 4:1 X mux and 6:1 Z mux.
* Barrel shifter can be implemented using the two DSP48 Slice.
* DSP48 Slice can be used as a counter to count up by one on each clock cycle. Additionally, can be used subtraction input for counting down.
* Binary division in the DSP48 slice can be performed using shift and subtract or multiply and subtract. Its built-in shifter, multiplier, and adder/subtracter units support this operation.
* Square root is computed using successive multiplication and subtraction. An N-bit number's square root has N/2 bits. For fractional results, N/2 cycles compute the integer part, and later cycles compute the fractional part.

**Chapter 4 : MAC FIR Filters**

* MAC FIR Filters performs multiplication operations sequantially. This situation, while improves resources using, reduces performance. MAC FIR Filters performance is calculated by this equation :

**Maximum Input Sample Rate = Clock Speed / Number of Taps**

* If the coefficients possess a symmetric shape, the maximum sampled rate is doubled but this conditions has costlier structure.
* The following image demonstrates structure of Single Multiplier MAC FIR Filter

A diagram of a computer

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* The following image demonstrates stucture of Symmetric MAC FIR Filter.

A diagram of a computer system

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* In FIR filters, bit width increases, so it is limited by rounding and quantization. For rounding and quantization, the full-precision output must be calculated using the generic saturation level and coefficient-specific saturation level techniques.
* If embedded block RAMs are used for data flow control, resource usage decreases.
* The multiplier number can be increased to increase the value of sample rate. The following image shows the Dual-Multiplier MAC FIR Filter structure.

A diagram of a computer

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**Chapter 5 : Parallel FIR Filters**

* The performance of parallel FIR filters calculated by this equation :

Maximum Input Sample Rate = Clock Speed

* In transpose fir filter, input data is broadcast to all multipliers simultaneously. The following image demonstrates the sturcture of transpose FIR filter

A diagram of a machine

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* The adventages to using the Transposed FIR filter are low latency, efficent mapping to the DSP48 slice, no external logic. The disadvantage is that limited performance according to number of filter taps.
* The systolic FIR filter is considered an optimal solution for parallel filter architectures. The following image demonstrates the systolic FIR filter also uses adder chains to fully utilize the DSP48 slice architecture

A diagram of a machine

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* The adventages to using the Systolic FIR filter are highest performance, efficent mapping to the DSP48 slice, no external logic. The disadvantage is higher latency.
* The symmetric systolic FIR filter is very powerful in parallel FIR filters because it reduces the required number of multipliers by half. This provides an advantage due to the limited number of DSP48 slices. The following image demonstrates structure of symmetric systolic FIR filter.

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• One of the disadvantages of this filter type is the use of external sources.

**Chapter 6 : Semi Parallel FIR Filters**

* In semi parallel FIR filters, maximum sample rate, number of multipliers and number of clock cycle per result calculated by the following equations :

Maximum Input Sample rate = (Clock speed / Number of Coefficients) x Number of Multipliers

Number of Multipliers = (Maximum Input Sample rate x Number of Coefficients) / Clock speed

Number of Clock cycles per result = Number of Coefficients / Number of Multipliers

* In semi-parallel FIR filter implementation, the maximum sample rate is lower when using block RAM compared to distributed RAM. However, when the number of coefficients increases, resource usage may not be optimized, making it necessary to use block RAM.

**Chapter 7 : Multi Channel FIR Filters**

* In a typical multi-channel filtering scenario, multiple input channels are filtered using a separate digital filter for each channel.
* The following image demonstrated by the structure of 6-input, 8 tap multi channel FIR filter

A diagram of a computer system

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* The input samples contain a 7-cycle delay.
* The SRL16E is a very compact and efficient memory element.
* At each clock cycle, the counter selects a different input and sends it to the SRL16E shift register. After six cycles, the six input samples are sequentially loaded into a single stream.
* Coefficients are stored in SRL16. A single set is used if shared; otherwise, six SRL16s or RAMs are needed. Loading takes six cycles, and RAM reduces filter speed.