**Understanding Metastability in FPGAs**

* Metastability can cause the system failure in digital devices.
* All registers in FPGA have the timing requirements.
* For a register to operate correctly:
  + tsu (Setup Time): The data must remain stable for a certain period before the clock edge.
  + th (Hold Time): The data must remain stable for a certain period after the clock edge.
  + tco (Clock-to-Output Delay): The time it takes for the output to stabilize after the clock edge.

A diagram of a device

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* This figure demonstrates the tsu violation. As a result of the violation, the A and B outputs stabilized after the minimum tco time. The A and B outputs behaved differently, with one reaching the logical 1 level and the other settling at the logical 0 level.
* When transferring data between clock domains, synchronization is required.
* To prevent metastability in asynchronous signal transfers, a sequence of registers (synchronization chain) is used to synchronize the signal to the new clock domain. These registers provide extra time for the metastable signal to settle, and the length of the chain depends on the number of synchronized registers.
* Asynchronous signals or those between unrelated clock domains can change unpredictably, making their transitions difficult to predict. To manage this, designers use techniques like dual-clock FIFO or handshaking logic to allow signals time to settle and avoid metastability, ensuring proper system function.
* MTBF estimates the average time between instances when metastability could cause a design failure.
* A high MTBF indicates a more robust design and reduced metastability issues.

A black and white image of a mathematical equation

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* C1 and C2 constants depend on the device process and conditions. fCLK is the receiving clock domain frequency, and fDATA is the data toggle frequency. Faster frequencies reduce MTBF. tMET represents the available time for metastability to resolve and the timing slack of each register in the synchronization chain.
* The overall design MTBF depends on each synchronizer chain's MTBF. The failure rate is calculated by adding the failure rates of each chain.

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* FPGA vendors determine MTBF parameters by characterizing metastability. Altera uses a test circuit with a short, measurable MTBF.
* The tMET/C2 term has a big impact on the MTBF calculation. Metastability can be improved by optimizing the C2 constant or increasing the tMET.
* The metastability C2 constant depends on the process technology and supply voltage. As the voltage decreases, metastability MTBF worsens. Altera has optimized the FPGA architecture to improve metastability.

**Additional**

* Do not synchronize the same asynchronous signal in multiple places this may cause inconsistent behavior.
* Using synchronization chains for each bit is incorrect; a bus structure should be used instead.
* MTBF values can be indirectly measured using the "report\_synchronizer\_mtbf" command in the Vivado tool.(But not supported all Xilinx FPGA families)
* The timing slack in the paths between flip-flops allows metastable signals to settle. This duration is called the "available settling time."
* In the MTBF calculation, the total of the slacks at each stage of the synchronizer chain is used.