**White Paper – 272 Summary**

* The de-assertion of the reset signal must be synchronized with the clock signal to ensure proper operation of all flip-flops; otherwise, metastability and inconsistencies may occur.
* When the reset signal is released asynchronously to the clock, flip-flops become active at different times, and some may enter metastability. This risk increases with higher clock frequencies.
* The reset must be handled carefully in circuits with feedback, while in circuits without feedback, a reset is not actually necessary.
* **Reset Costs**
  + **Consumes routing resources**: Reduces freedom for other connections, potentially lowering system performance.
  + **Consumes logic resources**: Increases design size by using extra logic and flip-flops.
  + **Prevents efficient feature usage**: Prevents features like SRL16E from being fully utilized due to lack of reset support.
  + **Affects system performance**: Additional logic levels and increased placement time impact performance.
  + **Increases place and route time**: Adding a reset signal lengthens placement and routing times.