**White Paper – 272 Summary**

* The de-assertion of the reset signal must be synchronized with the clock signal to ensure proper operation of all flip-flops; otherwise, metastability and inconsistencies may occur.
* When the reset signal is released asynchronously to the clock, flip-flops become active at different times, and some may enter metastability. This risk increases with higher clock frequencies.
* The reset must be handled carefully in circuits with feedback, while in circuits without feedback, a reset is not actually necessary.
* **Reset Costs**
  + **Consumes routing resources**: Reduces freedom for other connections, potentially lowering system performance.
  + **Consumes logic resources**: Increases design size by using extra logic and flip-flops.
  + **Prevents efficient feature usage**: Prevents features like SRL16E from being fully utilized due to lack of reset support.
  + **Affects system performance**: Additional logic levels and increased placement time impact performance.
  + **Increases place and route time**: Adding a reset signal lengthens placement and routing times.

**White Paper – 275 Summary**

* In the design, LUT usage should be **minimized** as much as possible; otherwise, a performance drop may occur.
* Each flip-flop has a set of dedicated control inputs to support set, reset, and clock enable controls.
* The flip-flops can not support a mixture of asynchronous and synchronous controls on the same flip-flop.
* When an asynchronous global reset is used, if a local reset is required, it leads to dedicating a pin for the local synchronous reset within the LUT, which can increase the use of the LUT and decrease performance.
* To optimize a design, it is necessary to examine the flip-flops available in the FPGA and design accordingly.
* The priority states of a flip-flop are given below as an example. The characteristics of the flip-flops to be used in designs should be examined. This way, by optimizing resource usage in the design, performance improvements can be achieved.

A diagram of a clock

AI-generated content may be incorrect.