**WP272**

**WHAT IS WP272 ?**

The Xilinx White Paper **WP272**, titled **"Get Smart About Reset: Think Local, Not Global"**, focuses on effective reset strategies in FPGA design. It challenges the traditional use of **global reset signals** and advocates for **local reset techniques** to improve design efficiency, reliability, and performance.

* Although the global reset signal is generally considered not to be timing-critical, it is emphasized that the de-assertion of the reset signal becomes a timing-critical event, especially at high clock frequencies.
* The circuits that include feedback and a state machine may become unstable if the reset is not handled correctly.
* Since Xilinx FPGAs have embedded processors, they automatically initialize registers, minimizing the need for global resets
* A localized reset network synchronizes the reset of critical flip-flops with the clock, reducing timing errors and ensuring a more reliable FPGA design. Related to this sentences, I added new vhdl files that name is async\_reset\_ctrl