**CS 303 Logic and Digital System Design** Assigned : 16/04/2024
Laboratory Assignment #03 Pre-lab due : 21/04/2025 23:59

### An Up/Down Counter

We would like to design a single digit hexadecimal up/down counter, which counts up (i.e., ...0, 1, 2, ..., D, E, F, 0, ...) when button UP is pressed, and counts down (i.e., ...1, 0, F, E, ...) when button DOWN is pressed. Each button press should increment or decrement the counter by only one. As an example, if the current count is 5, the generation of the sequence 5-6-7-8 should require 3 consecutive clicks on the UP button. (If you still in doubt with the operation, ask your TA or your instructor. A demo will be done during class hours.)

You are provided with a project template in *Digital* in a file named *lab3pre.zip*. The top design is in *testbench.dig*. When opened, a module named *controller.dig* will be seen along a seven segment display, and a clock input with 100 Hz frequency. Additionally, two buttons labeled UP and DOWN are present, which will be used to increment or decrement the counter, respectively.

You are expected to place your counter design in *controller.dig*. Inside this module, you are provided with a syncronous up/down counter. The counter will increment or decrement as long as the respective input is asserted, hence a direct connection from the buttons to these inputs will not do.

Requirements:

- Full synchronous design: all FFs to be driven with the 100 Hz clock, and no clock gating.
- Full schematic design.

Submit your *controller.dig* which contains your design. Do not change any of the input/output terminals.

In addition, you will need to set-up the FPGA toolchain for the synthesis of this circuit, for which additional instructions will be provided promptly.

### In-lab

During the laboratory session, you will export your circuit in *controller.dig* to a verilog file named *controller.v* You will be provided with some additional supporting files, so that you will be able to test your up/down counter on the Tang Nano 9 FPGA board, which will be done during the session. You will also be asked to make some modifications to our design and re-test.

You are advised to try producing *controller.v* before the laboratory session by selecting

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File -> Export -> Export to Verilog
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on *Digital*, and make sure that the export is error free.

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