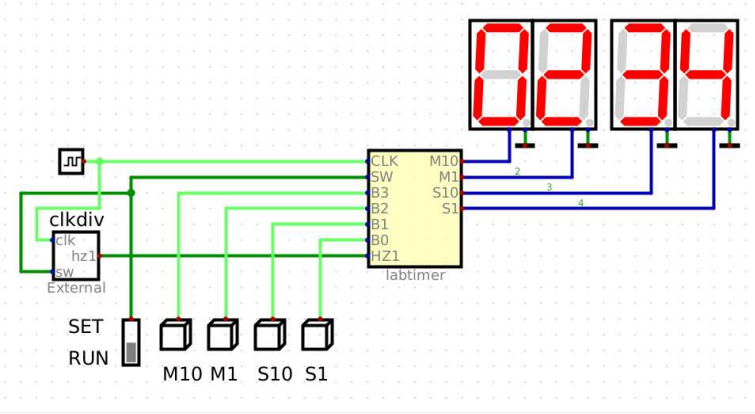
CS 303 Logic and Digital System Design Assigned : 27/04/2025
Term Project Demo and Due Date : 20/05/2025

A Laboratory Timer using the Tang Nano 9K

Timers are essential tools of a laboratory where the duration of a process needs to be measured precisely. They typically show the time in MM:SS format, and start the down count from a set value in the range 00:01–99:59. Another essential feature is that the count proceeds forward once 00:00 is reached, which is used to measure the overtime.

We would like to perform the full schematic design of such a timer, and demonstrate its operation on the Tang Nano 9K FPGA board. The design will be done on *Digital* using the template provided in *labtimer_template.zip* on SUcourse, in which the top level circuit is *testbench.dig*. A sample run of the working circuit is shown in the figure:



Your design is to go into the block labeled *labtimer*, which accepts inputs from four buttons, a toggle switch, and the clock signal. The additional input labeled as HZ1 is a pulse of exactly one clock period and frequency of 1 Hz, which can be used as a time base. Please be warned that *labtimer.dig* (which does not contain any circuit components, as you might imagine) has GND connections made to the M10, M1, S10, and S1 outputs, just to avoid errors when you attempt to run *testbench.dig* in its form that comes out from *labtimer_template.zip*. DO NOT FORGET TO REMOVE these, as they are not part of the design. A warning label is included in *labtimer.dig*. Remove that label as well to avoid clutter.

A full schematic design is expected; no blocks to be implemented in Verilog. All flip-flops of the design should be clocked with the master CLK signal of the circuit, which is 100 Hz in *Digital*, and 27 MHz on the Tang Nano 9K. A sequential design compatible with general digital design rules is expected. Clock gating is absolutely prohibited, such designs will not be accepted.

The circuit is expected to function as follows: in SET mode, buttons M10, M1, S10, and S1 are expected to advance (by one) their respective digit on the display (i.e., 10s digit of minutes, 1s digit of minutes, 10s digit of seconds, and 1s digit of seconds, respectively, from left to right.) M10, M1, and S1 are expected to roll to 0 after 9, while S10 should do this after 5. Moving the switch to RUN mode should initiate the down count. After 00:00 is reached, the counter is expected to start counting upwards indicating overtime. Moving back to SET should stop the count (in either direction), and initiate the set operation again. You may see *demoDigital.mp4* for a visual description of the operation.

You are provided with a Verilog template in **labtimer_template_verilog.zip** that can be used for testing your design on your FPGA board, Simply export *labtimer.dig* into *labtimer.v*, place that into the *labtimer_template_verilog* folder, compile and upload. A *Makefile* is included for those who prefer the *make* design flow instead of using VS Code. You may want to watch *demoTangNano.mp4*.

On the demo day, you will demonstrate your circuit in *Digital*, export *labtimer.dig*, place *labtimer.v* into the template folder, compile and upload your design to your FPGA board, demonstrate its functionality, and finally upload all *.dig* files and *labtimer.v* to SUcourse. You will be assigned time slots for the demo, watch for further announcements. No makeup for the demo. Upon finishing, you will return your FPGA board, and you will be handed the form that you have signed.

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