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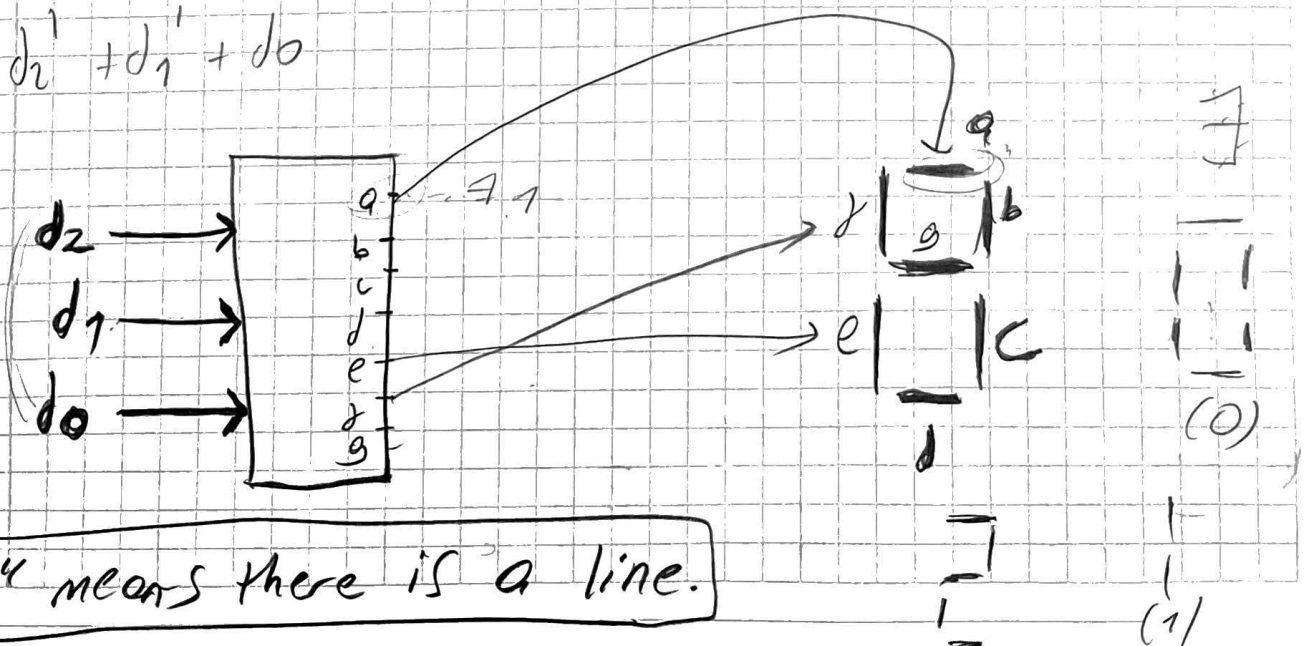
Lab assignment #1

- To display 7 numbers, 3 bits is enough. If we wanted to show 9 numbers we shall have used 4 bits.

d_2	d_1	d_0	Decimal	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	1	1	0	1	1	0	0	0	0
0	1	0	2	1	1	0	1	1	0	1
0	1	1	3	1	1	1	1	0	0	1
1	0	0	4	0	1	1	0	0	1	1
1	0	1	5	1	0	1	1	0	1	1
1	1	0	6	1	0	1	1	1	1	1
1	1	1	7	1	1	1	0	0	0	0

$a = d_2' + d_1' + d_0$



"4" means there is a line.

minterms

- $a = \Sigma(0,2,3,5,6,7)$ = minterms

$a = \underbrace{d_2' d_1' d_0'}_{0} + \underbrace{d_2' d_1 d_0'}_{2} + \underbrace{d_2' d_1 d_0}_{3} + \underbrace{d_2 d_1' d_0'}_{5} + \underbrace{d_2 d_1 d_0'}_{6} + \underbrace{d_2 d_1 d_0}_{7}$

- $b = \Sigma(0,1,2,3,4,7)$

$b = \underbrace{d_2' d_1' d_0'}_{0} + \underbrace{d_2' d_1' d_0}_{1} + \underbrace{d_2' d_1 d_0'}_{2} + \underbrace{d_2' d_1 d_0}_{3} + \underbrace{d_2 d_1' d_0'}_{4} + \underbrace{d_2 d_1 d_0}_{7}$

- $c = \Sigma(0,1,3,4,5,6,7)$

$c = \underbrace{d_2' d_1' d_0'}_{0} + \underbrace{d_2' d_1' d_0}_{1} + \underbrace{d_2' d_1 d_0}_{3} + \underbrace{d_2 d_1' d_0'}_{4} + \underbrace{d_2 d_1' d_0}_{5} + \underbrace{d_2 d_1 d_0'}_{6} + \underbrace{d_2 d_1 d_0}_{7}$

- $d = \Sigma(0,2,3,5,6)$

$d = \underbrace{d_2' d_1' d_0'}_{0} + \underbrace{d_2' d_1 d_0'}_{2} + \underbrace{d_2' d_1 d_0}_{3} + \underbrace{d_2 d_1' d_0}_{5} + \underbrace{d_2 d_1 d_0'}_{6}$

- $e = \Sigma(0,2,6)$

$e = \underbrace{d_2' d_1' d_0'}_{0} + \underbrace{d_2' d_1 d_0'}_{2} + \underbrace{d_2 d_1 d_0'}_{6}$

- $f = \Sigma(0,4,5,6,7)$

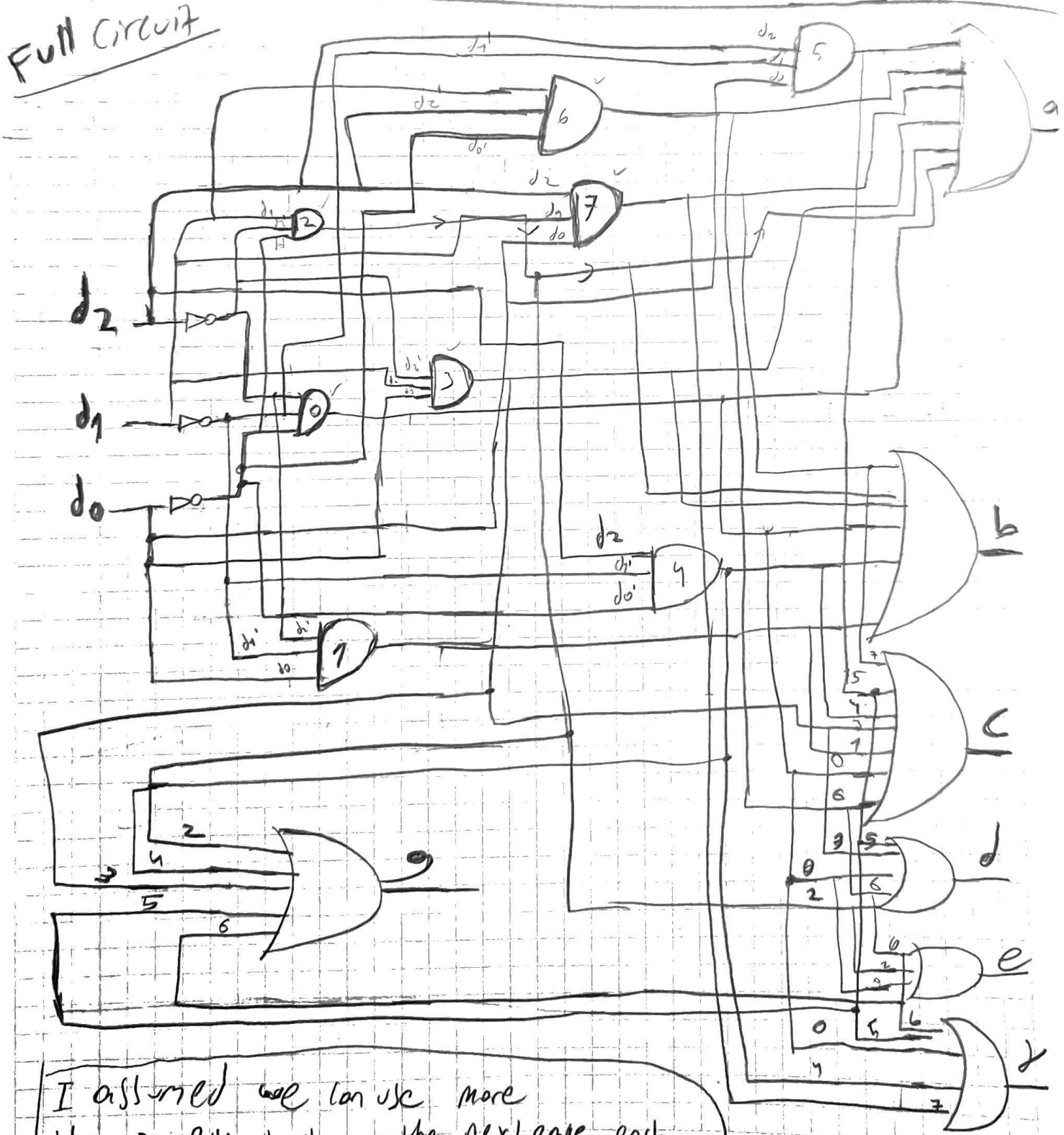
$f = \underbrace{d_2' d_1' d_0'}_{0} + \underbrace{d_2 d_1' d_0'}_{4} + \underbrace{d_2 d_1' d_0}_{5} + \underbrace{d_2 d_1 d_0'}_{6} + \underbrace{d_2 d_1 d_0}_{7}$

1,4,

- $g = \{2, 3, 4, 5, 6\}$

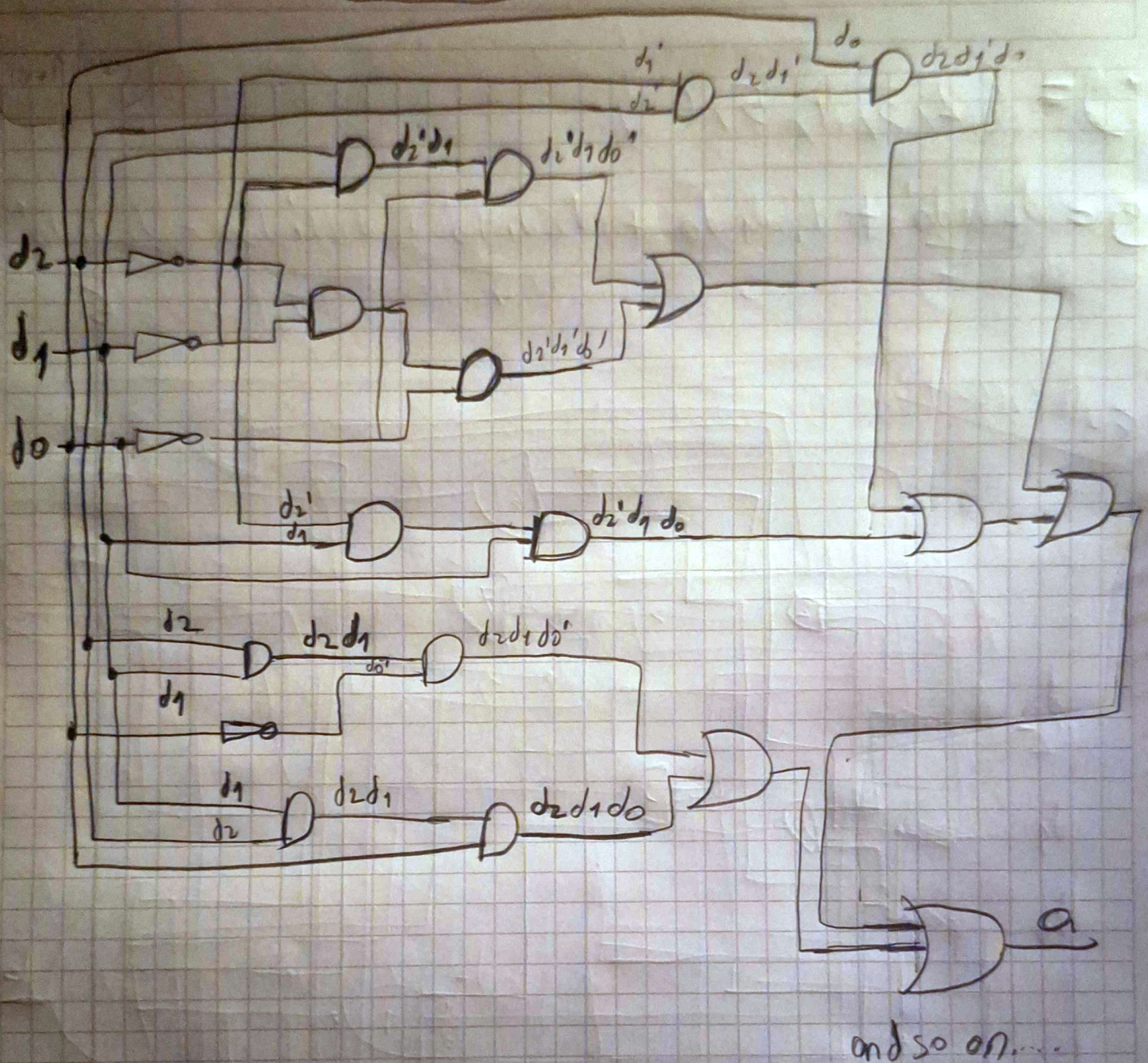
$$g = \underbrace{d_2' d_1 d_0'}_{2} + \underbrace{d_2' d_1 d_0}_{3} + \underbrace{d_2 d_1' d_0'}_{4} + \underbrace{d_2 d_1' d_0}_{5} + \underbrace{d_2 d_1 d_0'}_{6}$$

Full circuit



I assumed we can use more than 2 inputs but in the next page each segments are designed with 2 inputs for the gates.

2 inputs


d_2
d_1
d_0
d_2' d_1
d_1' d_0'
d_2' d_1' d_0'
d_2' d_1
d_2 d_1'
d_2' d_1' d_0'
d_2' d_1 d_0
d_2 d_1
d_2 d_1 d_0'
d_1
d_1 d_2
d_2 d_1
d_2 d_1 d_0
a
and so on....