CS 303 Logic and Digital System Design
Laboratory Assignment #1

Assigned : 25/02/2025
Sessions : 04/03/2025
Preliminary Work Due : 03/03/2025 23:59

A 3-bit input octal to seven segment decoder is to be designed. The circuit will accept binary combinations 000, 001, 010, 011, 100, 101, 110, 111, and drive a seven segment display to show 0, 1, 2, 3, 4, 5, 6, 7, respectively.

1. Construct the truth tables for segment outputs a through g with d2, d1, and d0 as inputs.
2. Design 7 circuits to individually drive the segments, composed of AND, OR and INV gates.
3. Demonstrate your solution by simulating this circuit using *Digital*. Your circuit is expected to be placed into the block labeled "oct2seven" in Fig. 1.

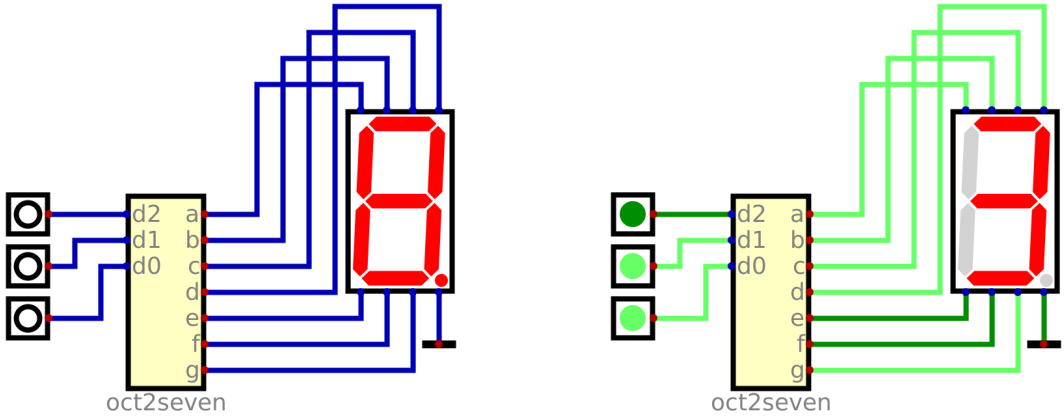

Fig. 1: An octal to seven segment decoder with 3-bit input (left), and sample run (right.)

The file *lab1_2025.zip* contains the top level test circuit in *sevensegment.dig*, while the circuit to be designed is to be drawn in *oct2seven.dig*, which is currently producing all zeros as output.

Submit:

1. Your truth tables and drawings of designed circuits (as a .pdf file), and
2. The modified *oct2seven.dig* file which contains your design.

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