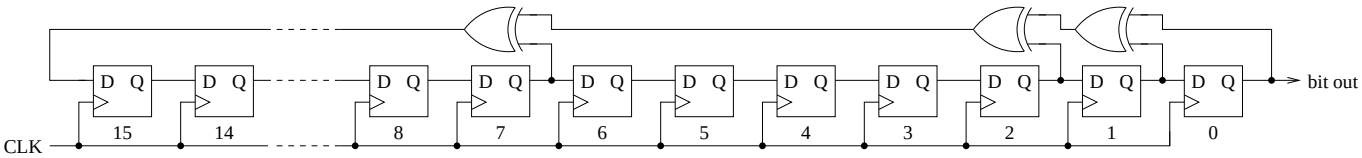
CS 303 Logic and Digital System Design Lab Session : 06/05/2025
Laboratory Assignment #4 Pre-lab due : 05/05/2025 23:59

A Pseudo-Random Number Generator using an LFSR

We would like to design a pseudo-random number generator using a 16-bit LFSR with tap positions at 0, 1, 2, and 7, as in the figure:



Each time BUTTON0 of the FPGA board is pressed, the register is expected to shift out 3 bits, which will be stored in an additional 3-bit shift register to generate a number in the range 0–7. Display this number on the rightmost digit of the seven-segment display. You are expected to initialize the shift register as the lower 4 digits of your student ID. As an example, bits should be set to 1001001101010110 if your ID ends as 9356.

Design your circuit in *Digital* using schematic entry, and submit your *.dig* file before the deadline of the pre-lab assignment. Also make sure that your design runs on your FPGA board.

In-lab

During the laboratory session, you will demonstrate your circuit to your TA. You will then be asked to make modifications to your design, demonstrate again, and upload your new *.dig* file.

□