

MINI_PROJECT

Block name : MUL3

Team Members

Sahana S Kori
Sanika Kumbar
Roopa

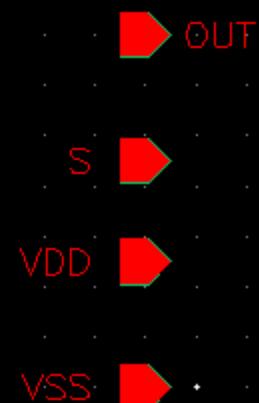
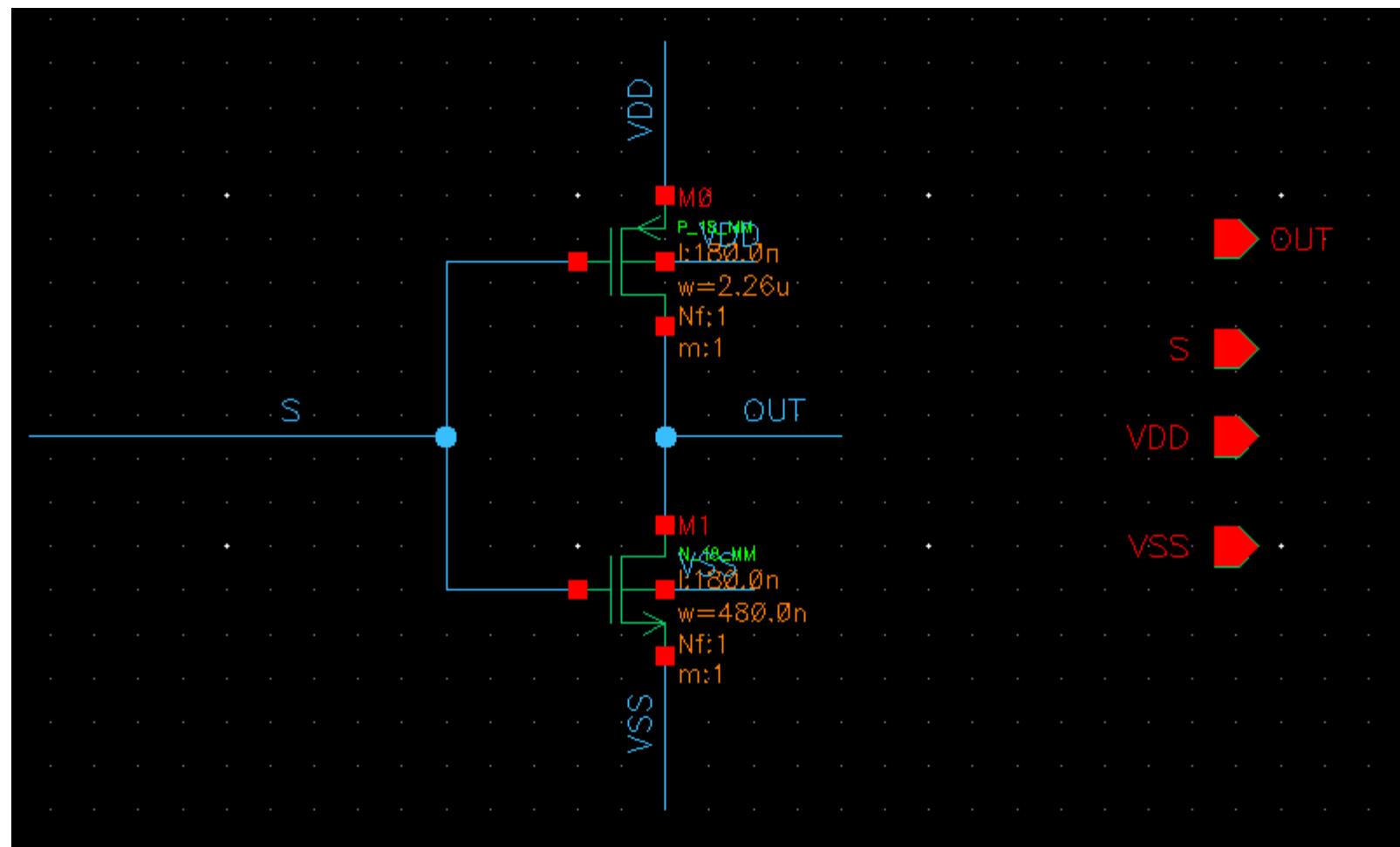
INTRODUCTION

- A mul3 block in a datapath or ALU is a specialized multiplier that specifically multiplies a value by 3.
- It's optimized because multiplying by a constant (3) can be implemented with fewer gates than a general-purpose multiplier (using only adder and shift logic).

Sub-blocks in this MUL3

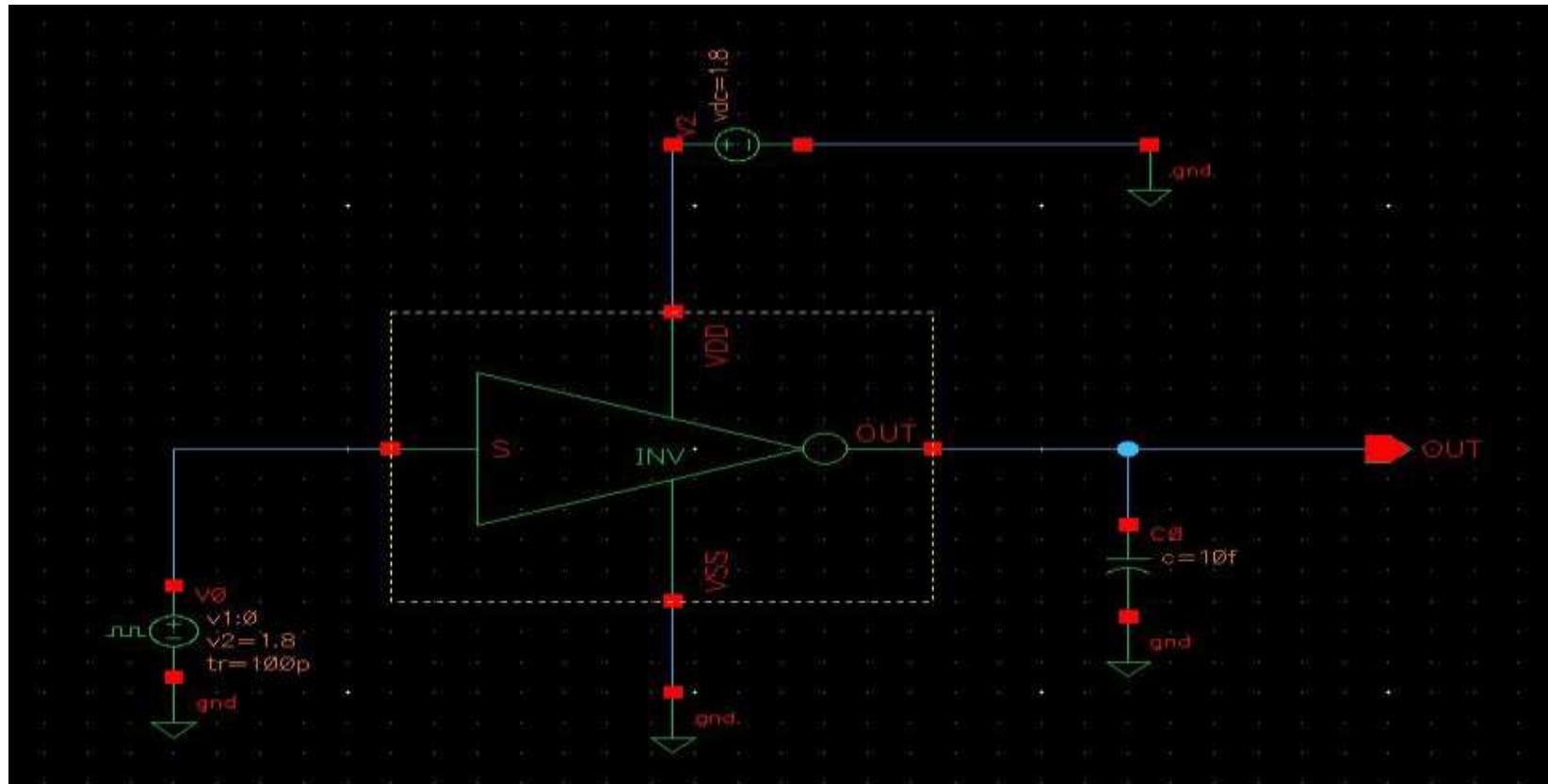
1. INVERTER
2. HALF_ADDER
3. FULL_ADDER
4. MUL2

INVERTER SCHEMATIC

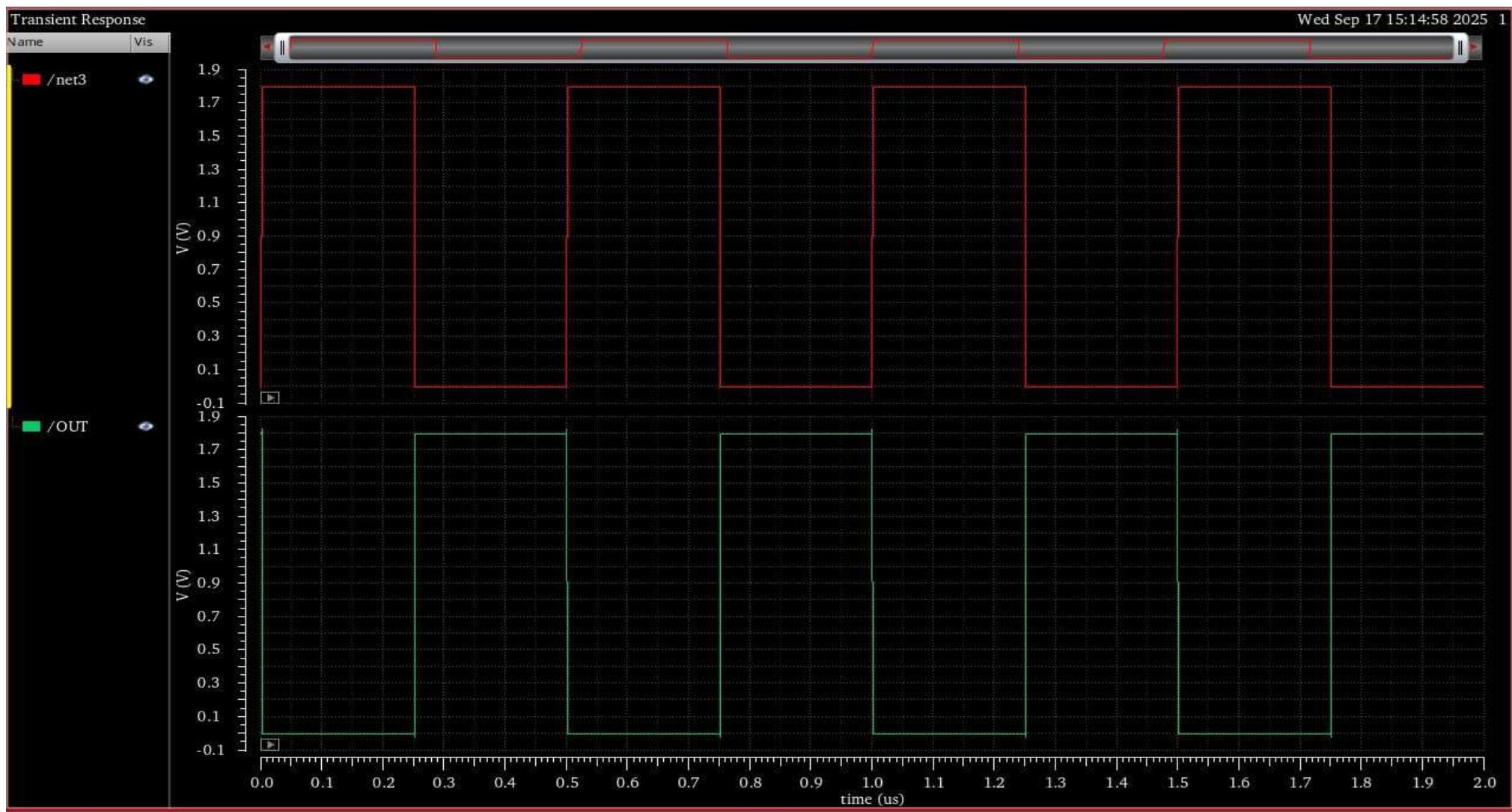


Input	Output
A	Y
0	1
1	0

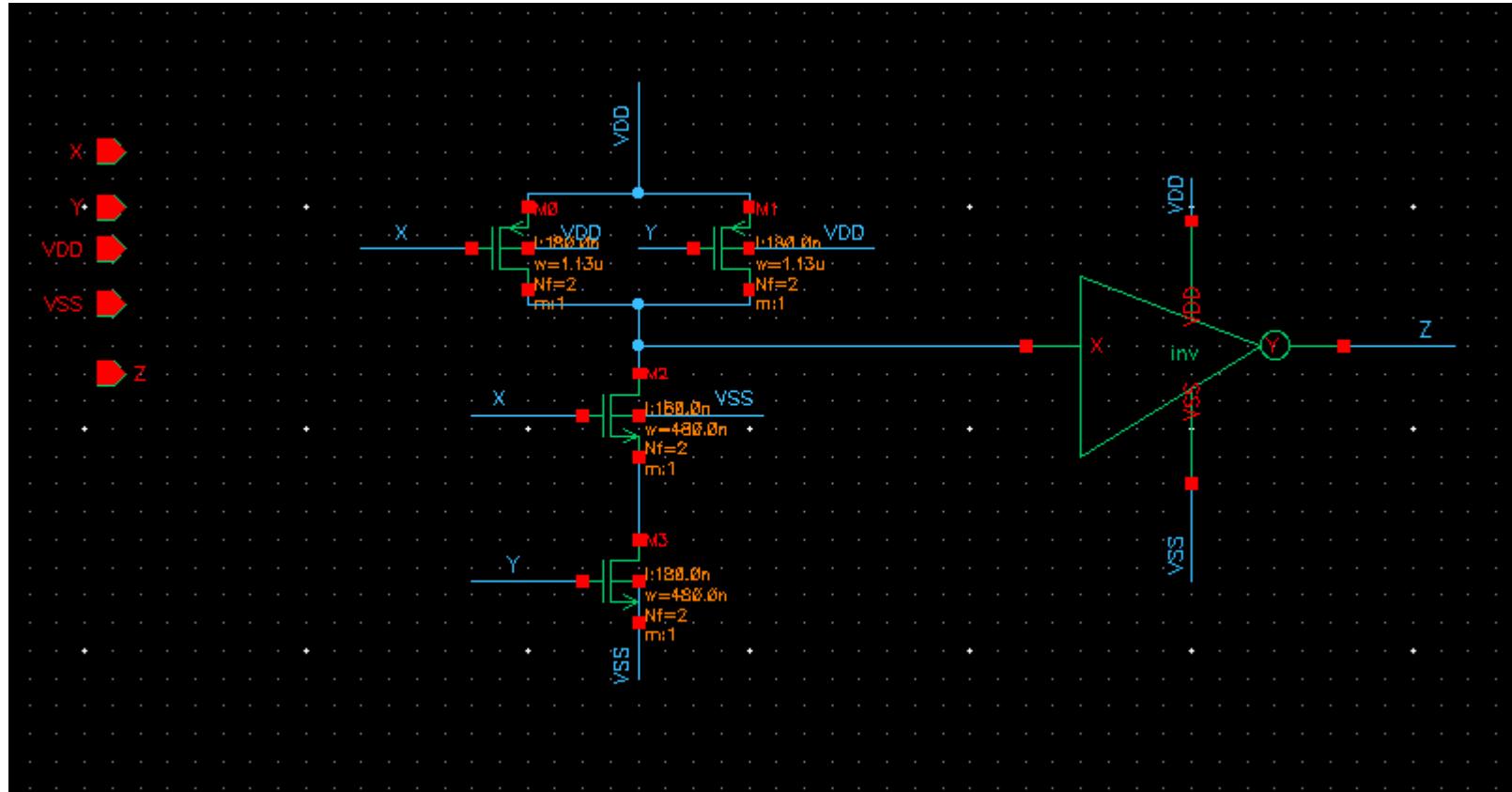
INVERTER TESTBENCH



INVERTER SIMULATIONS

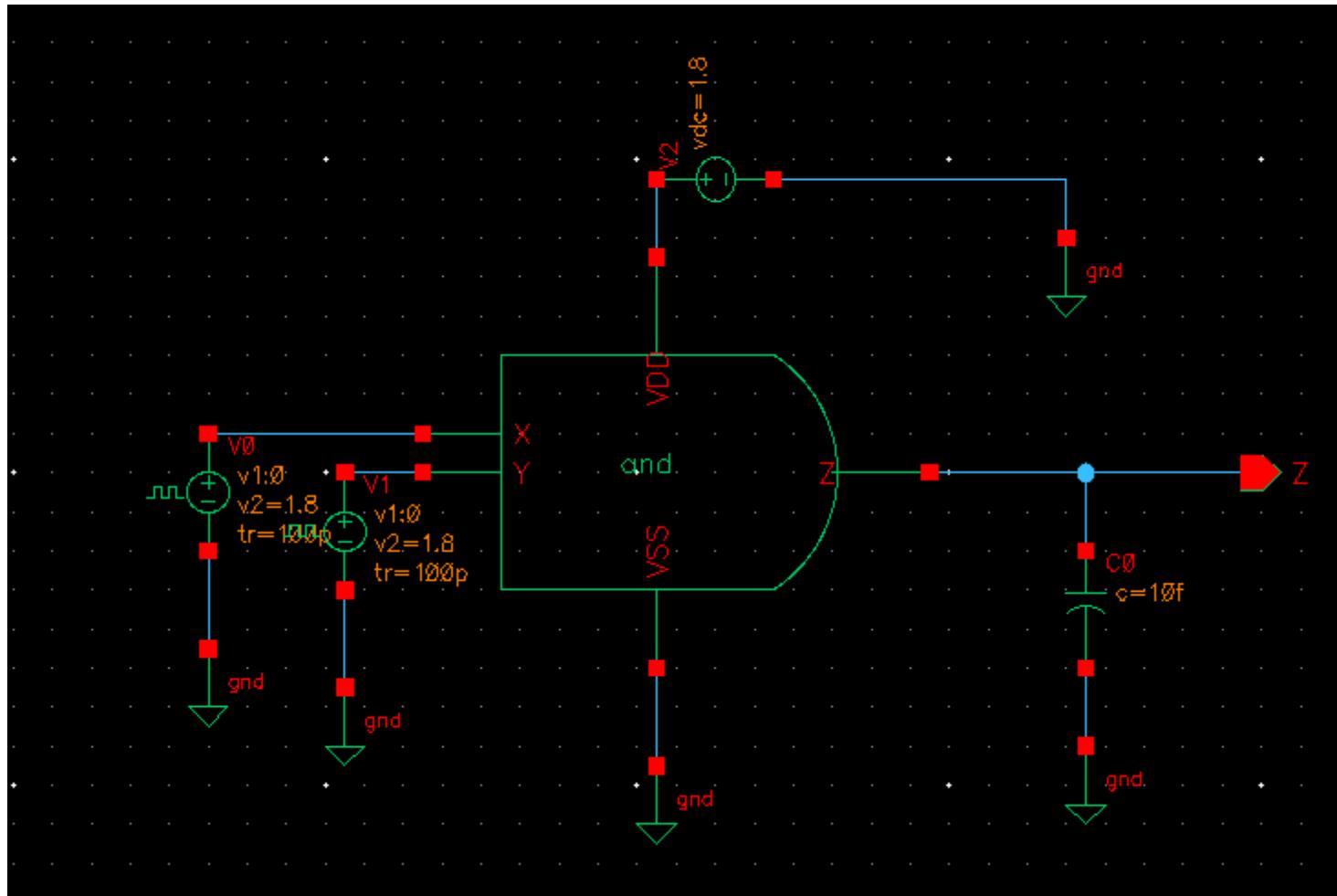


AND SCHEMATIC

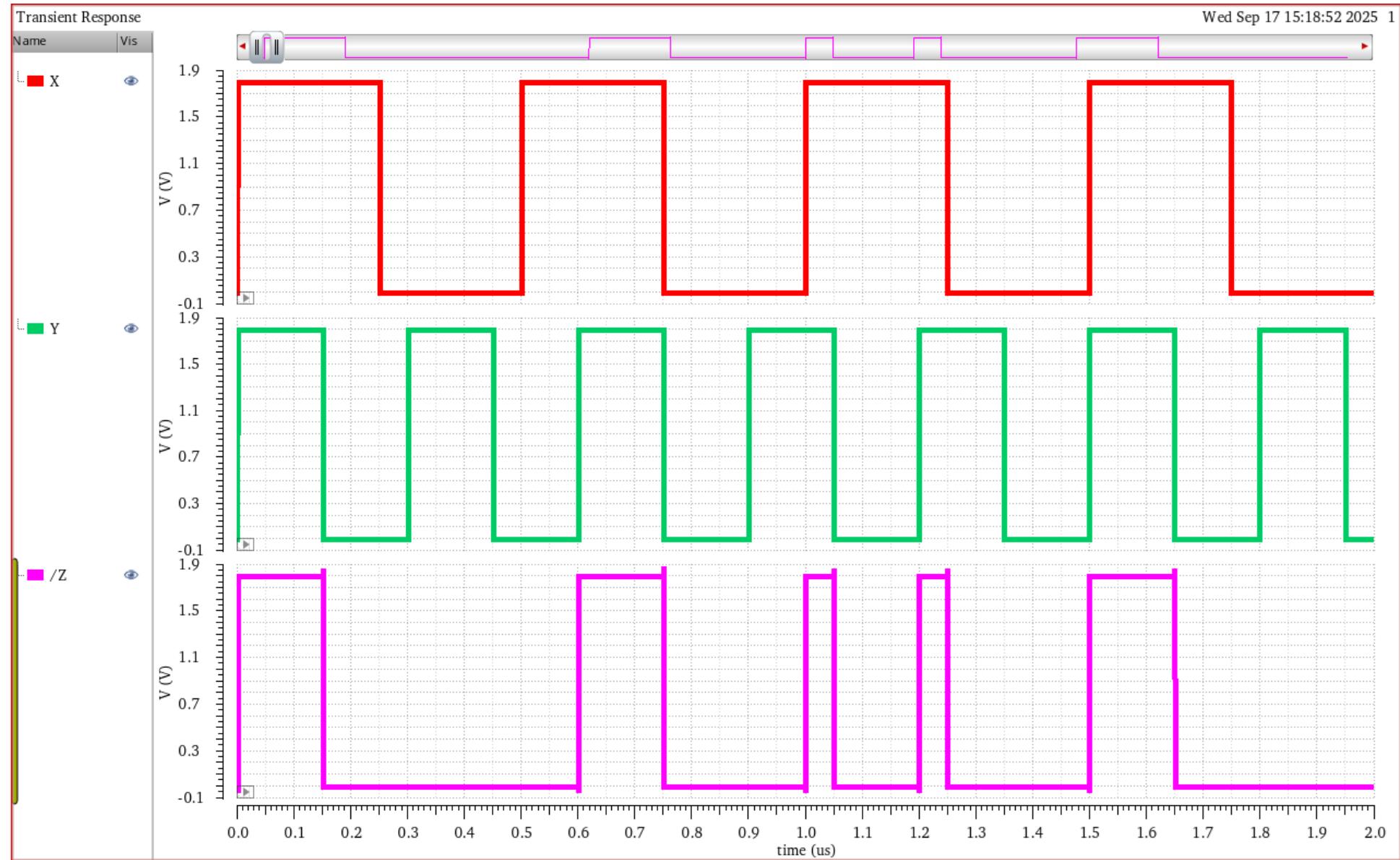


Input	Output
0	0
0	1
1	0
1	1

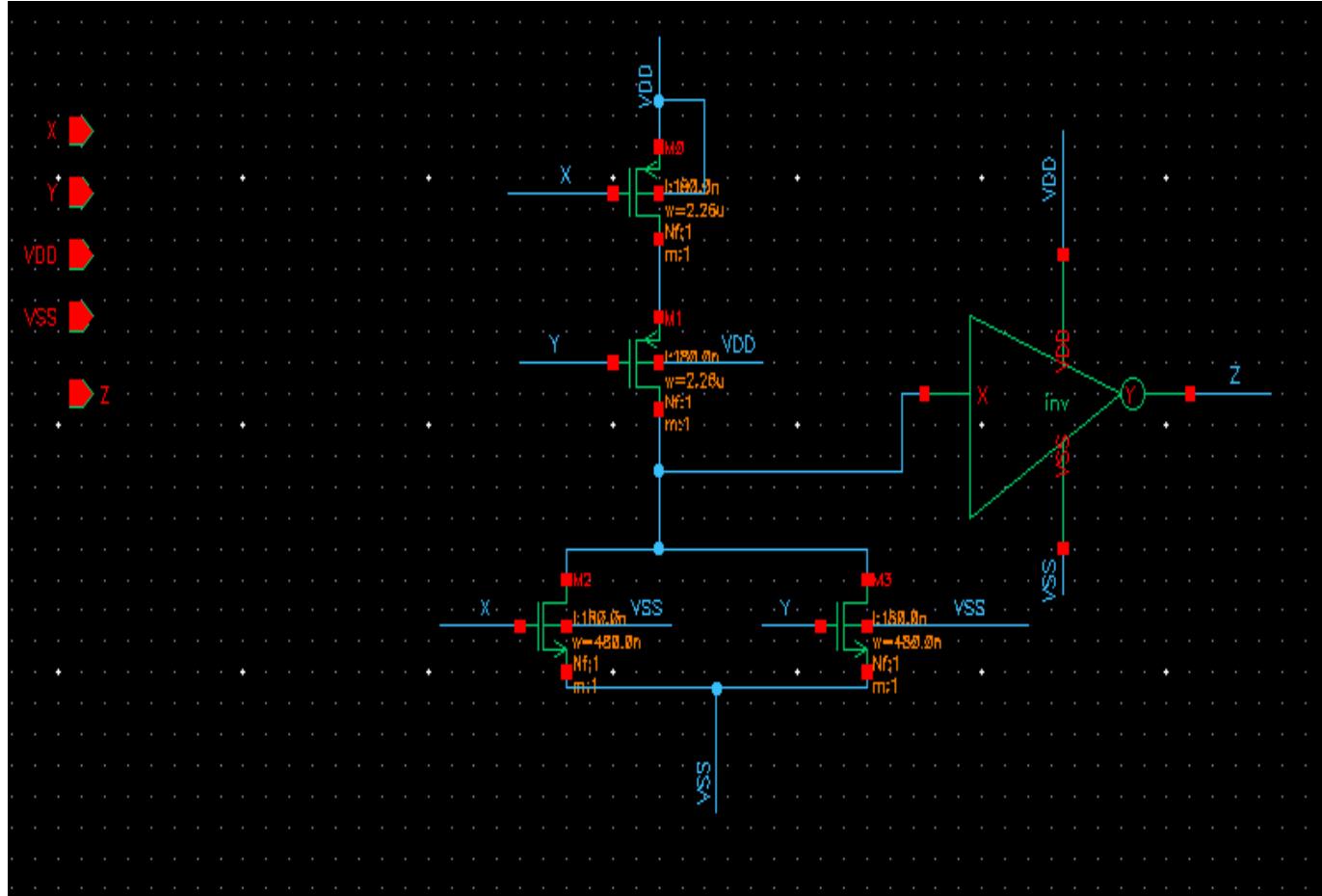
AND TESTBENCH



AND SIMULATIONS

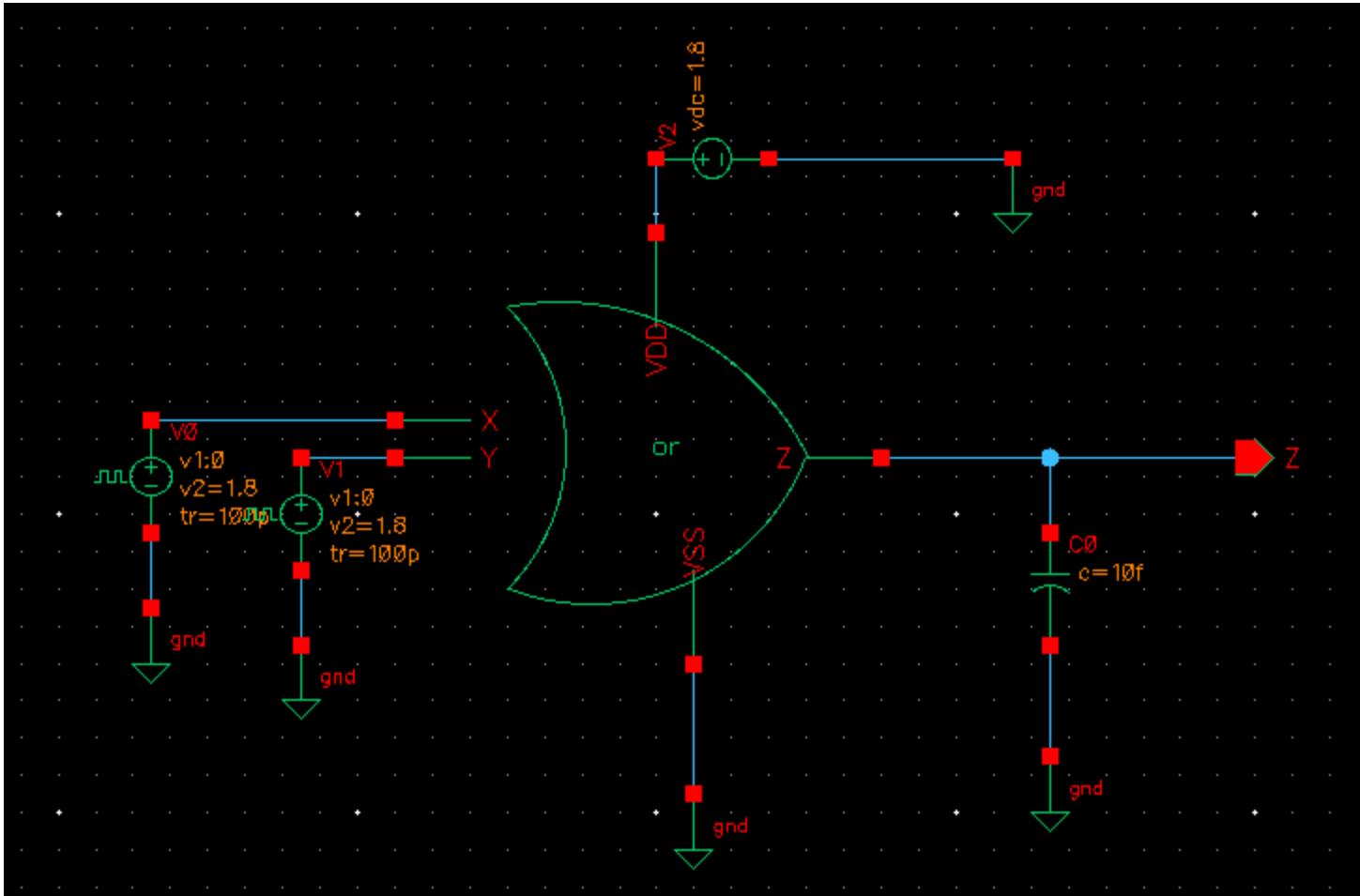


OR SCHEMATIC

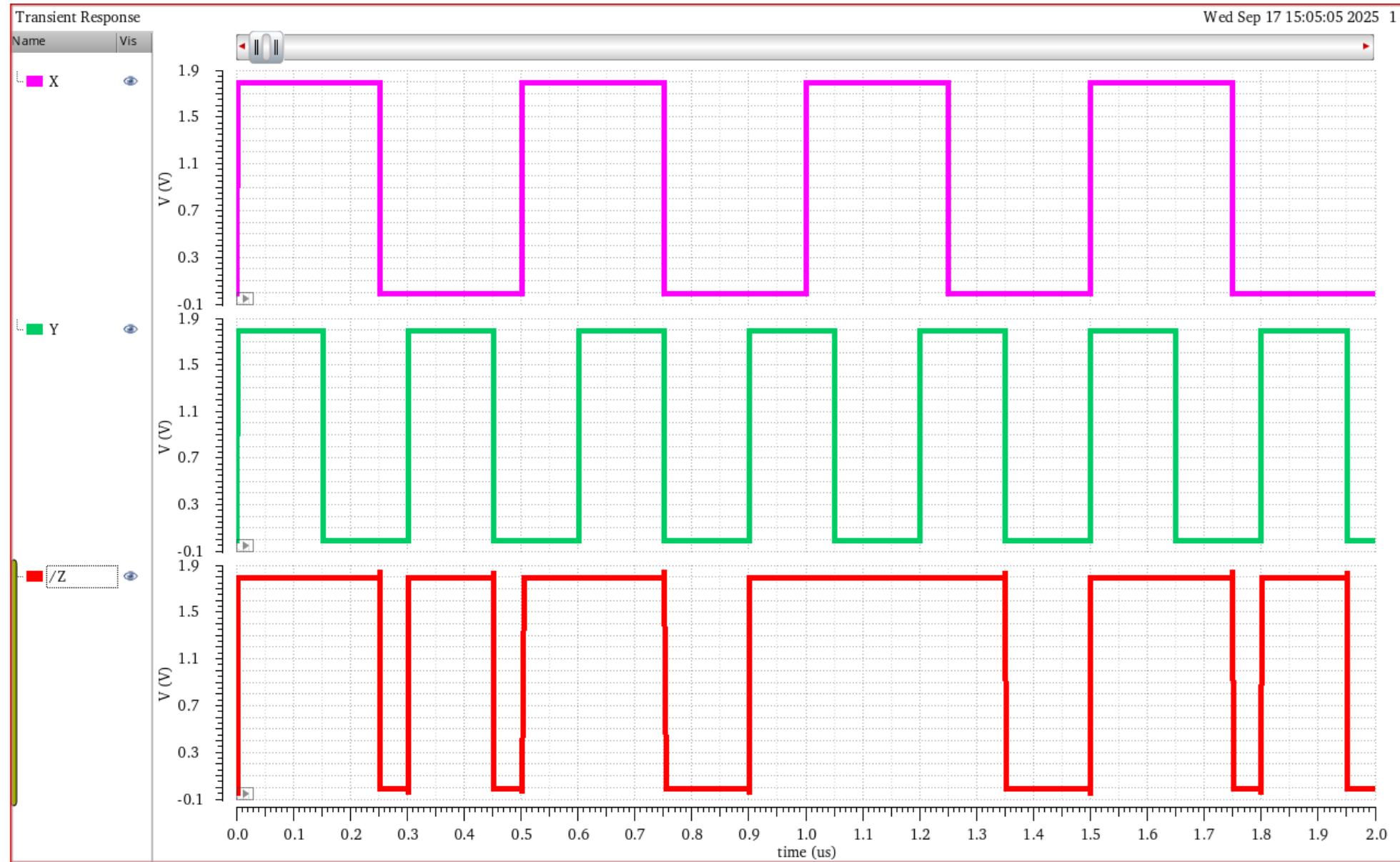


A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

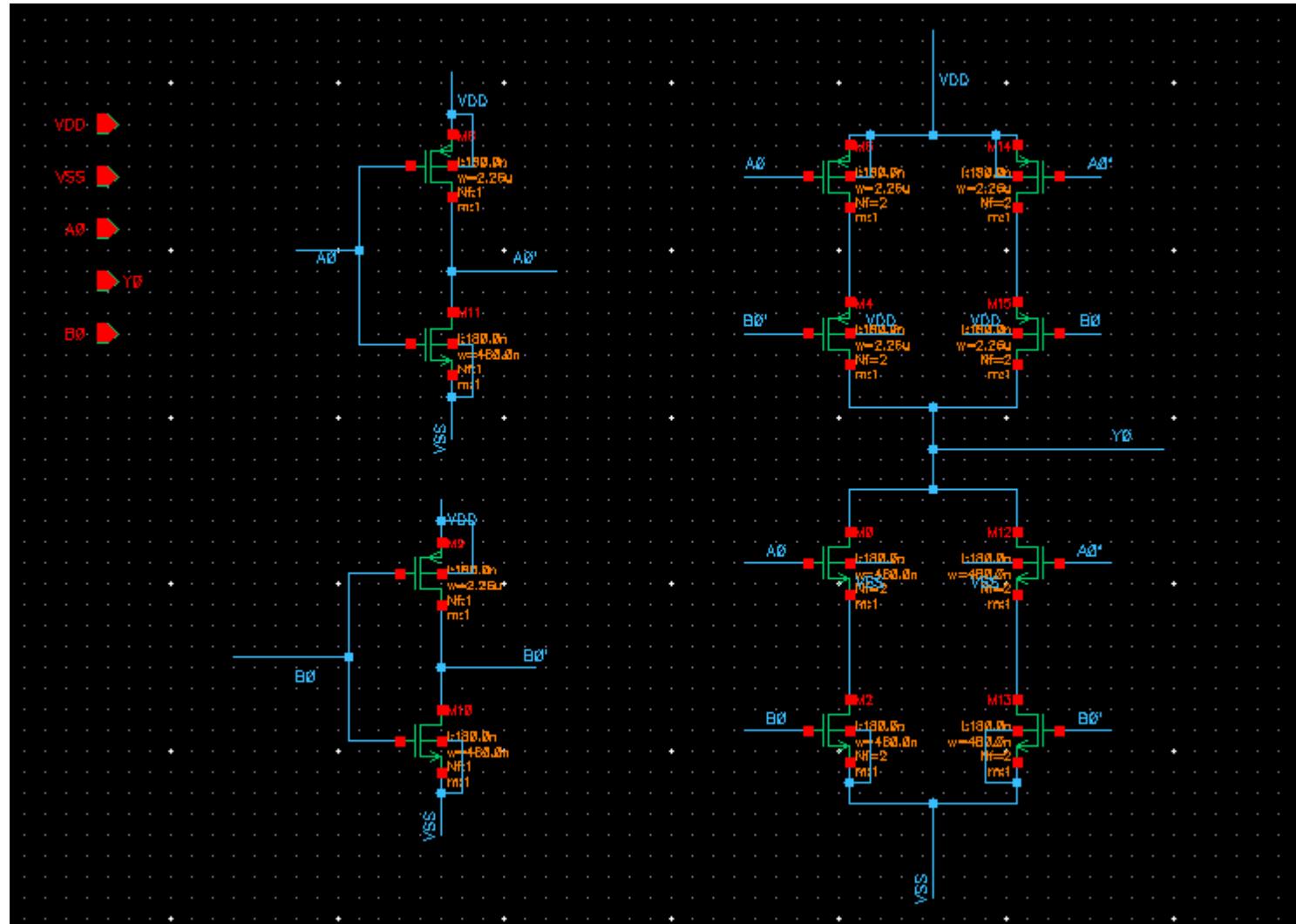
OR TESTBENCH



OR SIMULATIONS

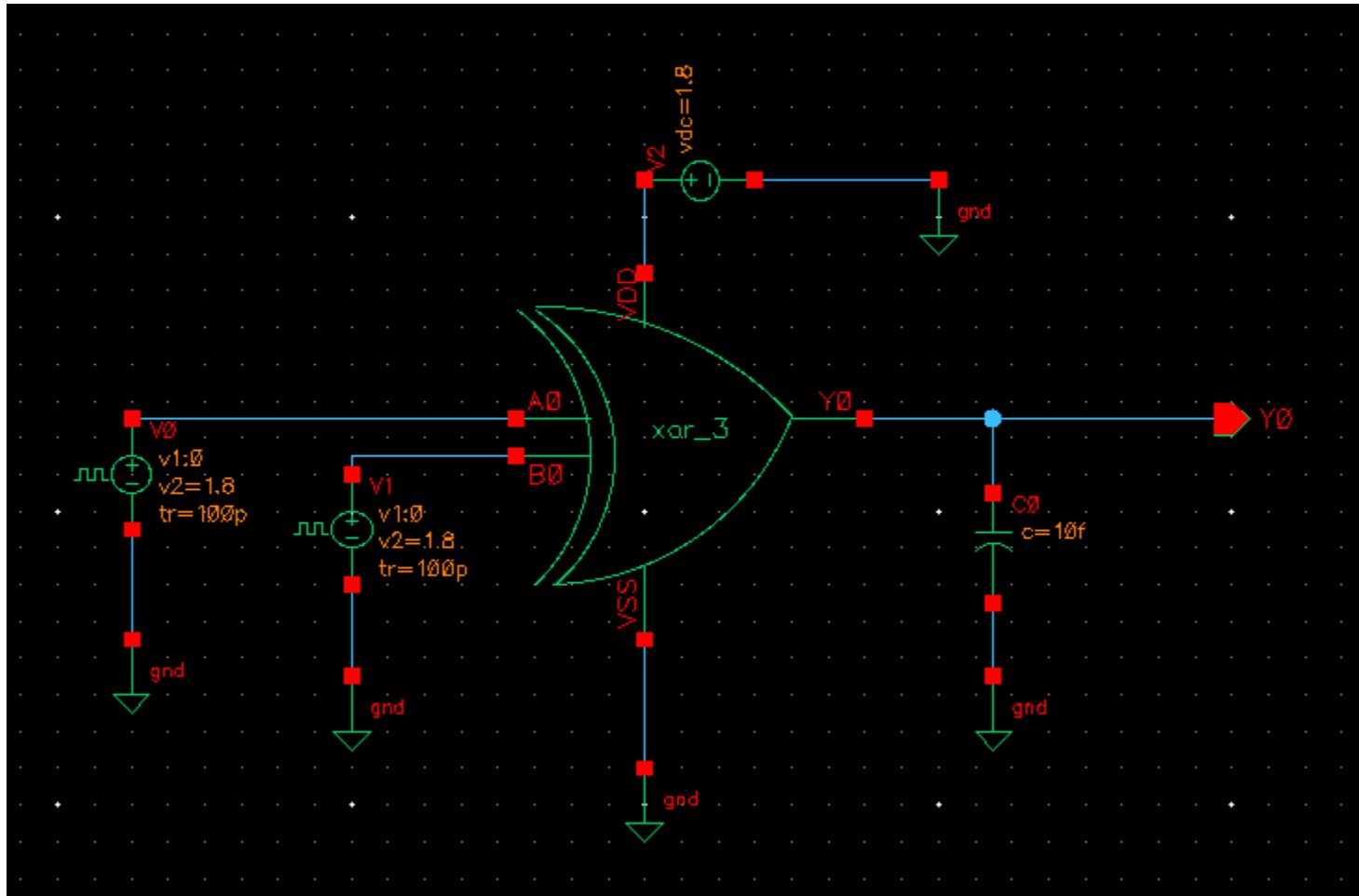


XOR_2 SCHEMATIC



Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

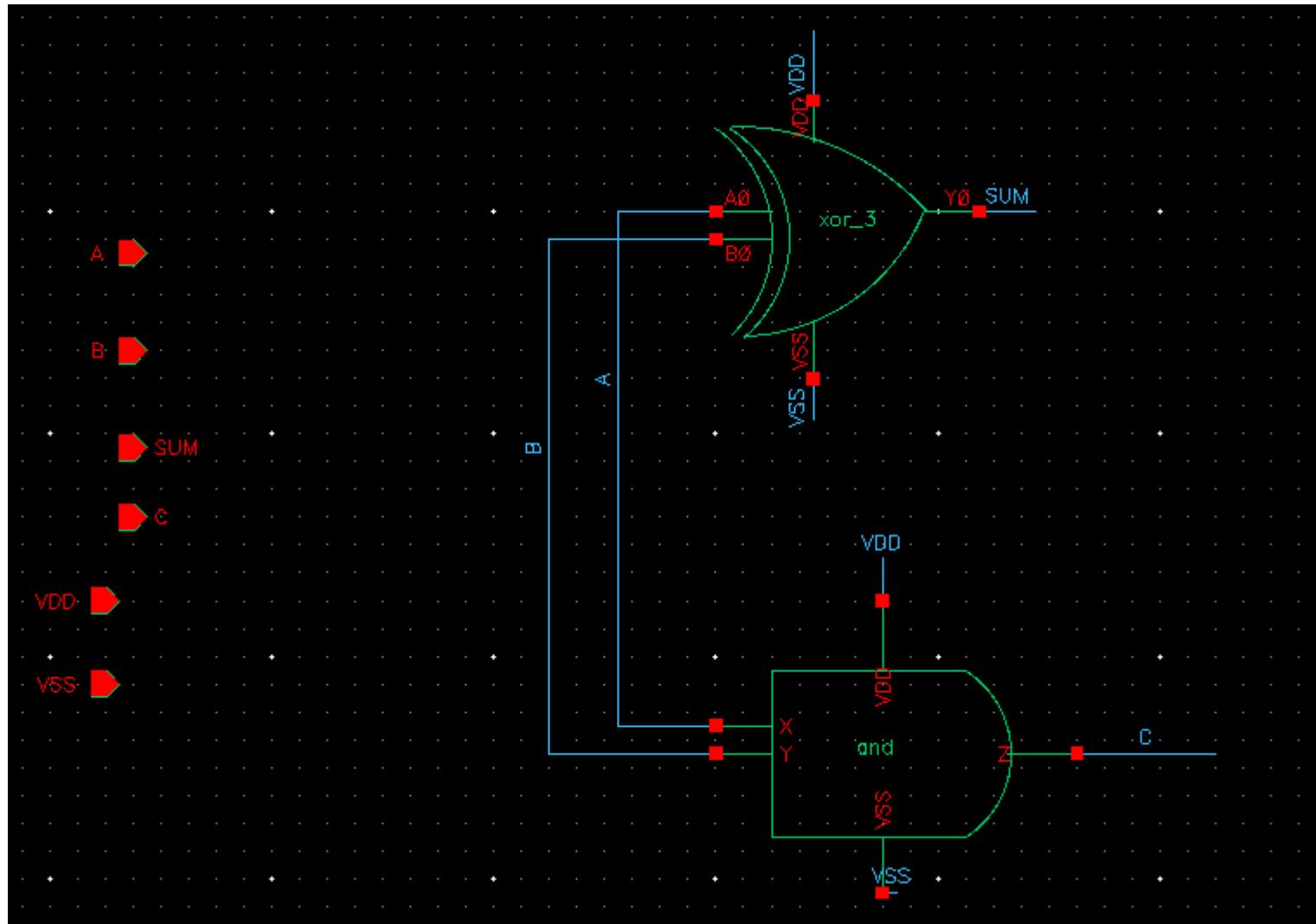
XOR_2 TESTBENCH



XOR_2 SIMULATIONS

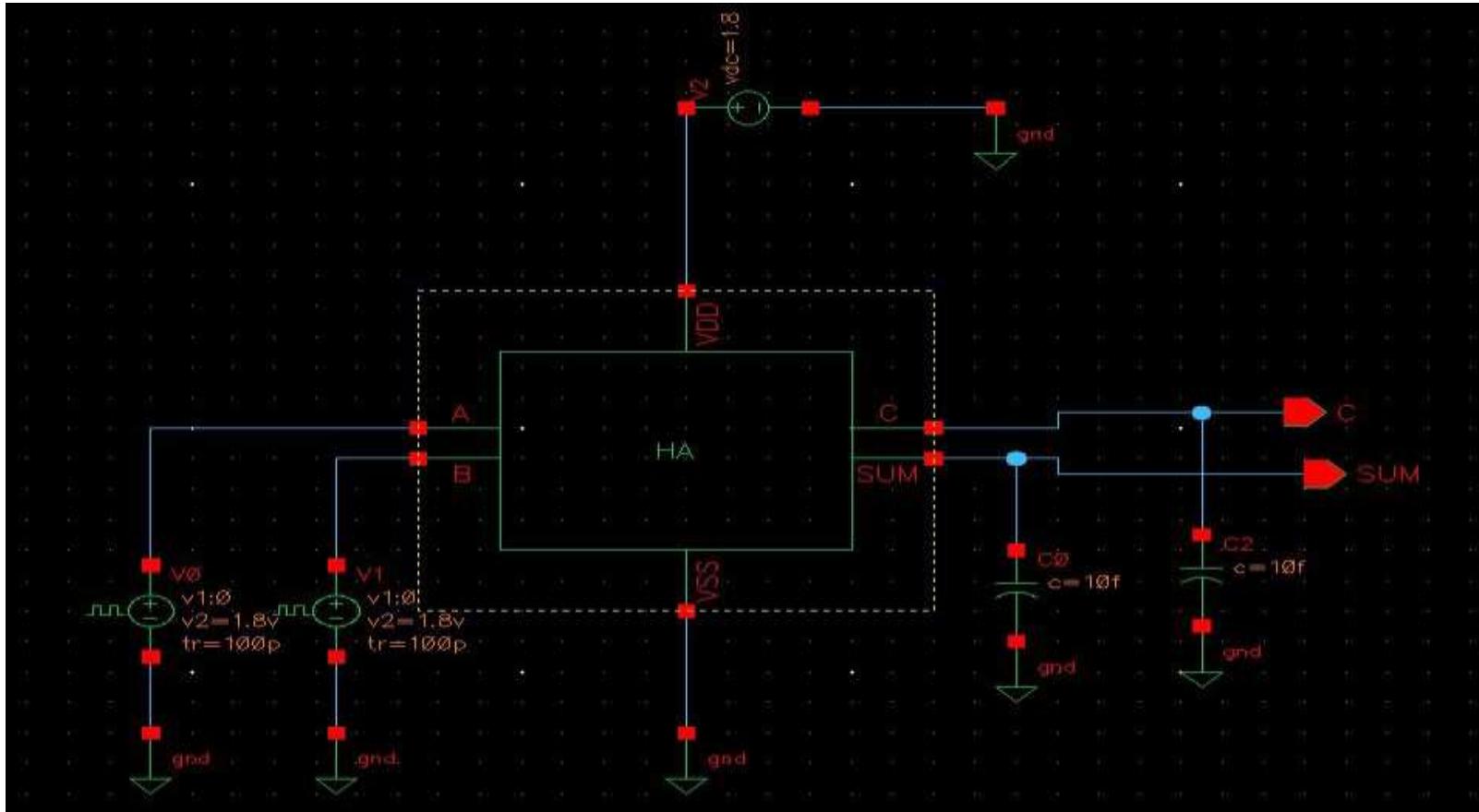


HALF_ADDER SCHEMATIC

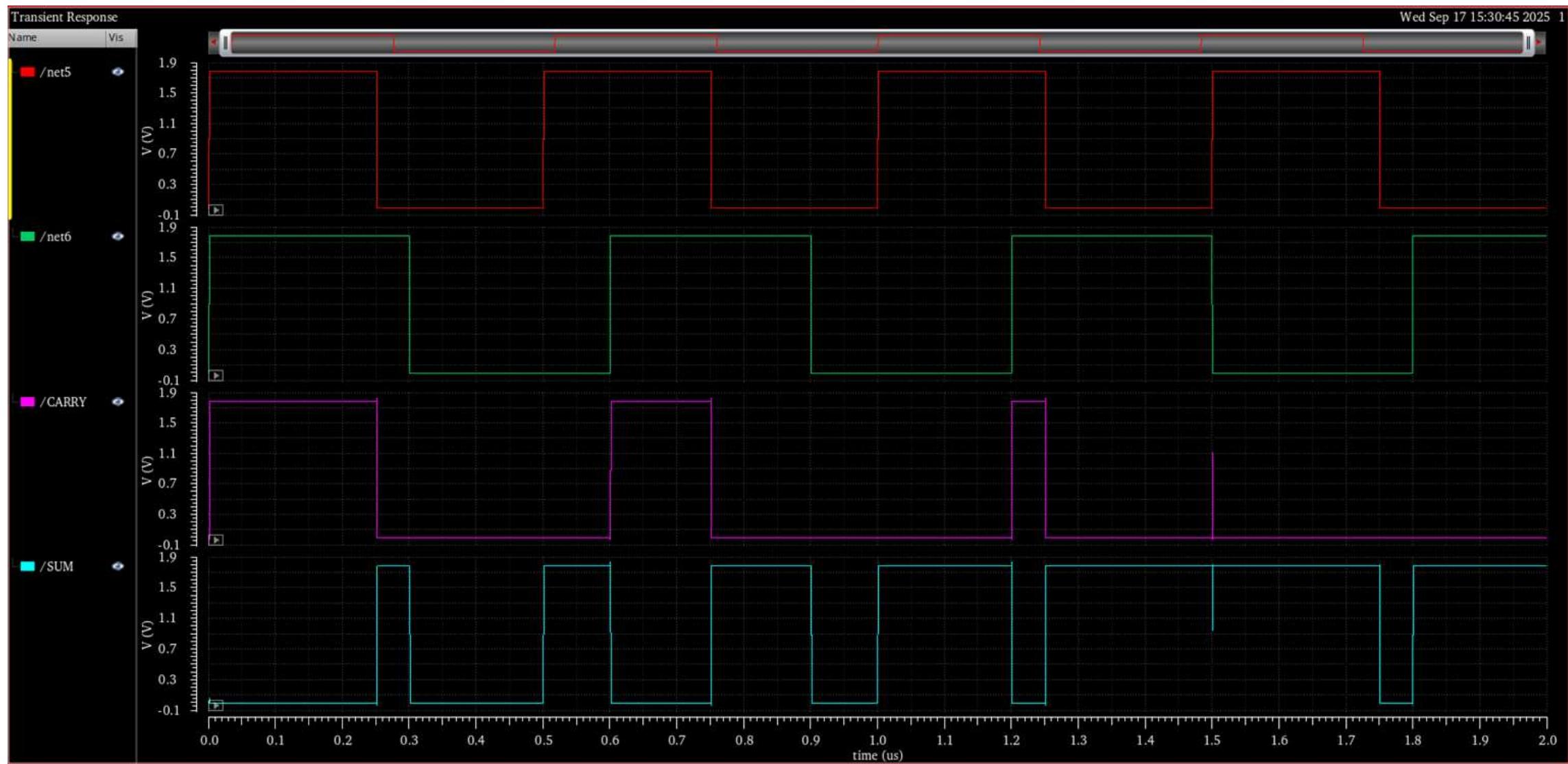


Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

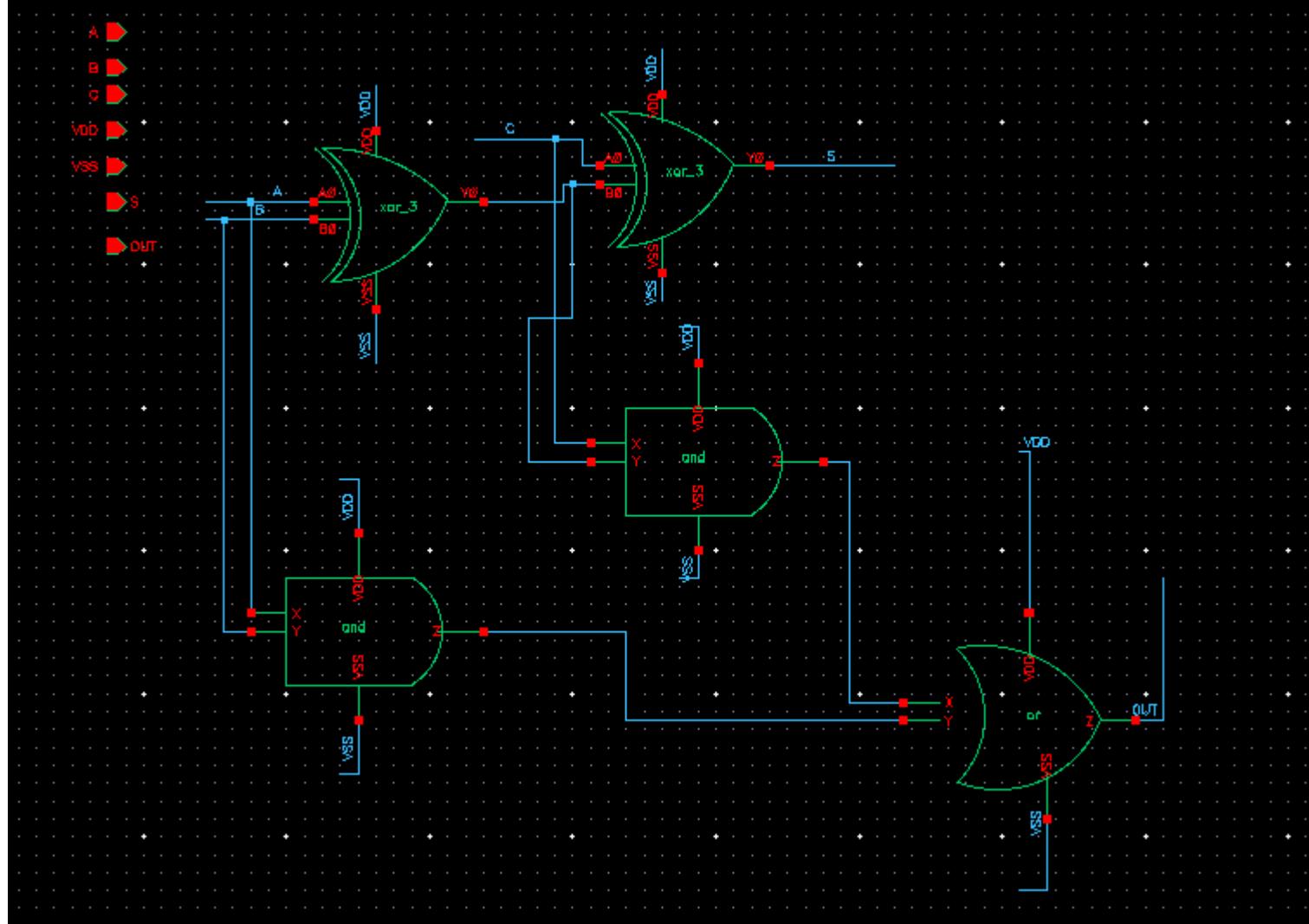
HALF_ADDER TESTBENCH



HALF_ADDER SIMULATIONS

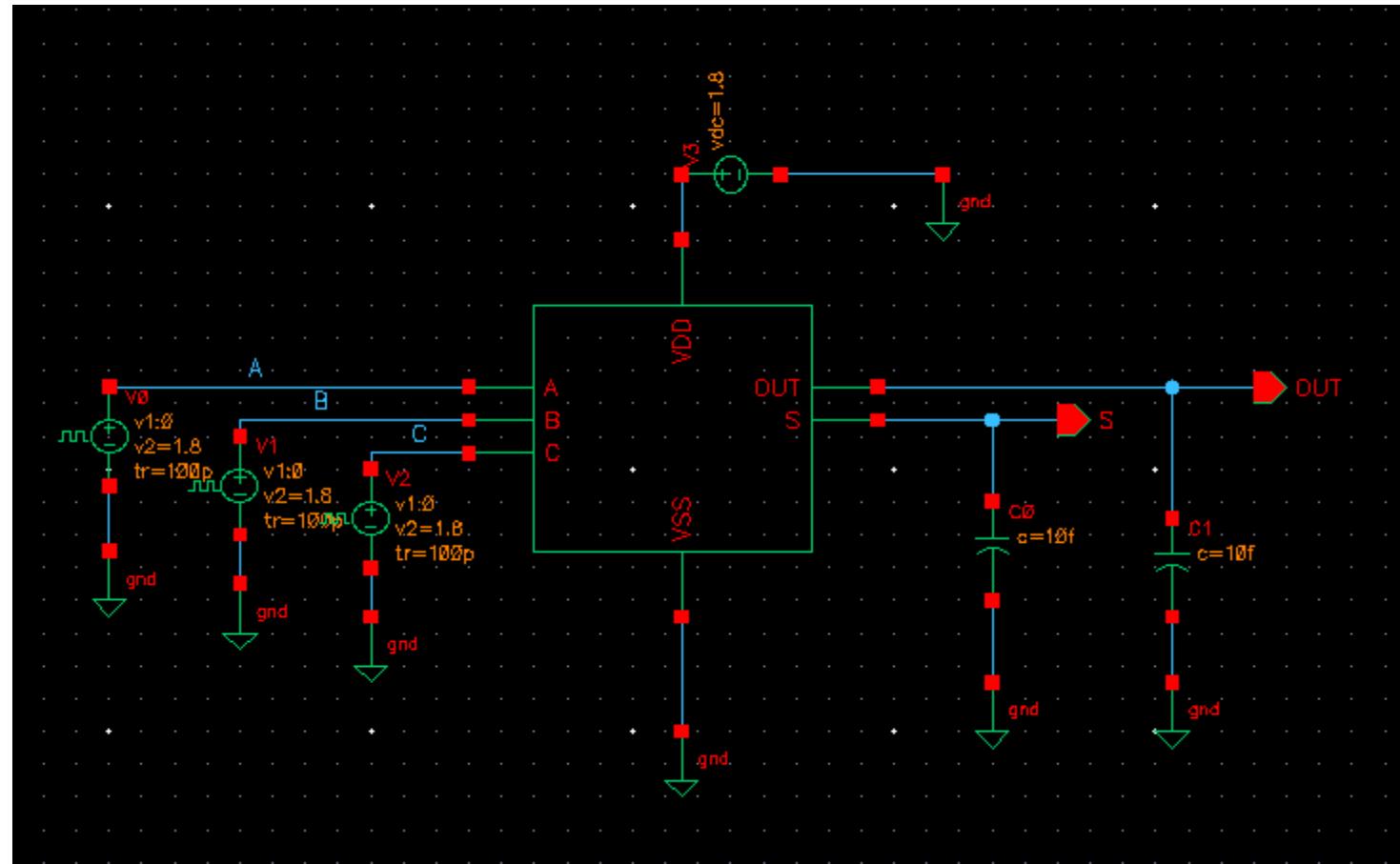


FULL_ADDER SCHEMATIC

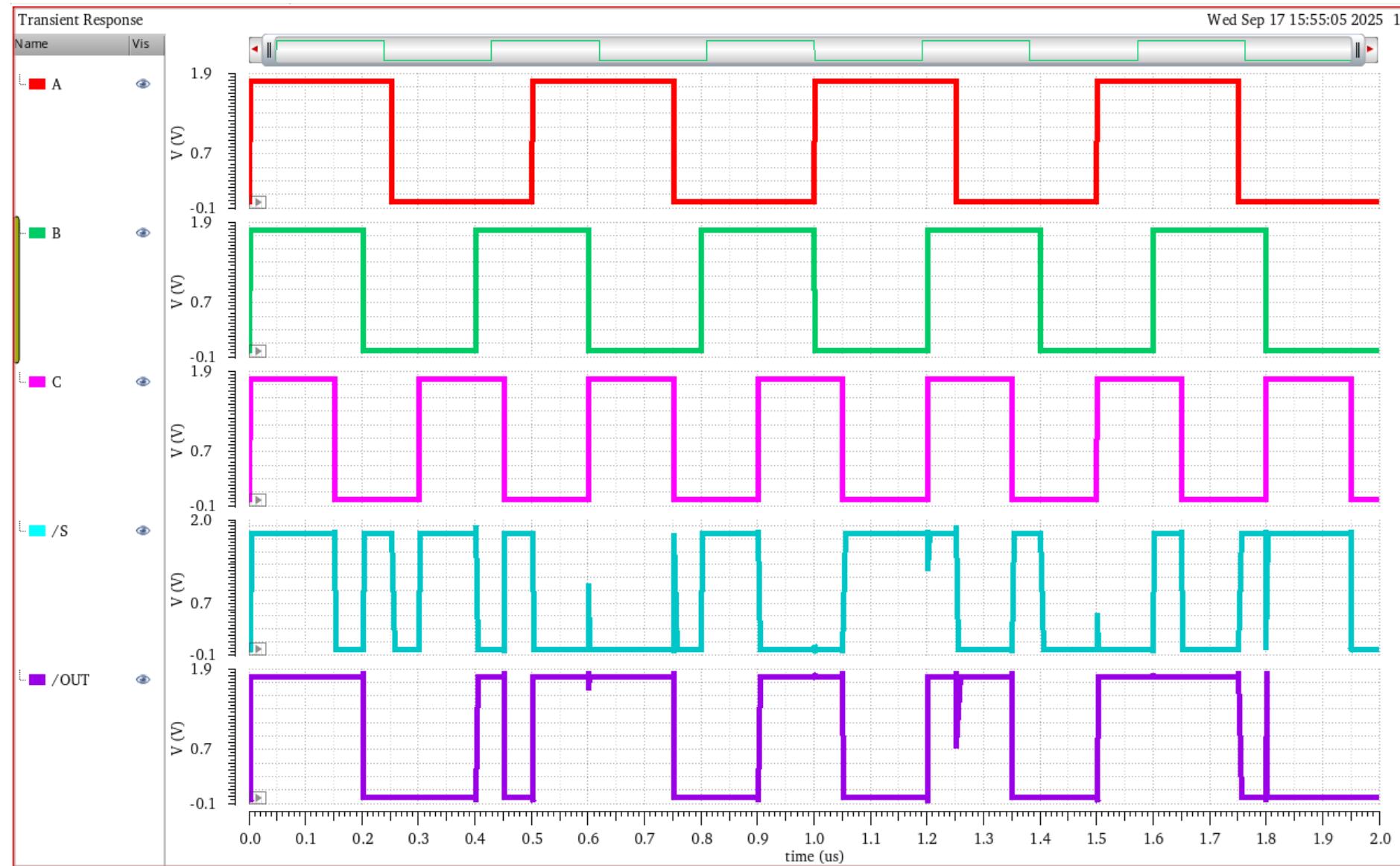


A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

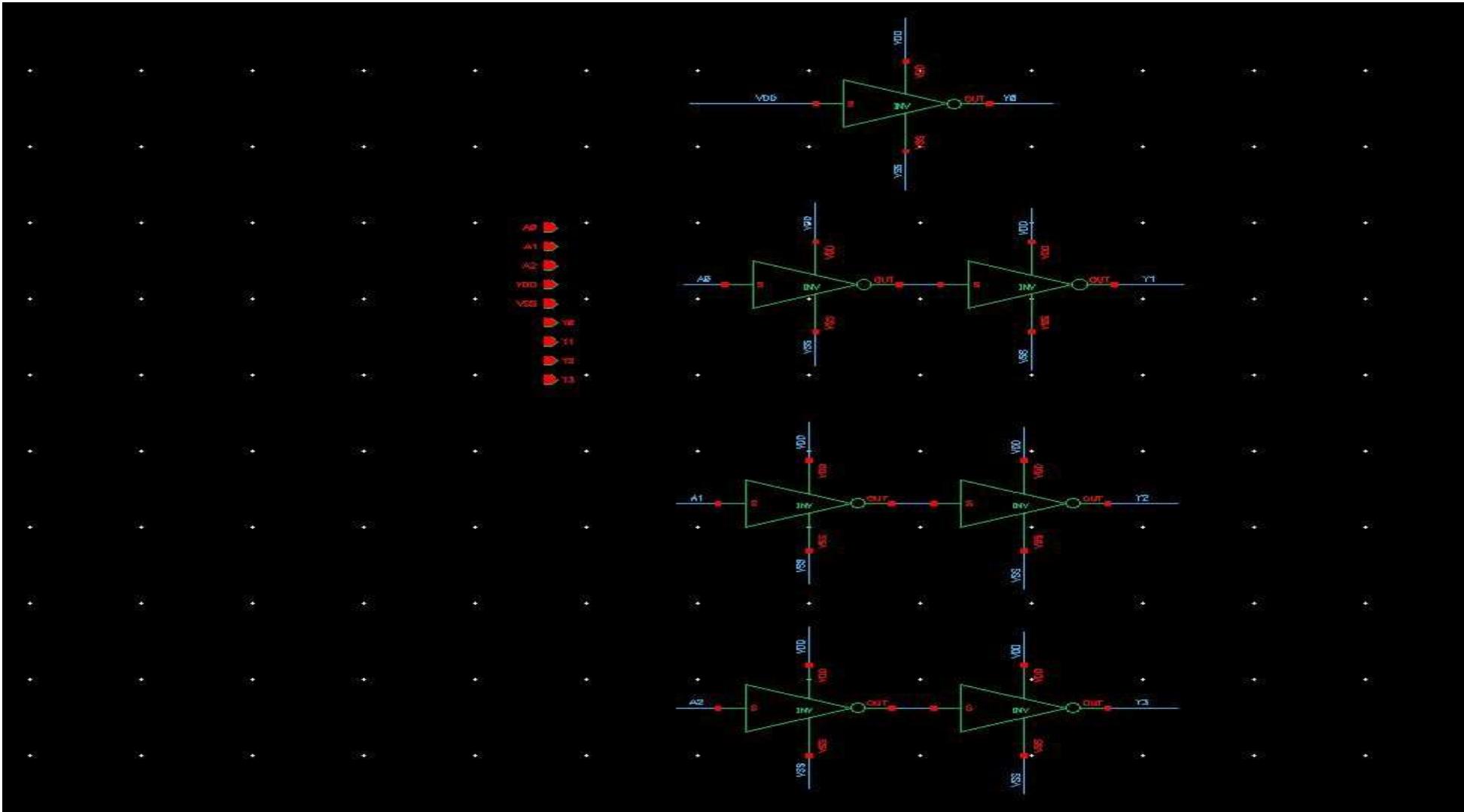
FULL_ADDER TESTBENCH



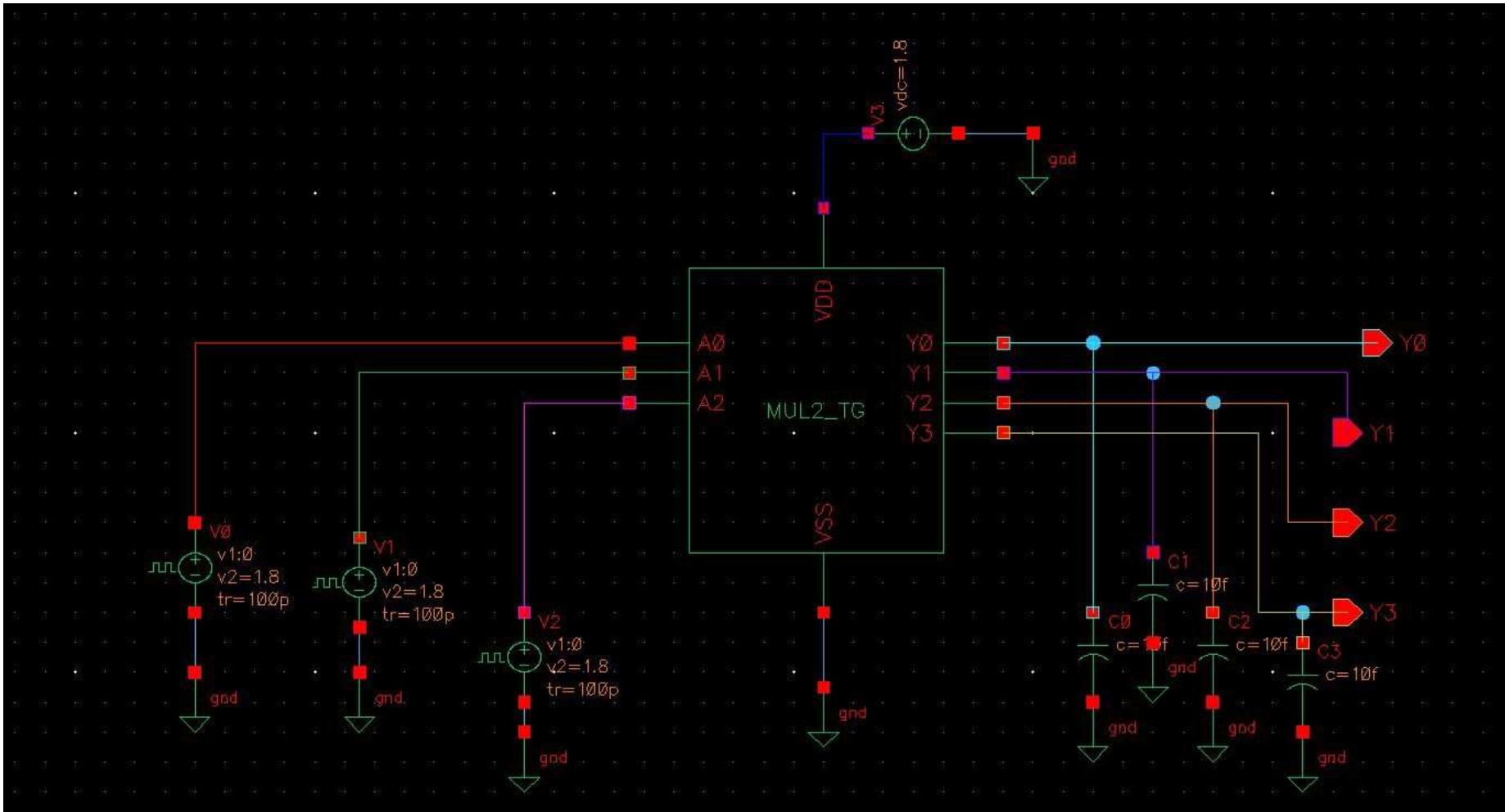
FULL_ADDER SIMULATIONS



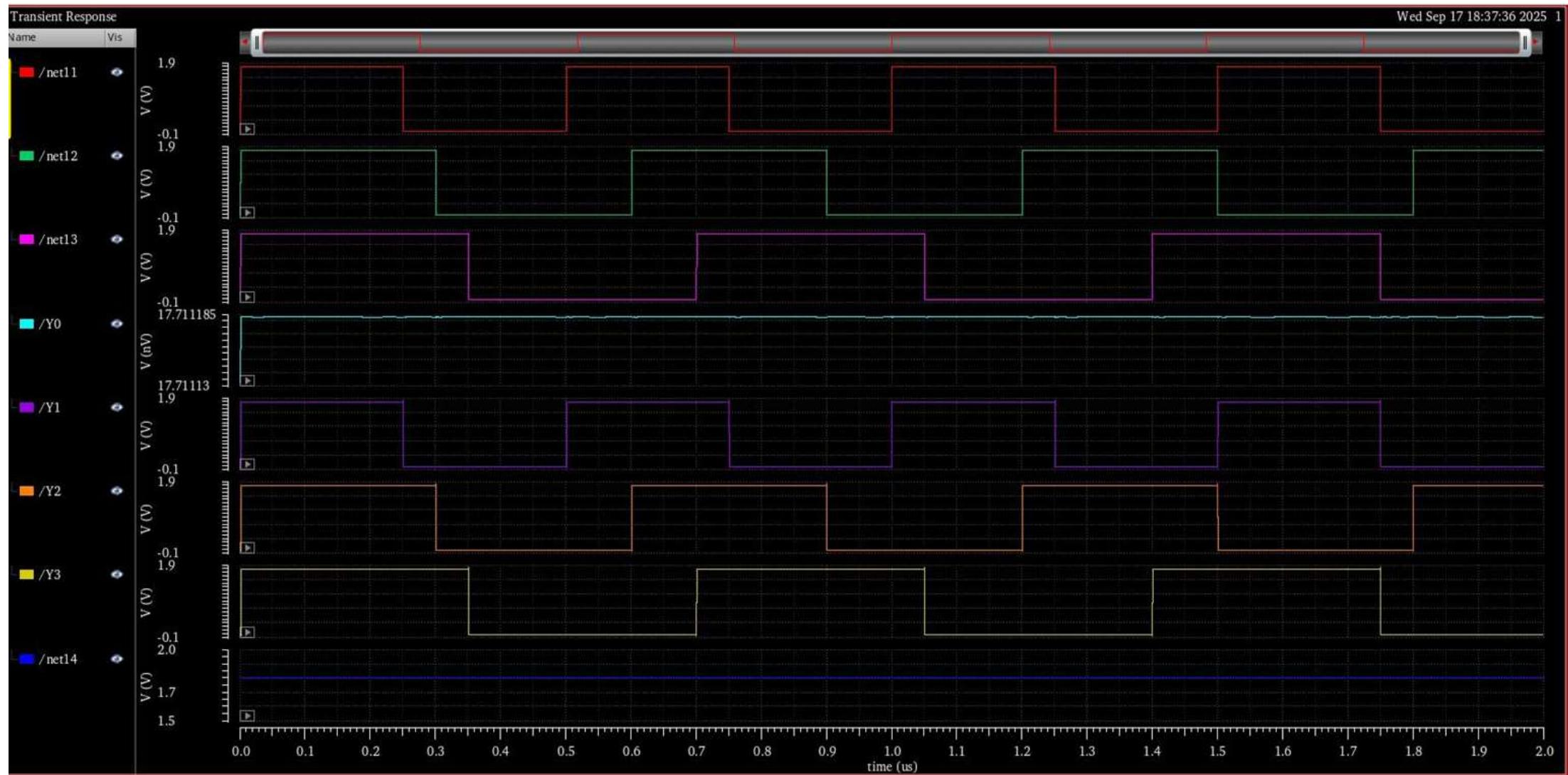
MUL2 SCHEMATIC



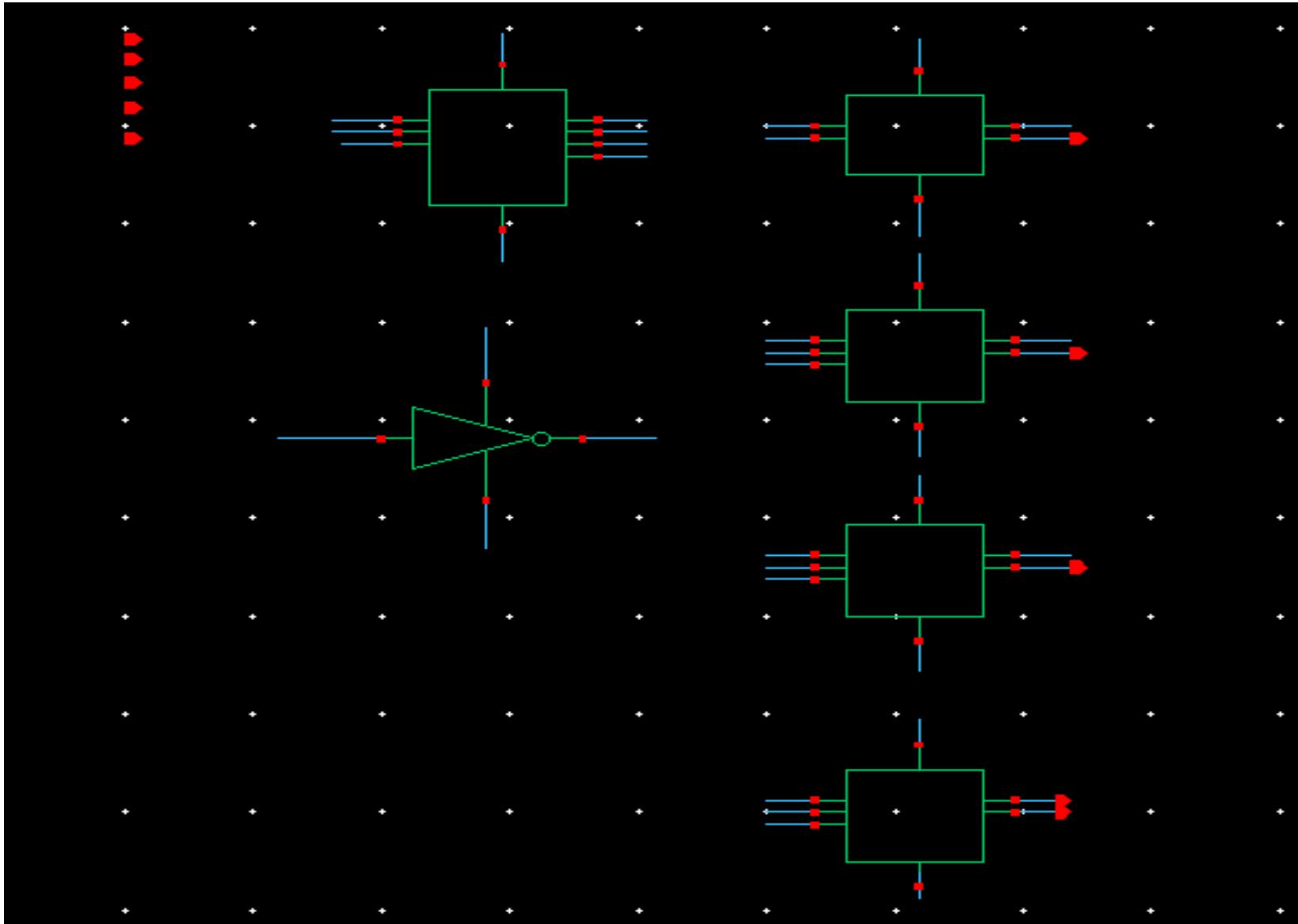
MUL2 TESTBENCH



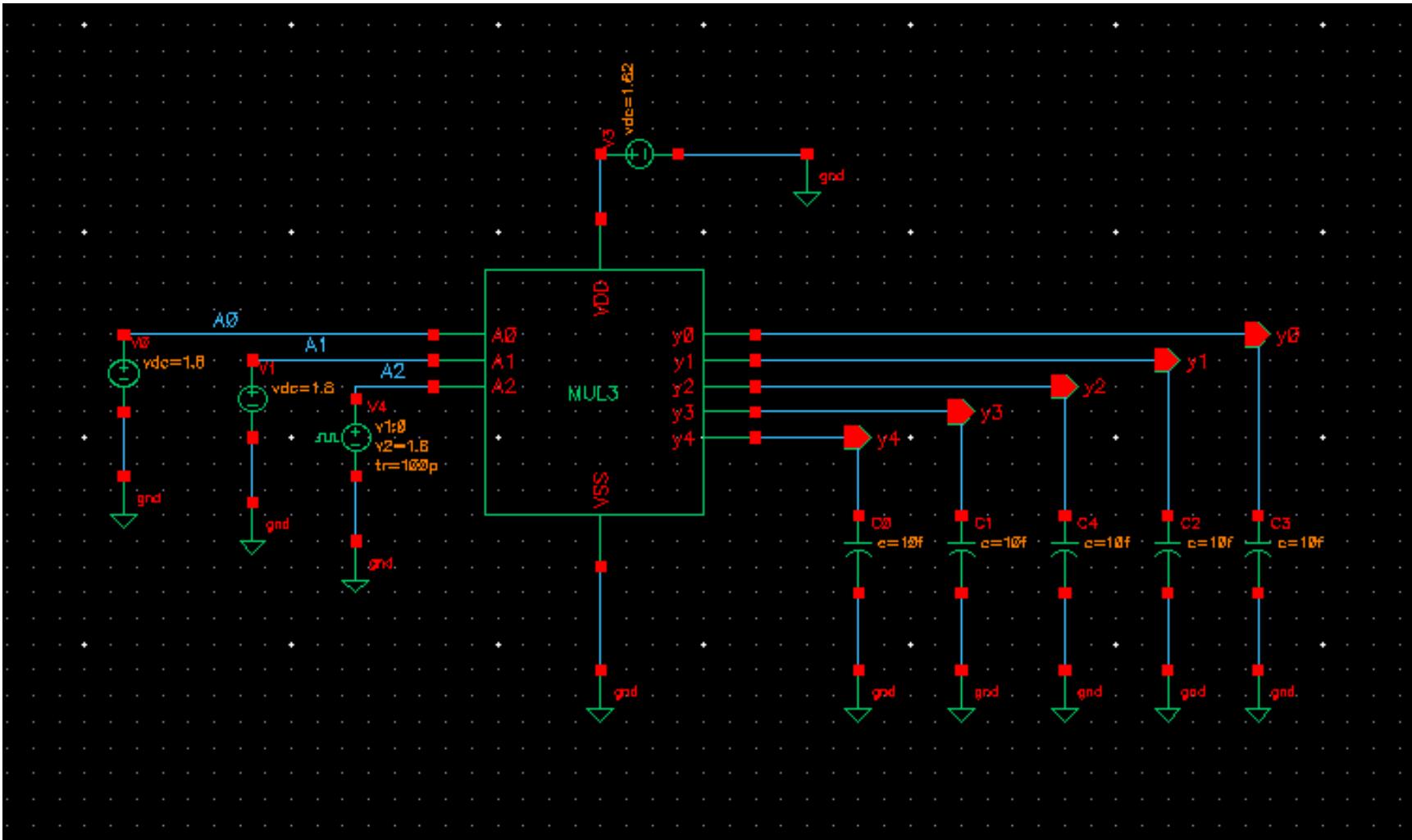
MUL2 SIMULATIONS



MUL3 SCHEMATIC



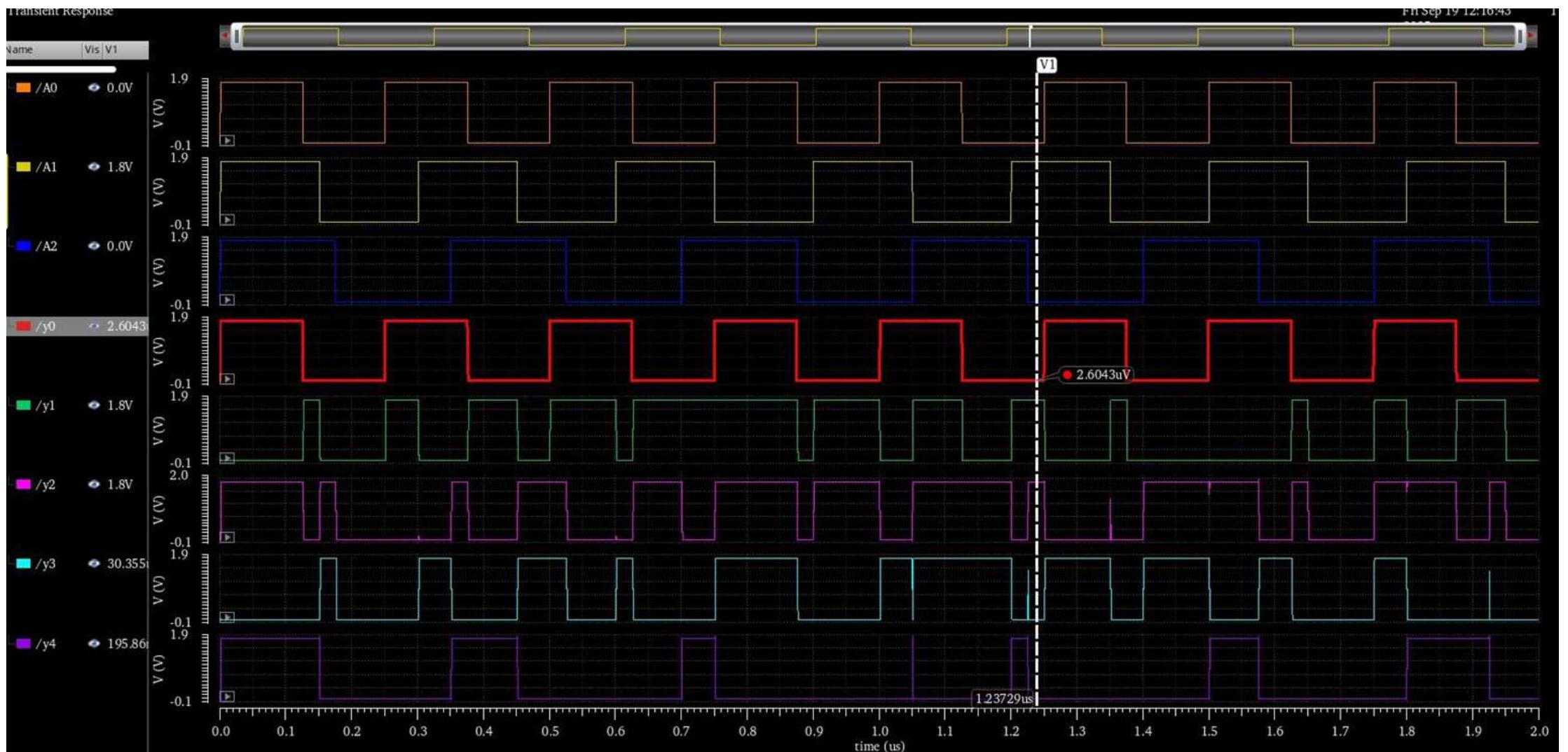
MUL3 TESTBENCH



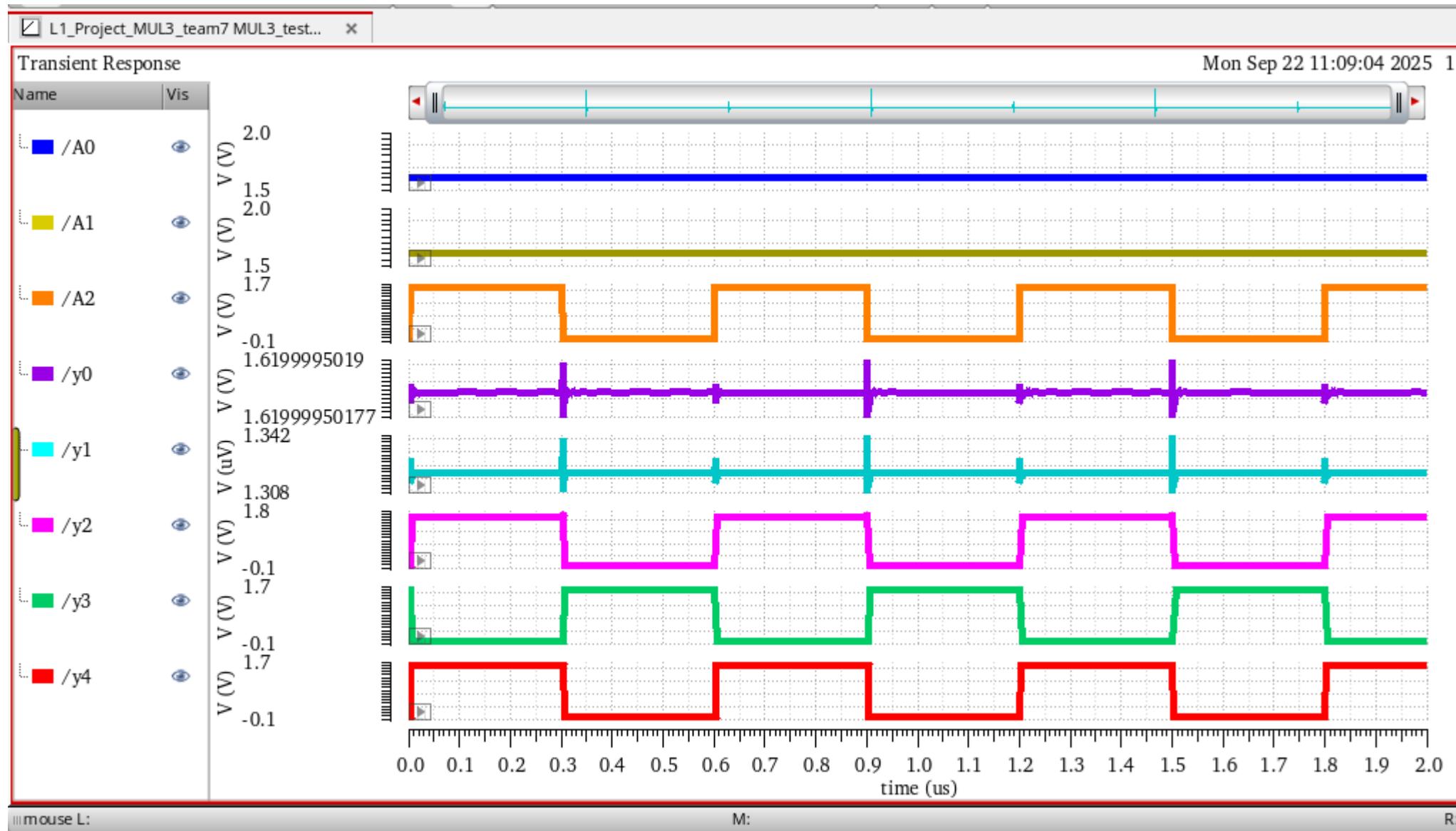
TRUTH TABLE _ MUL3

VDD	A2	A1	A0	Y4	Y3	Y2	Y1	Y0
1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1
1	0	1	0	0	0	1	1	0
1	0	1	1	0	1	0	0	1
1	1	0	0	1	1	1	0	0
1	1	0	1	0	1	1	1	1
1	1	1	0	1	0	0	1	0
1	1	1	1	1	0	1	0	1

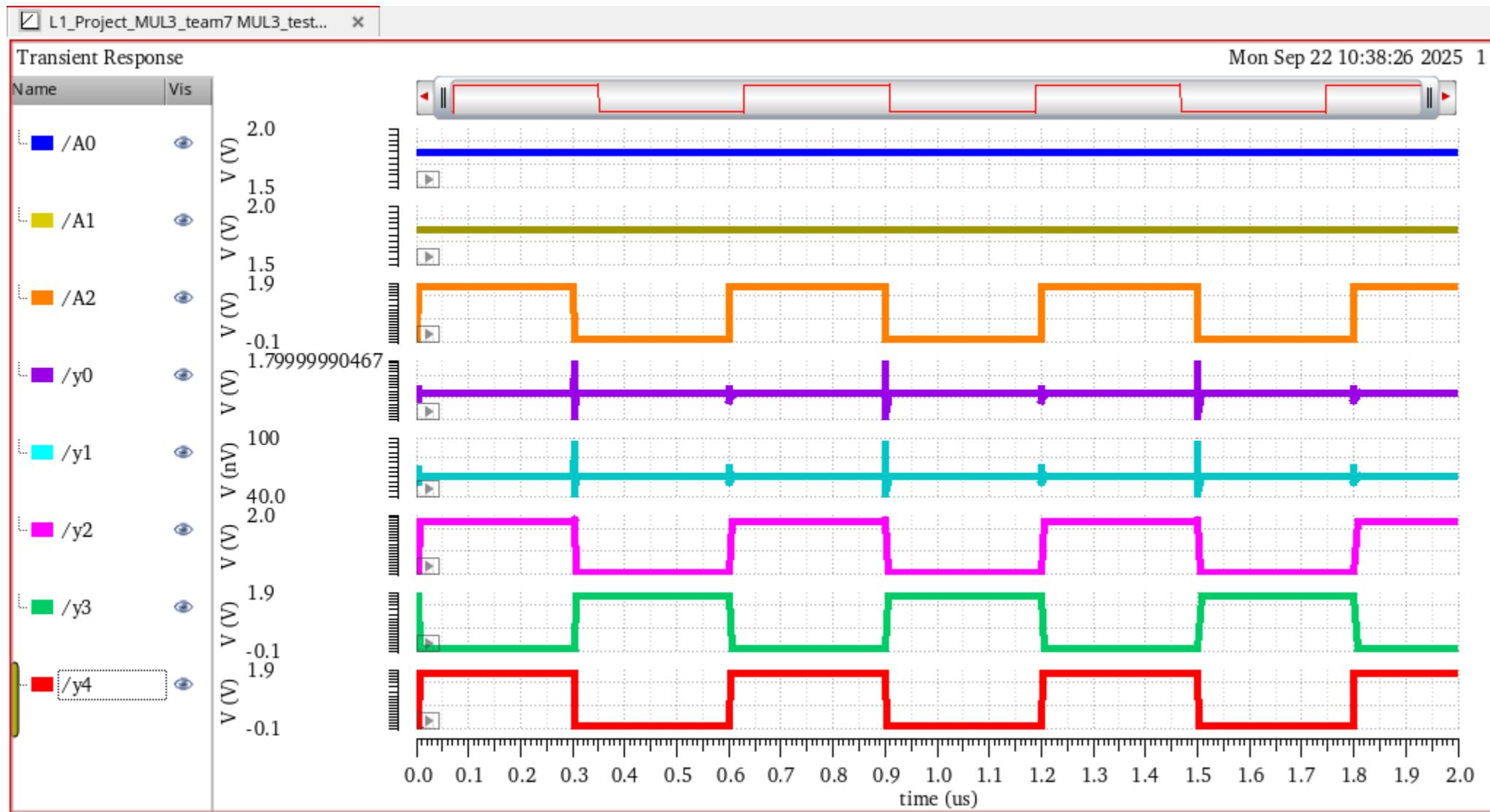
MUL3 SIMULATIONS



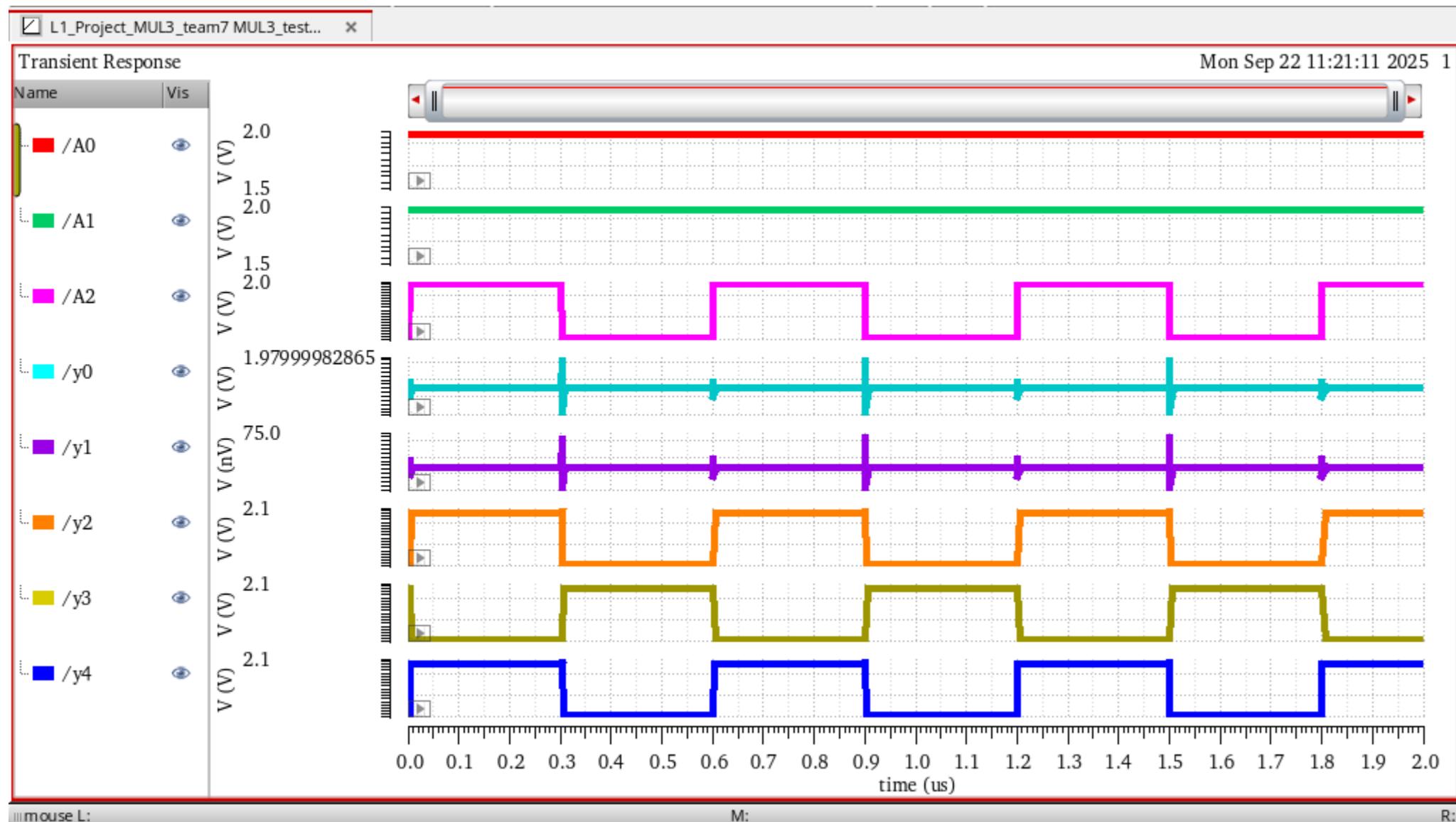
ss – slow-slow , 1.62 , 100 degree



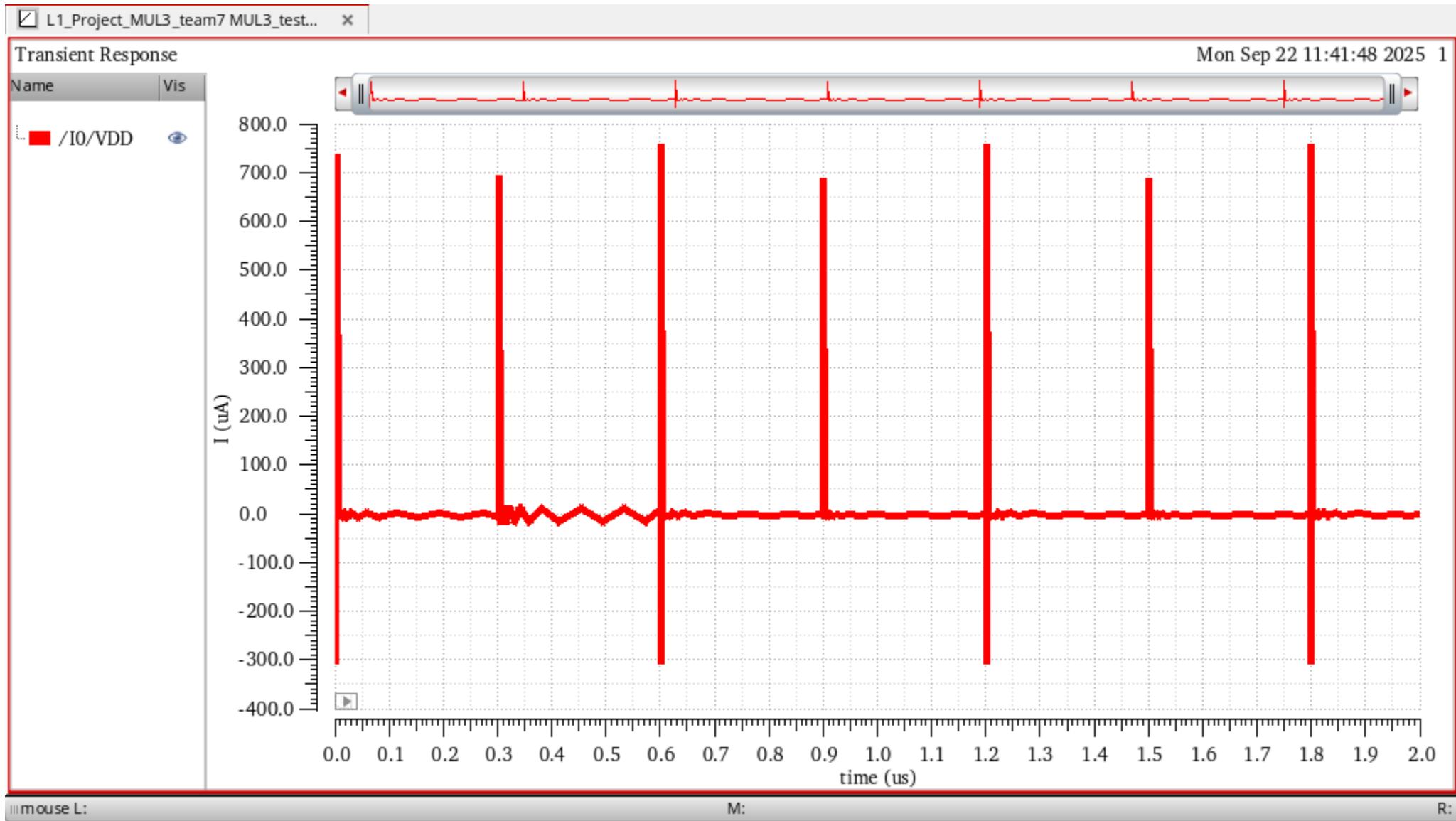
tt – typical-typical , 1.8 , 27 degree



ff – fast-fast , 1.98 , 0 degree



Current Waveform



WORST DELAY A2 □ Y3

PROCESS	ss	tt	ff
RISE DELAY	540.02ps	345.902ps	257.22ps
FALL DELAY	633.54ps	338.173ps	286.748ps
CURRENT	1.010uA	1.1uA	1.257uA

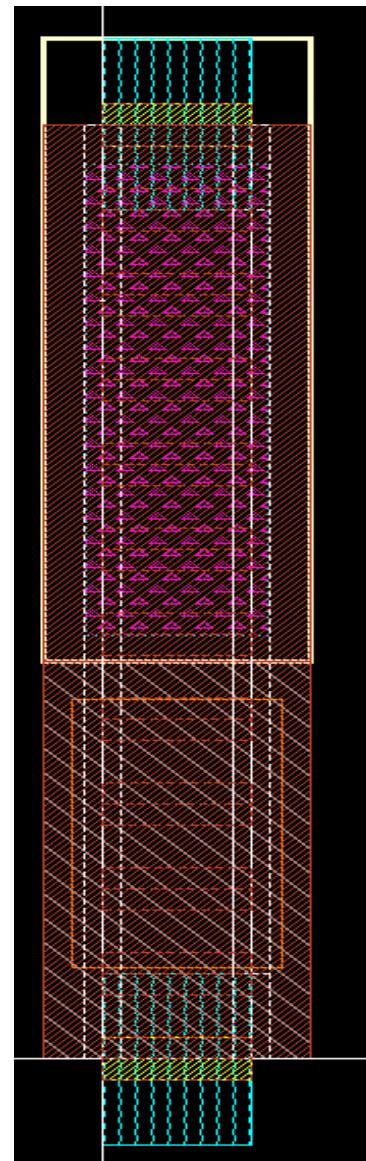
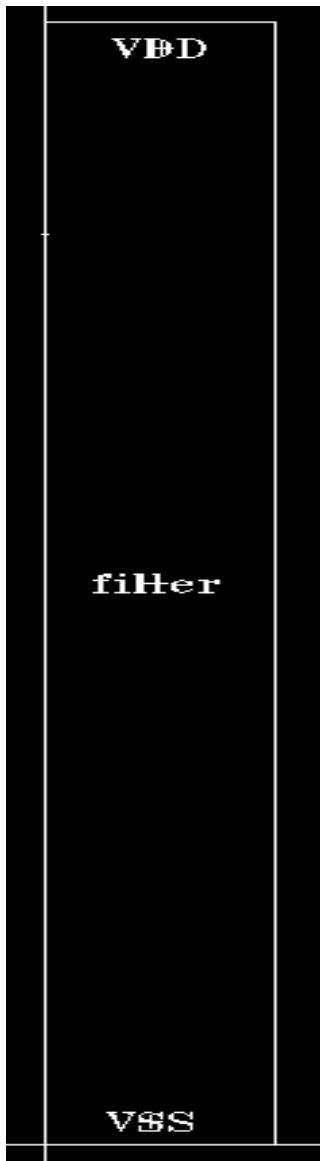
Number of Transistors used = 160

- More delay is in ss
- More current is in ff

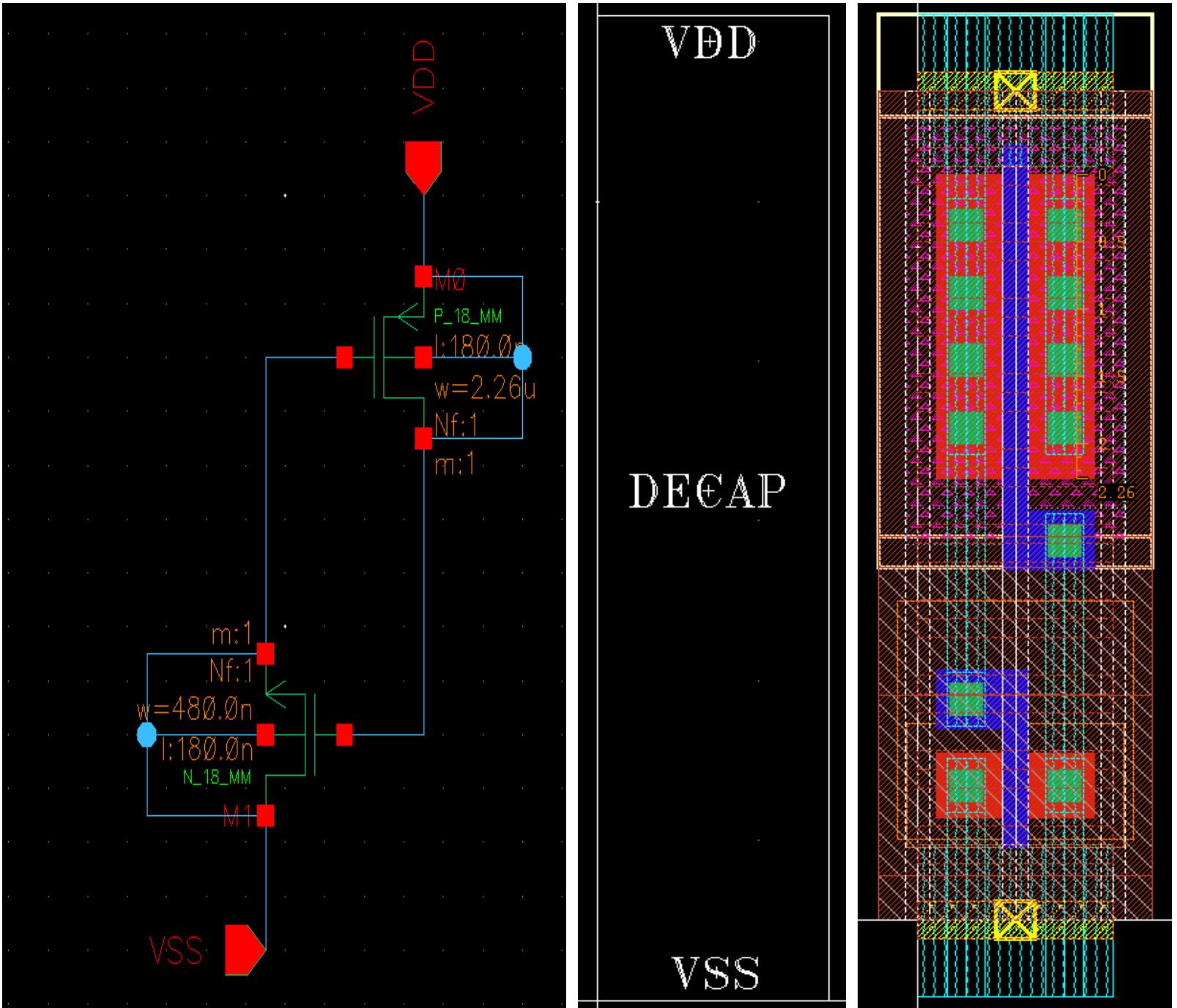
APPLICATIONS

1. Arithmetic and logic units (ALUs)
2. Digital Signal Processing
3. Graphics and Image Processing
4. Computer Graphics / Geometry

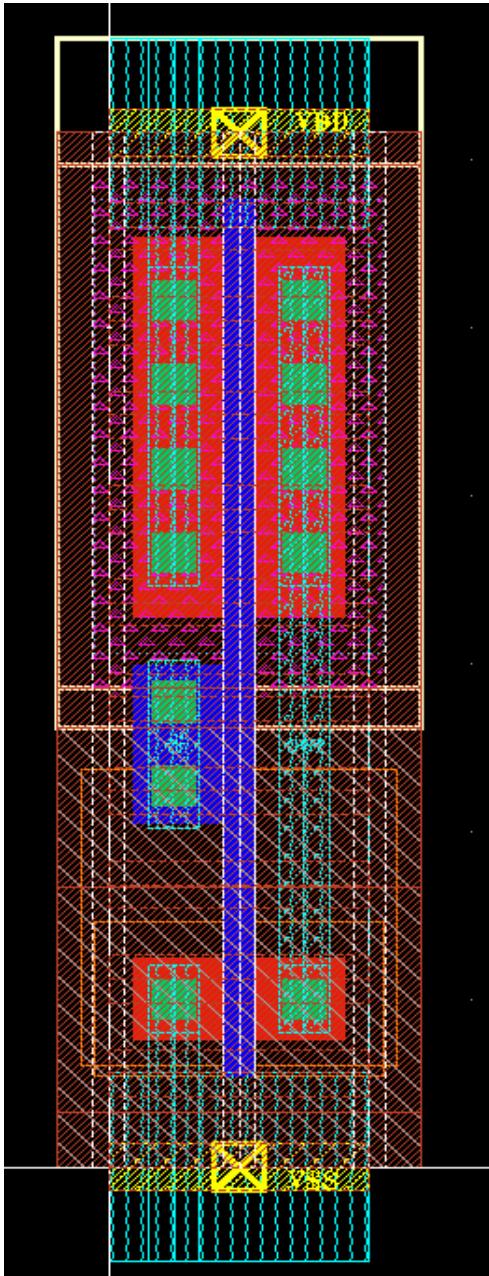
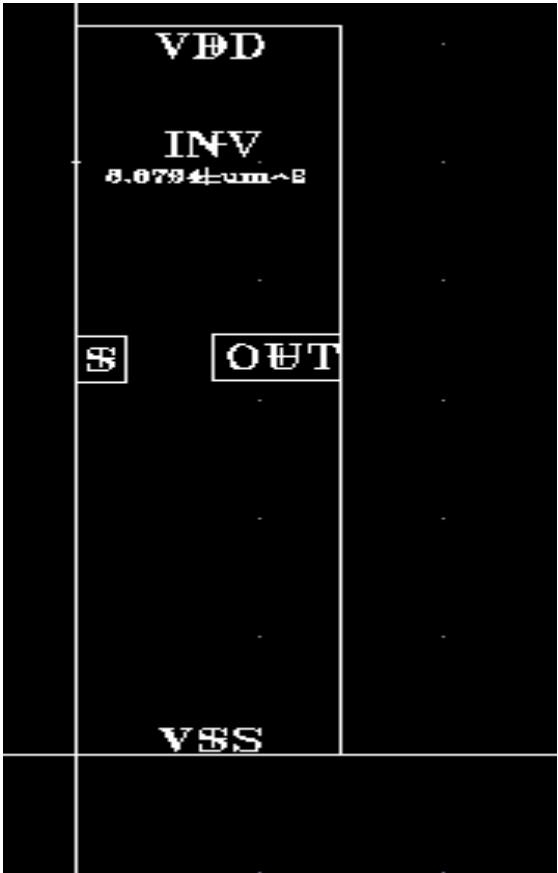
Filler Floor Plan and Layout:



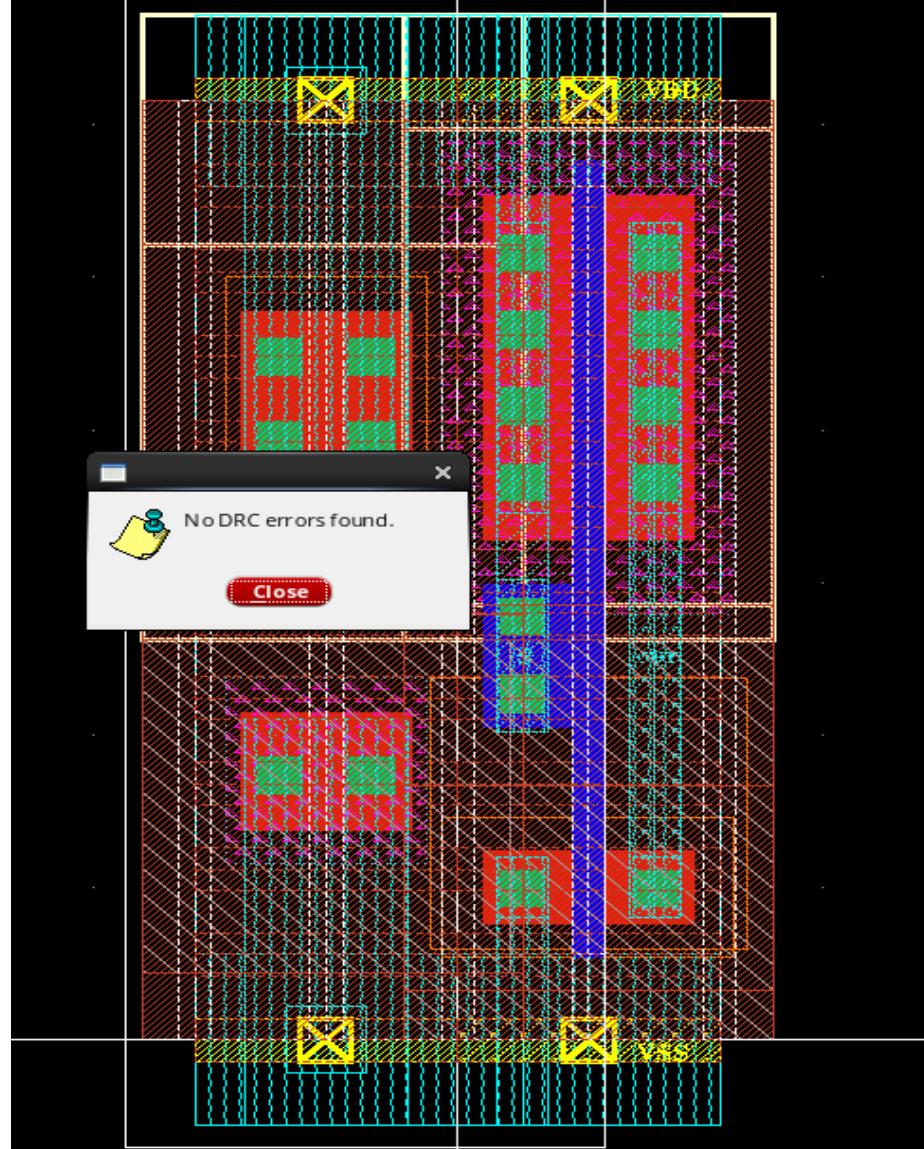
Decap Schematic, Floor Plan, Layout:



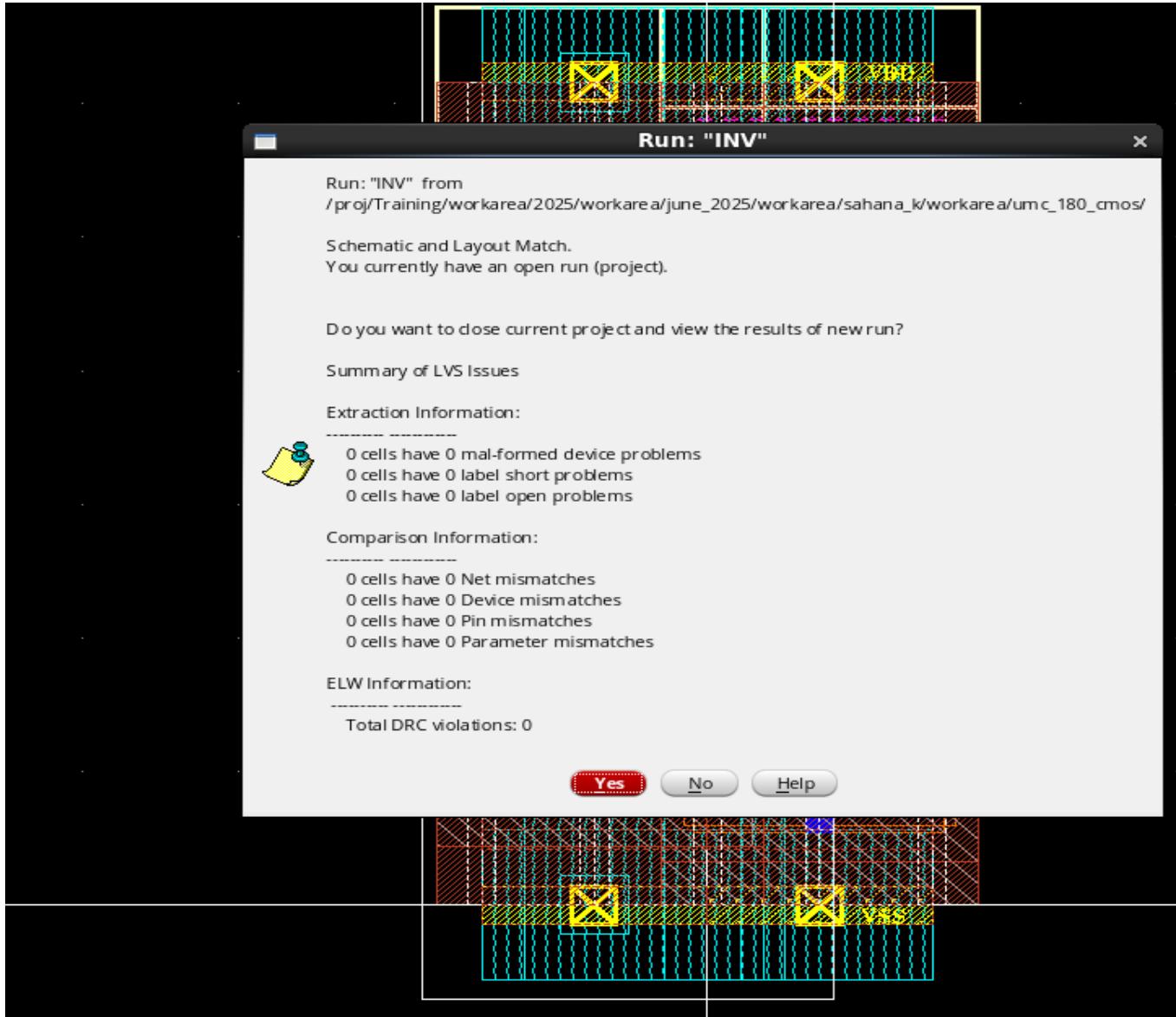
Inverter Floor Plan and Layout:



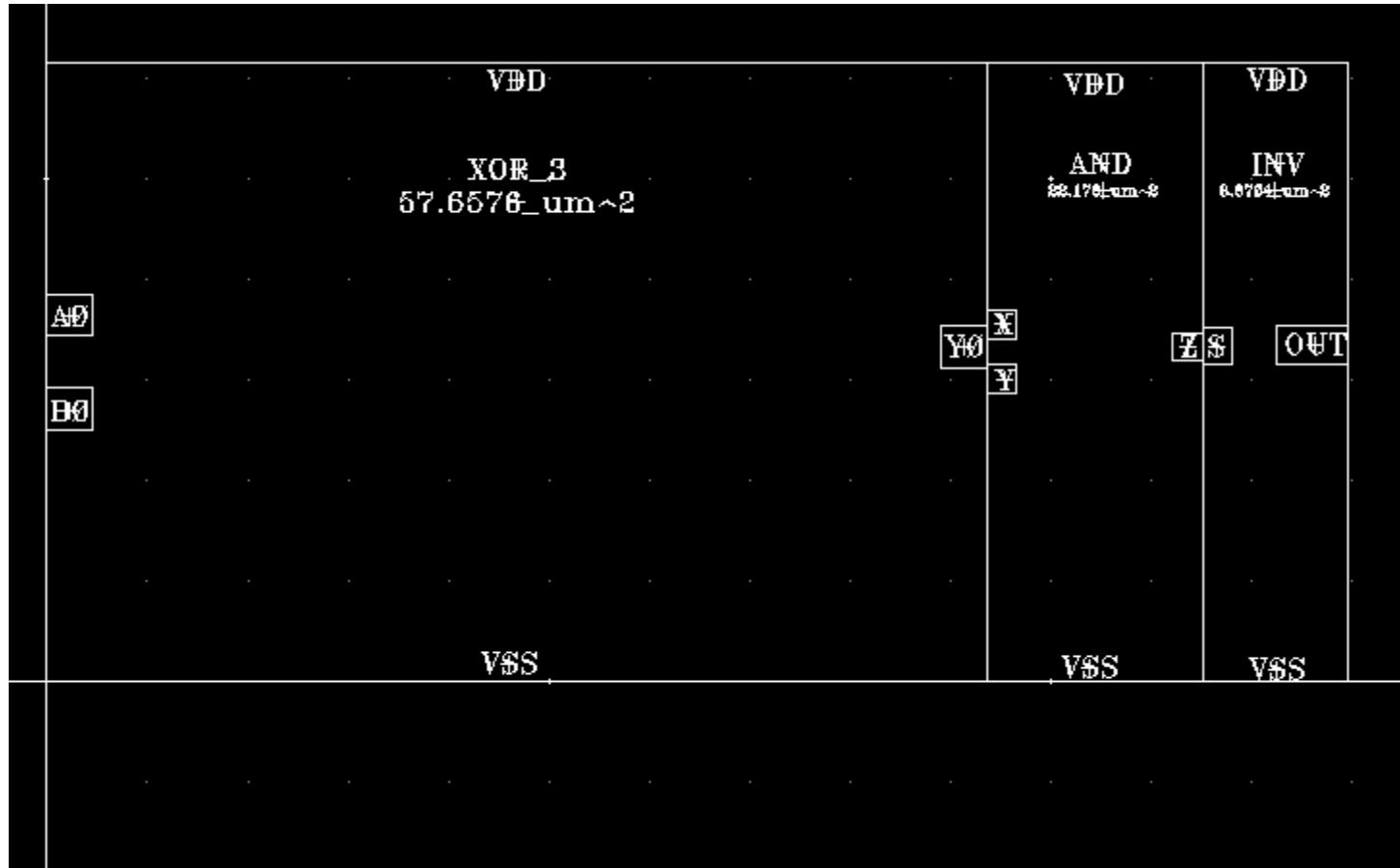
DRC Check:



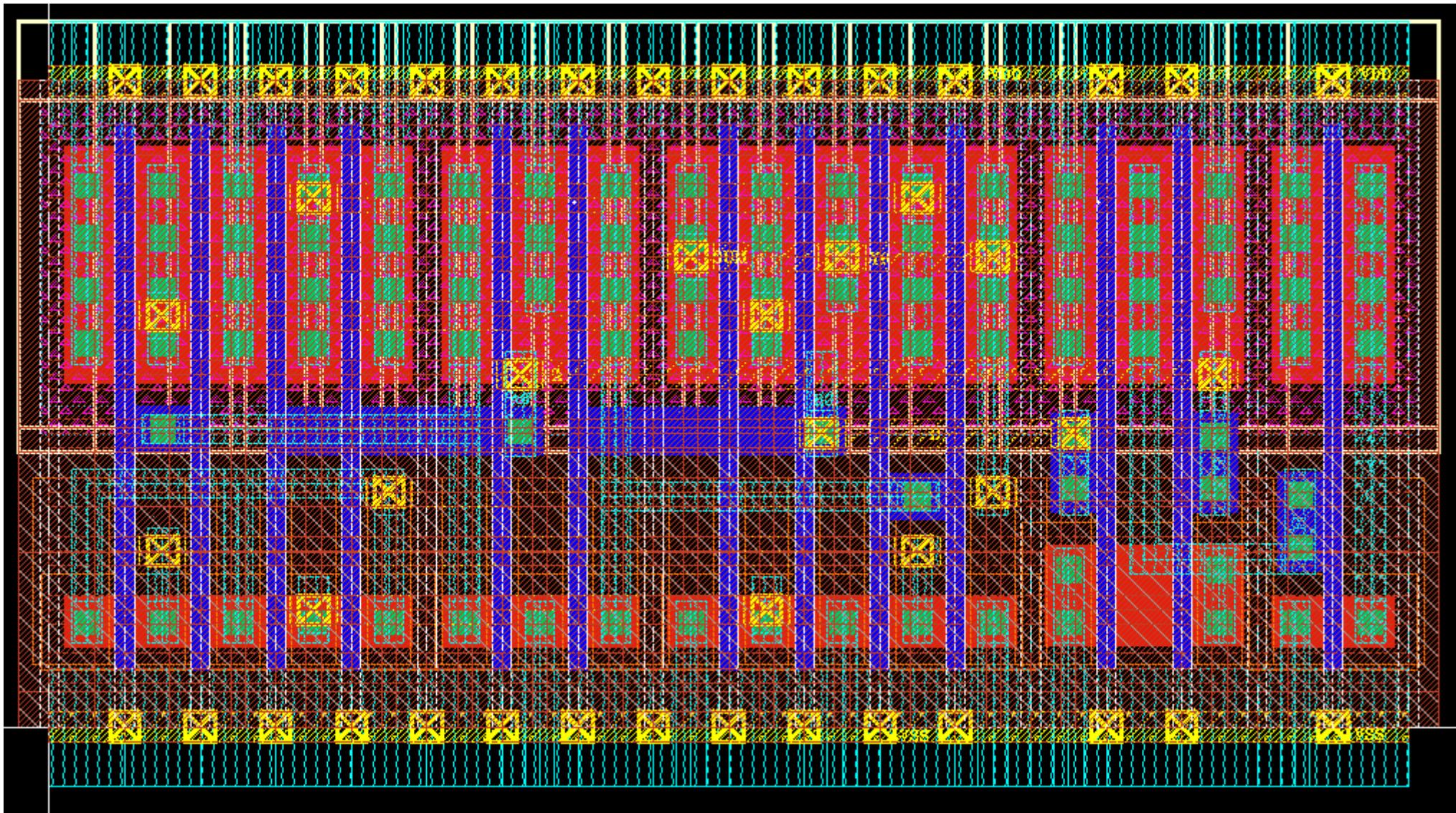
LVS Check:



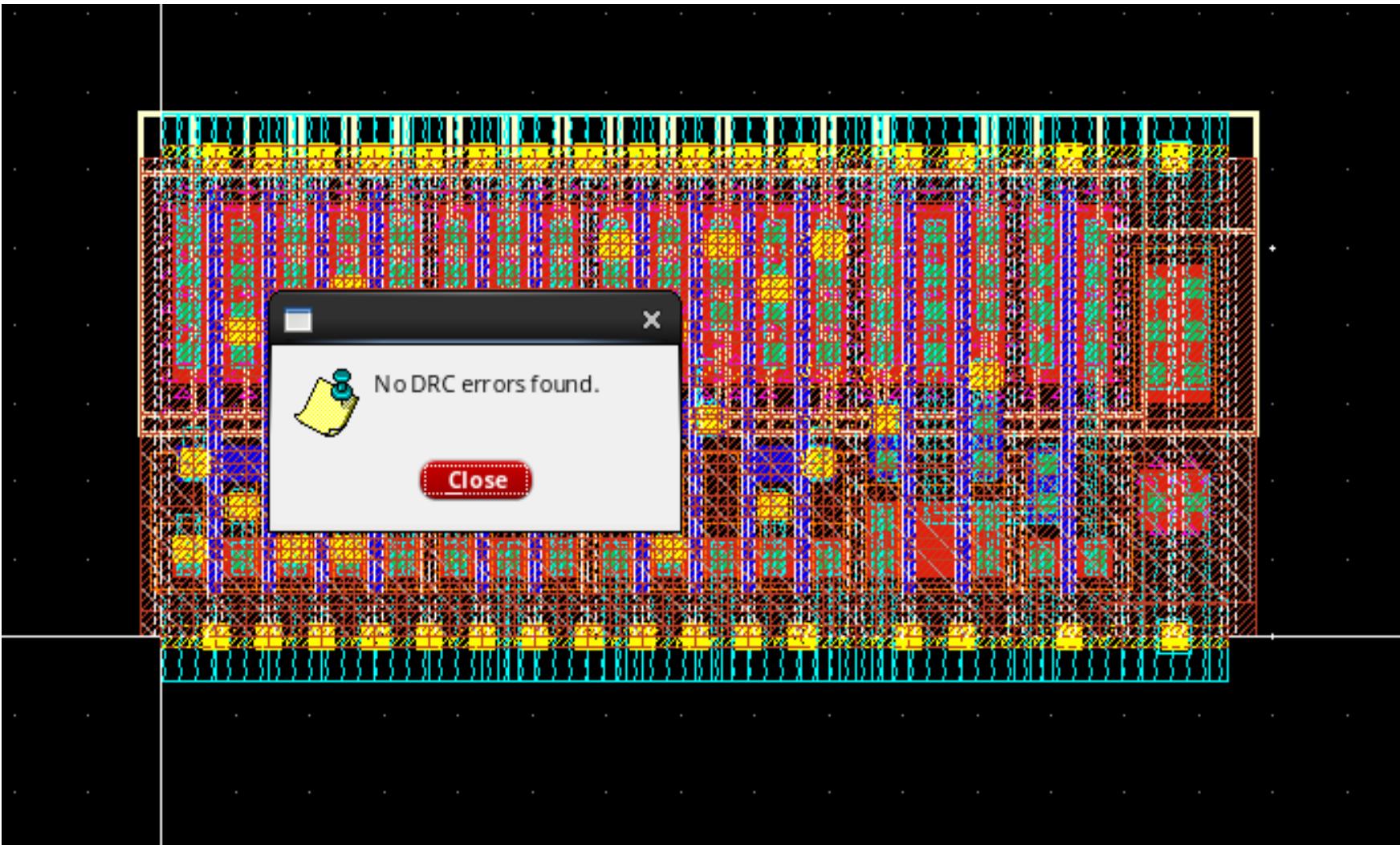
Half Adder Floor Plan:



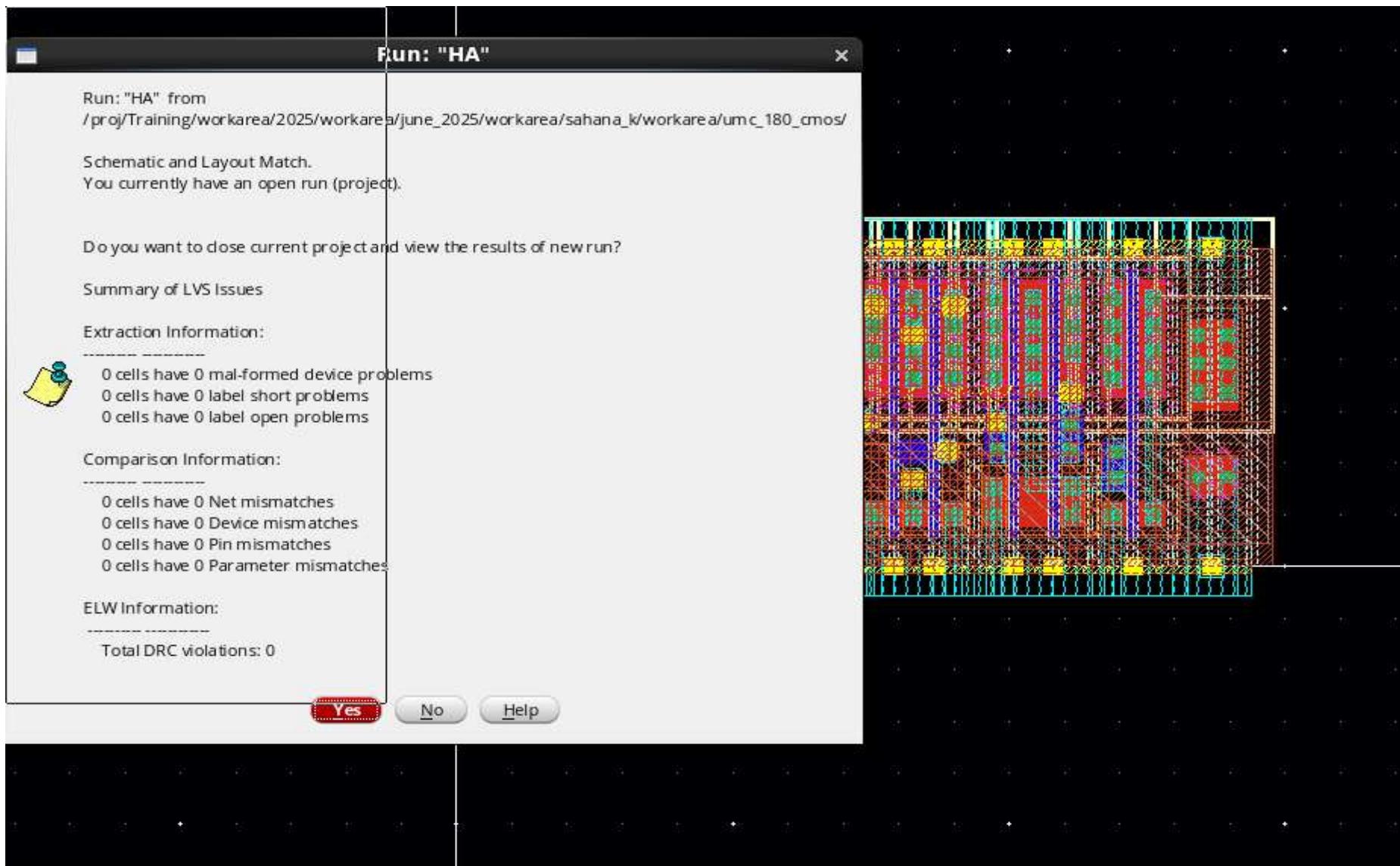
Half Adder Layout:



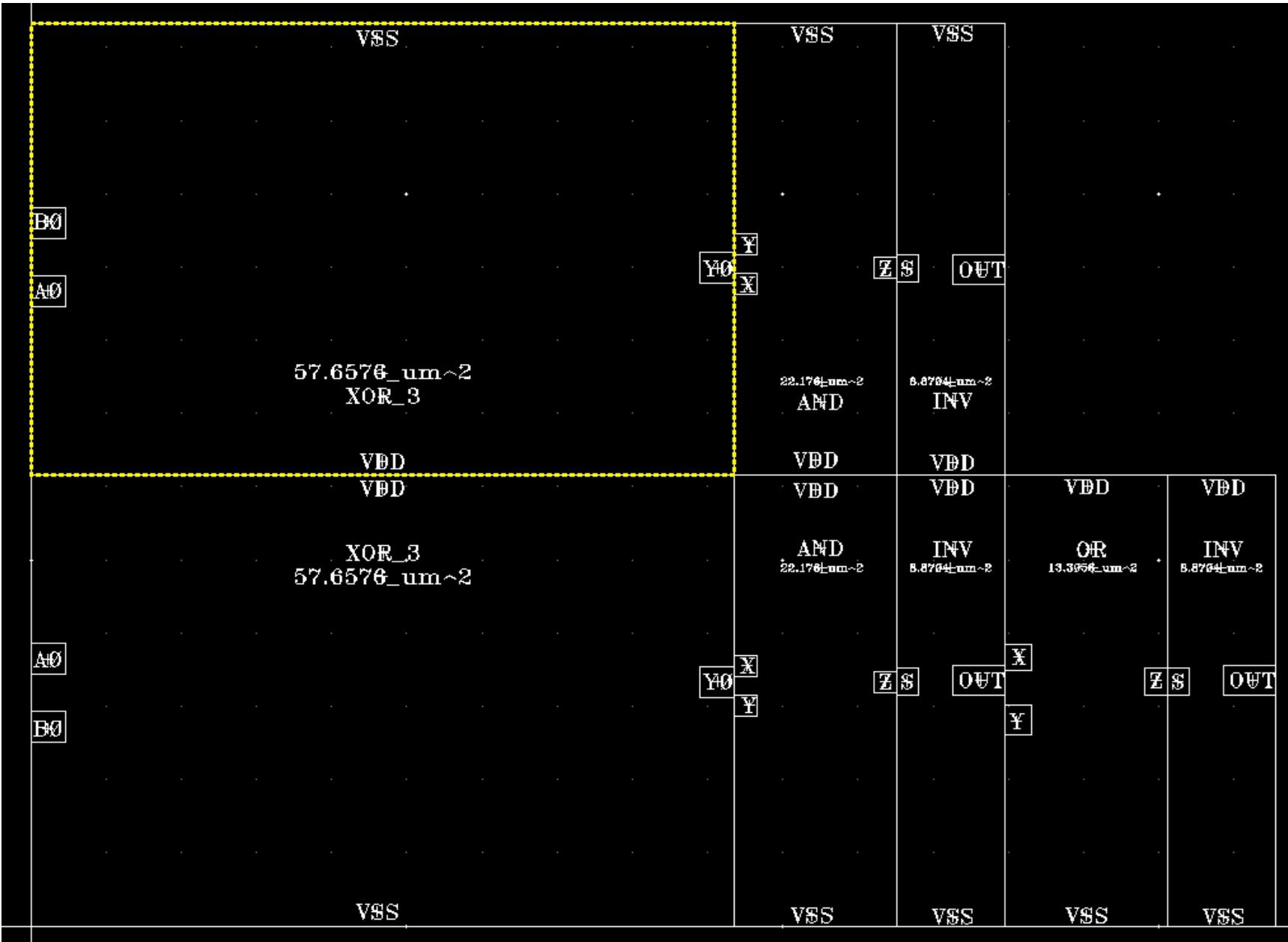
DRC Check:



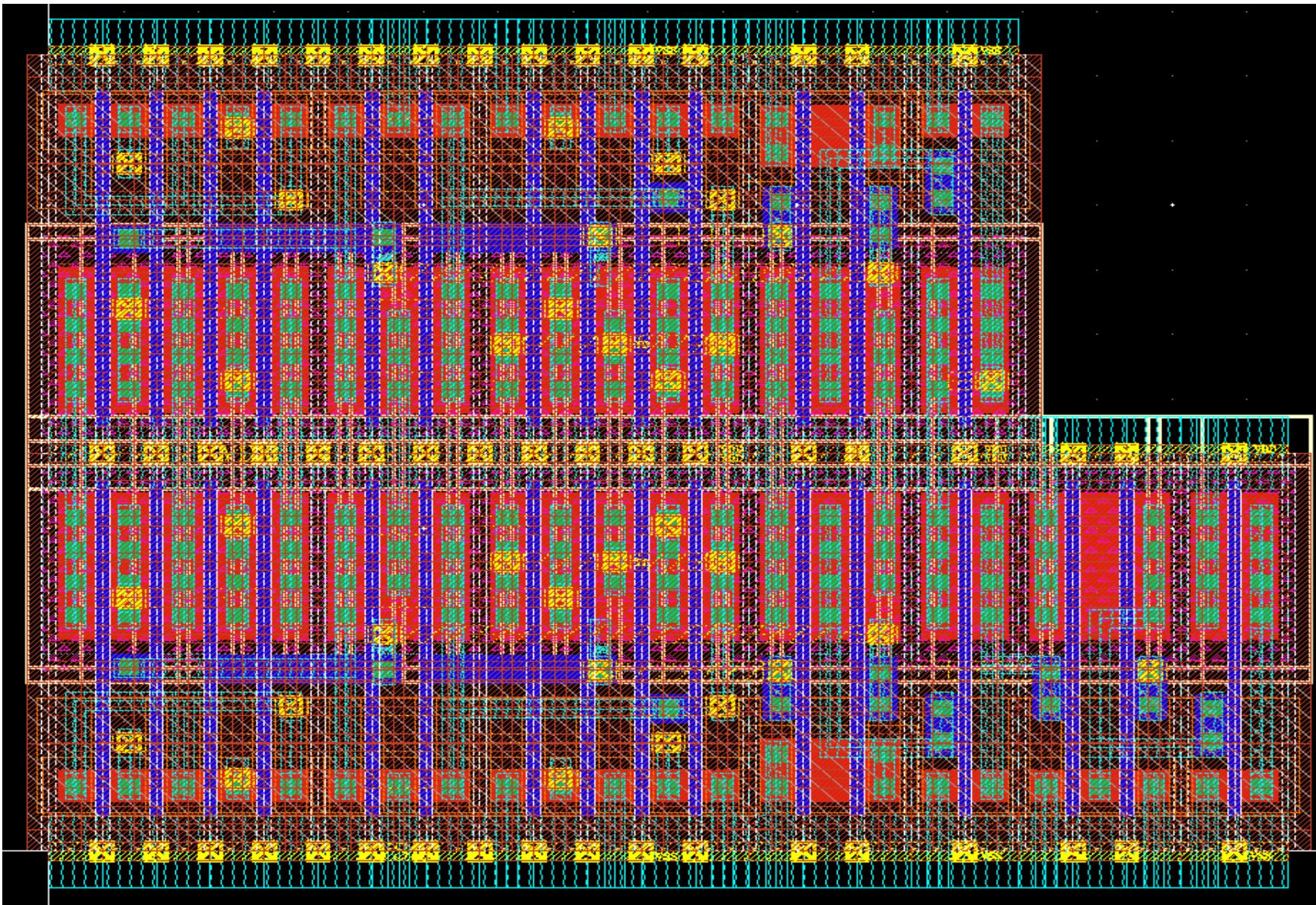
LVS Check:



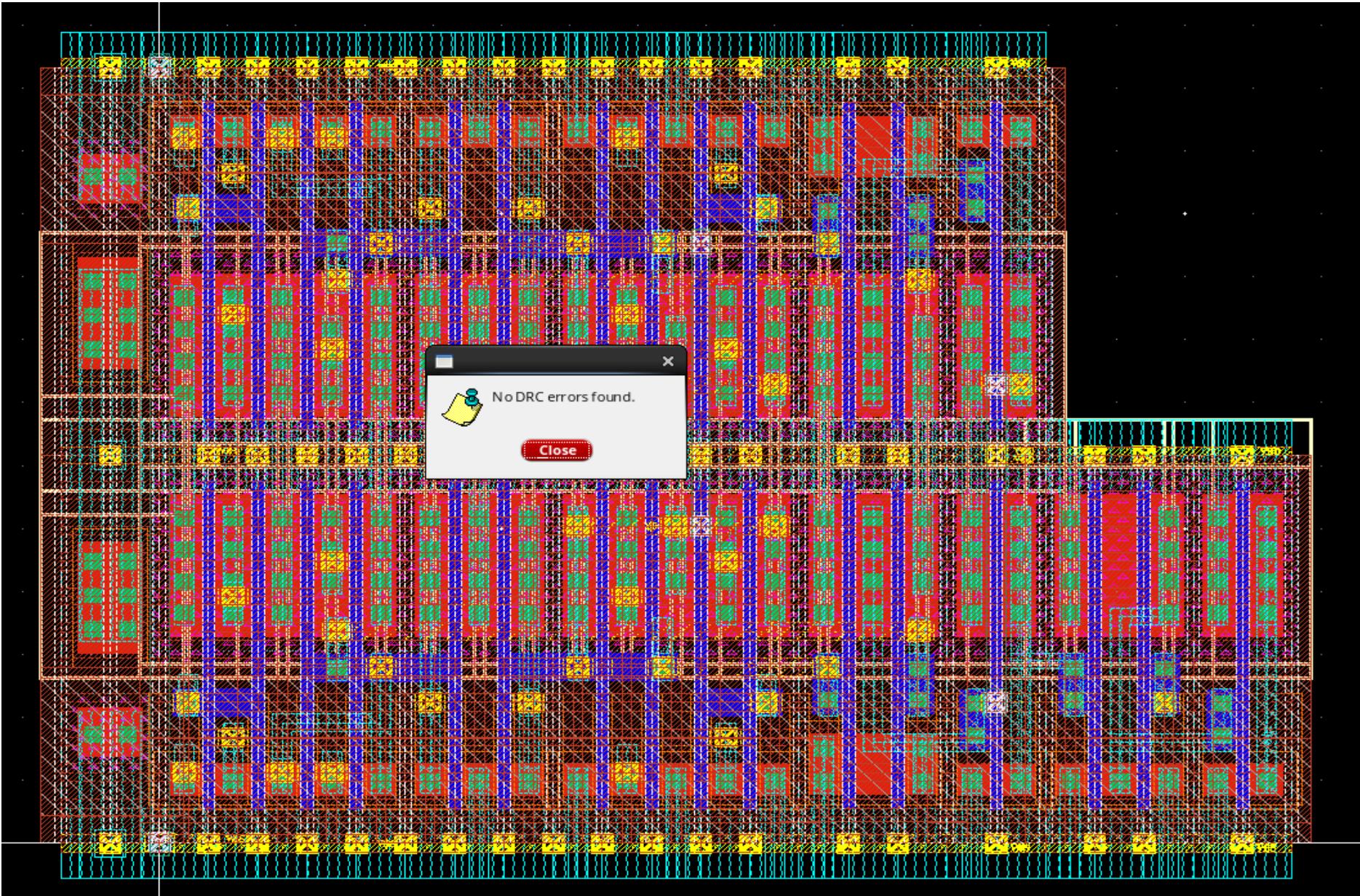
Floor Plan of Full Adder:



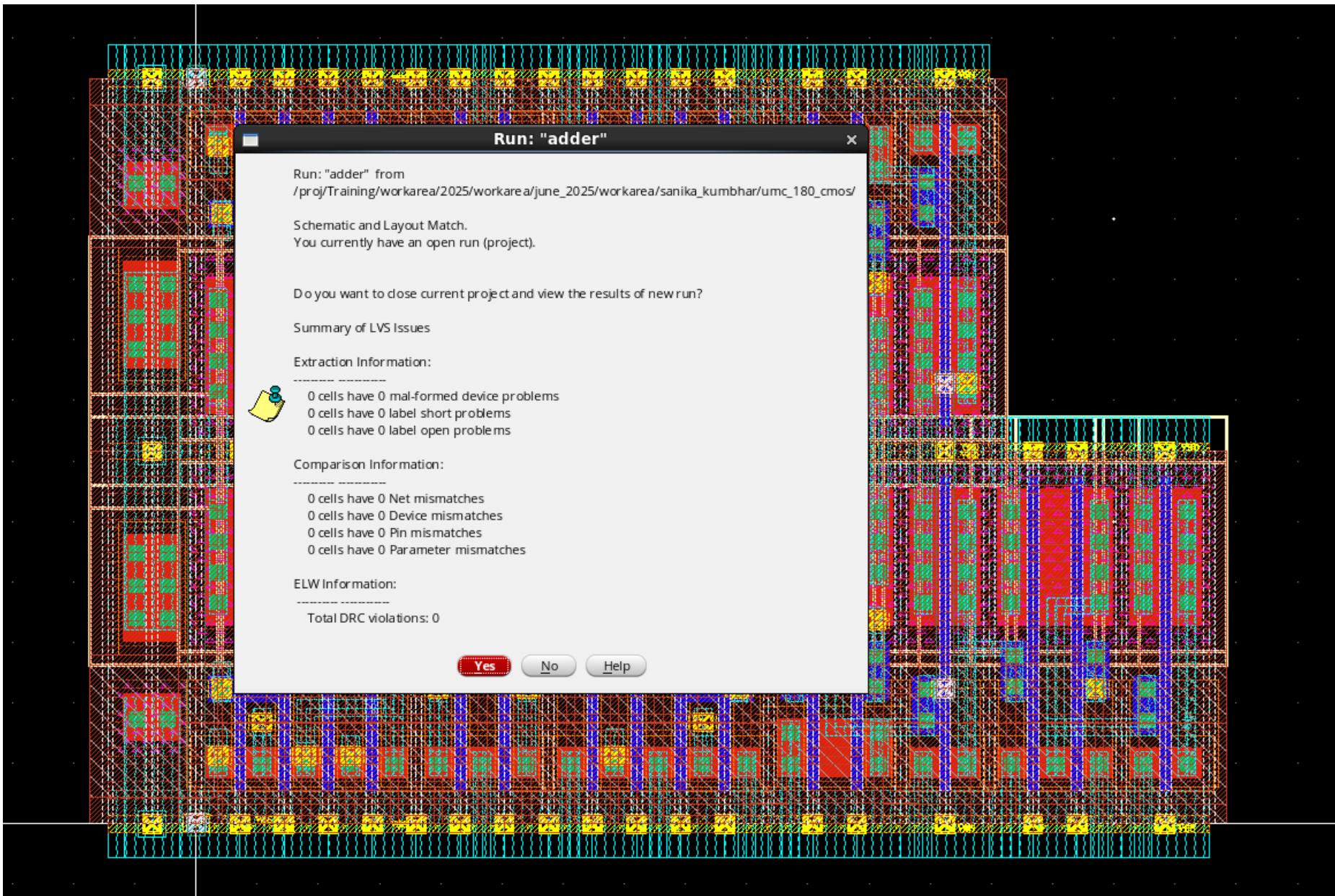
Layout of Full Adder:



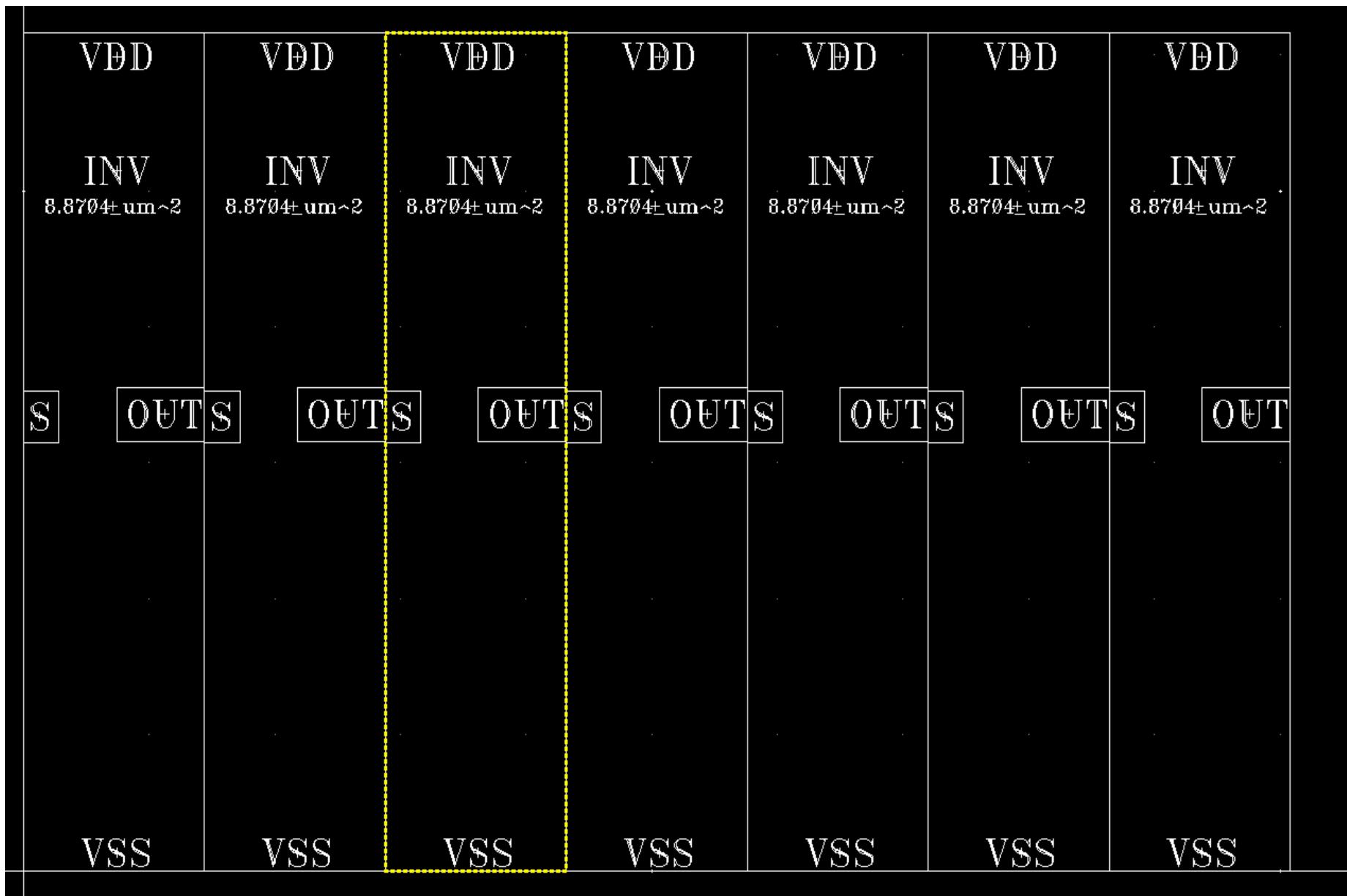
DRC Check:



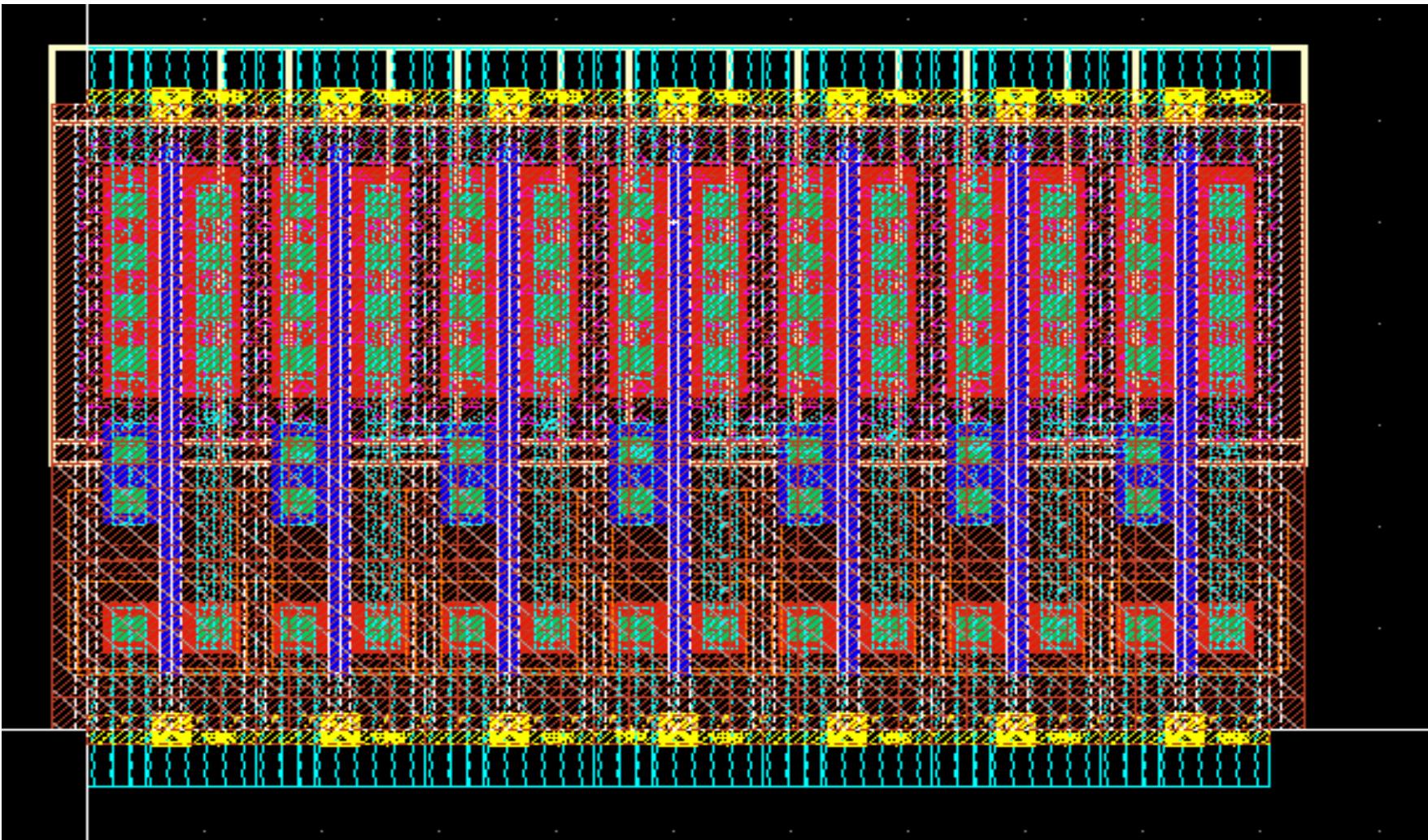
LVS Check:



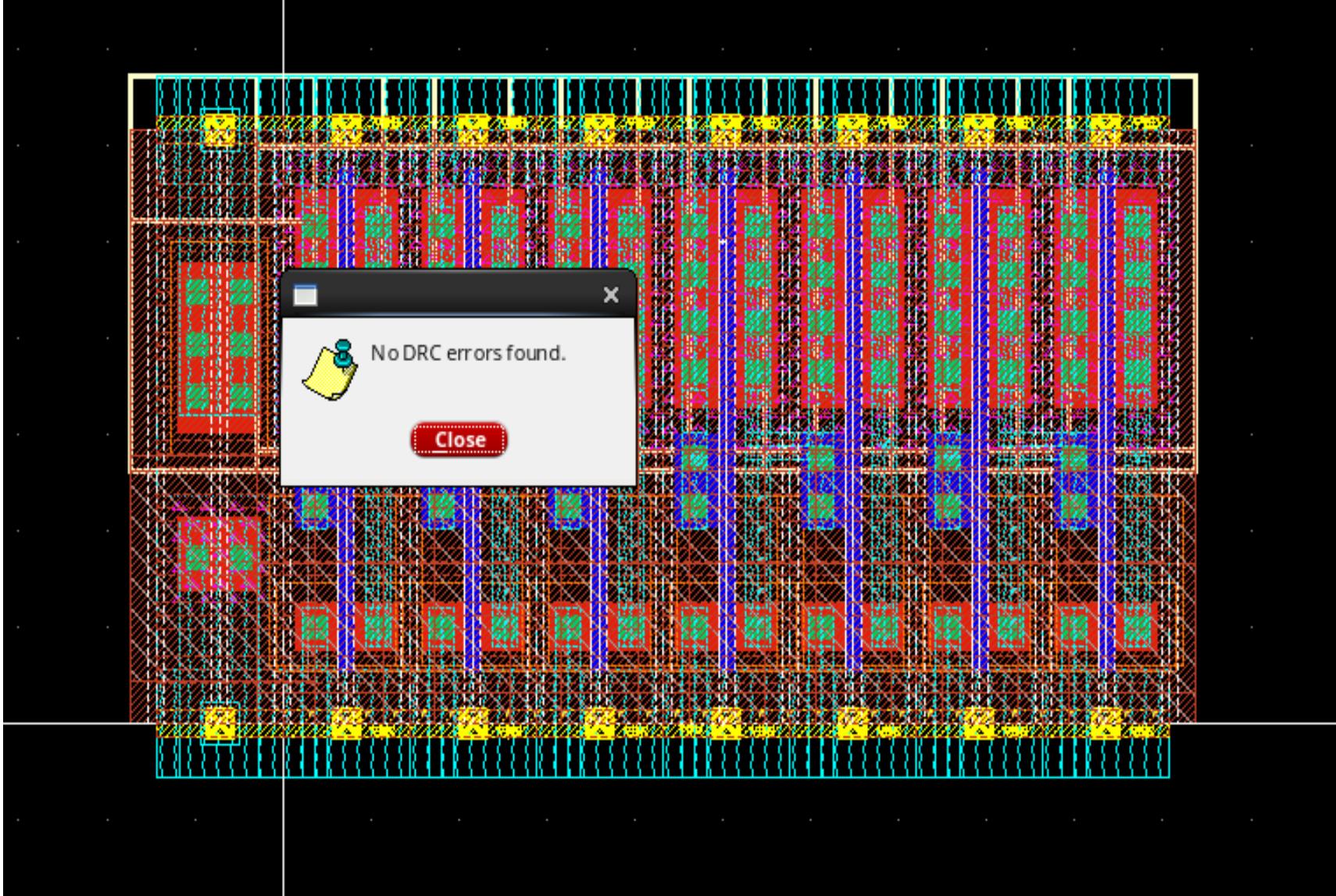
Floor Plan of MUL2:



Layout of MUL2:



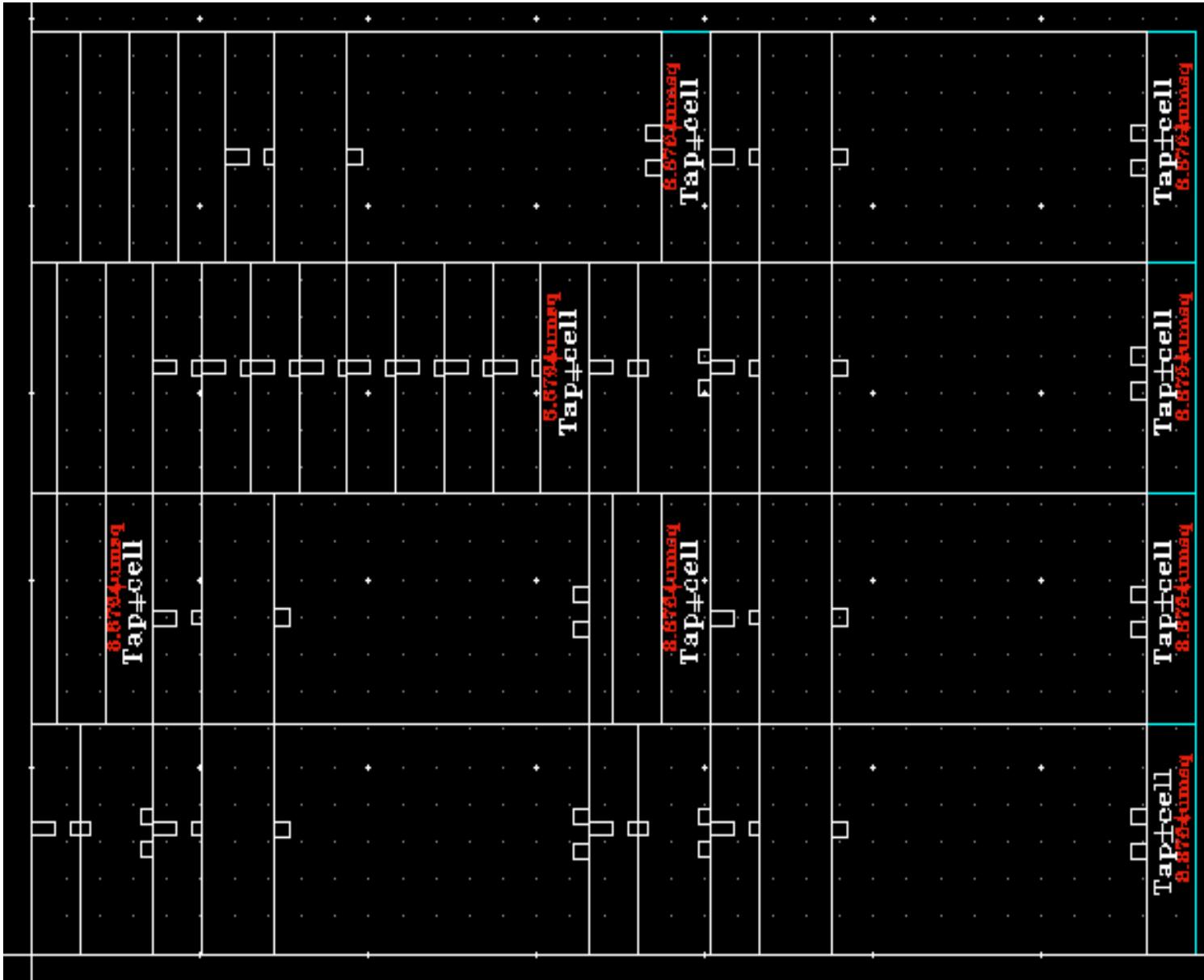
DRC Check:



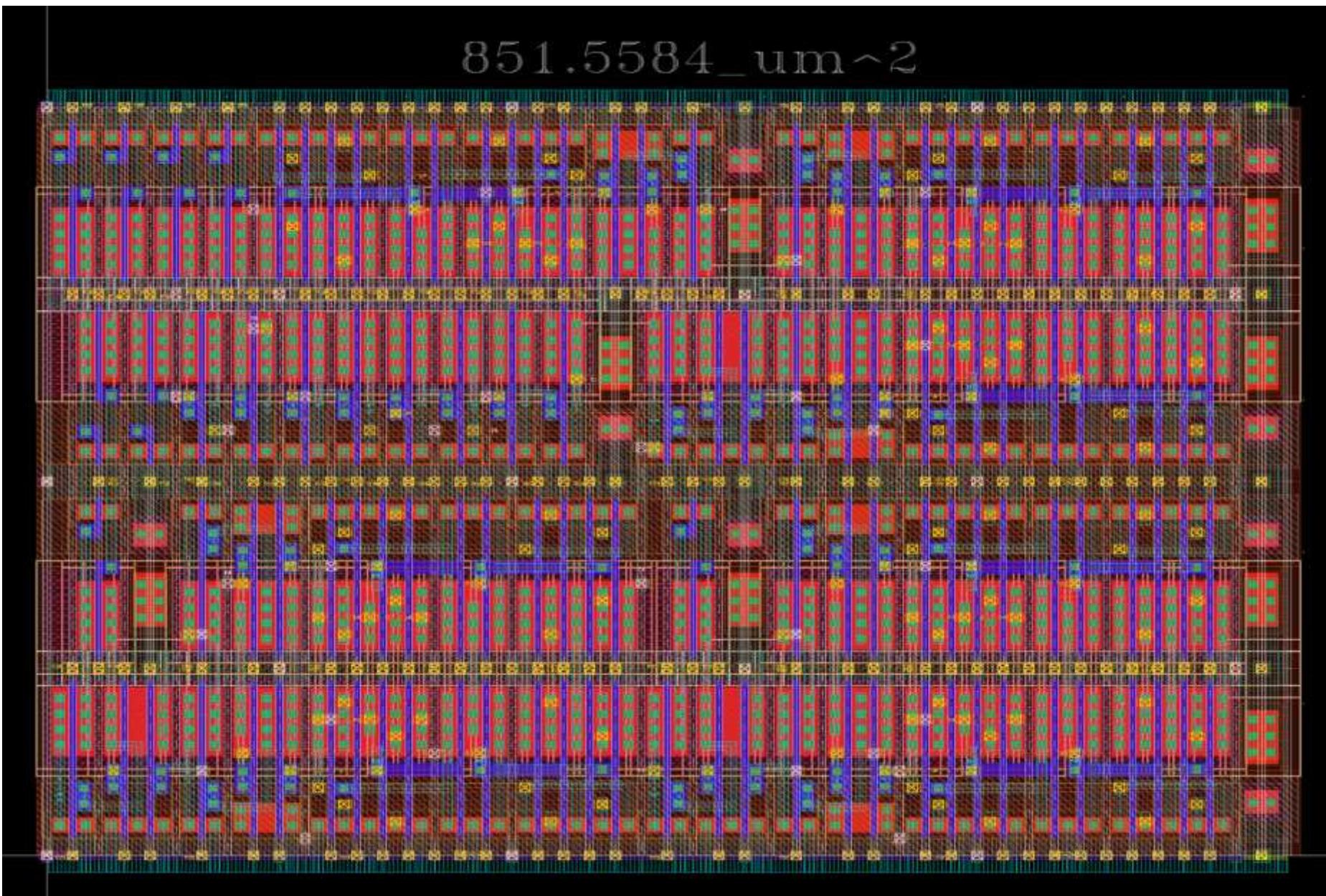
LVS Check:



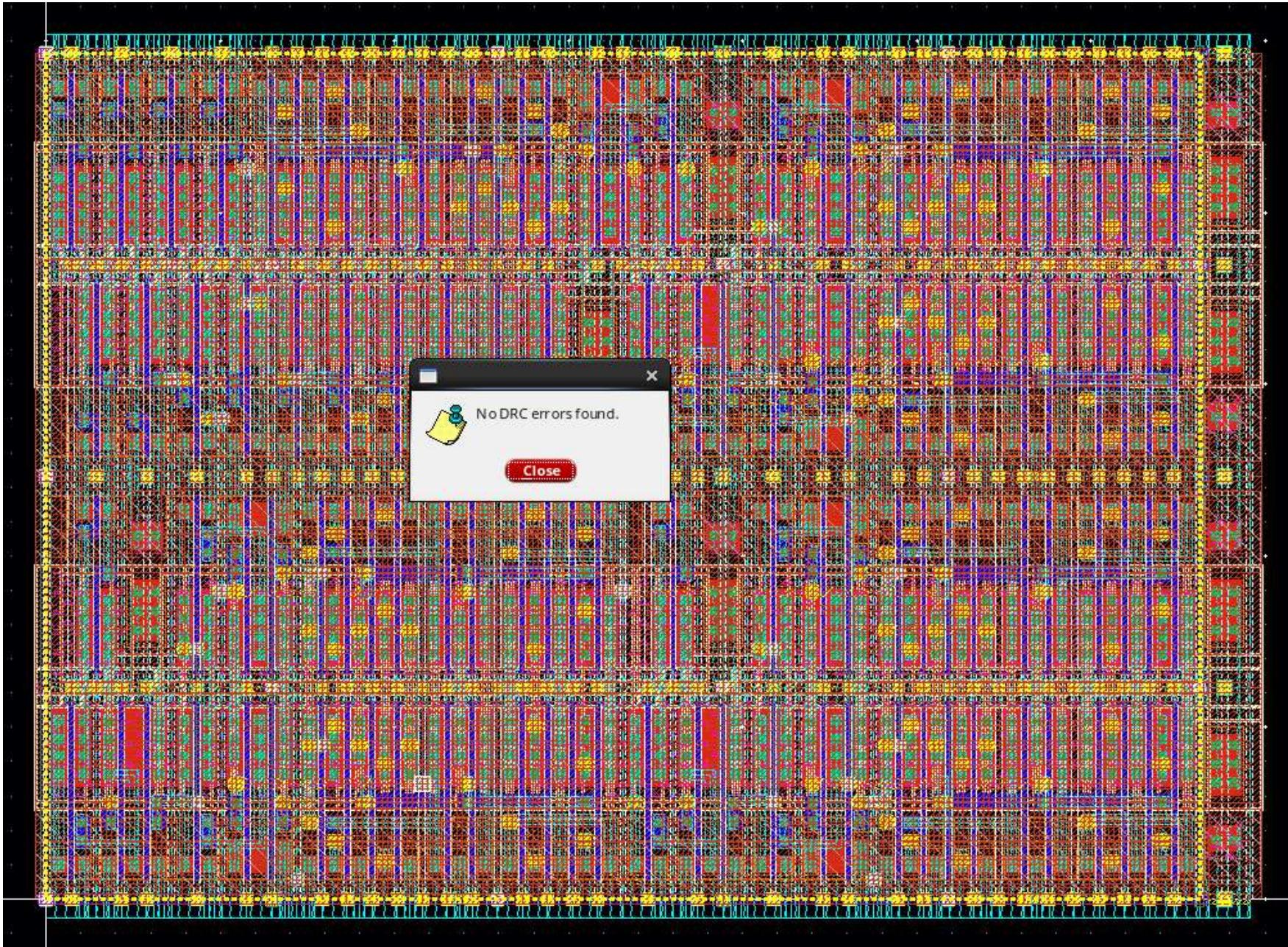
Floor Plan of MUL3:



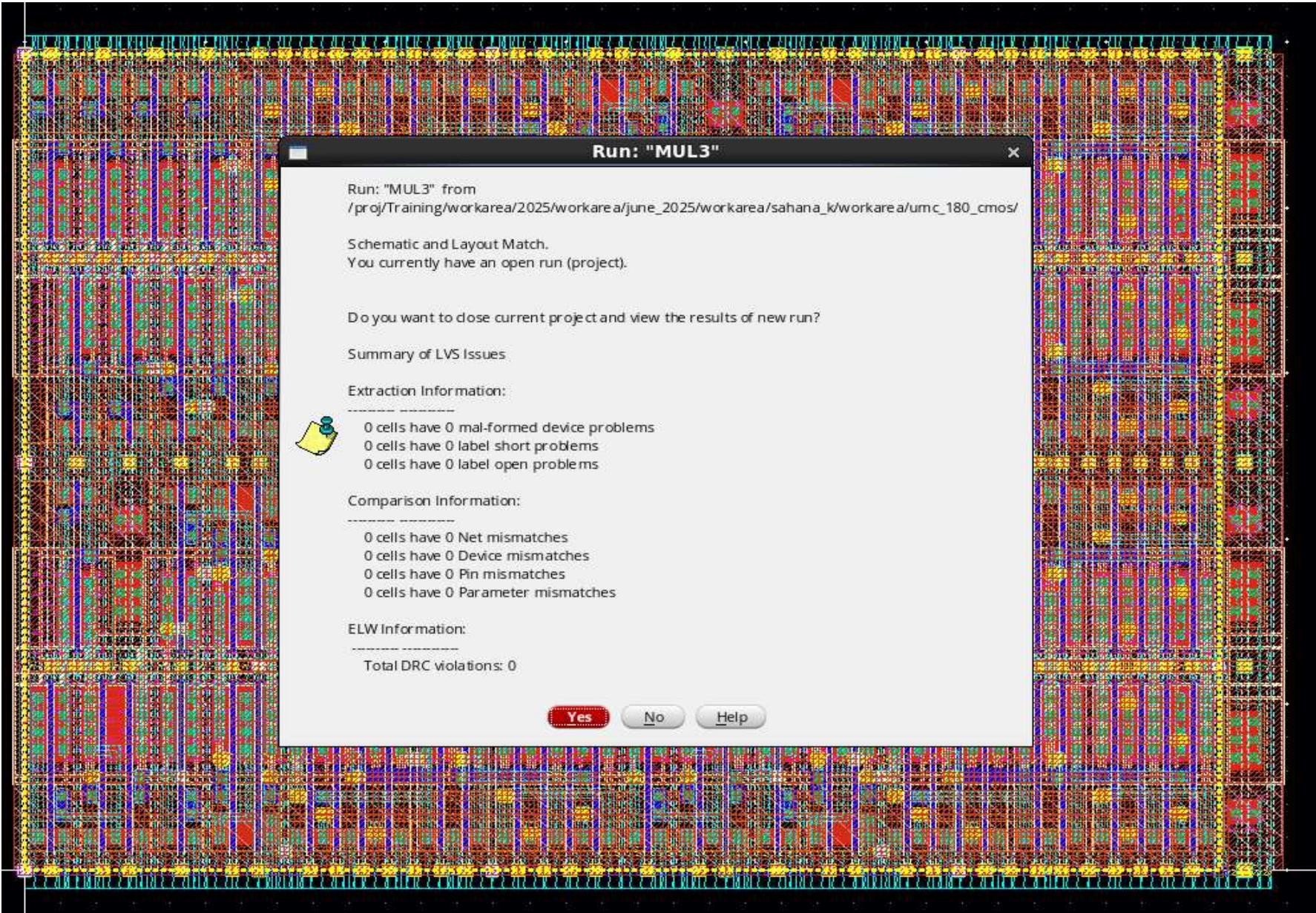
Layout of MUL3:

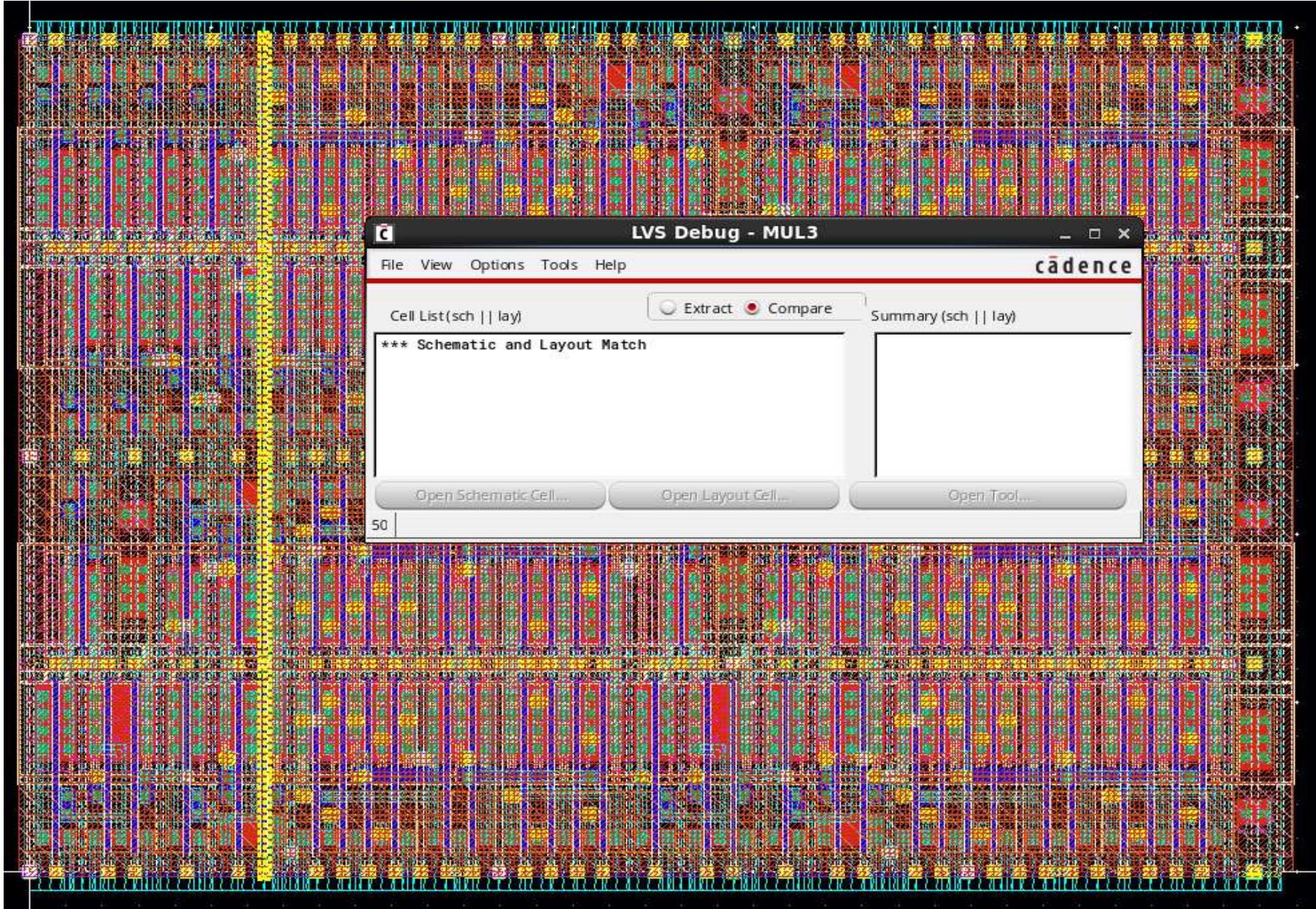


DRC Check:

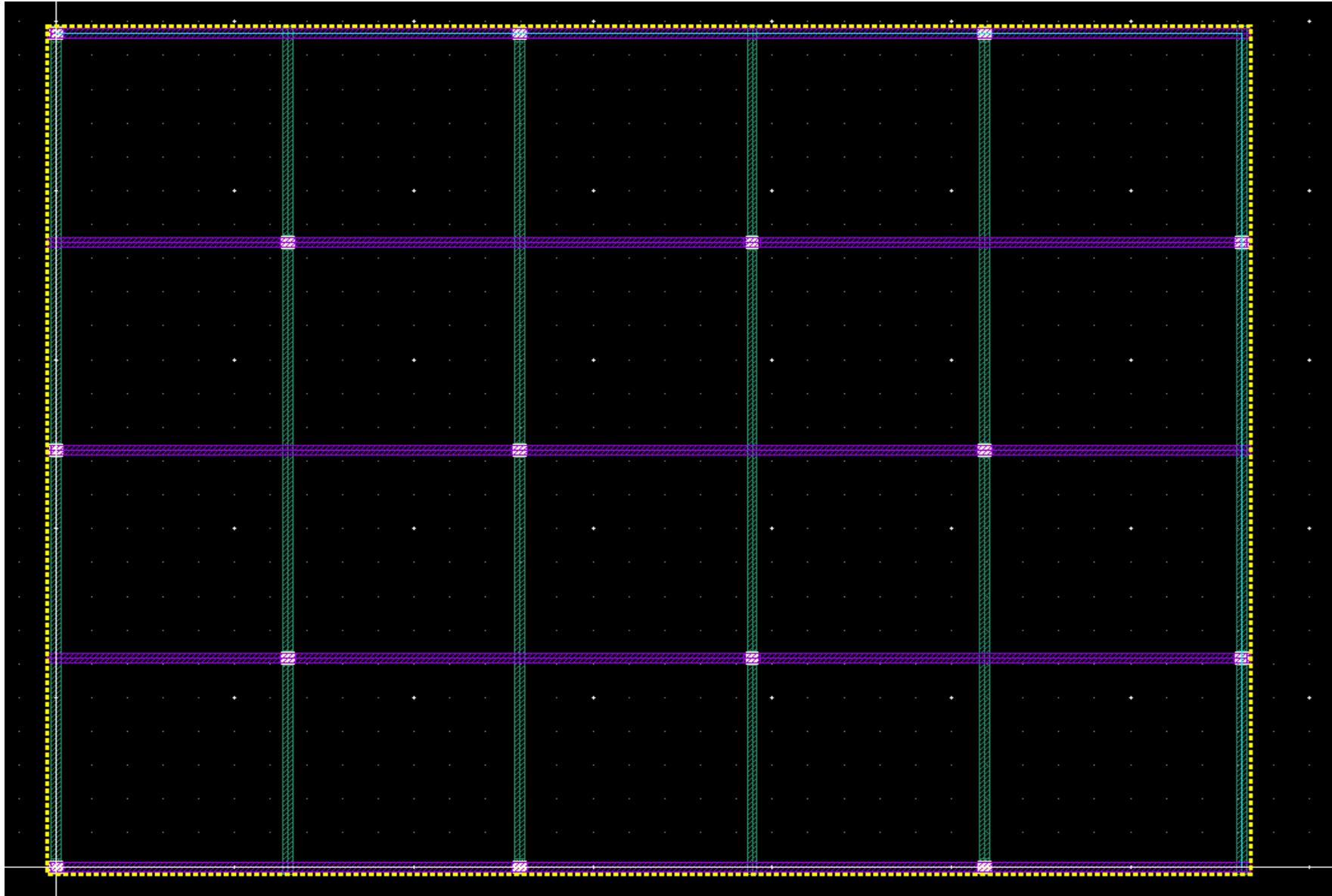


LVS Check:





Power Mesh:



Learning outcomes from Sahana:

1. As the team lead, I developed valuable management and coordination skills.
2. I learned the importance of optimizing floorplans through multiple iterations to ease placement and routing.
3. Encountering various errors improved our problem-solving abilities and understanding of design issues.
4. I also gained knowledge about decaps, fillers, and the benefit of frequent DRC checks to minimize final errors.
5. Overall, leading the team was a valuable experience. It enhanced my teamwork and coordination skills while making the learning process enjoyable.
6. Together, we identified and resolved different types of errors through effective communication and collaboration.

Learning outcomes from Sanika:

1. We divided the main block into sub-blocks — Half Adder, Full Adder, and Mul2. I focused on Mul2 to understand its functionality, role in Mul3, and how it reduces circuit complexity. Then I studied the main block (Mul3), prepared its truth table, and learned why Y4 remains zero while the last two outputs are 1.
2. After schematic and simulation, I performed delay, PVT, and current analysis, identifying the longest delay paths. During floorplanning, I learned about schematic–layout connectivity (XL) and “Generate from Source.” I completed the Mul2 layout, created a stick diagram for XOR3, and with Roopa, handled routing challenges to minimize Metal2 usage.
3. I designed Decap and filler cells and understood their importance in layout design. For the main MUL3 layout, our team worked together, cleared DRC errors, and solved LVS issues caused by missing tap cells.
4. This project gave me strong practical knowledge of circuit design, layout creation, and verification

Learning outcomes from Roopa:

1. I learned what is floorplanning how to do floorplanning, How it eases further steps in layout.
2. I learned placement of devices, How to do it and why is it important.
3. Learned what is power planning and how to do it and how it affects it for layout.
4. Our project is MUL3, I learned what is MUL3, how it works and it's functionality, where it is used.

Challenges Faced:

Initially, we worked on the functionality and design of the decap cell, followed by editing the layout template as per the project requirements. Later, we realized that tapcells were not placed in the bottom row, which caused VSS connectivity errors during LVS. To resolve this issue, we had to add tapcells properly, which led to an increase in the overall block area and required us to modify the floorplan accordingly. These adjustments and corrections were among the key challenges our team faced during the project.

THANK YOU