# LEVEL SHIFTER

This document present the simulation and output of the Level shifter based on a regulated cross-coupled pull-up network.

- A level shifter is a circuit that converts signal voltage levels between different domains, allowing safe communication between components operating at different voltage standards. It ensures compatibility in mixed-voltage systems commonly found in modern integrated circuits.
- The basic architecture of a CMOS level shifter usually includes a pair of cross-coupled inverters, which form a bistable circuit, and a pair of NMOS and PMOS transistors that manage the level conversion.

## Working Principle

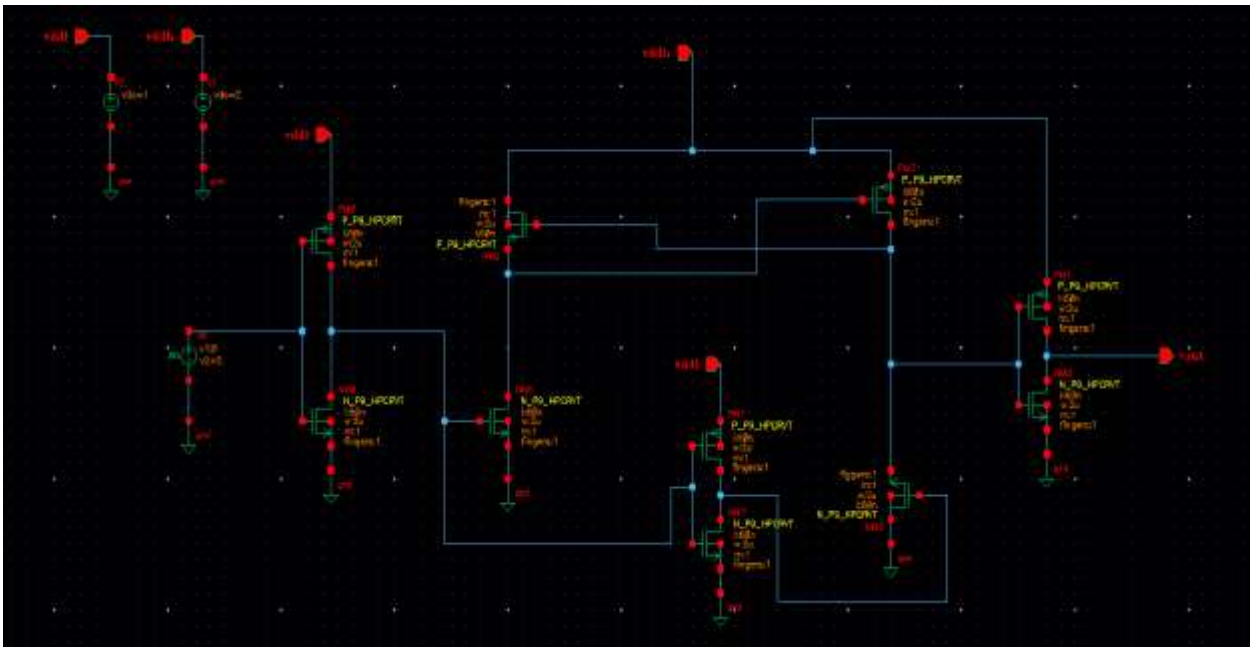
### High-to-Low Conversion

- Initial State: If VDDH = 0 and VDDL = 0, the input voltage (e.g., 1.8mV) will decay towards microvolts due to leakage currents in the circuit.
- Voltage Translation: When VDDH = 0 and VDDL is increased incrementally, the input voltage is translated from volts to millivolts proportionally.
- This ensures proper high-to-low transition at the output.

### Low-to-High Conversion

- Operation: When VDDH > VDDL and the input voltage is less than VDDH, the circuit converts the output to the high voltage domain.
- For example, with an input of 2V and an output requirement of 5V, set VDDH = 5V and ensure VDDL < VDDH.
- Output Dependence: The output voltage always depends on the values of VDDH and VDDL, ensuring flexibility for various use cases.

## Schematic of Level shifter



## Simulation Results

| | VDDH | VDDL | INPUT | OUTPUT |
|---|---|---|---|---|
| **HIGH TO LOW** | 0V | 0V | In millivolts | In microvolts |
| | 0V | 1V | In volts | In millivolts |
| | 2V | 1V | 5V | 2V |
| **LOW TO HIGH** | 5V | 1V | 2V | 5V |
| | 3V | 2V | 1.8V | 3V |

**Transient Analysis**

1. Perform a transient simulation to analyze the level shifter's performance over time.
2. Observe the input and output waveforms to ensure proper level shifting

# Results and Simulations

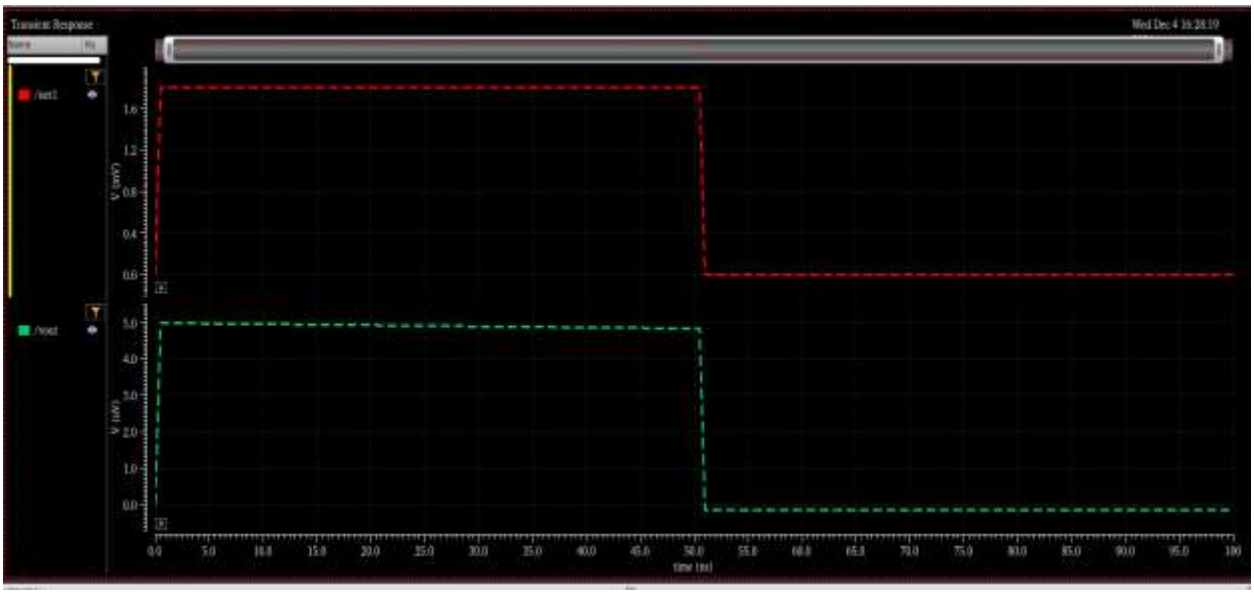


**Fig 7.1.1 Transient response of high to low level shift (millivolts to microvolts)**

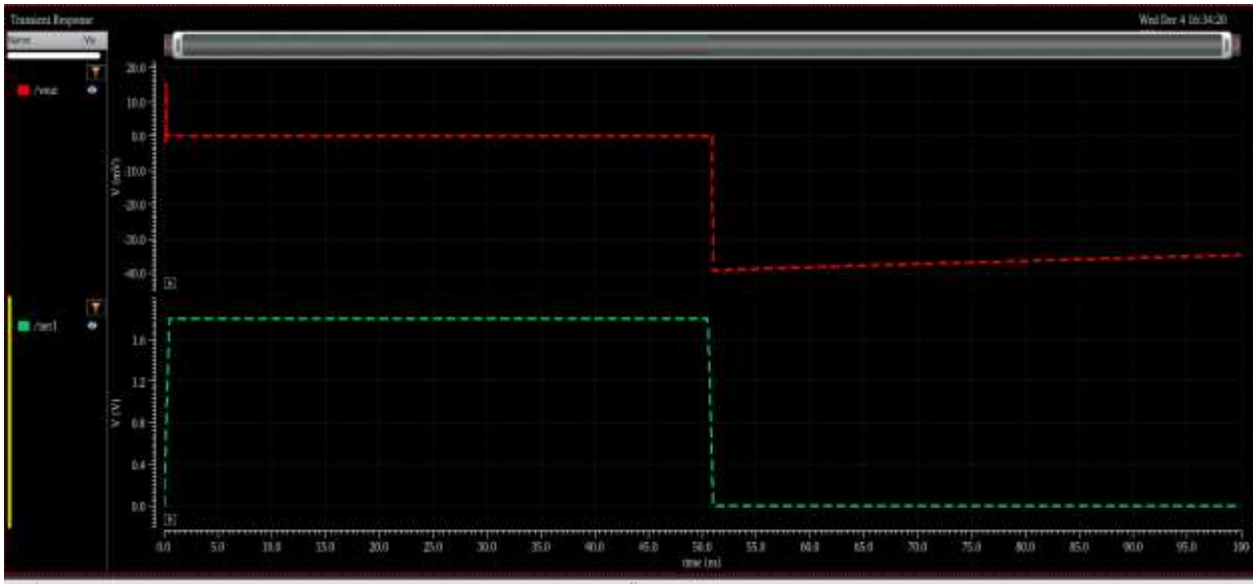


**Fig 7.1.2 Transient response of high to low level shift (volts to milivolts)**

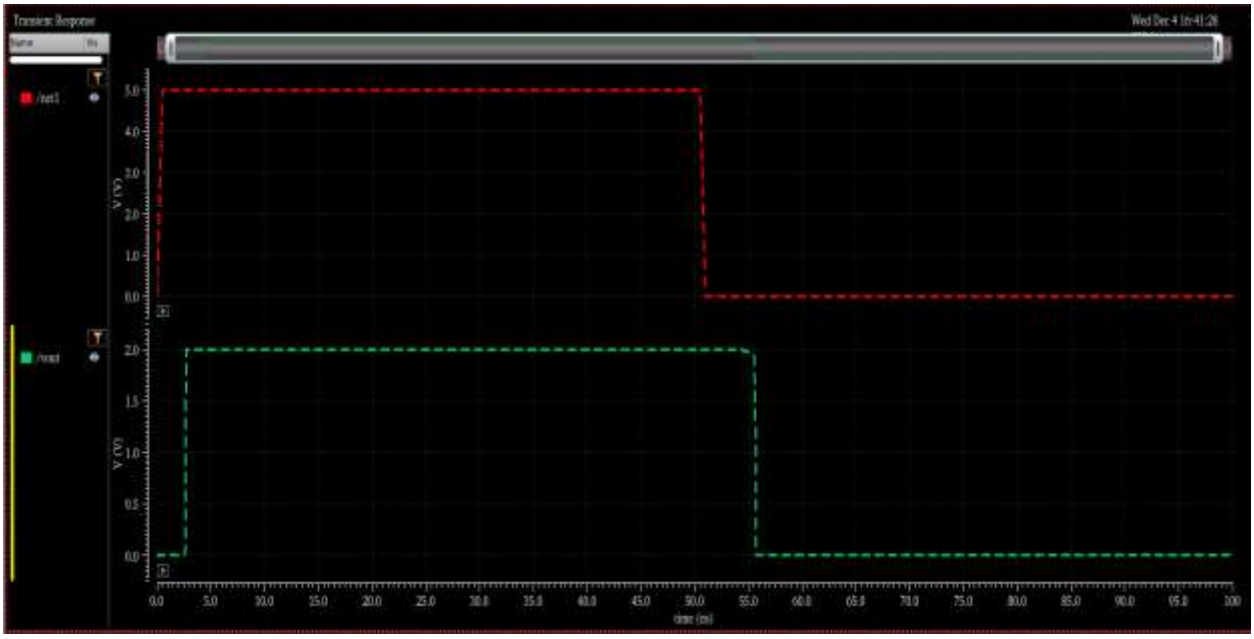


**Fig 7.1.3 Transient response of high to low level shift (5volts to 2 volts)**

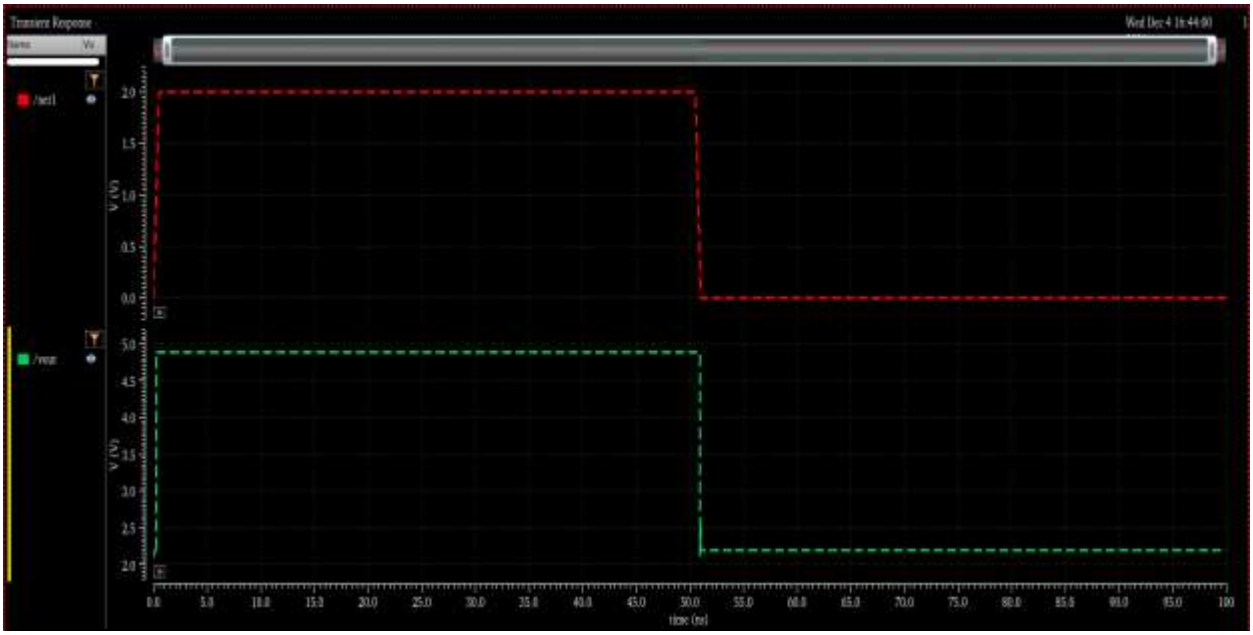


**Fig 7.1.4 Transient response of low to high level shift (2volts to 5volts)**

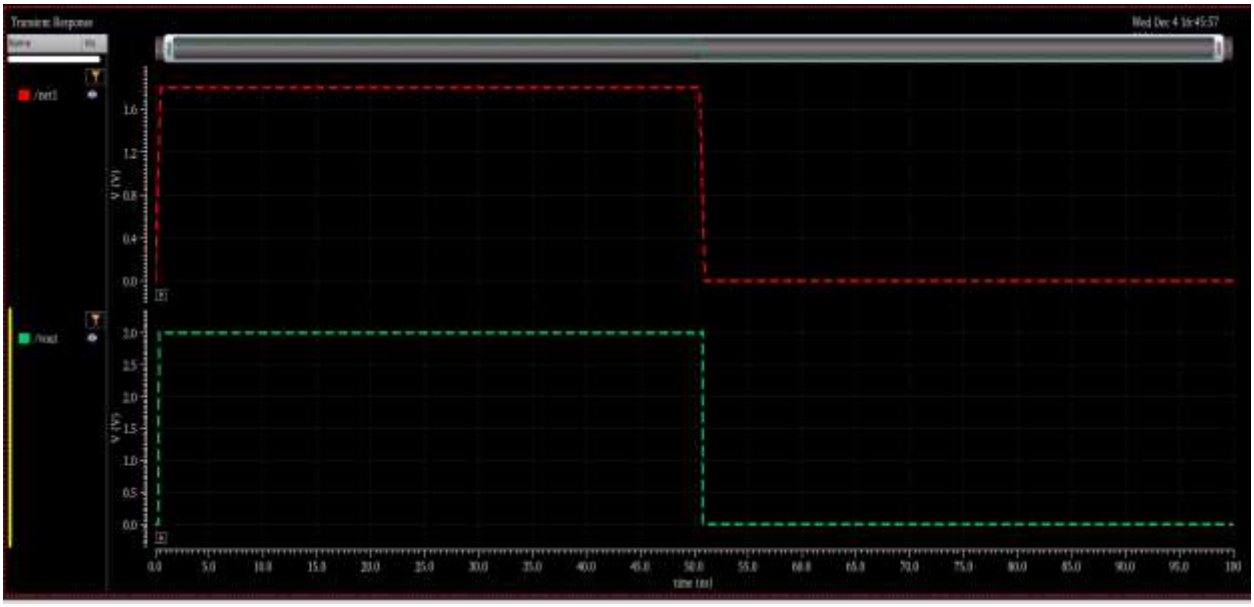


**Fig 7.1.5 Transient response of low to high level shift (1.8volts to 3volts)**

## Conclusion

A voltage level shifter using a cascade voltage switch with a regulated cross-coupled pull-up network was simulated in Cadence with 28 nm CMOS technology. It effectively handled voltage shifts from high to low and low to high (e.g., 5V to 2V, 1.8V to 3V), with low static power consumption due to the cross-coupled design reducing direct paths from supply to ground.