

# Two-Stage CMOS Operational Amplifier (Op-Amp) Portfolio

## Objective

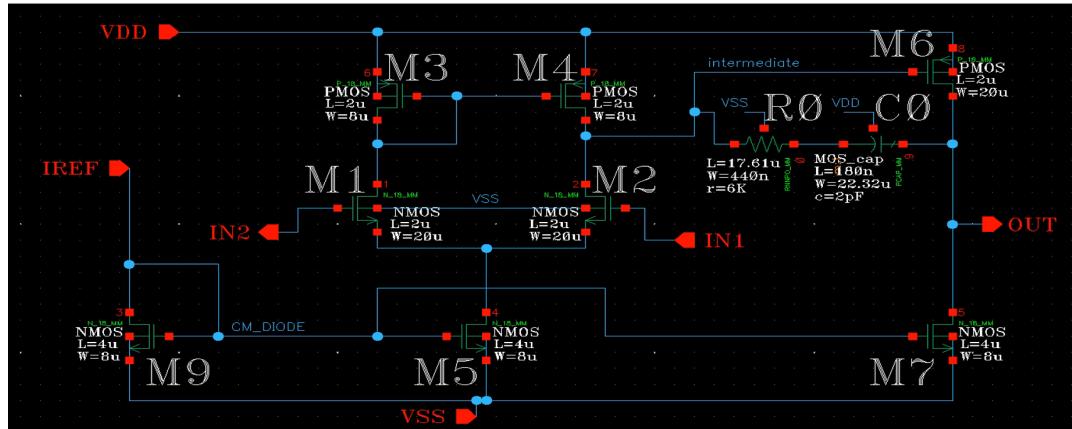
To design, simulate, and layout a two-stage CMOS operational amplifier (Op-Amp) using the UMC 180nm technology node, ensuring proper biasing, stability, and gain performance.

## Tools Used

- Cadence Virtuoso – Schematic design and layout
- Mentor Graphics Calibre – DRC and LVS verification
- UMC 180nm PDK – Device models and design rules

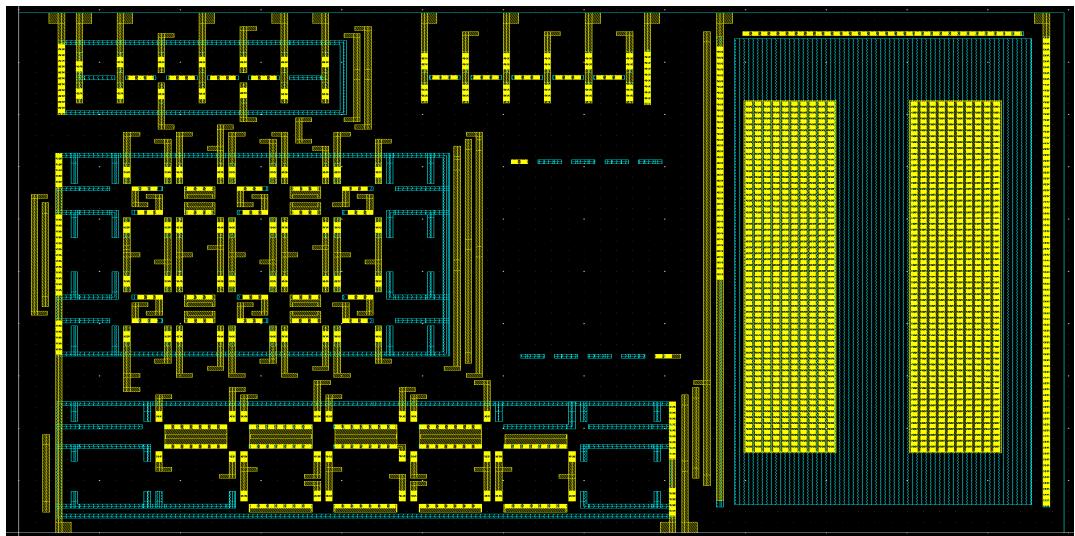
## Schematic

### Schematic

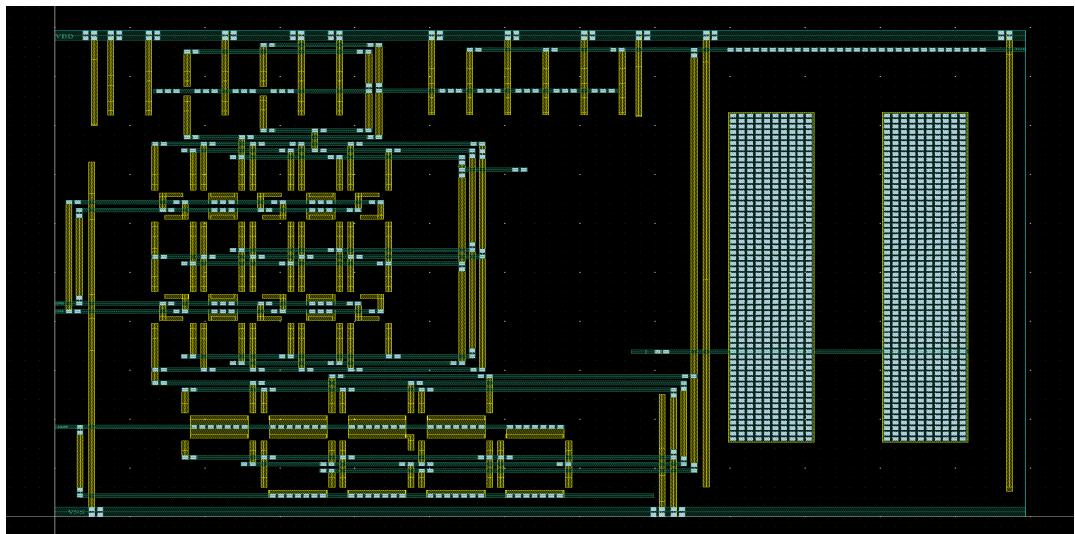


The schematic represents the two-stage CMOS operational amplifier with differential input and current mirror load.

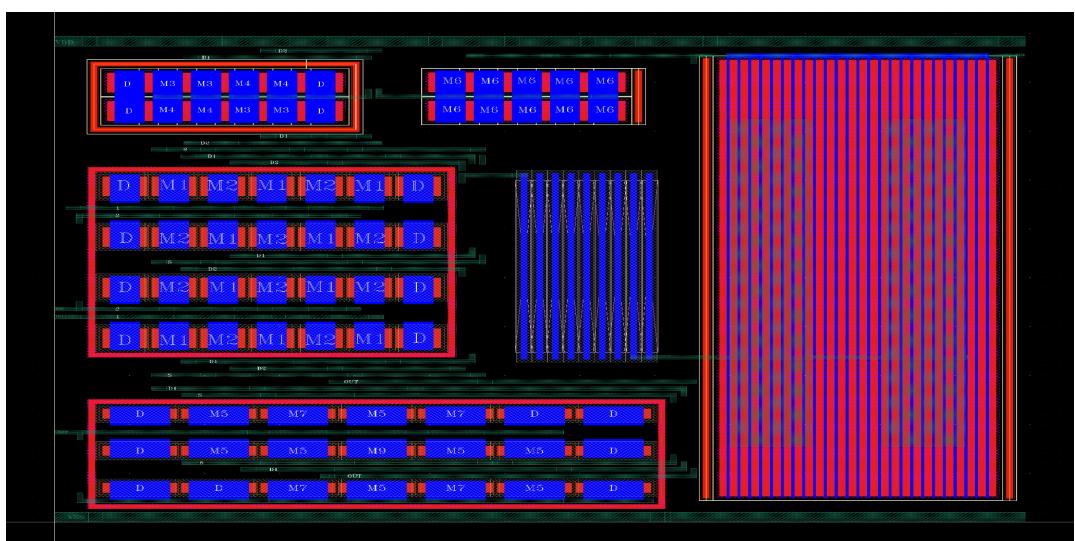
## Layout Stages



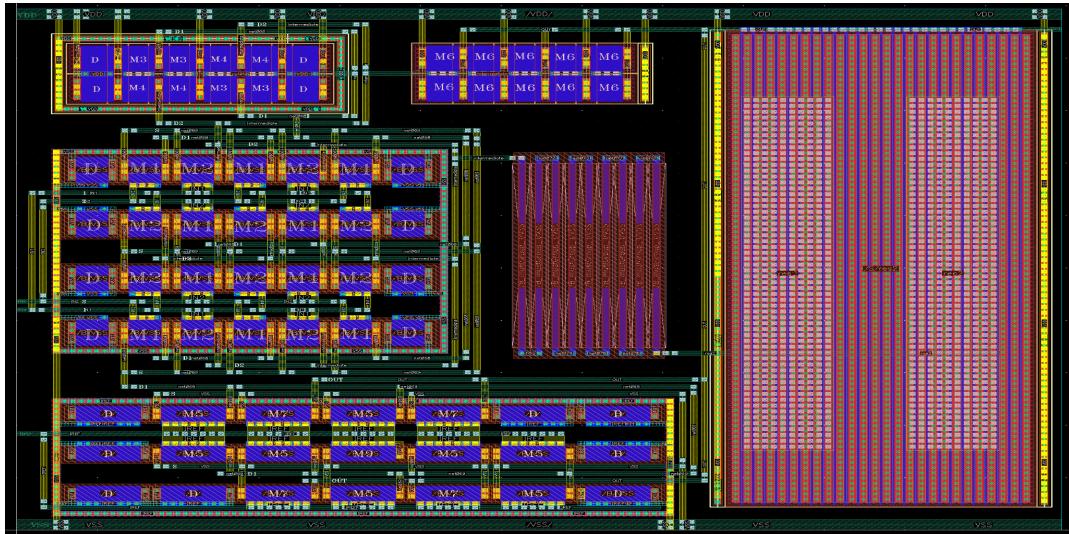
Differential Pair Layout (M1, M2)



Intermediate Stage (M2, M3)

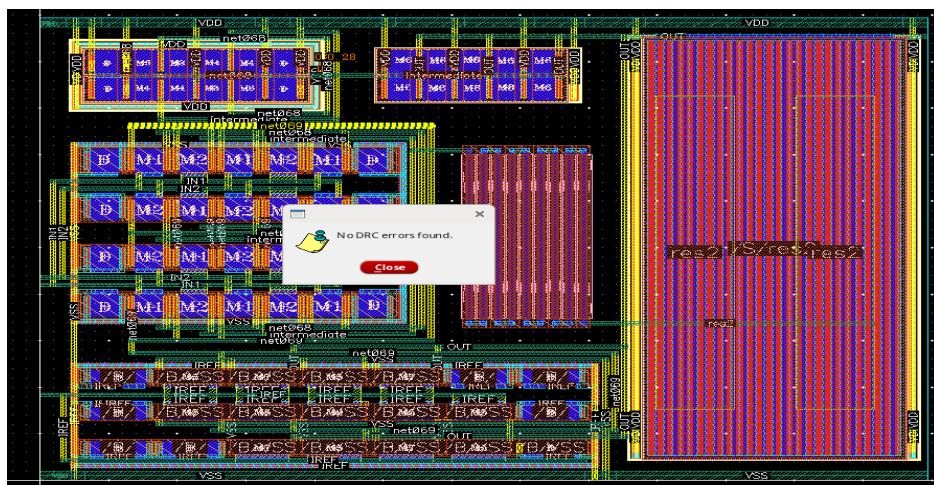


## Driver and Output Stage (M3, Differential Pair)

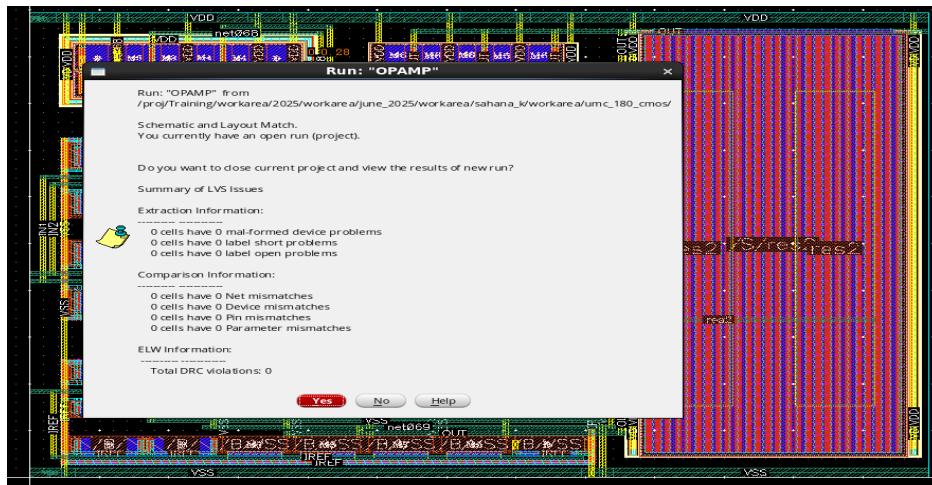


Final Op-Amp Layout

## Verification Results



DRC Report – No design rule violations found.



LVS Report – Layout and schematic perfectly match, confirming design correctness.

## Conclusion

The two-stage CMOS Op-Amp was successfully designed, laid out, and verified with clean DRC and LVS checks, confirming functionality and manufacturability.