

Target SWD/JTAG port with ESD protection

DESIGN NOTE:
For SWD + SWO, SPI1 + USART1 is used
For JTAG, SPI2 is used (SWO not available)

DESIGN NOTE:
T_VCC is read before
enabling 3.3V power.

U4: NUF8401MNT4G

Pin	Signal
1A	T_SWO_TDO
1B	T_SWDIQ_TMS
2A	T_GNDDetect
2B	T_RESET
3A	T_SWDClk_JCLK
3B	T_SWO_TDO
4A	T_TDI
4B	T_RESET
5A	T_VCP_TX
5B	T_VCP_RX
6A	T_TDI
6B	T_RESET
7A	T_VCP_TX
7B	T_VCP_RX
8A	T_TDI
8B	T_RESET
17	GND

U5: STDC14

Pin	Signal
1	+5V
2	T_VCC
3	T_VCC
5	GND
7	GND
11	T_GNDDetect
4	T_SWDIQ_TMS
6	T_SWDClk_JCLK
8	T_SWO_TDO
9	T_TDI
10	T_RESET
12	T_NRST
13	T_VCP_RX
14	T_VCP_TX

ESD protection + 100 ohm current limiting chip

Board-edge castellated vias

The diagram illustrates the internal routing of a PCB with board-edge castellated vias. It shows a cross-section of the board with various layers and components.

- Top Layer (Blue):** Contains the signal traces for J2 and J3. J2 is connected to T_SWDIO_TMS (9), T_SWDCLK_CLK (8), T_SWO_TDO (7), T_GNDDetect (6), T_TDI (5), T_RESET (4), T_VCP_TX (3), T_VCP_RX (2), and a common ground (1). J3 is connected to T_VCC (3), GPI01 (2), and GPI02 (1).
- Core Layer (Green):** Contains the signal traces for J4 and J5. J4 is connected to T_VCC (3), GPI01 (2), and GPI02 (1). J5 is connected to T_VCC (3), GPI01 (2), and GPI02 (1).
- Bottom Layer (Red):** Contains the signal traces for J6 and J7. J6 is connected to T_VCC (3), GPI01 (2), and GPI02 (1). J7 is connected to T_VCC (3), GPI01 (2), and GPI02 (1).
- Power Plane (Yellow):** A central layer labeled +5V, which is connected to the power pins of J2, J3, J4, J5, J6, and J7.
- Castellated Vias:** The vias are located at the edges of the board, allowing for direct connection to the components on the other side.

MCU I/O

U1A
hs-probe-stm32

PA0-WKUP	N3	✗
PA1	N2	✗
PA2	P2	✗
PA3/ADC1_IN3	R2	→ T_VCC_MEAS
PA4	N4	✗
PA5	P4	✗
PA6	R3	✗
PA7	F15	✗
PA8	F15	✗
PA9/USB_OTG_FS_VBUS	F15	→ FS_VBUS
PA10	D15	✗
PA11/USB_OTG_FS_DM	C15	→ D_FS_N
PA12/USB_OTG_FS_DP	B15	→ D_FS_P
PA15	A13	✗

U1B
hs-probe-stm32

PB0	R5	✗
PB1	R4	✗
PB2	M6	✗
PB3/SPI1_SCK	A6	→ SPI1_CLK
PB4/SPI1_MISO	A9	→ SPI1_MISO
PB5/SPI1_MOSI	A6	→ SPI1_MOSI
PB6/USART1_TX	B6	✗
PB7/USART1_RX	B5	→ USART1_RX
PB8/LED2	A5	→ LED2
PB9	B4	✗
PB10/USB_SEL	R12	→ USB_SEL
PB11	R13	✗
PB12	P12	✗
PB13/USB_OTG_HS_VBUS	P13	→ HS_VBUS
PB14/USB_OTG_HS_DM	R14	→ D_HS_N
PB15/USB_OTG_HS_DP	R15	→ D_HS_P

U1C
hs-probe-stm32

PC0	M2	✗
PC1	M3	✗
PC2	M4	✗
PC3	M5	✗
PC4	N5	✗
PC5	P5	✗
PC6	H15	✗
PC7	G15	✗
PC8	G14	✗
PC9	F14	✗
PC10/LED1	B14	→ LED1
PC11	B13	✗
PC12	A12	✗
PC13	D1	✗
PC14-OSC32_IN	F1	✗
PC15-OSC32_OUT	F1	✗

U1D
hs-probe-stm32

PD0	B12	✗
PD1	C12	✗
PD2	D12	✗
PD3	D11	✗
PD4	D10	✗
PD5/USART2_TX	C11	→ USART2_TX
PD6/USART2_RX	B11	→ USART2_RX
PD7	A11	✗
PD8/GPIO1	P15	→ GPIO1
PD9	P14	✗
PD10/GPIO2	N15	→ GPIO2
PD11	N14	✗
PD12	N13	✗
PD13	M15	✗
PD14	M14	✗
PD15	L14	✗

U1E
hs-probe-stm32

PE0/LED3	A4	→ LED3
PE1	A3	✗
PE2/T_VCC_EN	A2	→ T_VCC_EN
PE3	A1	✗
PE4	B1	✗
PE5	B2	✗
PE6	B3	✗
PE7	R8	✗
PE8	P8	✗
PE9	P9	✗
PE10	R9	✗
PE11	P10	✗
PE12	R10	✗
PE13	N11	✗
PE14	P11	✗
PE15	R11	✗

U1G
hs-probe-stm32

PG0	M7	✗
PG1	M7	✗
PG2	L15	✗
PG3	K15	✗
PG4	K14	✗
PG5	K13	✗
PG8	H14	✗
PG9	C10	✗
PG10	B10	✗
PG11	B9	✗
PG12	B8	✗
PG13/RESET	A8	→ RESET
PG14/GNDDet	A7	→ GNDDetect
PG15	B7	✗

U1I
hs-probe-stm32

PI0	F14	✗
PI1/SPI2_SCK	D14	→ SPI2_CLK
PI2/SPI2_MISO	C14	→ SPI2_MISO
PI3/SPI2_MOSI	D13	→ SPI2_MOSI
PI4	D4	✗
PI5	C4	✗
PI6	C3	✗
PI7	C2	✗
PI8	D2	✗
PI9	D3	✗
PI10	E3	✗
PI11	D4	✗

Circuit Diagrams:

Top Circuit: A voltage divider circuit. T_VCC is connected to a 5.1k resistor (R102), which is connected to T_VCC_MEAS. T_VCC_MEAS is also connected to another 5.1k resistor (R101), which is connected to ground.

Bottom Circuit: A voltage divider circuit. FS_VBUS is connected to a 1k resistor (R9), which is connected to HS_VBUS. HS_VBUS is also connected to a 1k resistor (R9), which is connected to +5V.

LED Driver Circuit: A circuit for driving three LEDs (LED1, LED2, LED3) using an LTST-C19HE1WT LED driver. The driver is connected to +5V and ground. The LEDs are connected to the driver's output pins (1, 2, 3) through resistors R5, R6, and R7 respectively.

Probe power and optional target power

USB-C port with USB MUX

Diagram illustrating the connection of a USB-C port with a USB MUX (U8, USB3740B-AI9) to a USB connector (J1).

Components and Connections:

- U8 (USB3740B-AI9):** USB MUX chip.
 - VDD (Pin 10) is connected to +3.3V (C28, 0.1uF).
 - GND (Pin 8) is connected to ground.
 - DP_2 (Pin 6) is connected to DP (Pin 10).
 - DM_2 (Pin 7) is connected to DM (Pin 9).
 - OE_N (Pin 2) is connected to OE_N (Pin 3).
 - DM_1 (Pin 1) is connected to DM_1 (Pin 4).
 - S (Pin 4) is connected to S (Pin 3).
- J1 (USB Connector):**
 - PWR_FLAG (A4) is connected to +5V.
 - CC1 (A5) is connected to CC1 (Pin 5).
 - CC2 (B5) is connected to CC2 (Pin 6).
 - D- (A7) is connected to D- (Pin 7).
 - D+ (B7) is connected to D+ (Pin 8).
 - GND (A1, B8) is connected to ground.
 - SHIELD (S1) is connected to ground.

DESIGN NOTE:
On startup the FS port is connected for access to the STM32 USB bootloader. The firmware can then switch over to the HS port.

Sheet: /		
File: hs-probe.sch		
Title: Rusty High-Speed Probe		
Size: A3	Date: 2020-07-19	Rev: v1.1
KiCad E.D.A.	kiCad 5.1.6	Id: 1/1